VERILOG CODE

```
module battery_monitor(
   input wire clk,
   input wire [7:0] voltage,
   input wire [7:0] temperature,
   output reg undervoltage,
   output reg overvoltage,
   output reg overtemperature,
   output reg system_fault
);
parameter VOLTAGE_LOW  = 8'd50;
parameter VOLTAGE_HIGH = 8'd200;
parameter TEMP_HIGH    = 8'd80;

always @(posedge clk) begin
   undervoltage     <= (voltage < VOLTAGE_LOW);
   overvoltage      <= (voltage > VOLTAGE_HIGH);
   overtemperature  <= (temperature > TEMP_HIGH);
   system_fault     <= (voltage < VOLTAGE_LOW) ||
                       (voltage > VOLTAGE_HIGH) ||
                       (temperature > TEMP_HIGH);
end

endmodule
```

TEST BENCH CODE

```
`timescale 1ns/1ps
module battery_tb();
reg clk;
reg [7:0] voltage;
reg [7:0] temperature;
wire undervoltage, overvoltage, overtemperature, system_fault;
// Instantiate the Unit Under Test (UUT)
battery_monitor uut (
   .clk(clk),
   .voltage(voltage),
   .temperature(temperature),
   .undervoltage(undervoltage),
   .overvoltage(overvoltage),
   .overtemperature(overtemperature),
   .system_fault(system_fault)
);
// Clock generation: 10ns period
initial begin
   clk = 0;
   forever #5 clk = ~clk;
end

// Test stimulus
```

```
initial begin
    // Normal operation
    voltage = 8'd100; temperature = 8'd30;
    #20;
    // Undervoltage
    voltage = 8'd40; temperature = 8'd45;
    #20;
    // Overvoltage
    voltage = 8'd210; temperature = 8'd50;
    #20;
    // Overtemperature
    voltage = 8'd150; temperature = 8'd90;
    #20;
    // Multiple faults
    voltage = 8'd30; temperature = 8'd100;
    #20;

    $finish;
end
endmodule
```