SCAD Architecture Project Paper

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1 Instruction Set Architecture

Aside from the mandatory move instruction, our Instruction Set Architecture (ISA) needs to have instructions for loading immediate values, jumping to fixed addresses and branching.

```
 1   // Load operands from memory
 2   immediate <op1_address> // op1_address into the control unit output
 3   move ctrl.o0, load.i0
 4   immediate <op2_address>
 5   move ctrl.o0, load.i0
 6
 7   // Load result destination address
 8   immediate <result_address>
 9   move ctrl.o0, store.i0 // tell
10
11   // Send parameters to compare unit
12   move load.o0, cmp.i0
13   move load.o0, cmp.i1
14
15   move cmp.o0, ctrl.i0 //move to control unit input for branch
16   branch yes // branch to yes if control unit input != 0
17   no:
18      immediate 1
19      jump both
20   yes:
21      immediate 0
22   both
23      move ctrl.o0, store.i1 // move to data input of the store unit
```

2 Move Instruction Bus

2.1 2-Phase Commit

To take into account both stalls of source and destination functional units, the control unit sends move instructions in two phases, both of which are indicated by a rising edge of the "valid" flag. First, with phase low, the functional units only check whether there is space in the corresponding input and output buffers. When stalls are asserted, the control unit waits some time until retrying. When no functional unit stalls, the phase being high signals a "write".
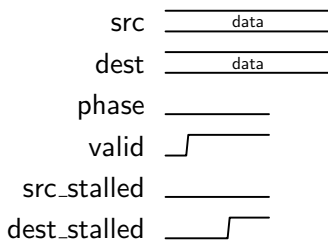

Figure 1: A timing diagram

3   Control Unit and Data Network

To keep the MIB simple, we will have the control unit send immediate values, and receive branch conditions through the data network. While broadcasting immediate values through either the MIB or a separate bus may be the faster alternative, having the control unit send them through the data network keeps the architecture cleaner.

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