



Vehicle Camera Recorder SOC Solution

Preliminary

Oct. 15, 2014

Version 0.1



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VEHICLE CAMERA RECORDER SOC SOLUTION

1. GENERAL DESCRIPTION

The GPCV1248A, a highly integrated SoC (System-On-a-Chip) for vehicle camera recorder, is based on a high performance and power efficient ARM7TDMI core operating at up to 144MHz and is enhanced with image, video processing, power saving, and system peripherals.

The high-speed MJPEG engine is capable of supporting up to 720P 30fps video compression. Other main features include a high-performance Image Signal Processing (ISP) hardware-accelerating pipeline to boost the conventional raw-data CMOS sensor up to 3M pixels and an HDMI Tx for HDTV output to deliver high-resolution graphics. The GPCV1248A processor is designed to connect with various types of memory card interfaces such as SD, SDHC, SDIO, and MMC.

These fully featured peripherals and functions make GPCV1248A one of the best vehicle camera SoC solutions in the industry-making your products more competitive in today's market.

2. FEATURES

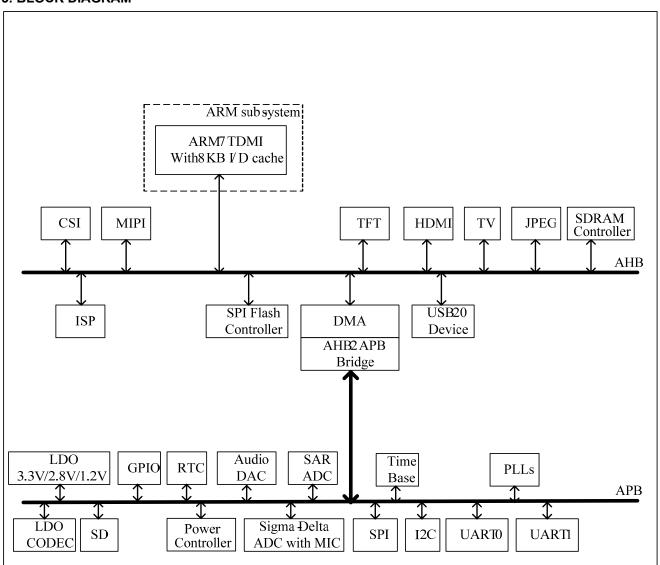
- ARM7TDMI CPU with 8KB unified ID-cache, embedded JTAG
 ICE, and working frequency up to 144MHz.
- JPEG CODEC supports MJPEG 1280x720 30fps encode/decode function.
- ISP for CMOS sensor raw data processing.
- SPI Flash controller which supports 1-bit/2-bit/4-bit IO mode.
 The max. freq. of SPI clock is 70MHz.
- HDMI V1.2 supports both 480p and 720p
- TV encoder with 10-bit VDAC
- Video-in & CMOS sensor interface and CCIR601/CCIR656

standard supported.

- MIPI RX with one data lane supported.
- TFT-LCD controller.
 - UPS051. (serial RGB)
 - UPS052. (serial RGB dummy)
 - Parallel-RGB with 18/16/8-bit data(6-6-6,5-6-5,8)
 - I80 (8-bit system bus) I/F type.
 - CCIR601/CCIR656.
- Universal Serial Bus (USB) 2.0 high/full speed compliance device.
- Watchdog timer.
- SD/ SDHC/ SDIO/ MMC card interfaces.
- SPI (master/slave) interface with data rate up to 24Mbps.
- Two UART (asynchronous serial I/O) interfaces with baud rate up to 1.8432Mbps and 115.2Kbps. The UART interface can be configured as smart card interface(ISO7816)
- I2C controller
- Built-in power control macro which provide two power control pin for power on/off control and 2 PWM output for driving LED.
- 3.6V(BAT_IN) to 3.3V LDO for I/O
- 3.3V to 1.2V LDO for core logic
- 3.6V(BAT_IN) to 2.8V LDO for CMOS sensor
- Dedicated 3.6V(BAT_IN) to 3.3V LDO for ADC/DAC.
- Independent power Real-time clock (RTC).
- Internal 12MHz generator(XCKGEN) with 32768Hz Crystal input.
- 16-bit stereo DAC (2-channel) for audio playback.
- 12-bit ADC with four line-in channels and two internal channels for battery and 1.2V measurement.
- 16-bit Sigma-Delta ADC with MIC and PGA
- LQFP128



3. BLOCK DIAGRAM





4. SIGNAL DESCRIPTION

PKG No	Name	Group	Туре	Normal Function Description
1	X32KO	RTC	AO	X'tal 32768Hz output
2	PLL_V33	PLL	Р	3.3V PLL Power
3	X12MI	PLL	Al	X'tal 12MHz input
4	V12	CORE PWR	Р	1.2V Core Power
5	VSS	Digital GND	Р	Digital ground
6	IOD15	SD	Ю	SD DATA2
7	IOD12	SD	10	SD DATA3
8	IOD10	SD	Ю	SD CMD
9	IOD11	SD	Ю	SD CLK
10	IOD13	SD	Ю	SD DATA0
11	IOD14	SD	10	SD DATA1
12	IOA8	GPIO	Ю	IOA8
13	IOA9	I2C	Ю	I2C_SCL
14	IOA10	I2C	10	I2C_SDA
15	V33	IO PWR	Р	3.3V IO Power
16	IOA11	TFT	Ю	TFT CS
17	IOA12	GPIO	10	IOA12
18	IOA13	GPIO	Ю	IOA13
19	VSS	Digital GND	Р	Digital ground
20	IOA14	GPIO	10	IOA14
21	IOA15	GPIO	10	IOA15
22	IOB5	GPIO	Ю	IOB5
23	IOB4	TFT	Ю	TFT TE
24	IOB3	TFT	Ю	TFT CLK
25	IOB2	TFT	Ю	TFT VSYNC
26	IOB1	TFT	10	TFT HSYNC
27	IOB0	TFT	Ю	TFT DE
28	IOC12	ICE	Ю	JTAG TDI
29	IOC13	ICE	Ю	JTAG TDO
30	V12	CORE PWR	Р	1.2V Core Power
31	IOC14	ICE	Ю	JTAG TCK
32	V33	IO PWR	Р	3.3V IO Power
33	IOC15	ICE	Ю	JTAG TMS
34	VSS	Digital GND	Р	Digital ground
35	IOB8	GPIO	Ю	IOB8
36	IOB9	GPIO	10	IOB9
37	IOB10	GPIO	10	IOB10
38	IOB11	GPIO	10	IOB11
39	IOB12	GPIO	10	IOB12
40	IOB13	GPIO	10	IOB13
41	IOB14	GPIO	10	IOB14
42	IOB15	GPIO	Ю	IOB15
43	USB_VDA_V33	USB	Р	3.3V USB Power
44	DM	USB	AIO	USB DM





PKG No	Name	Group	Туре	Normal Function Description
45	DP	USB	AIO	USB DP
46	USB_VDA_VSS	USB	Р	USB Ground
47	AOUT	VDAC	AO	VDAC AOUT
48	CBU	VDAC	AO	VDAC CBU
49	HDMI_V33	HDMI	Р	3.3V HDMI Power
50	HDMI_V12	HDMI	Р	1.2V HDMI Power
51	HDMI_VSS	HDMI	Р	HDMI ground
52	HDMI_VSS	HDMI	Р	HDMI ground
53	IOE7	HDMI	10	HDMI TXP2
54	IOE6	HDMI	10	HDMI TXN2
55	IOE5	HDMI	Ю	HDMI TXP1
56	IOE4	HDMI	Ю	HDMI TXN1
57	IOE3	HDMI	Ю	HDMI TXP0
58	IOE2	HDMI	Ю	HDMI TXN0
59	IOE1	HDMI	Ю	HDMI TXCP
60	IOE0	HDMI	Ю	HDMI TXCN
61	NC			
62	NC			
63	IOC11	CSI	Ю	CSI VSYNC
64	IOC10	CSI	Ю	CSI HSYNC
65	IOC9	CSI	Ю	CSI CLKO
66	IOC8	CSI	Ю	CSI CLKI
67	VSS	Digital GND	Р	Digital ground
68	V12	CORE PWR	Р	1.2V Core Power
69	IOC7	CSI	Ю	CSI D9
70	IOC6	CSI	Ю	CSI D8
71	IOC5	CSI	Ю	CSI D7
72	VSS	Digital GND	Р	Digital ground
73	IOC4	CSI	Ю	CSI D6
74	IOC3	CSI	10	CSI D5
75	V33	IO PWR	Р	3.3V IO Power
76	IOC2	CSI	Ю	CSI D4
77	IOC1	CSI	10	CSI D3
78	IOC0	CSI	Ю	CSI D2
79	VSS	Digital GND	Р	Digital ground
80	IOB6	CSI	Ю	CSI D0
81	IOB7	CSI	Ю	CSI D1
82	IOD6	SPI	Ю	SPI CS
83	IOD7	SPI	Ю	SPI CLK
84	V33	IO PWR	Р	3.3V IO Power
85	IOD8	SPI	Ю	SPI TX
86	IOD9	SPI	10	SPIRX
87	IOD0	SPIF	10	SPI Flash CSB
88	V12	CORE PWR	Р	1.2V Core Power
89	IOD1	SPIF	10	SPI Flash CLK



PKG No	Name	Group	Туре	Normal Function Description
90	IOD2	SPIF	Ю	SPI Flash RX0
91	IOD3	SPIF	Ю	SPI Flash RX1
92	IOD4	SPIF	Ю	SPI Flash RX2
93	IOD5	SPIF	10	SPI Flash RX3
94	IOA0	TFT	Ю	TFT D0
95	IOA1	TFT	Ю	TFT D1
96	IOA2	TFT	10	TFT D2
97	IOA3	TFT	10	TFT D3
98	IOA4	TFT	10	TFT D4
99	IOA5	TFT	10	TFT D5
100	IOA6	TFT	10	TFT D6
101	IOA7	TFT	10	TFT D7
102	RESETB	SYSTEM	I	External RESETB(Low active)
103	TEST	SYSTEM	I	Test enable(High active)
104	DACOL	AuDAC	AO	Audio DAC left channel output
105	DACOR	AuDAC	AO	Audio DAC right channel output
106	DACVREF	AuDAC	AO	Audio DAC/CODEC ADC VREF
107	V33_DA16	AuDAC	Р	3.3V Power for AuDAC/CODEC ADC/SAR ADC
108	VSS_DA16	AuDAC	Р	Ground for AuDAC/CODEC ADC/SAR ADC
109	LINEIN1	SAR ADC	Al	SAR ADC LINEIN1
110	LINEIN0	SAR ADC	Al	SAR ADC LINEINO
111	MICIN	CODEC ADC	Al	CODEC ADC microphone input
112	MICBIAS	CODEC ADC	AO	CODEC ADC microphone bias output
113	LINEINL	CODEC ADC	Al	CODEC ADC left channel input
114	LINEINR	CODEC ADC	Al	CODEC ADC right channel input
115	BAT_IN	SYSTEM	Р	Battery input
116	PWR_SEL	SYSTEM	I	Power mode selection 0: enable internal LDO33 1: disable internal LDO33
117	PWM0	SYSTEM	AO	PWM0 output; PWM0 can work even 3.3V and 1.2V is off. Only sink current capability.
118	PWR ON1	SYSTEM	Al	Power on key 1
119	PWM1	SYSTEM	AO	PWM1 output; PWM0 can work even 3.3V and 1.2V is off. Only sink current capability.
120	DC2DC_EN	SYSTEM	AO	DC2DC_EN output for external DC2DC or LDO control
121	REGV28	SYSTEM	Р	2.8V LDO output
122	PWR_ON0	SYSTEM	A1	Power on key 0
123	VSS	Digital GND	Р	Digital ground
124	V12	CORE PWR	Р	1.2V Core Power
125	NC			
126	NC			
127	V33_RTC	RTC	Р	3.3V RTC power; Don't short V33_RTC with other 3.3V power.
128	X32KI	RTC	Al	X'tal 32768

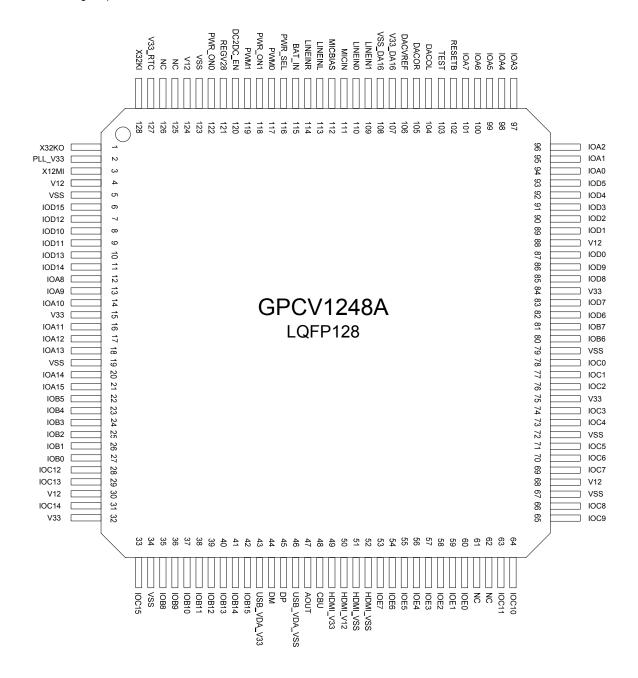
Note: AO: Analog Output, AI: Analog Input





4.1. Package Pin Sequence

LQFP128 Package Top View





5. ELECTRICAL SPECIFICATIONS

5.1. Absolute Maximum Rating

Rating	Symbol	Value	Unit
Supply Voltage 1	BAT_IN	-0.3 to 3.6	V
Supply Voltage 2	V33_RTC	-0.3 to 3.6	V
Supply Voltage 3	V33	-0.3 to 3.6	V
Supply Voltage 4	PLL_V33	-0.3 to 3.6	V
Supply Voltage 5	USB_VDA_V33	-0.3 to 3.6	V
Supply Voltage 6	HDMI_V33	-0.3 to 3.6	V
Supply Voltage 7	V33_DA16	-0.3 to 3.6	V
Supply Voltage 8	REG28	-0.3 to 3.6	V
Supply Voltage 9	HDMI_V12	-0.3 to 1.32	V
Supply Voltage 10	V12	-0.3 to 1.32	V
Input Voltage	V_{IN}	-0.3 to 3.6	V
Operating Temperature	T_A	-40~70	$^{\circ}\mathbb{C}$
Storage Temperature	T_{STG}	-40 to +150	$^{\circ}\mathbb{C}$

5.2. DC Characteristics

a		Limits				0 1111	
Characteristic	Symbol	Min.	Тур.	Max.	Unit	Condition	
Supply Voltage 1	BAT_IN	2.7	3.3	3.6	V	-	
Supply Voltage 2	V33_RTC	2.7	3.3	3.6	V	-	
Supply Voltage 3	V33	2.7	3.3	3.6	V	-	
Supply Voltage 4	PLL_V33	2.7	3.3	3.6	V	-	
Supply Voltage 5	USB_VDA_V33	3.0	3.3	3.6	V	-	
Supply Voltage 6	HDMI_V33	2.7	3.3	3.6	V	-	
Supply Voltage 7	V33_DA16	2.7	3.3	3.6	V	-	
Supply Voltage 8	REG28	2.7	3.3	3.6	V	-	
Supply Voltage 9	HDMI_V12	1.08	1.2	1.32	V	-	
Supply Voltage 10	V12	1.08	1.2	1.32	V	-	
Operating Current	Іор	-	180	-	mA	@144MHz, V33=3.3V, V12=1.32V, Sensor + ISP + JPEG encode 720p@30fps with 64Mb SDRAM; USB/VDAC/ADAC/CODEC ADC/SAR ADC/HDMI OFF; Not including external SD card, TFT and sensor.	
Sleep Current	l _{PD}	-	2	8.8	mA	BAT_IN=3.6V, V33=3.3V,V12=1.32V All clock and all macro are turn off.	
Power Down Current	I _{PD}		18	25	μА	All power is off except RTC and power control macro(BAT_IN=3.6V, V33=0V, V12=0V)	



Chava staviatia	Symbol		Limits		l lmi4	0 1111	
Characteristic		Min.	Тур.	Max.	Unit	Condition	
High Input Voltage	V_{IH}	0.7V33	-	V33	V	-	
Low Input Voltage	V_{IL}	VSS	-	0.3V33	V	-	
Crystal Frequency 1	-	-	32768	-	Hz	-	
Crystal Frequency 2	F _{CRYSTAL}	-	12	-	MHz	-	
System Clock	F_{SYS}	256Hz ¹	-	144	MHz	-	

Note1: By setting clock divider and changing system clock to SLOW mode (32768Hz).

5.3. Audio DAC Characteristics

Observatoristis		Limits		11-14	O a madifile m
Characteristic	Min. Typ.		Max.	Unit	Condition
Resolution	-	-	16	Bit	-
Full Scale Output Voltage	-	0.6*V33_DA16	-	Vp-p	-
THD+N (Fin = 0.997kHz)	-	0.1	-	%	-
Dynamic Range	71	74	1	dB	Fin=0.997KHz w/ -60dB output loading=32 ohm
Output Loading	32	-	-	ohm	-
Frequency Response	20	-	19200	Hz	-

5.4. Video DAC Characteristics

Characteristic		Limits		1114	O and distinguish	
	Min.	Тур.	Max.	Unit	Condition	
Resolution	-	9	10	Bit	Load=37.5Ohm	
INL	-	±2	-	LSB	-	
DNL	-	±0.3	-	LSB	-	
Voltage Reference Range	1.14	1.235	1.33	V	-	

5.5. CODEC ADC/MIC Characteristics

2		Limits			Condition	
Characteristic	Min.	Тур.	Max.	Unit		
Resolution	-	-	16	Bit	-	
Input Voltage Range	2.7	-	3.6	V	-	
SNR	-	85	-	dB	Boost=0dB, PGA=0dB, filter: 20K LPF + A weighting@V33_DA16=3.3V	
THD+N	-	78	-	dB	Boost=0dB, PGA=0dB, Fin=0.997KHz, Fs=48kHz @V33_DA16=3.3V	
Dynamic Range	-	84.7	-	dB	Boost=0dB, PGA=0dB, filter: 20K LPF + A weighting @V33_DA16=3.3V	
MICBIAS	-	2.45	-	V	-	
VREF	-	1.65	-	V	-	

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Oct. 15, 2014



5.6. SAR ADC Characteristics

Oh ava stavisti sa	Comple of		l lmi4		
Characteristics	Symbol	Min.	Тур.	Max.	Unit
SAR ADC Input Voltage Range	VIN_RANGE	2.7	-	3.6	V
Resolution of ADC	RESO	-	12	-	bits
Signal-to-Noise Plus Distortion of ADC from Line in	SINAD (Note 1)	-	59.88	-	dB
Effective Number of Bit	ENOB (Note 2)	-	9.66	-	bits
Integral Non-Linearity of ADC	INL	-	7	-	LSB (Note 4)
Differential Non-Linearity of ADC	DNL (Note 3)	-	6	-	LSB
No Missing Code		-	10	-	bits
AD Conversion Rate=ADCCLK/16	F _{CONV}	-	-	125K	Hz

Note1: The SINAD testing condition at VINLp-p = 0.8 * V33_AD, F_{CONV} = 62.5KHz, Fin = 1.0KHz Sine waves at V33_AD = 3.0V from the ADC input.

Note2: ENOB = (SINAD - 1.76) / 6.02.

Note3: This ADC can guarantee no missing code at 10 bits resolution.

Note4: LSB means Least Significant Bit (at 12 bits resolution).

5.7. 3.6V-to-3.3V Regulator for IO Characteristics

Observatoristics	0		1114		
Characteristics	Symbol	Min.	Тур.	Max.	Unit
Input Voltage	VREGI	3.0	-	3.6	V
Maximum Current Output	IREGO	1	1	300	mA
Output Voltage	VREGO	3.0	-	3.3	V
Standby Current	IREGS	-	-	2	uA

5.8. 3.3V-to-1.2V Regulator for Core Characteristics

Chamatanistica	Symbol	Limits			1114
Characteristics		Min.	Тур.	Max.	Unit
Input Voltage	VREGI	2.7	-	3.3	V
Maximum Current Output	IREGO	1	-	120	mA
Output Voltage	VREGO	1.08	1.2	1.32	V
Standby Current	IREGS	-	-	2	uA

5.9. 3.6V-to-2.8V Regulator for Sensor Characteristics

0	Symbol	Limits				
Characteristics		Min.	Тур.	Max.	Unit	
Input Voltage	VREGI	3.0	-	3.6	V	
Maximum Current Output	IREGO	1	-	60	mA	
Output Voltage	VREGO	2.8	3.3	3.3	V	
Standby Current	IREGS	1	-	2	uA	

5.10. 3.6V-to-3.3V Regulator for CODEC ADC/SAR ADC/Audio DAC Characteristics

Observatoristics	Symbol	Limits			1114
Characteristics		Min.	Тур.	Max.	Unit
Input Voltage	VREGI	3.0	-	3.6	V
Maximum Current Output	IREGO	1	-	20	mA





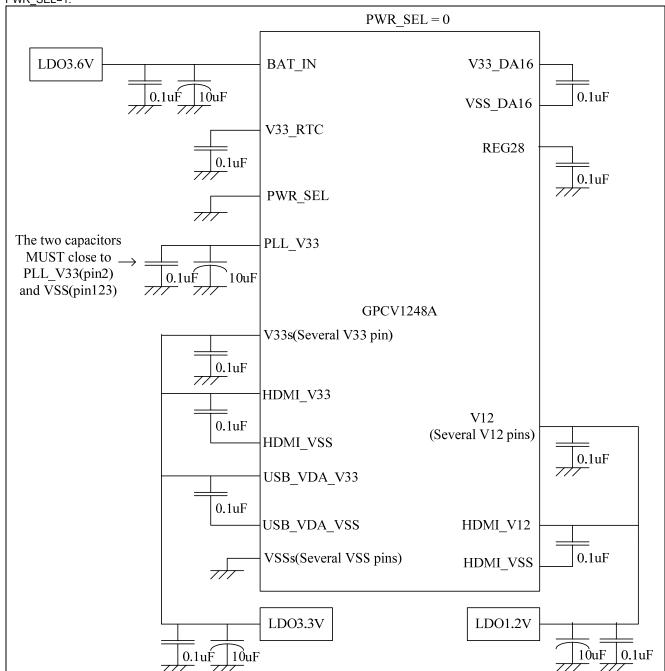
Chamadaviation	Symbol	Limits			11-24	
Characteristics		Min.	Тур.	Max.	Unit	
Output Voltage	VREGO	3.0	3.3	3.3	V	
Standby Current	IREGS	-	-	2	uA	



6. RECOMMENDED BOARD LAYOUT

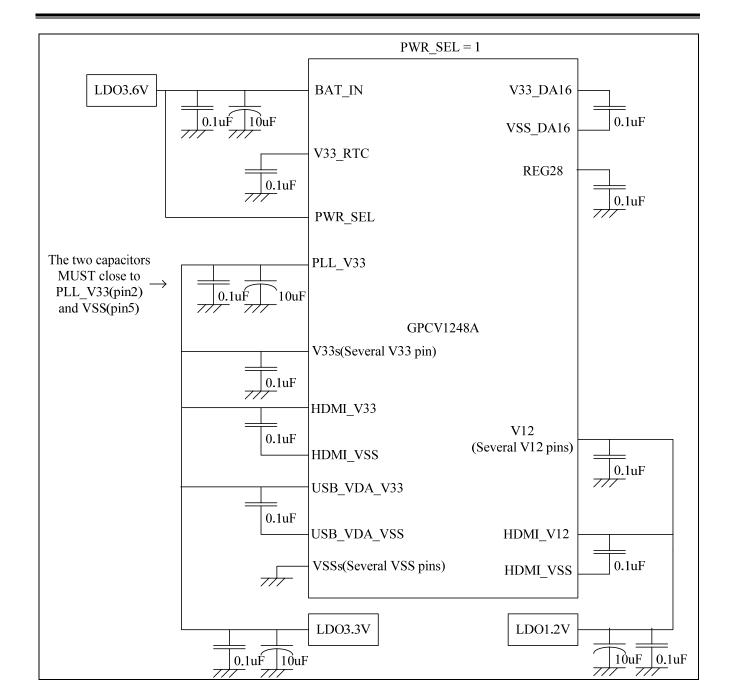
6.1. Power and Ground

All power and ground pins are connected as in the following diagram for general application. The decoupling capacitor of $0.1\mu F$ and $10\mu F$ should be connected to each corresponding power pin of the IC and $0.1\mu F$ capacitor must be as close as possible to the power pin. Each V33/V12 needs one $0.1\mu F$ capacitor and must be as close as possible to the power pin. There are two power settings which can be selected by PWR_SEL pin. With PWR_SEL=0, the internal LDO33 will be enabled. Internal LDO33 will always be disabled if PWR SEL=1.



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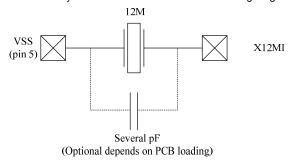




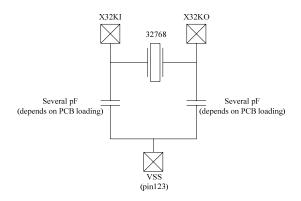


6.2. Crystal and PLL

When the 12MHz crystal is applied in the system, please connect the crystal circuit as indicated in the following diagram.



Note*: Please refer to the crystal's application circuit.



A Crystal (32768Hz) may be used for applications requiring precise time clocks. See the above diagram for details. **Note*:** Please refer to the crystal's application circuit.



7. PACKAGE/PAD LOCATIONS

7.1. Ordering Information

Product Number	Package Type		
GPCV1248A-NnnV-QL09x	Halogen Free Package		

Note1: Code number is assigned for customer.

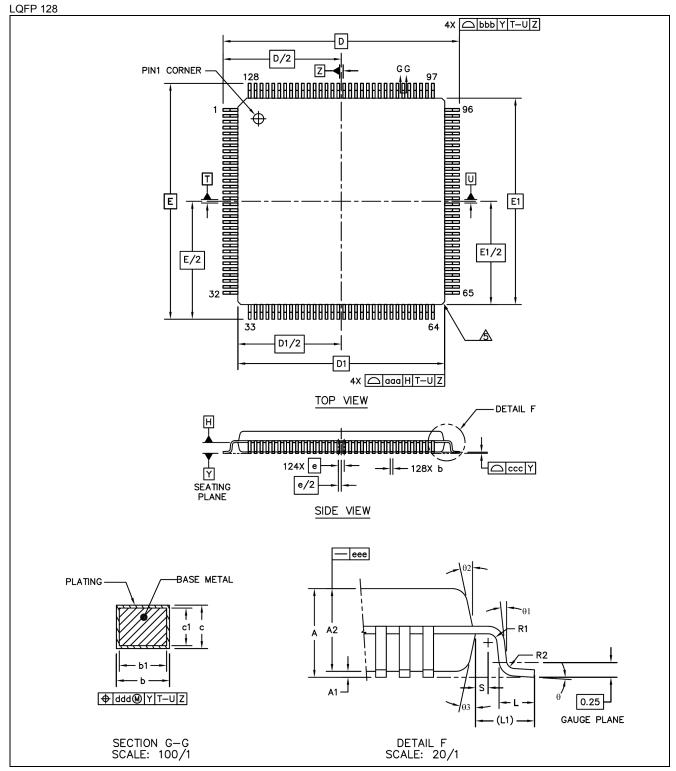
Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 1 - 9, serial number).



7.2. Package Information



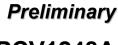


Symbol	Millimeter			
	Min.	Nom.	Max.	
Α	-	-	1.60	
A1	0.05	-	0.15	
A2	1.35	1.40	1.45	





Symbol	Millimeter			
	Min.	Nom.	Max.	
b	0.13	0.16	0.23	
b1	0.13	-	0.19	
С	0.09	-	0.20	
c1	0.09	-	0.16	
D		16.00 BSC		
E		16.00 BSC		
D1		14.00 BSC		
E1		14.00 BSC		
е	0.40 BSC			
L	0.45	0.60	0.75	
L1		1.00 REF		
θ	0°	3.5°	7°	
θ1	0°	-	_°	
θ2	11°	12°	13°	
θ3	11°	12°	13°	
R1	0.08	-	-	
R2	0.08	-	0.20	
S	0.20	-	-	
aaa		0.10		
bbb		0.20		
ccc		0.08		
ddd		0.07		
eee		0.05		





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9. REVISION HISTORY

Date	Revision #	Description	Page
Oct. 15, 2014	0.2	Modify pin67 and pin68 pad sequence	6,8
Aug. 28, 2014	0.1	Preliminary version.	20