RESET-Failure of HfO_2-Based Memristors at Cryogenic Temperatures

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Abstract

Memristors are two-terminal memory devices with programmable resistance, first theorized by Leon Chua in 1971 and fabricated by Hewlett-Packard in 2008. Recent advancements in manufacturing have made memristors more accessible. With the integration of CMOS, there are hopes of developing an in-memory computation system, particularly for environments requiring cryogenic operation, such as space or quantum computing systems. This study investigates RESET failure in HfO_2-based memristors at cryogenic temperatures. RESET failure is defined as a destructive event in which the device becomes permanently stuck at a fixed resistance. Using a B1500A Semiconductor Device Analyzer and a FormFactor PMC200 cryogenic probe station, the applied RESET voltage was progressively lowered at 77 K until failure occurred. Results indicate a wider range of HRS and LRS values for memristors at 77 K compared to room temperature. Memristors at 77K fail at or below -1.773 volts which is higher than room temperature devices at around -1.8 volts. However memristors at cryogenic temperatures fail more consistently than room temperature counterparts.

Key Words– Memristor, Reset Failure, B1500A, Cryogenic Temperatures.

1. Introduction

The purpose of this study is to investigate RESET failure in HfO_2-based memristors at cryogenic temperatures. This work builds on a previous study that examined RESET failure in similar devices at room temperature. Memristors are currently being explored for a variety of applications, including memory systems and neuromorphic computing. Ongoing research aims to integrate memristors into cryogenic environments, such as those found in space systems or quantum computing, where qubits operate at millikelvin temperatures. This study aims to provide further insight into the RESET characteristics of memristors at cryogenic temperatures, with the goal of improving existing memristor models and supporting more informed system-level design. The rest of the report is organized as follows, a brief review on the device physics and previous works. The methods and tests used in the evaluations. The measured results from said tests. Conclusions about finding and future recommendations.

2. Background

2.1 Device Physics

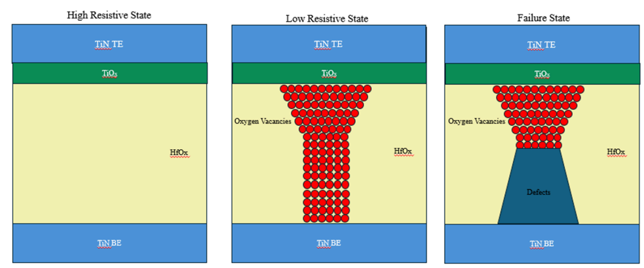

Figure 1: Diagram of HRS LRS and Failure State

A Memristors is a programmable piece of hardware with a variable resistive state. Ideal memristors are non volatile and can hold a specific resistive state indefinitely. The resistive state is based on the current accumulated over time. In this work there are two distinct states, a High Resistive State (HRS) and a Low Resistive State (LRS). In theory the device would be able to hold a number of intermediate states however we are only able to achieve two. The resistive state of a memristor is modulated by the movement of oxygen anions across filament layers. As seen in Figure 1 applying a voltage forms conductive channels, while reversing the polarity breaks them. It is hypothesized that increasing the reset voltage introduces defects into the filaments, causing the HRS and Low Resistive State LRS to converge, potentially leading to device shorting.[1].

2.2 Previous Study

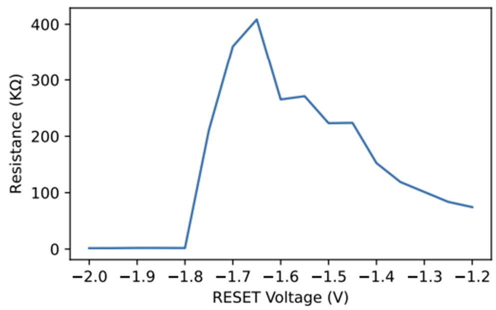

Figure 2: Example of Previous Resistance vs Reset Voltage Findings [1]

RESET-Failure as defined in the previous study is the max voltage applied across the device in which HRS and LRS converge and the memristor becomes stuck in a LRS. The nominal reset voltage was targeted at -1.5V. A switching cycle was applied to memristors, transitioning them from a High Resistive State (HRS) to a Low Resistive State (LRS), and then back to HRS while gradually decreasing the reset voltage. Partial reset occurred when the magnitude of the reset voltage was not large enough. As seen in Figure 2 the highest achieved HRS was 400k Ω, applying a reset voltage below -1.8 V permanently fixed the device at approximately 1.5k Ω.[1]

3. Methods and Testing

3.1 Equipment Used

Figure 3: FormFactor PMC200 Probe Machine

In order to test the 1T1R memristors on the Ravens 1 Chip a FormFactor PMC200 Probe Machine was used as seen in Figure 3. As seen in Figure 4 three probes were used, one for the top of the memristor, one to act as the ground and one to activate the gate of the NMOS.

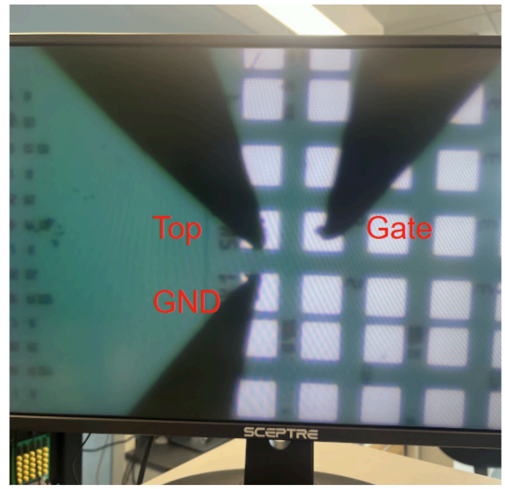

Figure 4: Microscope of Probe Machine and Touch Pads

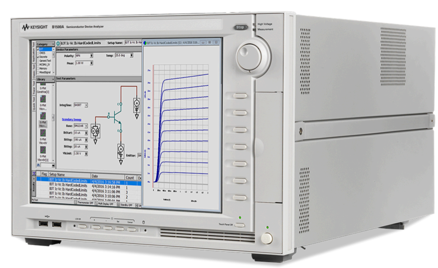

Figure 5: Keysight B1500A Semiconductor Tester

The waveform was applied using a Keysight B1500A Semiconductor Device Analyzer displayed in Figure 5. The setup included three Source Measurement Units (SMUs) and two Waveform Generator/Fast Measurement Units (WGFMUs). To switch between the WGFMUs and SMUs, two Remote Sense and Switch Units (RSUs) were used. [2]. Figure 6 below illustrates the full connection and setup.

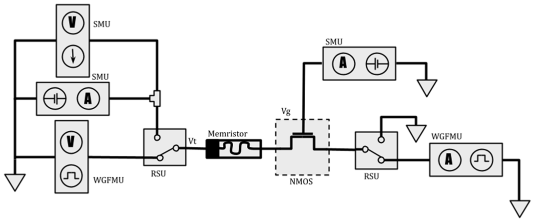

Figure 6: Circuit Diagram of Test Setup

Two SMUs are connected via a T-joint and routed into the top RSU. A WGFMU is also connected to this RSU, which then leads to the back left probe of the probe station, making contact with the top of the memristor. Another SMU is connected directly to the back right probe, which interfaces with the gate of the NMOS transistor. A second WGFMU is connected to a separate RSU, which also includes a ground connection. This second RSU is linked to the front left probe, which connects to the source of the NMOS.

3.2 Programming

The B1500A was programmed using two different libraries. The SMUs were controlled using the publicly available PyVISA packages. [3]. The WGFMU's were controlled using a custom set of pybinding which adapted C++ controls from the manufacturers.[4,5]. All code is available in the neuromorphic-utk BitBucket under a folder labeled probe station.

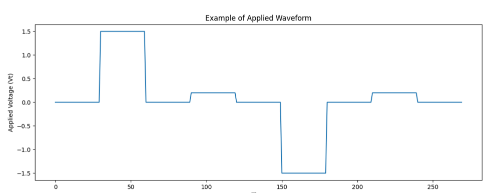

Figure 7: Example of Applied Waveform

The main test file is named read_test.py. [6]. Figure 7 displays an example of the basic waveform used. The first pulse is the forming step which uses the WGFMU at the top to apply a voltage while the bottom WGFMU at the bottom acts as a ground reading the current. The second step is a read step which switches to the SMU's. The first SMU applies a small voltage while also reading the current through. The second SMU reads the voltage applied. The third step switches back to the WGFMU's to apply the reset step which sees a negative voltage applied across the memristor. Finally a second read step is applied.

3.3 Tests

Three different tests were used on each memristor. A Binary Variation, Analog Programming, and finally a Reset Failure test.

3.3.1 Binary Variation

The Binary Variation test was performed to verify memristor functionality and to collect data on LRS and HRS variability. The test consisted of 10 cycles, where the memristor was alternately set to LRS and reset to HRS using the standard waveform shown in Figure 7. The set voltage peaked at 1.5 V, and the reset voltage at -1.5 V. The gate voltage was fixed at 1.2 V throughout the test.

3.3.2 Analog Programming

The Analog Programming test evaluated the memristor's analog tuning capability at cryogenic temperatures. It used the same basic waveform and set/reset voltages as in the Binary Variation test. However, during the set phase, the gate voltage was varied from 0.5 V to 1.6 V to assess the device's response to different control levels. During the reset phase, the gate voltage remained constant at 1.2 V to ensure a complete reset to HRS. A total of 32 different gate voltages were tested.

3.3.3 Reset Failure

The Reset Failure test aimed to characterize the maximum reset voltage that could be applied before the device failed to return to HRS. The standard waveform was used, with a set voltage of 1.5 V and a fixed gate voltage of 1.2 V. The reset voltage was gradually decreased between cycles, ranging from -1.5 V to -2.5 V. Multiple tests were conducted across this voltage range to observe the failure threshold.

4. Results

The data was formatted into JSON files and then read using a python script labeled plot-read_data.py[7] which uses the numpy and matplotlib libraries.

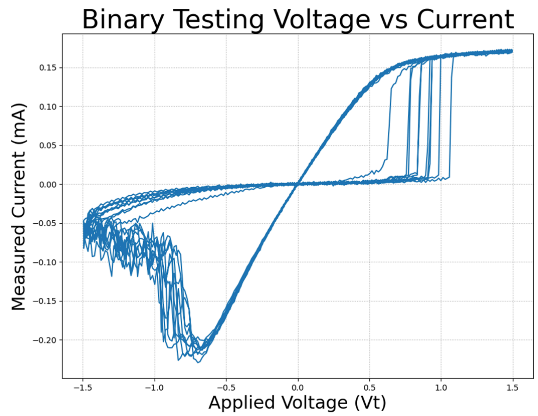

Figure 8: Example of Voltage vs Current Graph for Binary Test Cycles

Figure 8 displays an example of an applied voltage vs measured current curve for a binary variation test of one memristor.

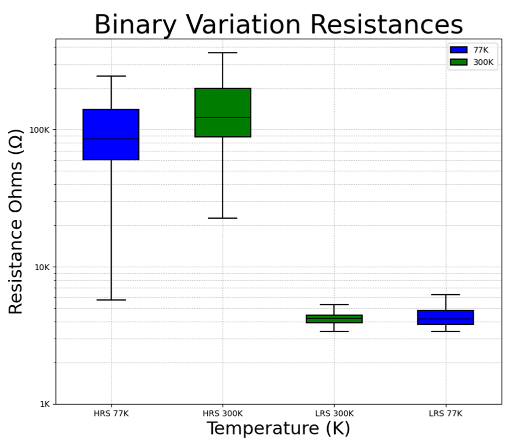

Figure 9: LRS and HRS of Binary Test

Figure 9 displays the measured HRS and LRS for the two different temperatures.

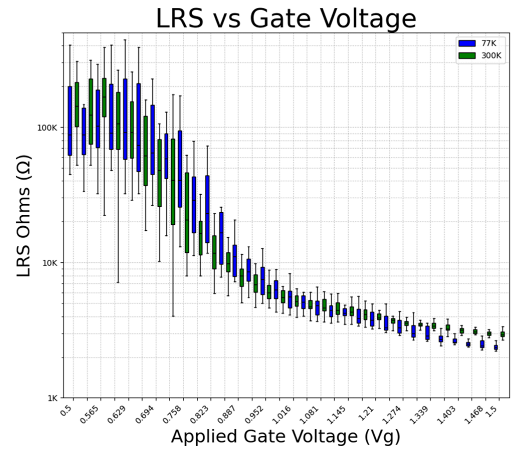

Figure 10: LRS of Analog Programming Test

Figure 10 displays the measured LRS vs the gate voltage applied during the set step.

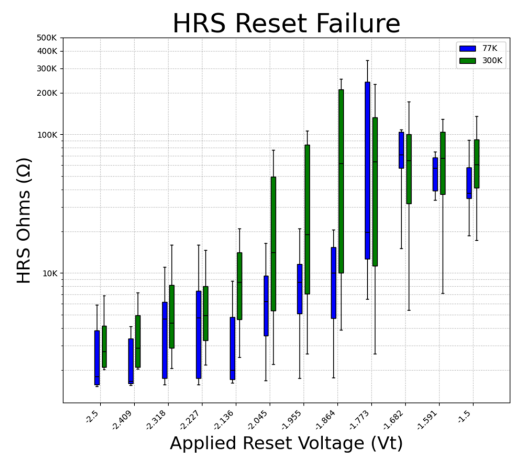

Figure 11: HRS of Reset Failure Test

Figure 11 displays the measured HRS value vs the applied reset voltage.

5. Conclusion

Only data from working memristors was considered in our analysis. About 2 out of every 3 memristors were faulty and deemed unusable. Main takeaways from the data are:

- The binary test results show a wide variation in both HRS and LRS values.
- Memristors tested at 300K had slightly higher average HRS values and tighter distributions.
- Analog programming tests reveal that gate voltages below 1 V are insufficient to properly set the memristor.

- Reset failure tests indicate that memristors at 77K tend to fail at a higher reset voltage, around -1.773 V.
- These failures also occur more consistently at 77K than at room temperature.

Circuit designs using memristors require special consideration to ensure reliable operation in cryogenic environments. One of the main challenges is still reliability and consistency of manufactured memristors.

6. Acknowledgments

Thank you to Dr. Ahmedullah Aziz for use of the B1500A and to Graham Buchanan for support throughout the project Appreciation is also given to SUNY Polytechnic Institute for fabricating the 1T1R memristors. Finally thank you to the National Science Foundation for funding author Kanoa Parker's Undergraduate Research Experience at the University of Tennessee Knoxville.

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