

AD8603/AD8607/AD8609

FEATURES

Low offset voltage: 50 μ V maximum
Low input bias current: 1 pA maximum
Single-supply operation: 1.8 V to 5 V
Low noise: 22 nV/ $\sqrt{\text{Hz}}$
Micropower: 50 μ A maximum
Low distortion
No phase reversal
Unity gain stable

APPLICATIONS

Battery-powered instrumentation
Multipole filters
Sensors
Low power ASIC input or output amplifiers

GENERAL DESCRIPTION

The AD8603/AD8607/AD8609 are single/dual/quad micro-power rail-to-rail input and output amplifiers, respectively, that feature very low offset voltage as well as low input voltage and current noise.

These amplifiers use a patented trimming technique that achieves superior precision without laser trimming. The parts are fully specified to operate from 1.8 V to 5.0 V single supply or from ± 0.9 V to ± 2.5 V dual supply. The combination of low offsets, low noise, very low input bias currents, and low power consumption makes the AD8603/AD8607/AD8609 especially useful in portable and loop-powered instrumentation.

The ability to swing rail to rail at both the input and output enables designers to buffer CMOS ADCs, DACs, ASICs, and other wide output swing devices in low power, single-supply systems.

The AD8603 is available in a tiny 5-lead TSOT package. The AD8607 is available in 8-lead MSOP and 8-lead SOIC packages. The AD8609 is available in 14-lead TSSOP and 14-lead SOIC packages.

PIN CONFIGURATIONS

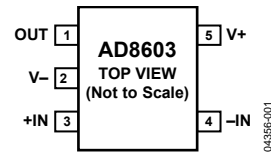


Figure 1. 5-Lead TSOT (UJ Suffix)



Figure 2. 8-Lead MSOP (RM Suffix)

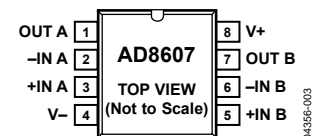


Figure 3. 8-Lead SOIC (R Suffix)

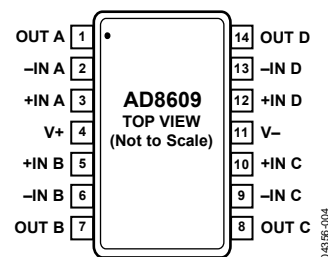


Figure 4. 14-Lead TSSOP (RU Suffix)

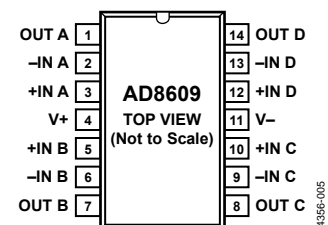


Figure 5. 14-Lead SOIC (R Suffix)

Rev. C

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REVISION HISTORY

6/08—Rev. B to Rev. C

Changes to Table 1	3
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Changes to Figure 15.....	7
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Changes to Figure 45 and Figure 47	13
Updated Outline Dimensions	14
Changes to Ordering Guide	16

6/05—Rev. A to Rev. B

Updated Figure 49	15
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10/03—Rev. 0 to Rev. A

Added AD8607 and AD8609 Parts	Universal
Changes to Specifications	3
Changes to Figure 35.....	10
Added Figure 41.....	11

8/03—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

$V_S = 5\text{ V}$, $V_{CM} = V_S/2$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V _{OS}	V _S = 3.3 V @ V _{CM} = 0.5 V and 2.8 V		12	50	μV
		−0.3 V < V _{CM} < +5.2 V		40	300	μV
		−40°C < T _A < +125°C, −0.3 V < V _{CM} < +5.2 V			700	μV
Offset Voltage Drift	ΔV _{OS} /ΔT	−40°C < T _A < +125°C		1	4.5	μV/°C
Input Bias Current	I _B			0.2	1	pA
		−40°C < T _A < +85°C			50	pA
		−40°C < T _A < +125°C			500	pA
Input Offset Current	I _{OS}			0.1	0.5	pA
		−40°C < T _A < +85°C			50	pA
		−40°C < T _A < +125°C			250	pA
Input Voltage Range	IVR		−0.3		+5.2	V
Common-Mode Rejection Ratio	CMRR	0 V < V _{CM} < 5 V	85	100		dB
		−40°C < T _A < +125°C	80			dB
Large Signal Voltage Gain	A _{VO}	R _L = 10 kΩ, 0.5 V < V _O < 4.5 V				
AD8603			400	1000		V/mV
AD8607/AD8609			250	450		V/mV
Input Capacitance	C _{DIFF} C _{CM}			1.9		pF
				2.5		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V _{OH}	I _L = 1 mA	4.95	4.97		V
		−40°C to +125°C	4.9			V
		I _L = 10 mA	4.65	4.97		V
		−40°C to +125°C	4.50			V
Output Voltage Low	V _{OL}	I _L = 1 mA		16	30	mV
		−40°C to +125°C			50	mV
		I _L = 10 mA		160	250	mV
		−40°C to +125°C			330	mV
Short-Circuit Current	I _{SC}			±70		mA
Closed-Loop Output Impedance	Z _{OUT}	f = 10 kHz, A _V = 1		36		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	1.8 V < V _S < 5 V	80	100		dB
Supply Current per Amplifier	I _{SY}	V _O = 0 V		40	50	μA
		−40°C < T _A < +125°C			60	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R _L = 10 kΩ		0.1		V/μs
Settling Time 0.1%	t _S	G = ±1, 2 V step		23		μs
Gain Bandwidth Product	GBP	R _L = 100 kΩ		400		kHz
		R _L = 10 kΩ		316		kHz
Phase Margin	∅ _O	R _L = 10 kΩ, R _L = 100 kΩ		70		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e _{n p-p}	0.1 Hz to 10 Hz		2.3	3.5	μV
Voltage Noise Density	e _n	f = 1 kHz		25		nV/√Hz
		f = 10 kHz		22		nV/√Hz
Current Noise Density	i _n	f = 1 kHz		0.05		pA/√Hz
Channel Separation	C _S	f = 10 kHz		−115		dB
		f = 100 kHz		−110		dB

AD8603/AD8607/AD8609

$V_S = 1.8\text{ V}$, $V_{CM} = V_S/2$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_S = 3.3\text{ V}$ @ $V_{CM} = 0.5\text{ V}$ and 2.8 V $-0.3\text{ V} < V_{CM} < +1.8\text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$, $-0.3\text{ V} < V_{CM} < +1.8\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$, $-0.3\text{ V} < V_{CM} < +1.7\text{ V}$		12 40	50 300	μV μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	4.5	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.2	1	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.1	0.5	pA
Input Voltage Range	IVR	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-0.3		+1.8	V
Common-Mode Rejection Ratio	CMRR	$0\text{ V} < V_{CM} < 1.8\text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$	80 70	98		dB dB
Large Signal Voltage Gain	A_{VO}	$R_L = 10\text{ k}\Omega$, $0.5\text{ V} < V_O < 4.5\text{ V}$	150	3000		V/mV
AD8603			100	2000		V/mV
AD8607/AD8609						
Input Capacitance	C_{DIFF} C_{CM}			2.1 3.8		pF pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 1\text{ mA}$ -40°C to $+125^\circ\text{C}$	1.65 1.6	1.72		V V
Output Voltage Low	V_{OL}	$I_L = 1\text{ mA}$ -40°C to $+125^\circ\text{C}$		38	60 80	mV mV
Short-Circuit Current	I_{SC}			± 10		mA
Closed-Loop Output Impedance	Z_{OUT}	$f = 10\text{ kHz}$, $A_V = 1$		36		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$1.8\text{ V} < V_S < 5\text{ V}$	80	100		dB
Supply Current per Amplifier	I_{SY}	$V_O = 0\text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$		40	50 60	μA μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$		0.1		V/ μs
Settling Time 0.1%	t_S	$G = \pm 1$, 1 V step		9.2		μs
Gain Bandwidth Product	GBP	$R_L = 100\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$		385 316		kHz kHz
Phase Margin	$\angle O$	$R_L = 10\text{ k}\Omega$, $R_L = 100\text{ k}\Omega$		70		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	$e_{n\text{ p-p}}$	0.1 Hz to 10 Hz		2.3	3.5	μV
Voltage Noise Density	e_n	$f = 1\text{ kHz}$ $f = 10\text{ kHz}$		25 22		nV/ $\sqrt{\text{Hz}}$ nV/ $\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 1\text{ kHz}$		0.05		pA/ $\sqrt{\text{Hz}}$
Channel Separation	C_S	$f = 10\text{ kHz}$ $f = 100\text{ kHz}$		-115 -110		dB dB

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	GND to V_S
Differential Input Voltage	± 6 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
Operating Temperature Range	–40°C to +125°C
Junction Temperature Range	–65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Package Characteristics

Package Type	θ_{JA} ¹	θ_{JC}	Unit
5-Lead TSOT (UJ)	207	61	°C/W
8-Lead MSOP (RM)	210	45	°C/W
8-Lead SOIC_N (R)	158	43	°C/W
14-Lead SOIC_N (R)	120	36	°C/W
14-Lead TSSOP (RU)	180	35	°C/W

¹ θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for a device soldered in a circuit board for surface-mount packages.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

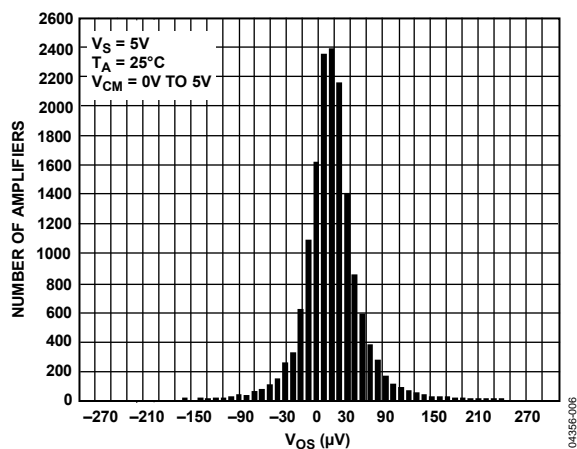


Figure 6. Input Offset Voltage Distribution

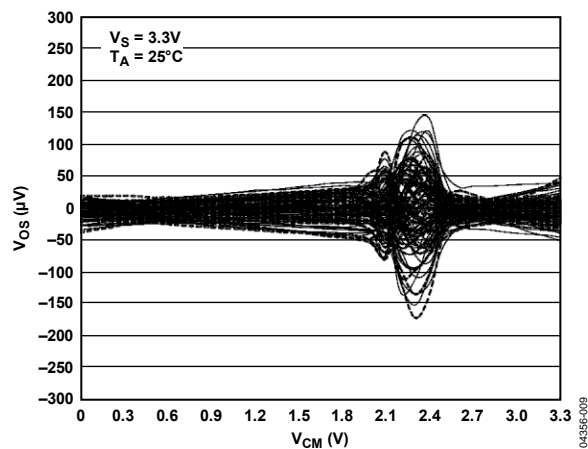


Figure 9. Input Offset Voltage vs. Common-Mode Voltage

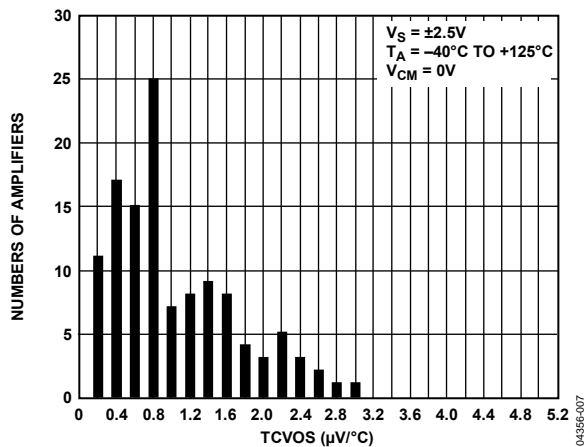


Figure 7. Input Offset Voltage Drift Distribution

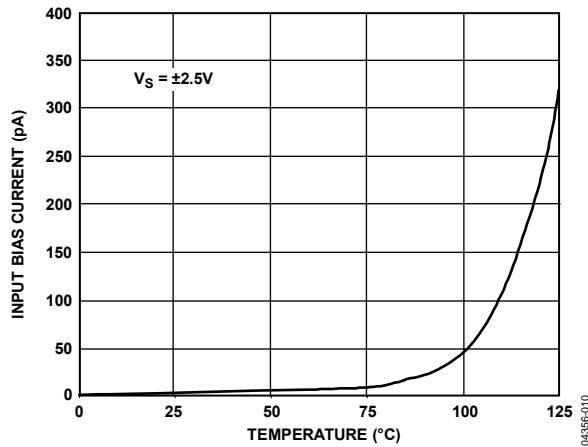


Figure 10. Input Bias Current vs. Temperature

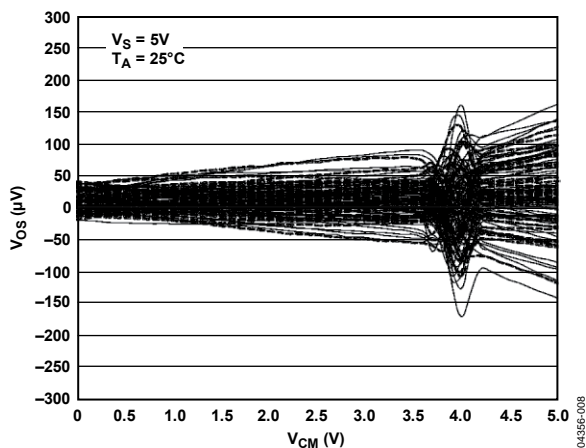


Figure 8. Input Offset Voltage vs. Common-Mode Voltage

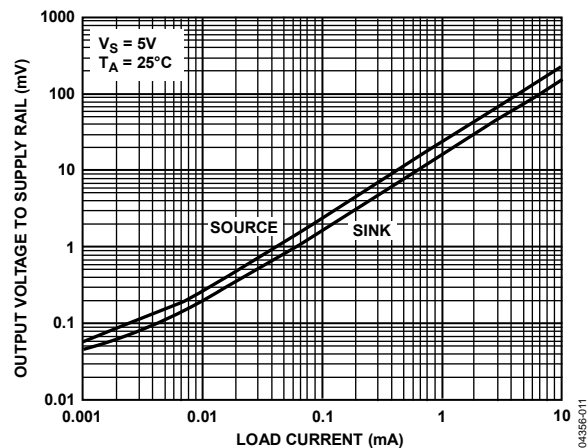


Figure 11. Output Voltage to Supply Rail vs. Load Current

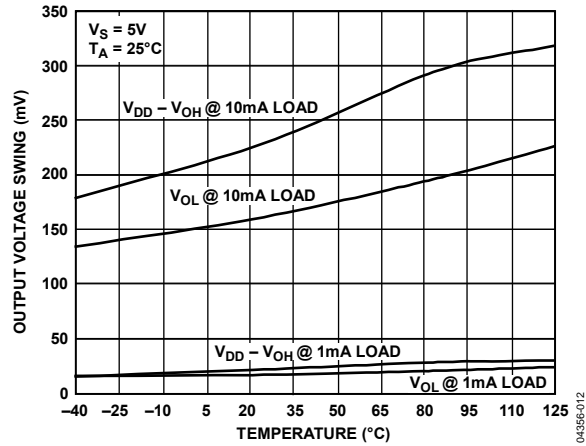


Figure 12. Output Voltage Swing vs. Temperature

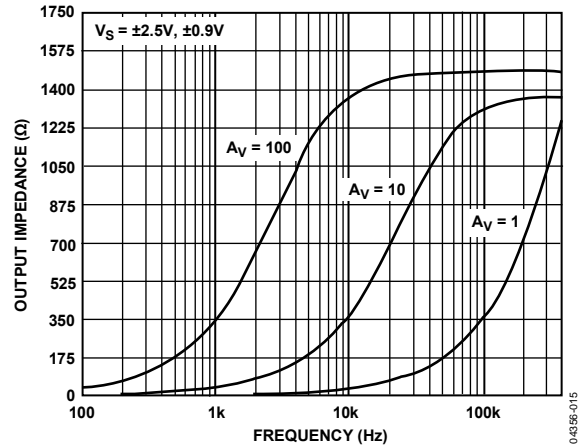


Figure 15. Output Impedance vs. Frequency

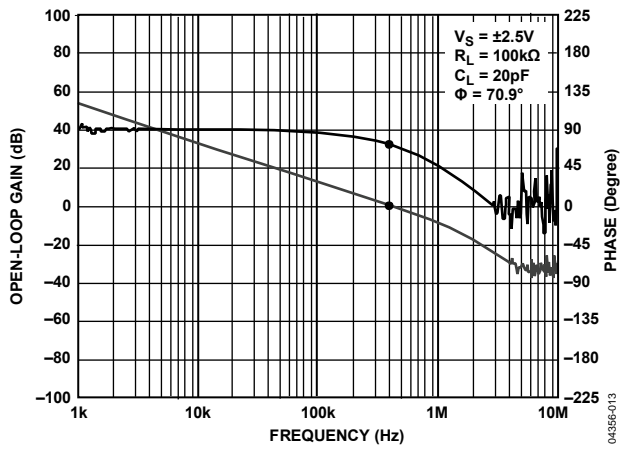


Figure 13. Open-Loop Gain and Phase vs. Frequency

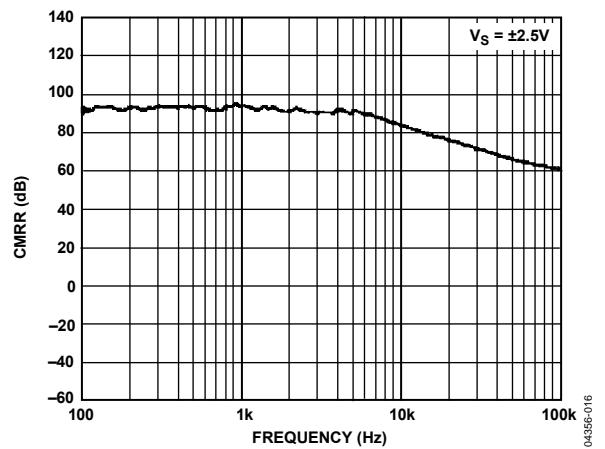


Figure 16. CMRR vs. Frequency

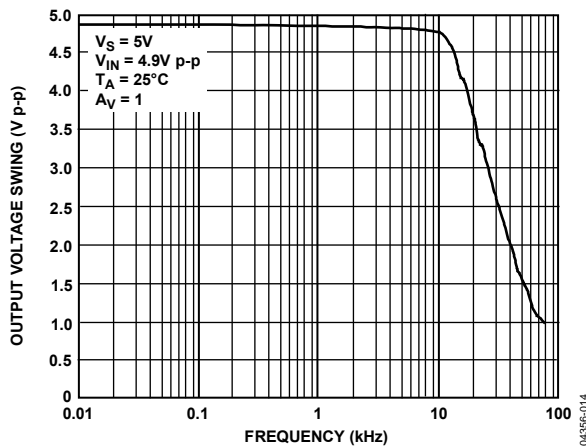


Figure 14. Closed-Loop Output Voltage Swing vs. Frequency

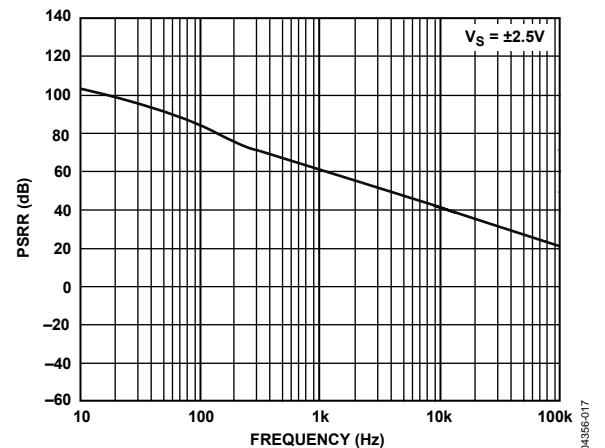


Figure 17. PSRR vs. Frequency

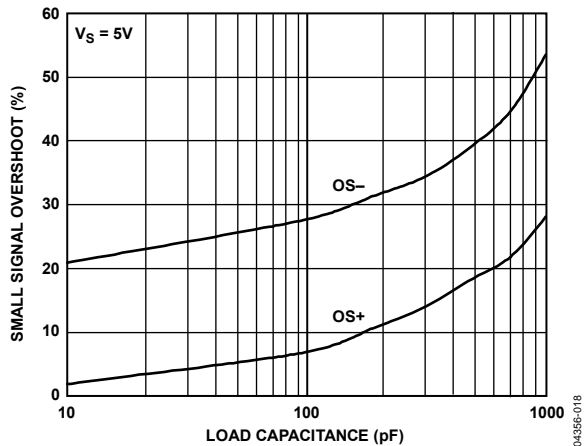


Figure 18. Small Signal Overshoot vs. Load Capacitance

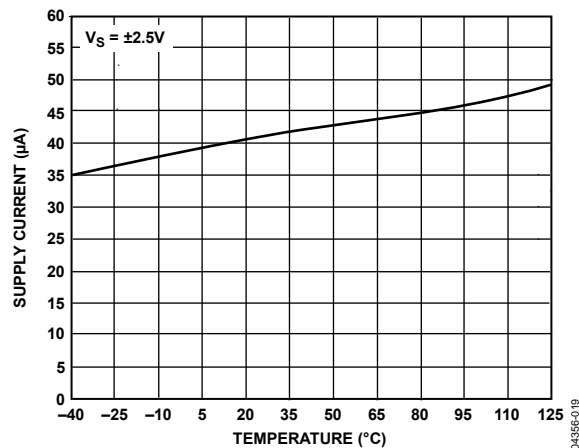


Figure 19. Supply Current vs. Temperature

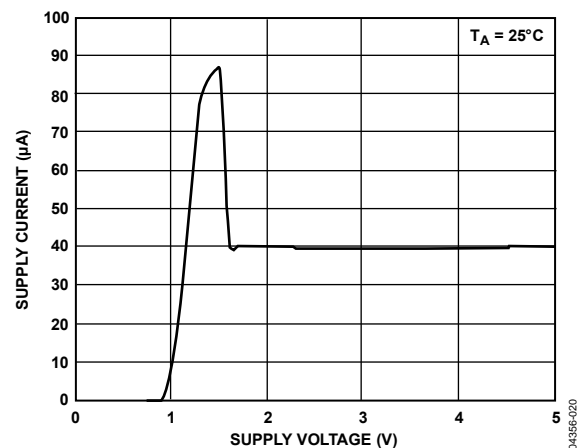


Figure 20. Supply Current vs. Supply Voltage

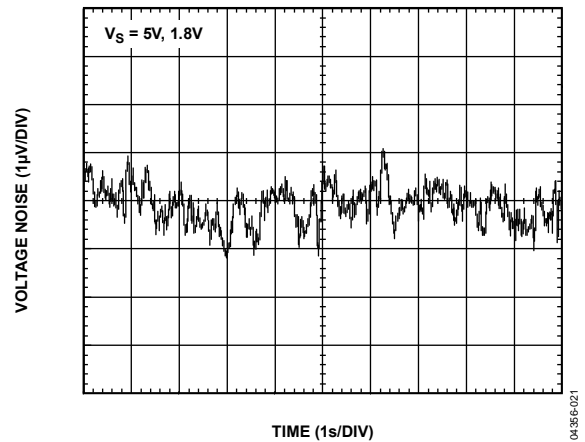


Figure 21. 0.1 Hz to 10 Hz Input Voltage Noise

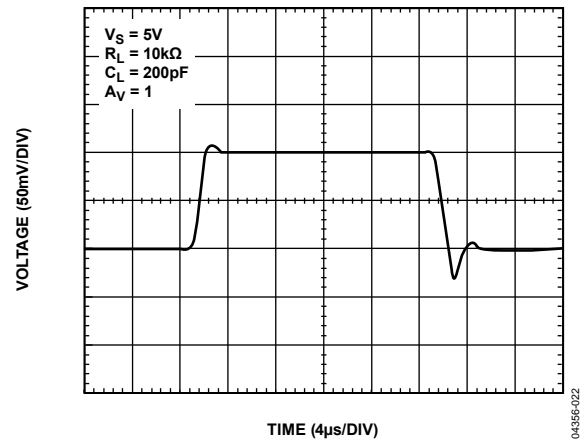


Figure 22. Small Signal Transient

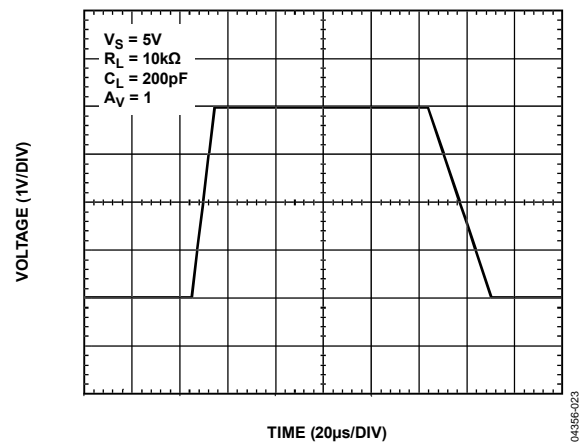


Figure 23. Large Signal Transient

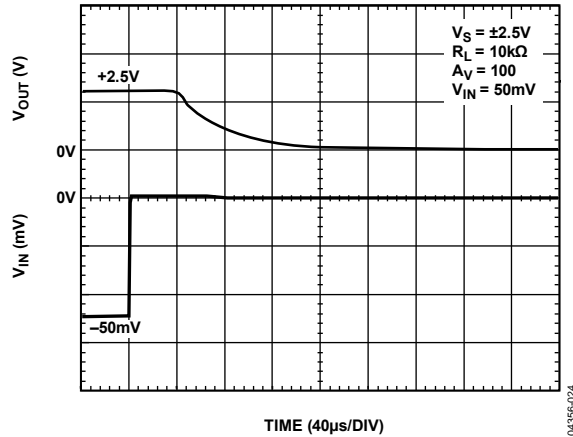


Figure 24. Negative Overload Recovery

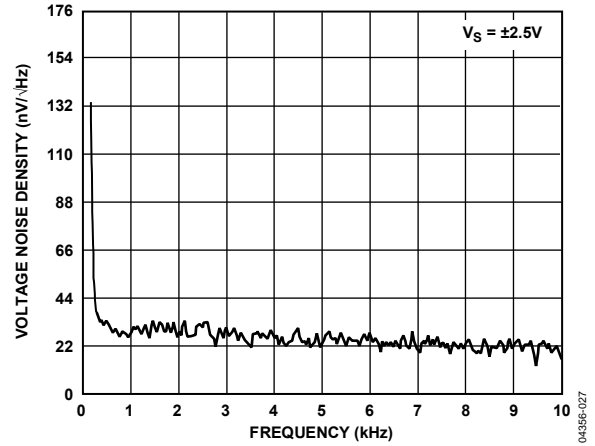


Figure 27. Voltage Noise Density vs. Frequency

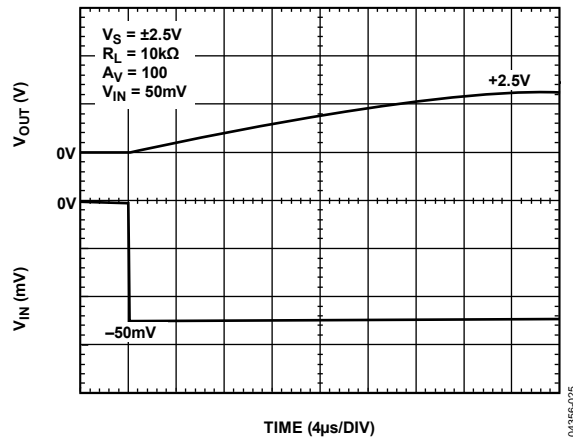


Figure 25. Positive Overload Recovery

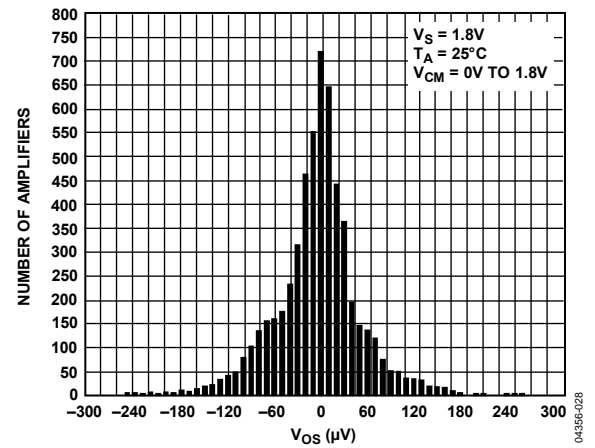


Figure 28. V_{OS} Distribution

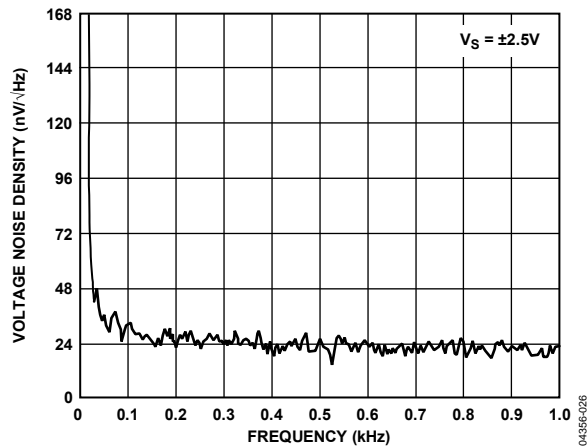


Figure 26. Voltage Noise Density vs. Frequency

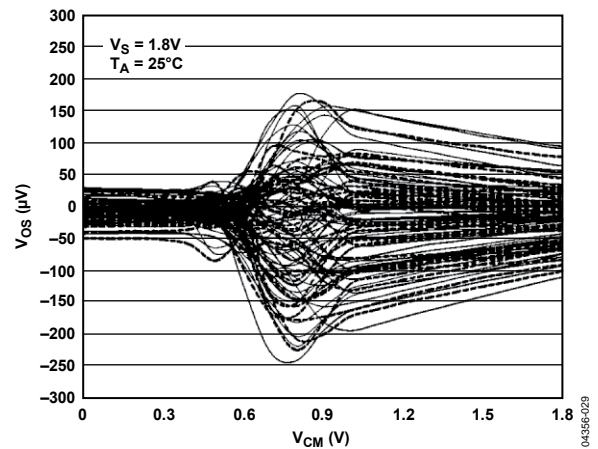


Figure 29. Input Offset Voltage vs. Common-Mode Voltage

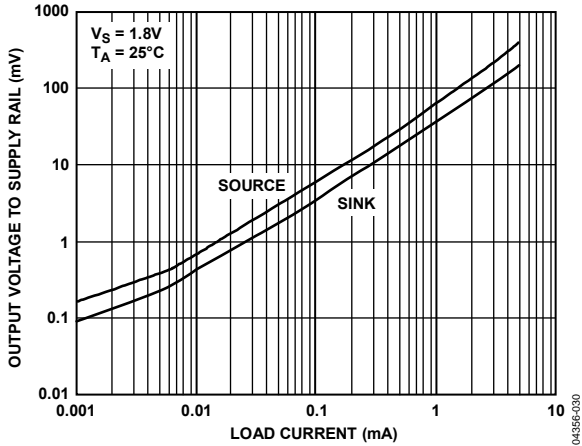


Figure 30. Output Voltage to Supply Rail vs. Load Current

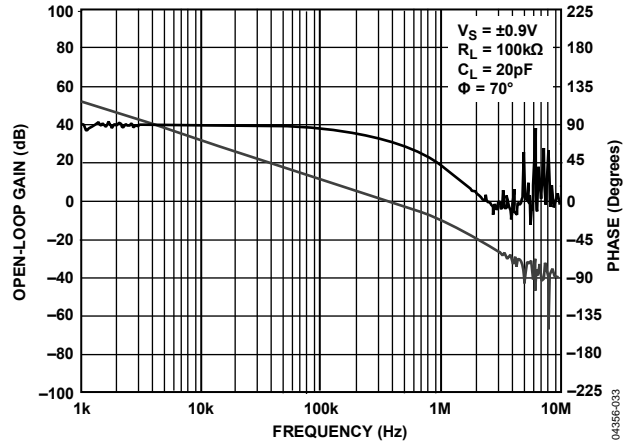


Figure 33. Open-Loop Gain and Phase vs. Frequency

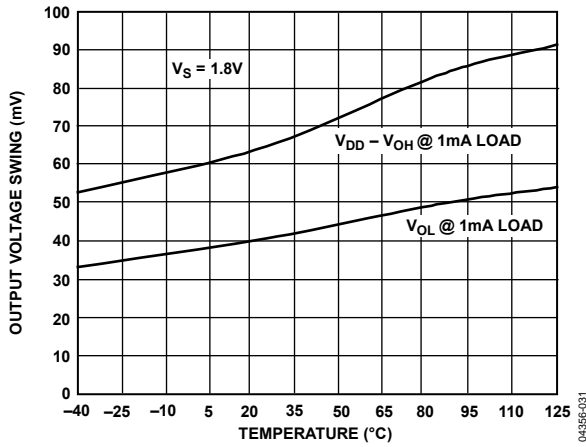


Figure 31. Output Voltage Swing vs. Temperature

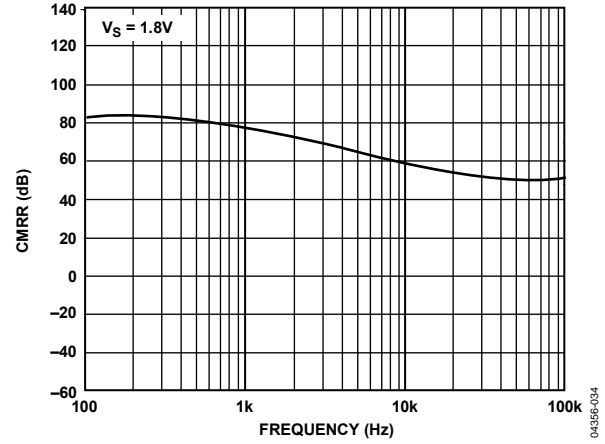


Figure 34. CMRR vs. Frequency

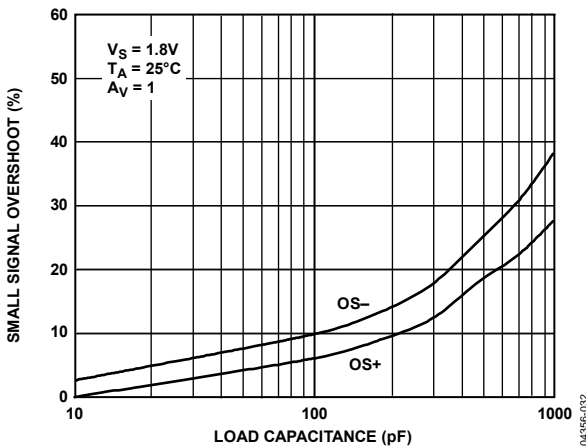


Figure 32. Small Signal Overshoot vs. Load Capacitance

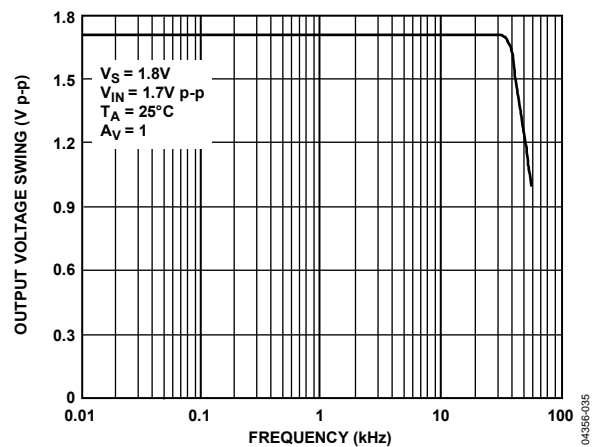


Figure 35. Closed-Loop Output Voltage Swing vs. Frequency

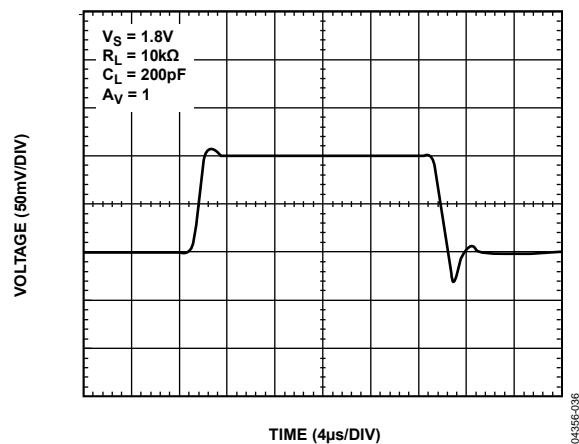


Figure 36. Small Signal Transient

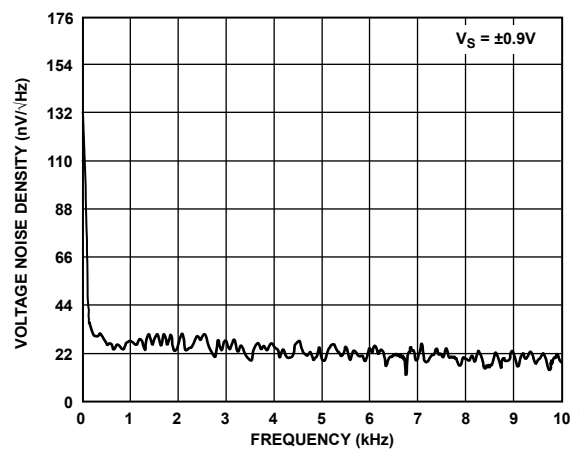


Figure 39. Voltage Noise Density vs. Frequency

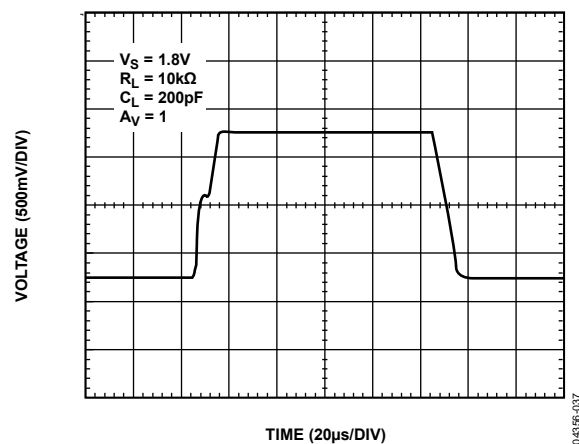


Figure 37. Large Signal Transient

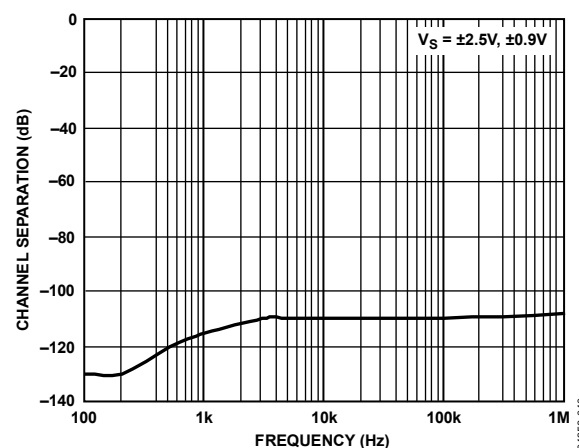


Figure 40. Channel Separation vs. Frequency

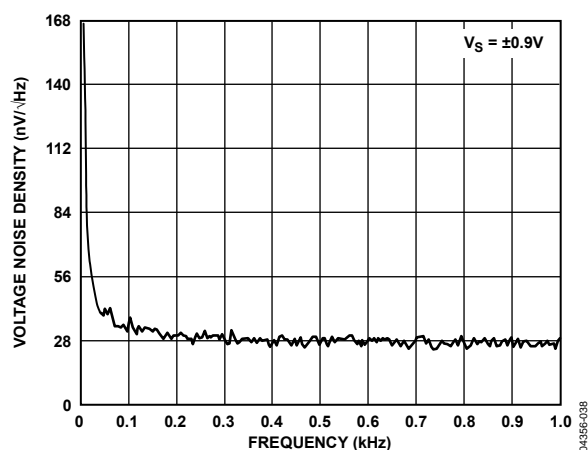


Figure 38. Voltage Noise Density vs. Frequency

APPLICATIONS

NO PHASE REVERSAL

The AD8603/AD8607/AD8609 do not exhibit phase inversion even when the input voltage exceeds the maximum input common-mode voltage. Phase reversal can cause permanent damage to the amplifier, resulting in system lockups. The AD8603/AD8607/AD8609 can handle voltages of up to 1 V over the supply.

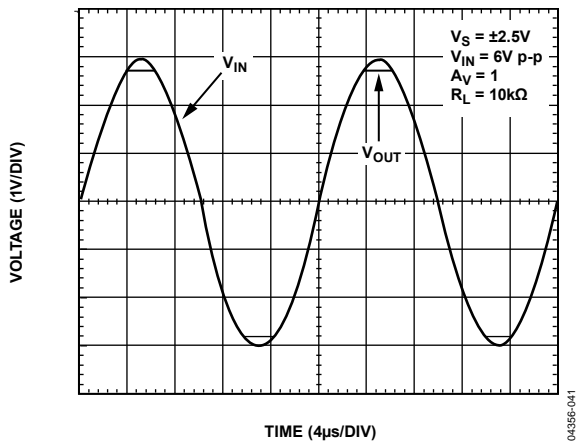


Figure 41. No Phase Response

INPUT OVERVOLTAGE PROTECTION

If a voltage 1 V higher than the supplies is applied at either input, the use of a limiting series resistor is recommended. If both inputs are used, each one should be protected with a series resistor.

To ensure good protection, the current should be limited to a maximum of 5 mA. The value of the limiting resistor can be determined from the following equation:

$$(V_{IN} - V_S)/(R_S + 200 \Omega) \leq 5 \text{ mA}$$

DRIVING CAPACITIVE LOADS

The AD8603/AD8607/AD8609 are capable of driving large capacitive loads without oscillating. Figure 42 shows the output of the AD8603/AD8607/AD8609 in response to a 100 mV input signal, with a 2 nF capacitive load.

Although it is configured in positive unity gain (the worst case), the AD8603 shows less than 20% overshoot. Simple additional circuitry can eliminate ringing and overshoot.

One technique is the snubber network, which consists of a series RC and a resistive load (see Figure 43). With the snubber in place, the AD8603/AD8607/AD8609 are capable of driving capacitive loads of 2 nF with no ringing and less than 3% overshoot.

The use of the snubber circuit is usually recommended for unity gain configurations. Higher gain configurations help improve the stability of the circuit. Figure 44 shows the same output response with the snubber in place.

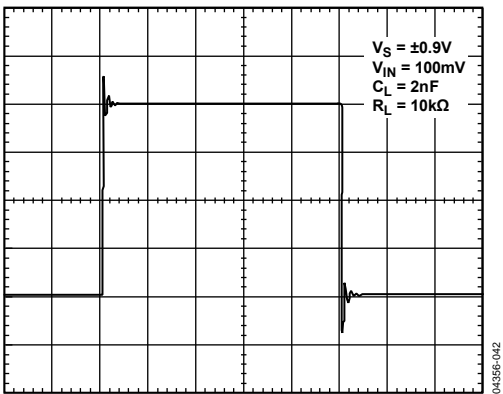


Figure 42. Output Response to a 2 nF Capacitive Load, Without Snubber

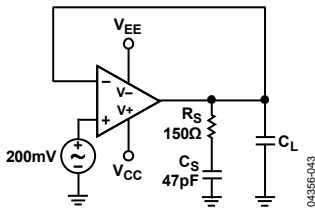


Figure 43. Snubber Network

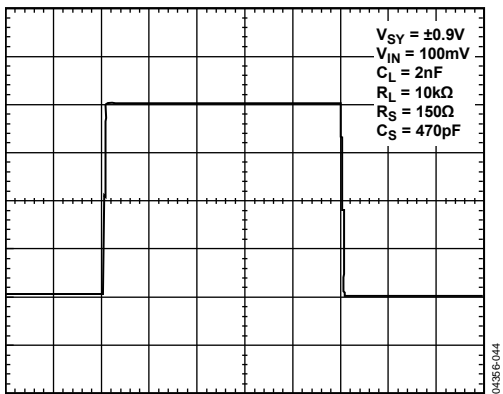


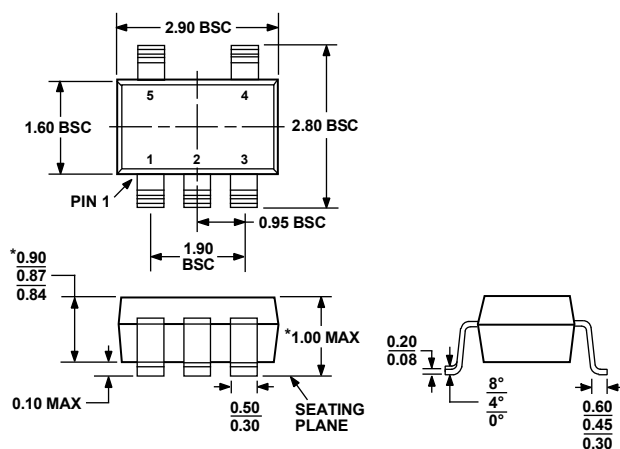
Figure 44. Output Response to a 2 nF Capacitive Load with Snubber

Optimum values for RS and CS are determined empirically; Table 5 lists a few starting values.

Table 5. Optimum Values for the Snubber Network

CL (pF)	RS (Ω)	CS (pF)
100 to ~500	500	680
1500	100	330
1600 to ~2000	400	100

OUTLINE DIMENSIONS

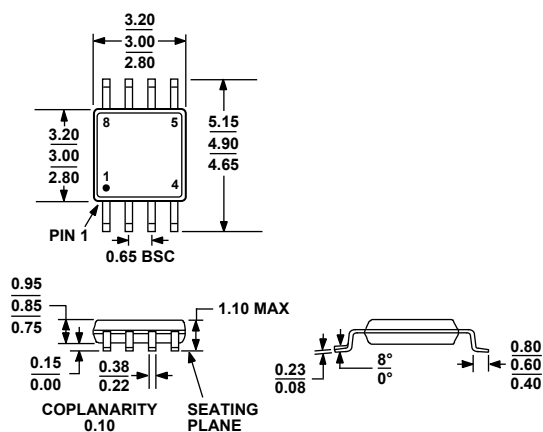


*COMPLIANT TO JEDEC STANDARDS MO-193-AB WITH THE EXCEPTION OF PACKAGE HEIGHT AND THICKNESS.

Figure 48. 5-Lead Thin Small Outline Transistor Package [TSOT]

(UJ-5)

Dimensions shown in millimeters

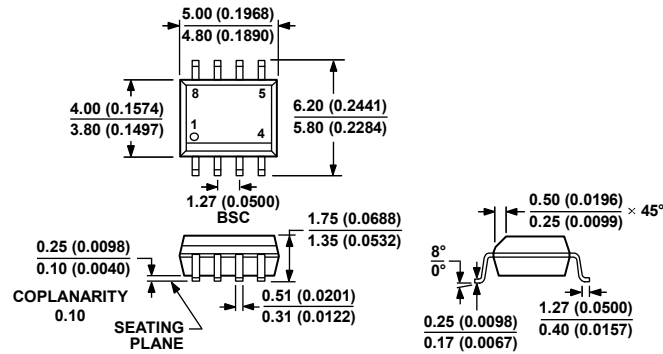


COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 49. 8-Lead Mini Small Outline Package [MSOP]

(RM-8)

Dimensions shown in millimeters

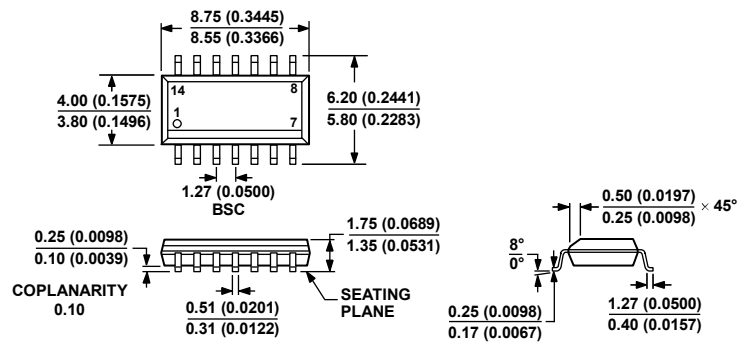


COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 50. 8-Lead Standard Small Outline Package [SOIC_N]
(R-8)

Dimensions shown in millimeters and (inches)

012A07-A

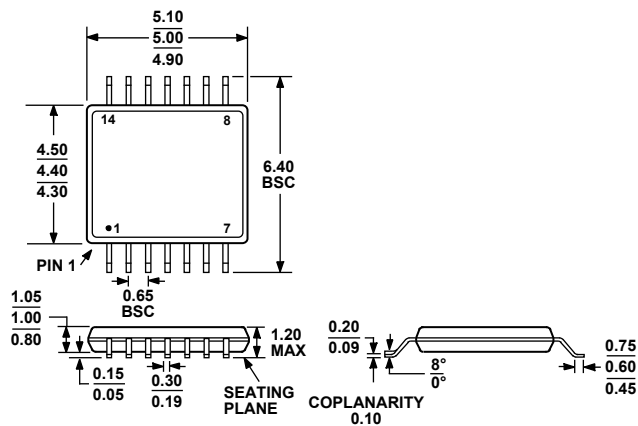


COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 51. 14-Lead Standard Small Outline Package [SOIC_N]
(R-14)

Dimensions shown in millimeters and (inches)

060606-A



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 52. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)

Dimensions shown in millimeters

AD8603/AD8607/AD8609

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8603AUJ-R2	−40°C to +125°C	5-Lead TSOT	UJ-5	BFA
AD8603AUJ-REEL	−40°C to +125°C	5-Lead TSOT	UJ-5	BFA
AD8603AUJ-REEL7	−40°C to +125°C	5-Lead TSOT	UJ-5	BFA
AD8603AUJZ-R2 ¹	−40°C to +125°C	5-Lead TSOT	UJ-5	A0X
AD8603AUJZ-REEL ¹	−40°C to +125°C	5-Lead TSOT	UJ-5	A0X
AD8603AUJZ-REEL7 ¹	−40°C to +125°C	5-Lead TSOT	UJ-5	A0X
AD8607ARM-R2	−40°C to +125°C	8-Lead MSOP	RM-8	A00
AD8607ARM-REEL	−40°C to +125°C	8-Lead MSOP	RM-8	A00
AD8607ARMZ-R2 ¹	−40°C to +125°C	8-Lead MSOP	RM-8	A0G
AD8607ARMZ-REEL ¹	−40°C to +125°C	8-Lead MSOP	RM-8	A0G
AD8607AR	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8607AR-REEL	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8607AR-REEL7	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8607ARZ ¹	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8607ARZ-REEL ¹	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8607ARZ-REEL7 ¹	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8609AR	−40°C to +125°C	14-Lead SOIC_N	R-14	
AD8609AR-REEL	−40°C to +125°C	14-Lead SOIC_N	R-14	
AD8609AR-REEL7	−40°C to +125°C	14-Lead SOIC_N	R-14	
AD8609ARZ ¹	−40°C to +125°C	14-Lead SOIC_N	R-14	
AD8609ARZ-REEL ¹	−40°C to +125°C	14-Lead SOIC_N	R-14	
AD8609ARZ-REEL7 ¹	−40°C to +125°C	14-Lead SOIC_N	R-14	
AD8609ARU	−40°C to +125°C	14-Lead TSSOP	RU-14	
AD8609ARU-REEL	−40°C to +125°C	14-Lead TSSOP	RU-14	
AD8609ARUZ ¹	−40°C to +125°C	14-Lead TSSOP	RU-14	
AD8609ARUZ-REEL ¹	−40°C to +125°C	14-Lead TSSOP	RU-14	

¹ Z = RoHS Compliant Part.