



UNIVERSITÀ DEGLI STUDI DI TRENTO

GROUP MAR01

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# REPORT OF THE EXPERIMENTS PERFORMED IN THE COURSE OF PHYSICS LABORATORY III

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# Experiment 1

## Basic circuits with an operational amplifier

In this experiment we have built five different circuits. The first is an open loop circuit with the operational amplifier uA741, the goal was to find the maximum voltage output by the op-amp. The last four circuits are in closed loop configuration with a negative feedback, they consist in a follower, a non inverting amplifier, an inverting amplifier and a weighted summing amplifier. We have measured the voltage input and the voltage output of every circuit.

### 1.1 Materials

- Operational amplifier uA741
- Resistors, nominal value:  $100\ \Omega$ ,  $220\ \Omega$
- Power supply RIGOL DP831A
- Waveform generator RIGOL DG1032
- Multimeter RIGOL DM3068
- Oscilloscope AGILENT 54261A

### 1.2 Experiment setup

In the first four circuits the output of the waveform generator was a sine wave of 100Hz frequency and a peak-peak voltage of 100mV. We measured the waveform input signal  $v_{in}$  and the output voltage  $v_o$  of the op-amp. The measurements were performed using an oscilloscope triggered externally, the signal acquired is an 8 cycles average. The voltage supply of the op-amp was set to  $v_{cc} = 15\text{V}$  for all the circuits.

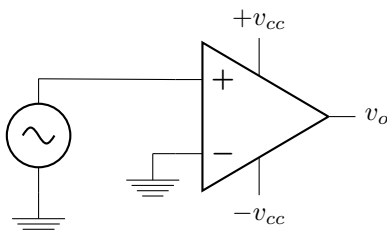


Figure 1.1: Open loop circuit

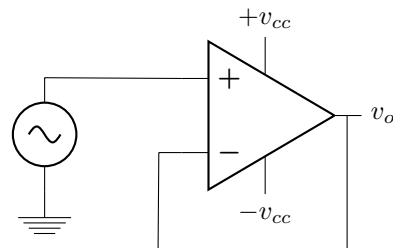


Figure 1.2: Follower

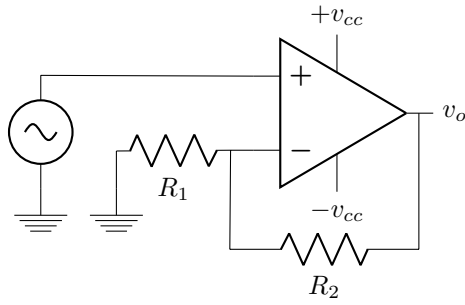


Figure 1.3: Non inverting amplifier

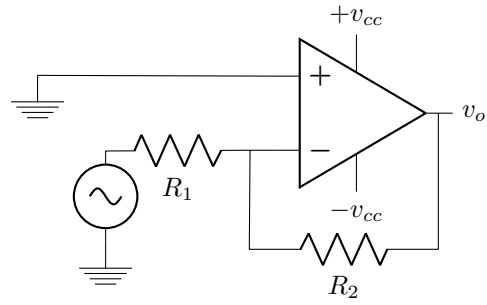


Figure 1.4: Inverting amplifier

For the last circuit we used another sine wave signal with the same 100Hz frequency and a different peak-peak voltage. The oscilloscope's setting and the measurement taken was the same as before. The values of the resistor are:  $R_1 = 99.89 \pm 0.02 \Omega$ ,  $R_2 = 218.37 \pm 0.04 \Omega$ ,  $R_3 = 99.89 \pm 0.02 \Omega$  (the measurement were made with the multimeter).

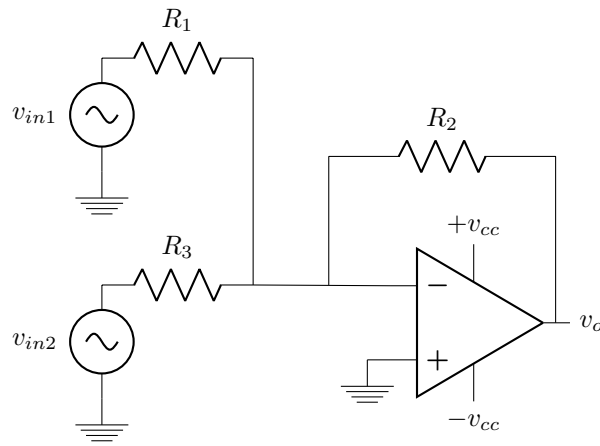


Figure 1.5: Weighted summing amplifier

### 1.3 Data analysis

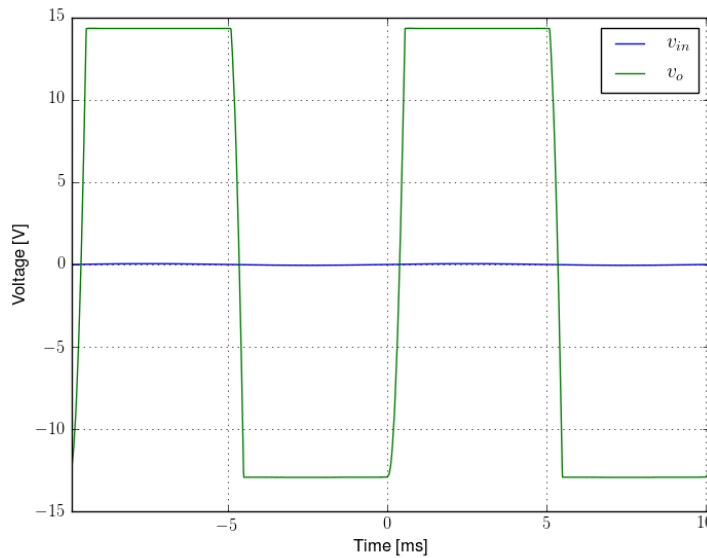


Figure 1.6: Open loop configuration

In the open loop configuration we get an output (visible in the figure one) that has a max absolute value of  $14.35 \pm 0.16^1$  V and a minimum value of  $-12.94 \pm 0.16^1$  V. In the ideal model we would expect the output to be infinite, as justified from the equation  $v_o = A_{ol}(v_+ - v_-)$  where  $A_{ol}$  tends to infinity. In the physical case the output voltage is constrained by the saturation voltage that's determined by the voltage applied to the op-amp. The minimum and maximum value of the output have different absolute value, due to the lack of symmetry between the *nnp* and *pnp* transistors in the final push-pull stage of the op-amp.

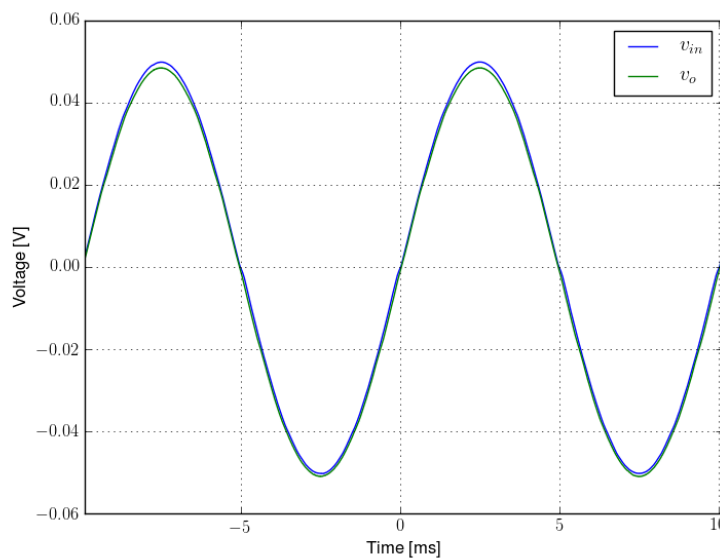


Figure 1.7: Emitter follower

<sup>1</sup>Error based on oscilloscope's 8 bit resolution

In the emitter follower we expect, ideally, an output voltage equal to the input one. But we can see in the plot a small discrepancy between the two signals: that is determined probably by the op-amp's offset, as we can see a downward translation in the output, and also by some other non ideal features of the op-amp.

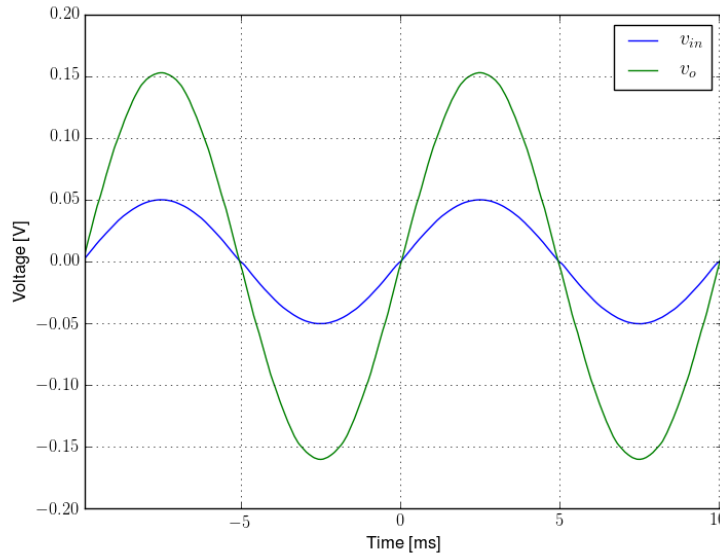


Figure 1.8: Non-inverting amplifier

In the non-inverting amplifier configuration we expect the output to be:  $v_o = v_{in}(1 + \frac{R_2}{R_1})$ . The theoretical value calculated using the  $v_{in}$  and  $R_2, R_1$  is  $320.3 \pm 1.9$  mV. This prediction is not compatible with the output measured  $313.4 \pm 0.8$  mV, probably because the op-amp is not ideal.

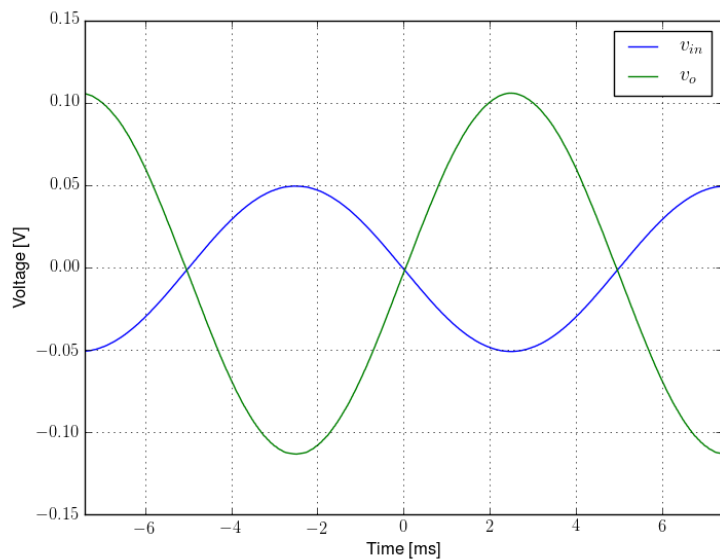


Figure 1.9: Inverting amplifier

In the inverting amplifier the output should be :  $v_o = -v_{in} \frac{R_2}{R_1}$ . The pk-pk of the output is  $219.4 \pm 0.8$  mV that is compatible with theoretical value  $219.8 \pm 1.9$  mV.

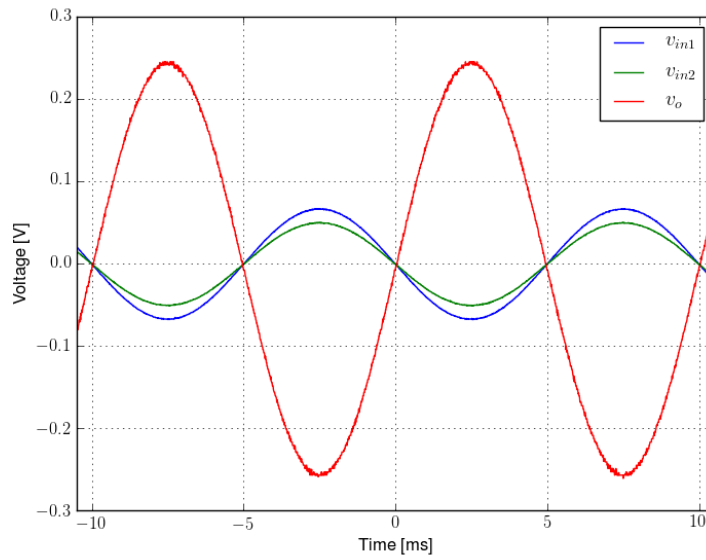


Figure 1.10: Weighted summing circuit

In the circuit (1.5) we used two inputs for acquiring an output voltage. This configuration sums these signals  $v_1 = 135.1 \pm 0.8$  mV and  $v_2 = 101.3 \pm 0.8$  mV using the resistors  $R_1$  and  $R_3$  as weights, giving as output  $v_o = -R_2(\frac{v_1}{R_1} + \frac{v_2}{R_3})$ , which gives a pk-pk value of  $516.7 \pm 2.7$  mV. The theory in this case it's not at all compatible with the measurement  $506 \pm 0.8$  mV, but that's, most likely, caused by the noise in the output.

## Experiment 2

# Let's get more confident with our little friend op-amp

We designed a non-inverting amplifier with a variable gain by using a trimmer. The second circuit designed was a summing amplifier with an unitary gain. We built a current source generator of 1 mA and tested it with a variable load. We tested the efficacy of the emitter follower configuration in mismatching the source's impedance. Last we designed a differential amplifier with a predetermined gain.

### 2.1 Materials

- Operational amplifier uA741
- Resistors and trimmers
- Power supply RIGOL DP831A
- Waveform generator RIGOL DG1032
- Multimeter RIGOL DM3068
- Oscilloscope RIGOL MS02102A
- Two capacitance of nominal value of 100nF

### 2.2 Experiment setup

In each circuit we powered the op-amp with a  $\pm 15$  V DC voltage and, in order to reduce possible noises, we added two 100nF capacitors connecting the op-amp's pins for the power supply with the ground. The input signal has a frequency of 100 Hz and a peak-peak voltage of 1V except for the differential amplifier. For every specific circuit we designed them as follow:

- Inverting amplifier: we placed a  $10\text{k}\Omega$  trimmer along the feedback branch in series to a resistor  $R_f = 983.9 \pm 0.1\Omega$ . In order to have a minimal gain of 5, we used  $R_{in} = 199.84 \pm 0.03\Omega$  as in figure (2.1).
- Summing amplifier: caring for the simplest calculations, we used  $R_1 = 1484.7 \pm 0.2\Omega \simeq R_2 = 1483.5 \pm 0.2\Omega$  so the equation is  $\frac{v_1 + v_2}{2} \left(1 + \frac{R_4}{R_3}\right)$ . For obtaining the sum of the input in output, we had to choose  $R_3 = R_4 = 1001.3 \pm 0.1\Omega$ . The inputs  $v_1$  and  $v_2$  are the same 100 Hz, 1 V peak-peak sine wave signal.



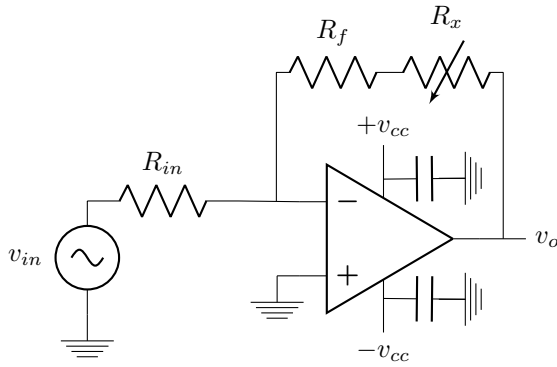


Figure 2.1: Inverting variable amplifier

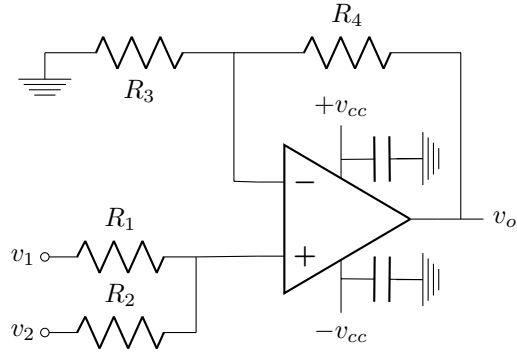


Figure 2.2: Non-inverting summing amplifier, unitary gain

- Emitter follower test: at first we built a circuit without the emitter follower using an input impedance of  $R = 100.2 \pm 1 \text{ k}\Omega$  and a load of  $R_L = 19.8 \pm 2 \text{ k}\Omega$ . Then we added the op-amp stage and compared the output measurements in the 2 different cases.

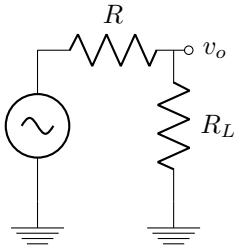


Figure 2.3: Test circuit without follower

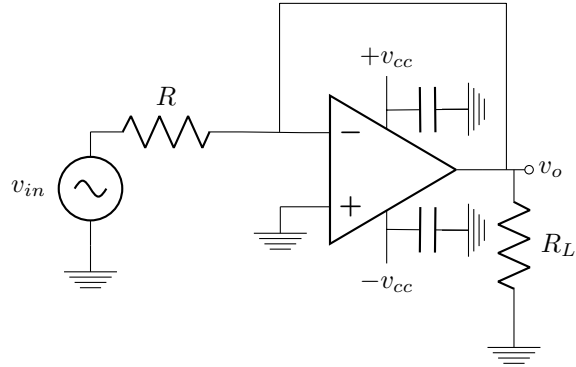


Figure 2.4: Test circuit with follower

- Current generator: the aim of this circuit is to generate a stable fixed current independent from the load. We generated a 1 mA current using a DC voltage source of 5 V and a  $4.9693 \pm 0.7 \text{ k}\Omega$  resistor. The load was simulated with a trimmer.
- Differential amplifier: the full equation the circuit in figure (2.6) is the following:

$$v_o = \frac{R_F}{R_1} \left[ \frac{v_b}{1 + R_f/R_y} \left( 1 + \frac{R_1}{R_f} \right) - v_a \right]$$

we first set to ground  $v_b$ , in this way we were able to set up the gain of the circuit (we chose it to be  $A = 2$  with  $R_F = 3 \pm 0.2 \text{ k}\Omega$  (5% error of nominal value)). After that we put the same signal of  $v_a$  in  $v_b$  with a resistor  $R_f$  and a variable resistor  $R_y$  made with  $R_2$  in series with a trimmer. We managed with the trimmer to get the output as close to zero as possible (Figure (2.7)). This means in the equation  $R_f/R_y = R_1/R_F$  so the new output is exactly what we want  $v_o = A(v_b - v_a)$ . For testing the amplifier we used  $v_a = 5 \text{ V}$  DC and for  $v_b$  a sine wave 1 V peak-peak 100 Hz with an offset of 5 V.

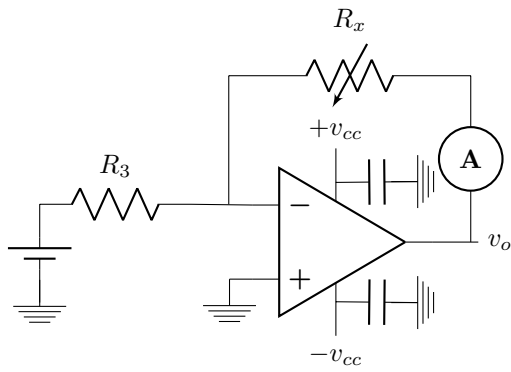


Figure 2.5: Current source generator

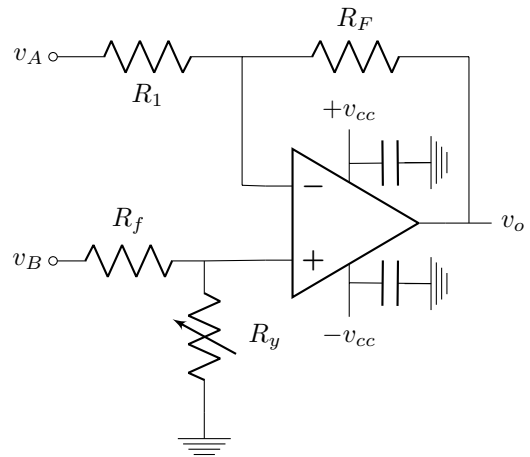


Figure 2.6: differential amplifier

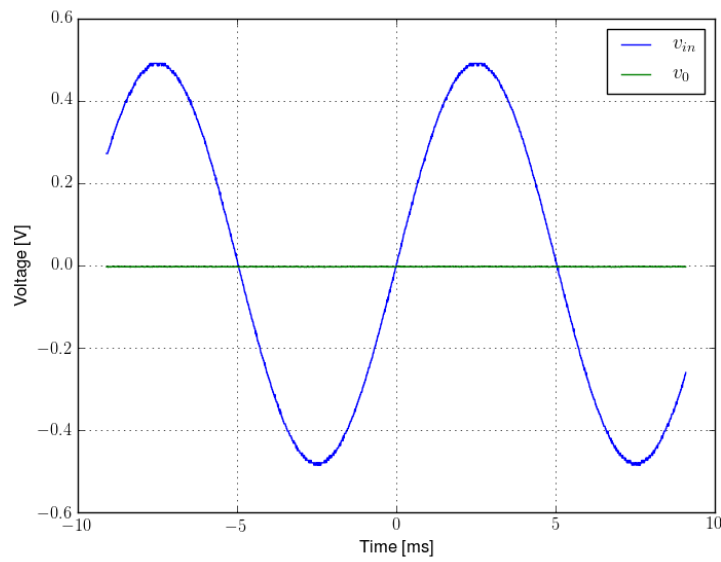


Figure 2.7: Calibration of the differential amplifier

## 2.3 Data analysis

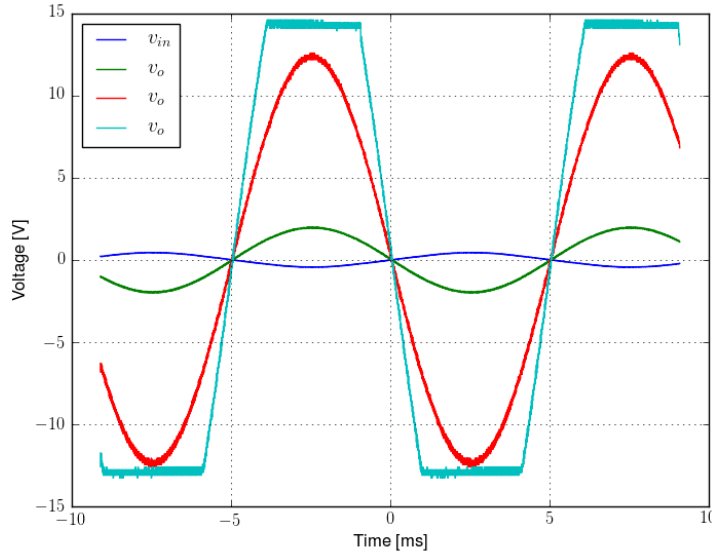


Figure 2.8: Variable amplifier

In the inverting amplifier we used a trimmer in order to vary the gain, in fact the equation is:

$$v_o = -v_{in} \frac{R_f + R_x}{R_{in}}$$

so increasing  $R_x$  cause output to linear increasing. The output voltage is limited by the op-amps's power supply voltage, it cannot increase further and the signal goes flat, as we can see in figure (2.8) (light blue line), this behavior is called "Clipping". The graphic also shows a discrepancy between the absolute value of maximum and minimum voltage during the clipping: this is due to the asymmetry between *pnp* and *nnp* transistors in the op-amp's final stage.

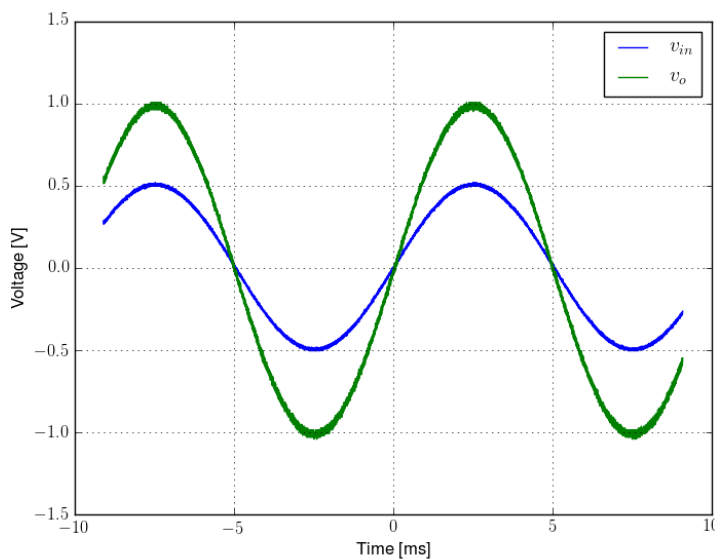


Figure 2.9: Weighted summing amplifier

In the non-inverting summing amplifier circuit we wanted the output to be the simple sum of the signals in entrance, that were identical: it means that the output signal must have double amplitude compared to the input one. The peak-peak voltage's theoretical expectation is  $2.0496 \pm 0.0009$  V while the measured one is  $2.032 \pm 0.001$  V. The incompatibility probably is due to the op-amp's non-ideality.

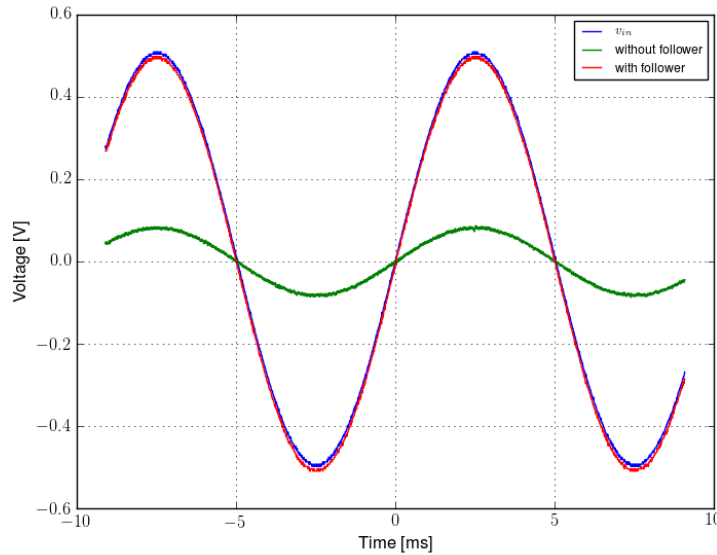


Figure 2.10: Emitter follower comparison

Let's now analyse the differences between circuits with and without follower stage. We can see in figure (2.10) that using the follower we obtain a replicated signal while without it the signal is shrunk due to the input impedance, in fact the op-amp stage's purpose is the impedance mismatching.

In the current generator circuit we firstly measured the output current that was the expected one, than we observed the independency from the trimmer resistance of the current value.

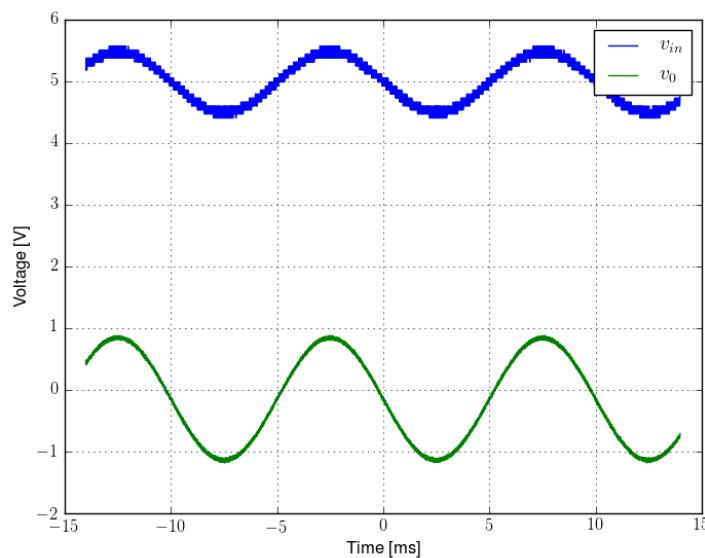


Figure 2.11: Differential amplifier

## *EXPERIMENT 2. LET'S GET MORE CONFIDENT WITH OUR LITTLE FRIEND OP-AMP 12*

In the differential amplifier circuit we measured an output cleared from the DC part present in the input, the output value was the AC part doubled compared to the input one. This is exactly how we expected the circuit to behave.

## Experiment 3

# Unfortunately the op-amp is not so ideal

In this set of experiments we dealt with the problems of a real op-amp such as the offset  $v_{os}$ , the bias currents  $i_{b+}, i_{b-}$ , the slew-rate, the maximum current output and the common gain  $A_{cm}$ , we performed the measures of these real parameters. The offset is studied with 3 different circuit and then compensated with a trimmer in the configuration suggested by the op-amp's datasheet. The bias currents was measured in two way, one for the bias current in the + 's op-amp input and one for the - 's op-amp input. The other parameters are studied simply adjusting the input for the measurement's purpose.

### 3.1 Materials

- Operational amplifier uA741
- Resistors, trimmer
- Power supply RIGOL DP831A
- Waveform generator RIGOL DG1032
- Multimeter RIGOL DM3068
- Oscilloscope RIGOL MS02102A

List of resistors used		
Resistor name	Value [ $\Omega$ ]	Uncertainty [ $\Omega$ ]
$R_{M\Omega}$	$982.0 \times 10^3$	$0.1 \times 10^3$
$R_{100k\Omega}$	$99.22 \times 10^3$	$0.01 \times 10^3$
$R_{10k\Omega}$	9906.2	1.2
$R_{k\Omega}$	1001.4	0.1
$R_{10\Omega}$	9.963	0.01
$R_{10k\Omega}^*$	9926.4	1.2
$R_{10\Omega}^*$	10.00	0.01

### 3.2 Experiment setup

In all the circuits we placed on the power supply's pins two capacitor each, one with high capacitace (nominal value  $470 \pm 23$  nF) and one with low capacitance ( $10.0 \pm 0.5$  nF). These were used for suppressing the high-frequency noise and contrastig the effect of any eventual change in the voltage of the power supply, that could move the offset voltage.

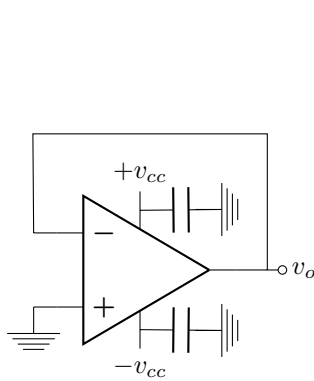


Figure 3.1: Offset voltage's direct measure

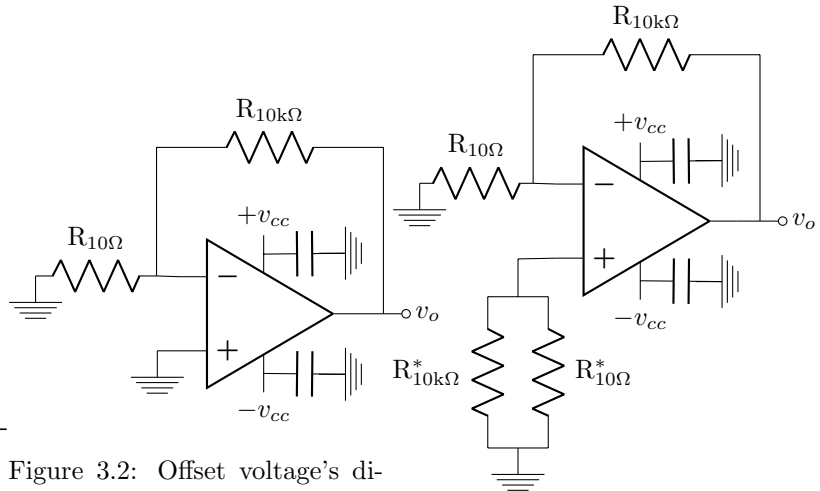


Figure 3.2: Offset voltage's direct measure with gain

Figure 3.3: Offset voltage's direct measure with gain and bias current correction

In the first circuit we acquired  $v_{os}$  directly by measuring with the multimeter the output voltage. We used the second circuit to amplify  $v_{os}$ , thus we used the output to calculate  $v_{os}$ . The third circuit is identical to the second circuit except for the added resistors in parallel that connect + to the ground. This was done for removing the influence of the bias current in the measurement. Exploiting this last circuit we removed  $v_{os}$  by using a trimmer and trying to make the output closest that we could to 0.

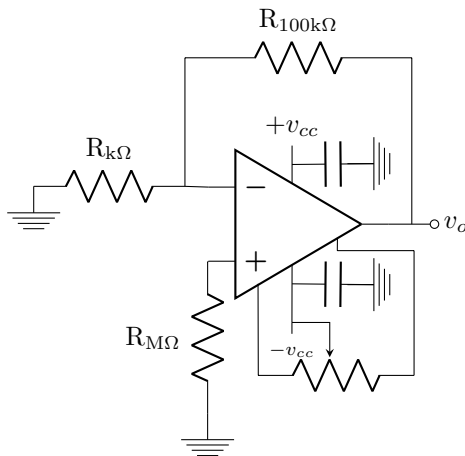


Figure 3.4: Positive bias current measure

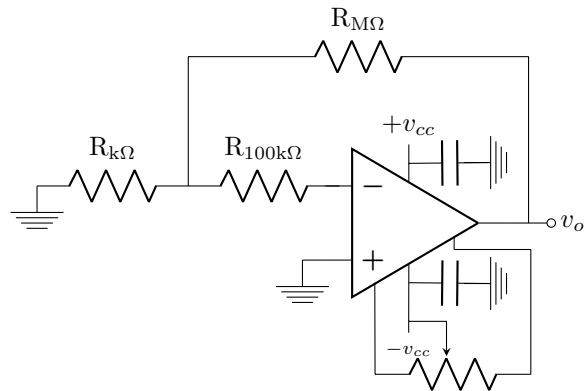


Figure 3.5: Negative bias current measure

The fourth circuit and fifth are used for measuring the current of bias indirectly using how the two currents are related to the output.

The sixth circuit was used for measuring the maximum current that the op-amp can erogate. In this configuration the oscilloscope's internal resitor was set to 50Ω

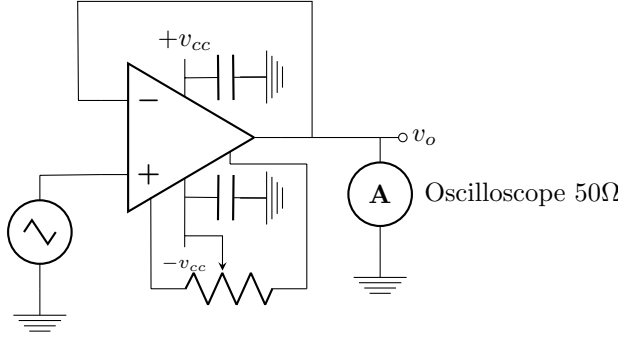


Figure 3.6: Max current measure

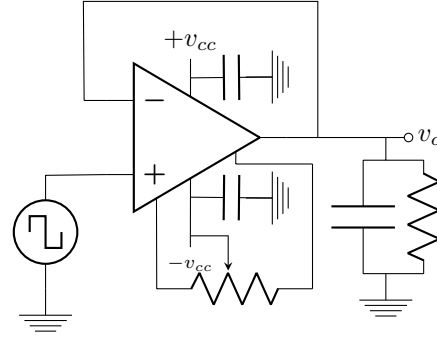


Figure 3.7: Slew rate

In the seventh circuit we measured the slew rate. As load the capacitor used was  $1 \pm 0.05$  nF and the resistor  $2 \pm 0.1$  k $\Omega$ . The input used was a 10 V square wave, so we acquired the image of the raising output.

In the last circuit we measured the common gain by using the differential amplifier with the same input 2 V peak-peak and 100 Hz.

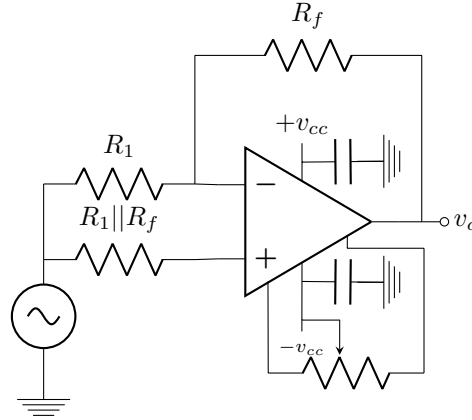


Figure 3.8: Common Gain

### 3.3 Data analysis

In the emitter follower (3.1) the output measured is  $-1.484 \pm 0.005$  mV. Being such a small output we expect to have problem with parasite resistor and other form of noise, that's why we don't consider the output too reliable, but it gives us an order of magnitude that is in agreement with the datasheet of the op-amp, that propouses a typical value of 1 mV and a maximum value of 5 mV.

In the amplifier (3.2) we can find  $v_{os}$ , by using

$$v_{os} = \frac{v_o}{1 + \frac{R_{10k\Omega}}{R_{10\Omega}}}$$

from the calculation we get  $v_{os} = -1.333 \pm 0.001$  mV, which is has the same order of magnitude and same sign of the previous result.

Then as stated in the experimental setup we corrected the circuit (3.3) for compensating the effect of the current of bias. With the same formula used for the previous amplifier we get an offset voltage of  $1.307 \pm 0.001$  mV. We used this circuit for nulling the offset with the trimmer.

In the fourth circuit (3.4) we calculated the current flowing in the non invertent pin by using

$$i_{b+} = \frac{v_o}{R_{M\Omega}(1 + \frac{R_{100k\Omega}}{R_{1k\Omega}})}$$



The value calculated is  $-39.042 \pm 0.009$  nA.

In the fifth circuit (3.5) instead we calculate the current flowing in the invertent pin by using

$$i_{b-} = \frac{v_o}{R_{100k\Omega}} \frac{R_{k\Omega}}{R_{M\Omega}}$$

above the value is  $-39.724 \pm 0.009$  nA. Now we can compute the current of bias  $i_b = \frac{|i_{b-}| + |i_{b+}|}{2} = 39.383 \pm 0.006$  nA and the offset current  $i_o = ||i_{b-}| - |i_{b+}|| = 0.68 \pm 0.01$  nA.  $i_b$  is less than 100 nA and near the typical value of 10 nA, as the datasheet states, but the offset current is a bit low being around a third of the typical value 2 nA.

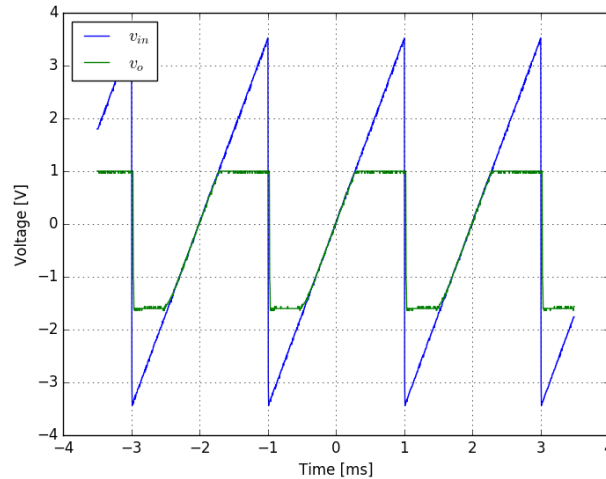


Figure 3.9: Saturated output caused by the maximum current erogated

In the sixth circuit (3.6) we calculated the maximum current erogated by computing the maximum/minimum output voltage over the resistance in the oscilloscope. In the plot is visible the different absolute value of the maximum and minimum output voltage, that's probably because the op-amp isn't perfectly symmetric in the packaging. So we opted to calculating two different maximum currents:  $i_{max} = 0.0201 \pm 0.0001$  A (when the output was positive) and  $i_{min} = 0.0328 \pm 0.0001$  (when the output was negative).

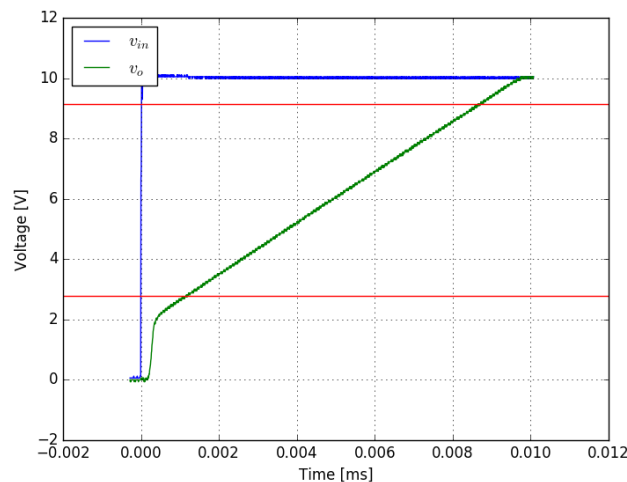


Figure 3.10: Saturated output caused by the maximum current erogated, red lines is 10% and 90% of the output

In the seventh circuit (3.7) we find that the slew rate of the op-amp used is  $0.85 \frac{\text{V}}{\mu\text{s}}$ , which is bigger than the typical value  $0.5 \frac{\text{V}}{\mu\text{s}}$ . One possible explanation of this would be that the slew rate depends on the amplitude of the signal, in our experiment the voltage was 50 times as large as in the test of visible in the datasheet, otherwise we have to conclude that our op-amp, has some difects that cause a larger slewrate.

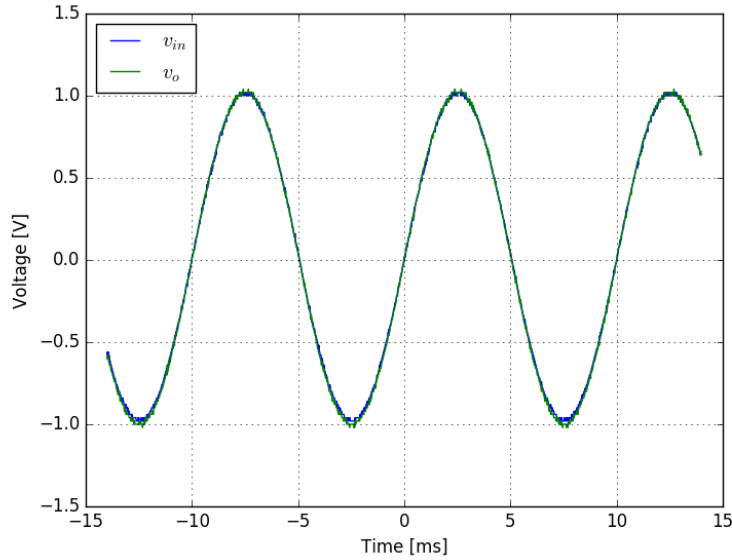


Figure 3.11: Saturated output caused by the maximum current erogated

In the last circuit (3.8) we measured the commond gain, by using

$$A_{CM} = \frac{2v_o}{v_{in1} + v_{in2}}$$

which gave us an unitary gain, as it is evident in the plot.