Università degli studi di Trento

Group **MAR01**

REPORT OF THE EXPERIMENTS PERFORMED IN THE COURSE OF PHYSICS LABORATORY III

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Contents

Experiment 1

Basic circuits with an operational amplifier

In this experiment we have built five different circuits. The first is an open loop circuit with the operational amplifier uA741, the goal was to find the maximum voltage output by the op-amp. The last four circuits are in closed loop configuration with a negative feedback and they consist in a follower, a non inverting amplifier, an inverting amplifier and a weighted summing amplifier. We have measured the voltage input and the voltage output of every circut.

1.1 Materials

- Operational amplifier uA741
- Resistors, nominal value: 100 Ω, 220 Ω
- Power supply RIGOL DP831A
- Waveform generator RIGOL DG1032
- Multimeter RIGOL DM3068
- Oscilloscope AGILENT 54261A

1.2 Experiment setup

In the first four circuits the output of the waveform generator was a sine wave of 100Hz frequency and a peak-peak voltage of 100mV. We measured the waveform input signal v_{in} and the output voltage v_o of the op-amp. The measurements were performed using an oscilloscope triggered externally, the signal acquired is an 8 cycles average. The voltage supply of the op-amp was set to $v_{cc} = 15$V for all the circuits.

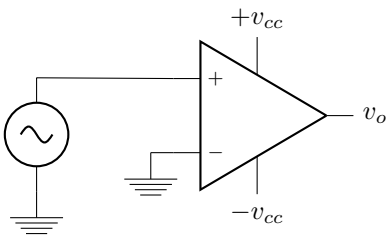


Figure 1.1: Open loop circuit

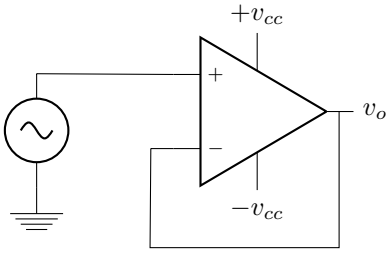


Figure 1.2: Follower

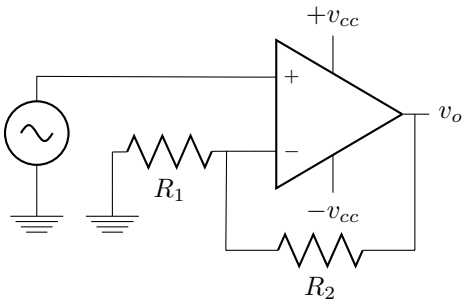


Figure 1.3: Non inverting amplifier

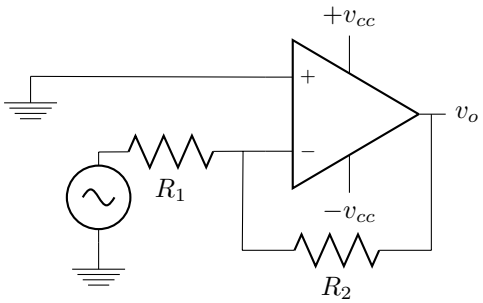


Figure 1.4: Inverting amplifier

For the last circuit we used again a sine wave signal with the same 100Hz frequency but a different peak-peak voltage. The oscilloscope's setting and the measurement taken was the same as before. The values of the resistor are: $R_1 = 99.89 \pm 0.02\,\Omega$, $R_2 = 218.37 \pm 0.04\,\Omega$, $R_3 = 99.89 \pm 0.02\,\Omega$ (the measurement were obtained with the multimeter).

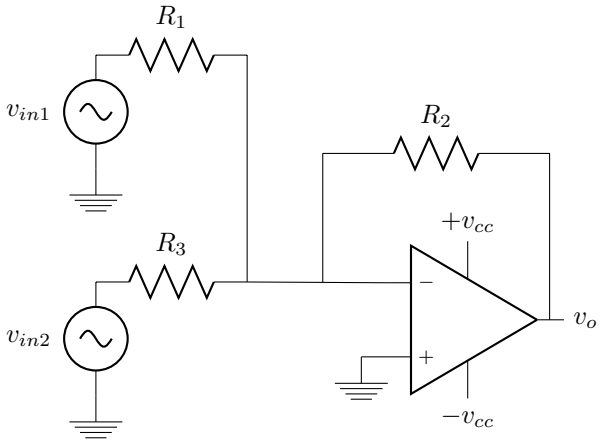


Figure 1.5: Weighted summing amplifier

1.3 Data analysis

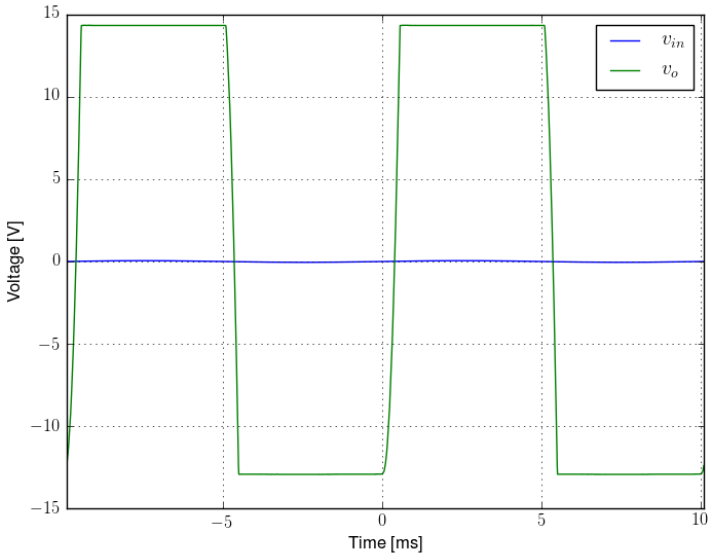


Figure 1.6: Open loop configuration

In the open loop configuration we get an output (visible in figure 1.6) that has a maximum absolute value of 14.35 ± 0.16[1] V and a minimum value of -12.94 ± 0.16[1] V. According to the ideal model we would expect the output to be infinite, as stated by the equation $v_o = A_{ol}(v_+ - v_-)$ where A_{ol} tends to infinity. In the physical case the output voltage is costrained by the saturation voltage that's determined by the voltage applied to the op-amp. The minimum and maximum output values are different in modulus, due to the lack of symmetry between the *npn* and *pnp* trasistors in the final push-pull stage of the op-amp.

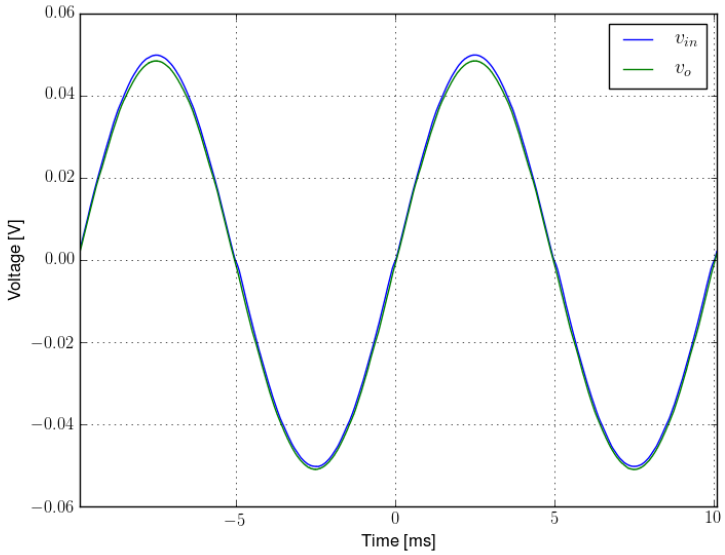


Figure 1.7: Emitter follower

[1]Error based on oscilloscope's 8 bit resolution

Regarding the emitter follower we expect, ideally, an output voltage equal to the input one. Actually we can see in the plot a small discrepancy between the two signals: that is probably determined by the op-amp's offset, as we can see a downward translation in the output, and also by some other non ideal features of the op-amp.

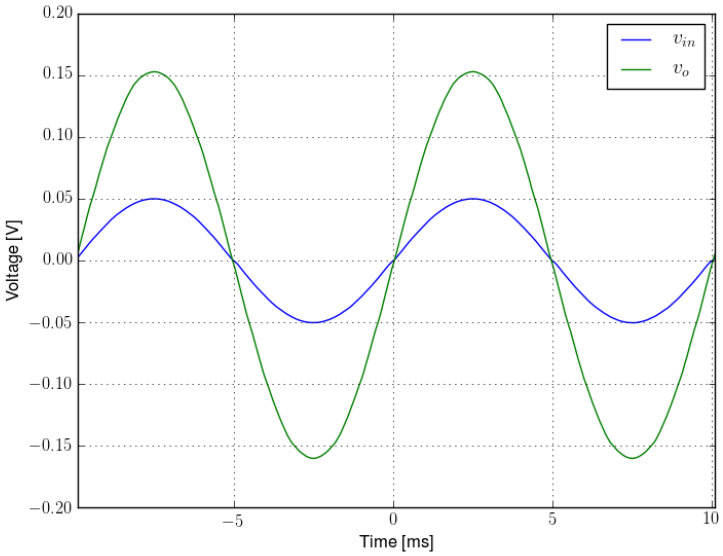


Figure 1.8: Non-inverting amplifier

In the non-inverting amplifier configuration we expect the output voltage to be: $v_o = v_{in}(1 + \frac{R_2}{R_1})$. The theoretical value for the peak-peak output voltage calculated using R_1, R_2 and v_{in} is 320.3 ± 1.9 mV. This prediction is not compatible with the output measured 313.4 ± 0.8 mV of a 3.3σ factor, probably because the op-amp is not ideal.

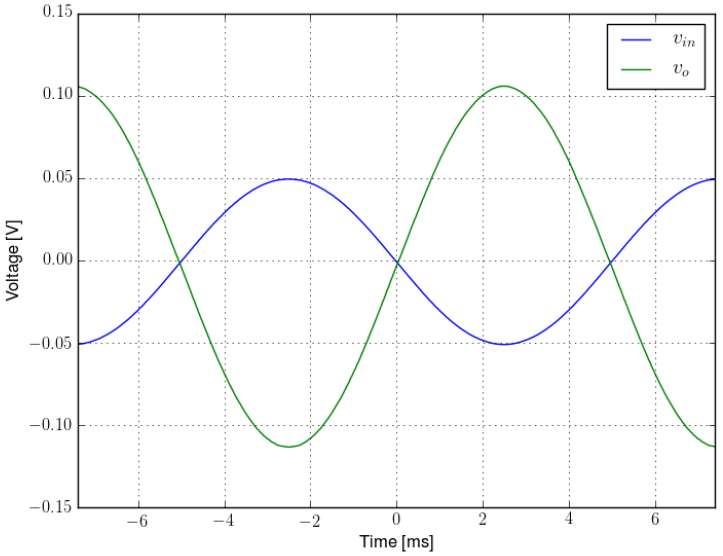


Figure 1.9: Inverting amplifier

In the inverting amplifier the output should be : $v_o = -v_{in}\frac{R_2}{R_1}$. The pk-pk value of the output is 219.4 ± 0.8 mV that is compatible with theoretical value 219.8 ± 1.9 mV.

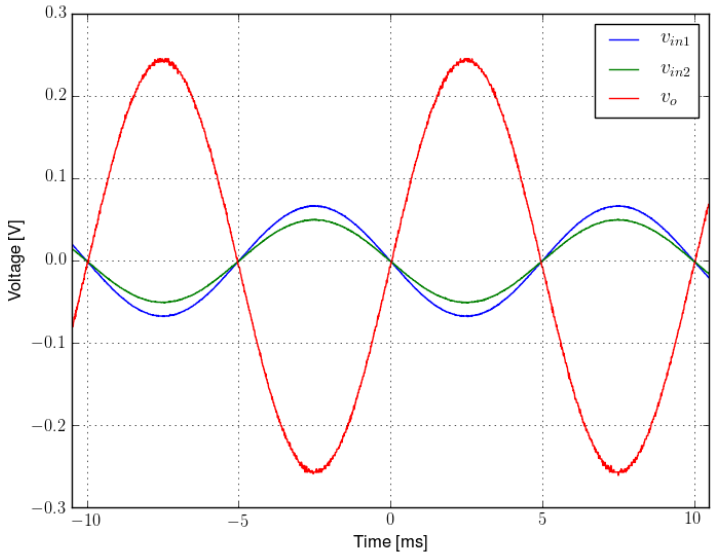


Figure 1.10: Weighted summing circuit

In the circuit 1.10 we used two inputs for aquiring an output voltage. This configuration sums these signals $v_1 = 135.1 \pm 0.8$ mV and $v_2 = 101.3 \pm 0.8$ mV using the resistors R_1 and R_3 as weights, giving as output $v_o = -R_2(\frac{v_1}{R_1} + \frac{v_2}{R_3})$, which gives a pk-pk value of 516.7 ± 2.7 mV. The theory in this case is not compatible with the measurament 506 ± 0.8 mV of a 3.8σ factor, a little more than the previous result, but that's most likely caused by the noise in the output.

Experiment 2

Let's get more confident with our little friend op-amp

We designed a non-inverting amplifier with a variable gain using a trimmer. The second circuit designed was a summing amplifier with unitary gain. We built a current source generator of 1 mA and tested it with various loads. We tested the efficacy of the emitter follower configuration in mismatching the source's impedence. At last we designed a differential amplifier with a predetermined gain.

2.1 Materials

- Operational amplifier uA741
- Resistors and trimmers
- Power supply RIGOL DP831A
- Waveform generator RIGOL DG1032
- Multimeter RIGOL DM3068
- Oscilloscope RIGOL MS02102A
- Two capacitance of nominal value of 100nF

2.2 Experiment setup

In each circuit we powered the op-amp with a ± 15 V DC voltage and, in order to reduce possible noises, we added two 100nF capacitors connecting the op-amp's pins for the power supply with the ground. The input signal has a frequency of 100 Hz and a peak-peak voltage of 1V except for the differential amplifier. For every specific circuit we designed them as follow:

- Inverting amplifier: we placed a 10kΩ trimmer along the feedback branch in series to a resistor $R_f = 983.9 \pm 0.1\Omega$. In order to have a minimal gain of 5, we used $R_{in} = 199.84 \pm 0.03\Omega$ as in figure (2.1).
- Summing amplifier: caring for the simplest calculations, we used $R_1 = 1484.7 \pm 0.2\Omega \simeq R_2 = 1483.5 \pm 0.2\Omega$ so the equation is $\frac{v_1 + v_2}{2}\left(1 + \frac{R_4}{R_3}\right)$. For obtaining the sum of the input in output, we had to choose $R_3 = R_4 = 1001.3 \pm 0.1\Omega$. The inputs v_1 and v_2 are the same 100 Hz, 1 V peak-peak sine wave signal.

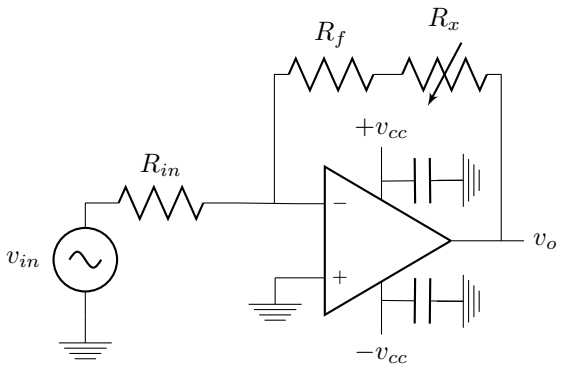


Figure 2.1: Inverting variable amplifier

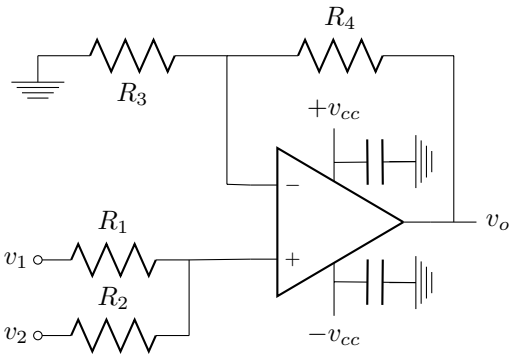


Figure 2.2: Non-inverting summing amplifier, unitary gain

- Emitter follower test: at first we built a circuit without the emitter follower using an input impedence of $R = 100.2 \pm 1\,\text{k}\Omega$ and a load of $R_L = 19.8 \pm 2\,\text{k}\Omega$. Then we added the op-amp stage and compared the output measurements in the 2 different cases.

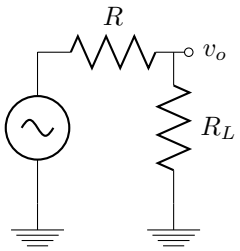


Figure 2.3: Test circuit without follower

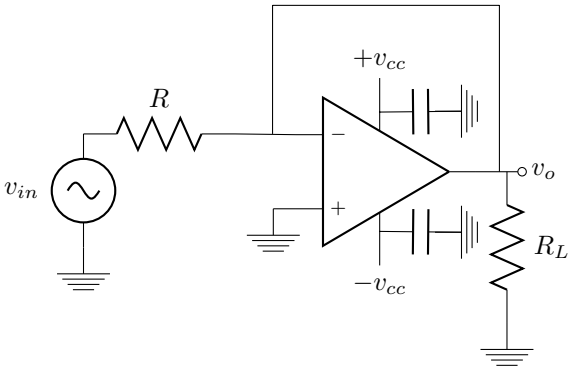


Figure 2.4: Test circuit with follower

- Current generator: the aim of this circuit is to generate a stable fixed current indipendent from the load. We generated a 1 mA current using a DC voltage source of 5 V and a 4.9693 ± 0.7 kΩ resistor. The load was simulated with a trimmer.
- Differential amplifier: the full equation the circuit in figure (2.6) is the following:

$$v_o = \frac{R_F}{R_1}\left[\frac{v_b}{1 + R_f/Ry}\left(1 + \frac{R_1}{R_f}\right) - v_a\right]$$

we first set to ground v_b, in this way we were able to set up the gain of the circuit (we chose it to be $A = 2$ with $R_F = 3 \pm 0.2\,\text{k}\Omega$ (5% error of nominalvalue)). After that we put the same signal of v_a in v_b with a resistor R_f and a variable resistor R_y made with R_2 in series with a trimmer. We managed with the trimmer to get the output as close to zero as possibile (Figure (2.7)). This means in the equation $R_f/R_y = R_1/R_F$ so the new output is exaclty what we want $v_0 = A(v_b - v_a)$. For testing the amplifier we used $v_a = 5$ V DC and for v_b a sine wave 1 V peak-peak 100 Hz with an offset of 5 V.

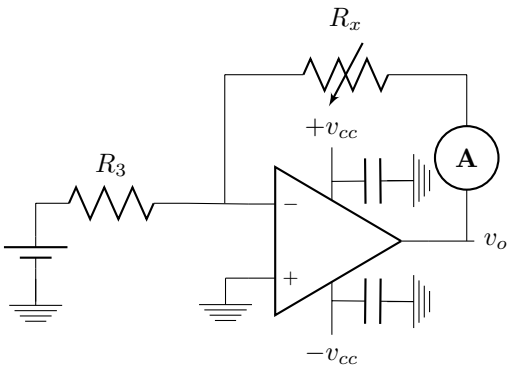


Figure 2.5: Current source generator

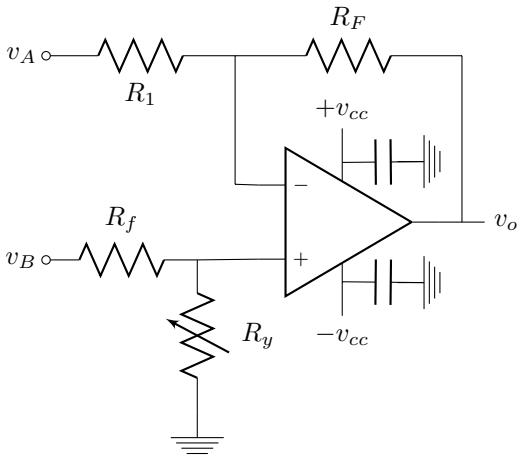


Figure 2.6: differential amplifier

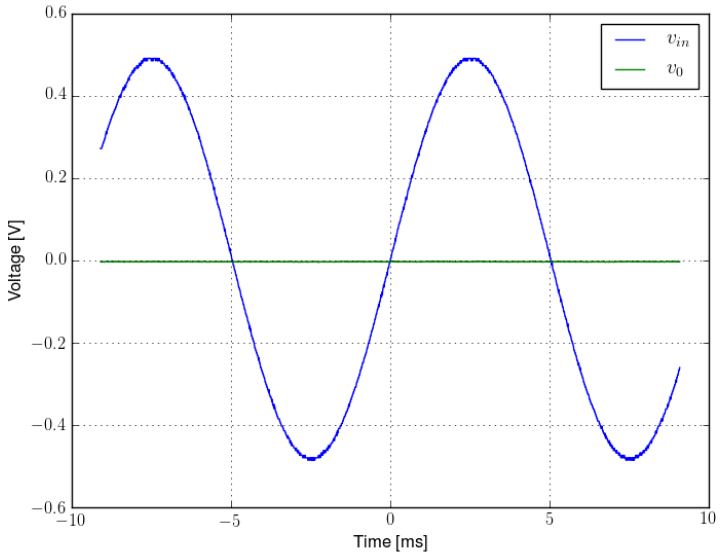


Figure 2.7: Calibration of the differential amplifier

2.3 Data analysis

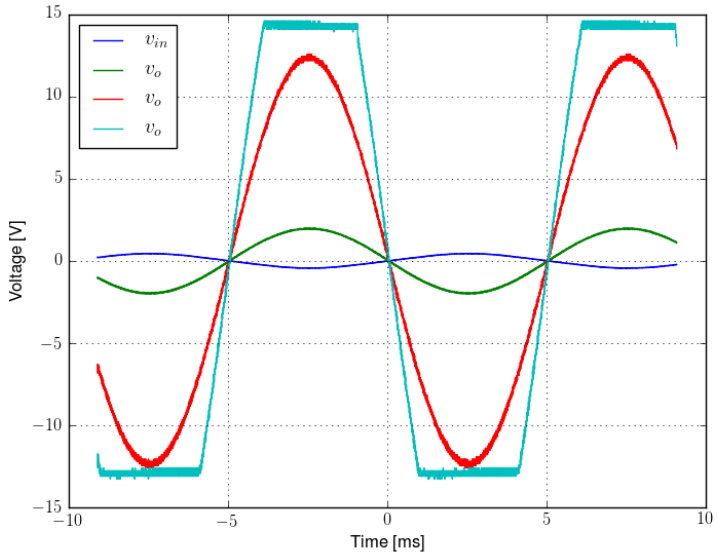


Figure 2.8: Variable amplifier

In the inverting amplifier we used a trimmer in order to vary the gain, in fact the equation is:

$$v_o = -v_{in}\frac{R_f + R_x}{R_{in}}$$

so increasing R_x cause the output to increase linearly. The output voltage is limited by the op-amps's power supply voltage, it cannot increase further and the signal goes flat, as we can see in figure (2.8) (light blue line), this behavior is called "Clipping". The graphic also shows a discrepance between the absolut value of maximum and minimum voltage during the clipping: this is due to the asimmetry between *pnp* and *npn* transistors in the op-amp's final stage.

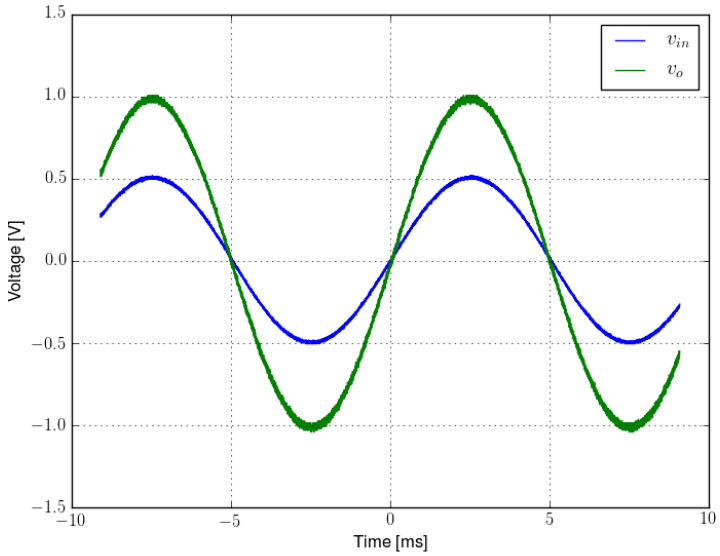


Figure 2.9: Weighted summing amplifier

In the non-inverting summing amplifier circuit we wanted the output to be the simple sum of the signals in entrance, that were identical: it means that the output signal must have double amplitude compared to the input one. The peak-peak voltage's theoretical expectation is 2.0496 ± 0.0009 V while the measured one is 2.032 ± 0.001 V. The incompatibility probably is due to the op-amp's non-ideality.

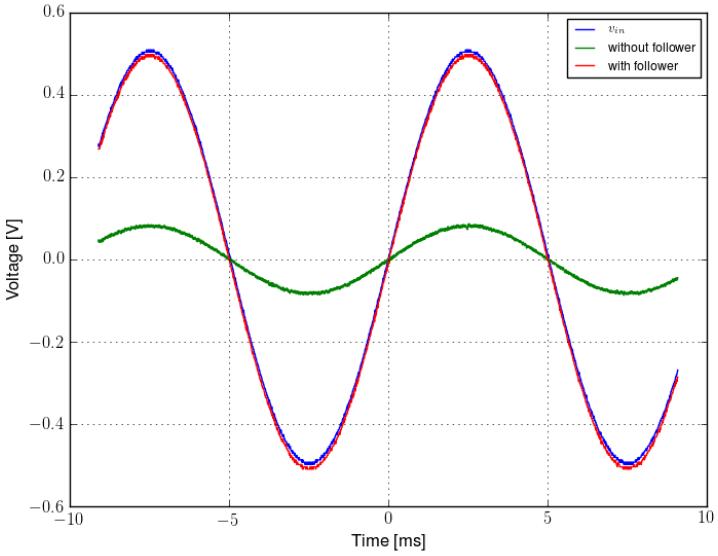


Figure 2.10: Emitter follower comparison

Let's now analyse the differences between circuits with and without follower stage. We can see in figure (2.10) that using the follower we obtain a replicated signal while without it the signal is shrinked due to the input impedence, in fact the op-amp stage's purpose is the impedence mismatching.

In the current generator circuit we firstly measured the output current that was the expected one, than we observed the indipendency from the trimmer resistence of the current value.

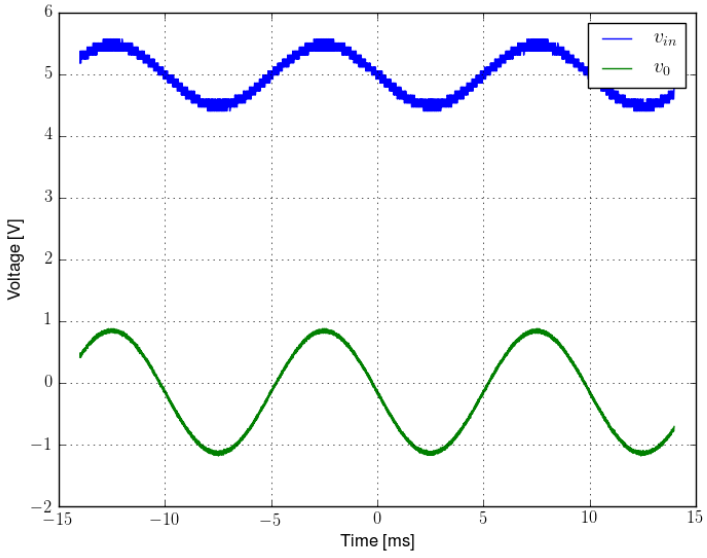


Figure 2.11: Differential amplifier

In the differential amplifier circuit we measured an output cleared from the DC part present in the input, the output value was the AC part doubled compared to the input one. This is exactly how we expected the circuit to behave.

Experiment 3

Unfortunately the op-amp is not so ideal

In this set of experiments we dealt with the problems of a real op-amp such as the offset v_{os}, the bias currents i_{b+}, i_{b-}, the slew-rate, the maximum current output and the common gain A_{cm}, we performed the measures of these real parameters. The offset is studied with 3 different circuit and then compensated with a trimmer in the configuration suggested by the op-amp's datasheet. The bias currents was measured in two way, one for the bias current in the +'s op-amp input and one for the −'s op-amp input. The other parameters are studied simply adjusting the input for the measurement's purpose.

3.1 Materials

- Operational amplifier uA741
- Resistors, trimmer
- Power supply RIGOL DP831A
- Waveform generator RIGOL DG1032
- Multimeter RIGOL DM3068
- Oscilloscope RIGOL MS02102A

List of resistors used		
Resistor name	Value [Ω]	Uncertainty [Ω]
$R_{M\Omega}$	982.0×10^3	0.1×10^3
$R_{100k\Omega}$	99.22×10^3	0.01×10^3
$R_{10k\Omega}$	9906.2	1.2
$R_{k\Omega}$	1001.4	0.1
$R_{10\Omega}$	9.963	0.01
$R^*_{10k\Omega}$	9926.4	1.2
$R^*_{10\Omega}$	10.00	0.01

3.2 Experiment setup

In all the circuits we placed on the power supply's pins two capacitor each, one with high capacitace (nominal value 470 ± 23 nF) and one with low capacitance (10.0 ± 0.5 nF). These were used for suppressing the high-frequency noise and contrastig the effect of any eventual change in the voltage of the power supply, that could move the offset voltage.

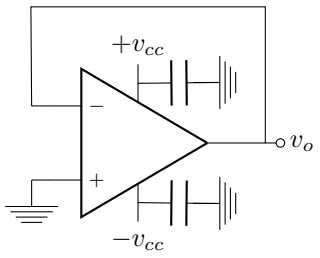


Figure 3.1: Offset voltage's direct measure

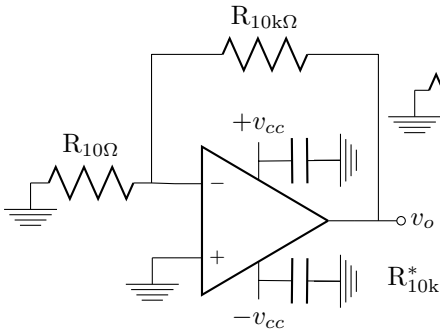


Figure 3.2: Offset voltage's direct measure with gain

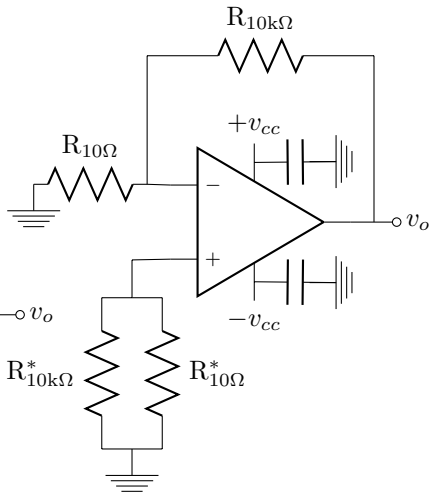


Figure 3.3: Offset voltage's direct measure with gain and bias current correction

In the first circuit we aquired v_{os} directly by measuring with the multimiter the output voltage. We used the second circuit to amplify v_{os}, thus we used the output to calculate v_{os}.
The third circuit is identical to the second circuit except for the added resistors in parallel that connect + to the ground. This was done for removing the influence of the bias current in the measurament. Exploiting this last circuit we removed v_{os} by using a trimmer and trying to make the output closest that we could to 0.

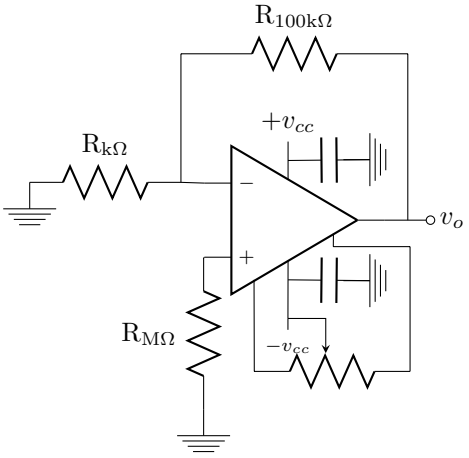


Figure 3.4: Positive bias current measure

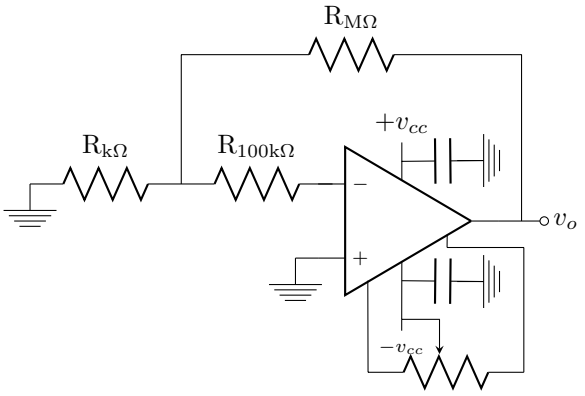


Figure 3.5: Negative bias current measure

The fourth circuit and fifth are used for measuring the current of bias indirectly using how the two currents are related to the output.
The sixth circuit was used for measuring the maximum current that the op-amp can erogate. In this configuration the oscilloscope's internal resitor was set to 50Ω

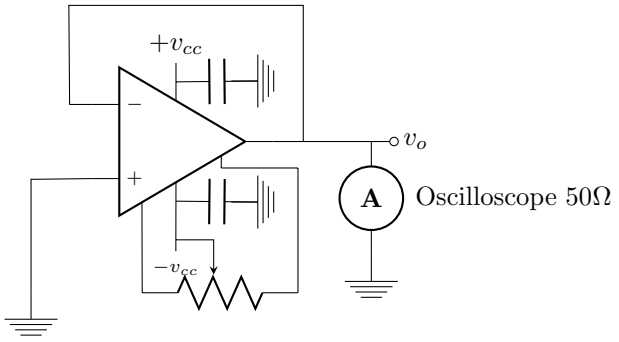


Figure 3.6: Max current measure

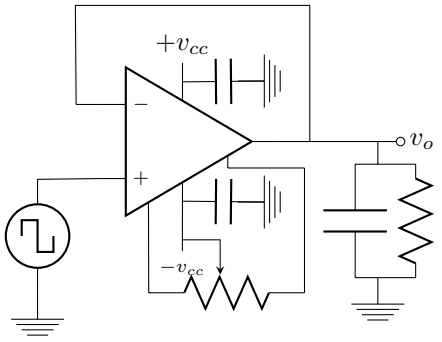


Figure 3.7: Slew rate

In the seventh circuit we measured the slew rate. As load the capacitor used was 1 ± 0.05 nF and the resistor 2 ± 0.1 kΩ. The input used was a 10 V square wave, so we aquired the image of the raising output.
In the last circuit we measured the common gain by using the differential amplifier with the same input 2 V peak-peak and 100 Hz.

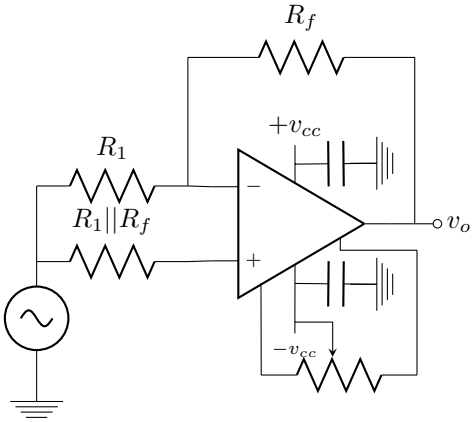


Figure 3.8: Common Gain

3.3 Data analysis

In the emitter follower (3.1) the output measured is -1.484 ± 0.005 mV. Being such a small output we expect to have problem with parassite resistor and other form of noise, that's why we don't consider the output too reliable, but it gives us an order of magnitude that is in agreement with the datasheet of the op-amp, that propouses a typical value of 1 mV and a maximum value of 5 mV.
In the amplifier (3.2) we can find v_{os}, by using

$$v_{os} = \frac{v_o}{1 + \frac{R_{10\text{k}\Omega}}{R_{10\Omega}}}$$

from the calculation we get $v_{os} = -1.333 \pm 0.001$ mV, which is has the same order of magnitude and same sign of the previous result.
Then as stated in the experimental setup we corrected the circuit (3.3) for compensating the effect of the current of bias. With the same formula used for the previous amplifier we get an offset voltage of 1.307 ± 0.001 mV. We used this circuit for nulling the offset with the trimmer.
In the fourth circuit (3.4) we calculated the current flowing in the non invertent pin by using

$$i_{b+} = \frac{v_o}{R_{\text{M}\Omega}(1 + \frac{R_{100\text{k}\Omega}}{R_{1\text{k}\Omega}})}$$

The value calculated is -39.042 ± 0.009 nA.
In the fifth circuit (3.5) instead we calculate the current flowing in the invertent pin by using

$$i_{b-} = \frac{v_o}{R_{100\text{k}\Omega}} \frac{R_{\text{k}\Omega}}{R_{\text{M}\Omega}}$$

above the value is -39.724 ± 0.009 nA. Now we can compute the current of bias $i_b = \frac{|i_{b-}|+|i_{b+}|}{2} = 39.383 \pm 0.006$ nA and the offset current $i_o = ||i_{b-}| - |i_{b+}|| = 0.68 \pm 0.01$ nA. i_b is less than 100 nA and near the typical value of 10 nA, as the datasheet states, but the offset current is a bit low being around a third of the typical value 2 nA.

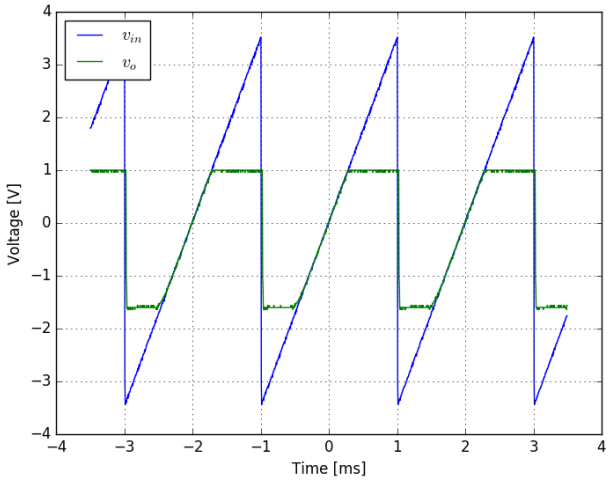


Figure 3.9: Saturated output caused by the maximum current erogated

In the sixth circuit (3.6) we calculated the maximum current erogated by computing the maximum/minimum output voltage over the resistance in the oscilloscope. In the plot is visible the different absolute value of the maximum and minimum output voltage, that's probably because the op-amp isn't perfectly symmetric in the packaging. So we opted to calculating two different maximum currents: $i_{max} = 0.0201 \pm 0.0001$ A (when the output was positive) and $i_{min} = 0.0328 \pm 0.0001$ (when the output was negative).

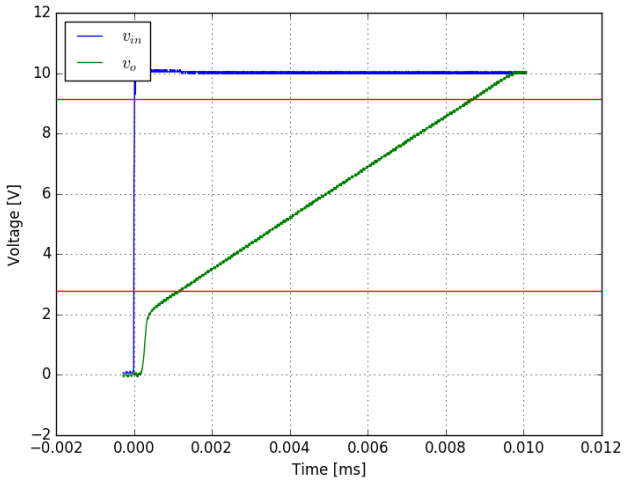


Figure 3.10: Saturated output caused by the maximum current erogated, red lines is 10% and 90% of the output

In the seventh circuit (3.7) we find that the slew rate of the op-amp used is $0.85\frac{\mathrm{V}}{\mu s}$, which is bigger than the typical value $0.5\frac{\mathrm{V}}{\mu s}$. One possible explenation of this would be that the slew rate depends on the amplitude of the signal, in our experiment the voltage was 50 times as large as in the test of visible in the datasheet, otherwise we have to conclude that our op-amp, has some difects that cause a larger slewrate.

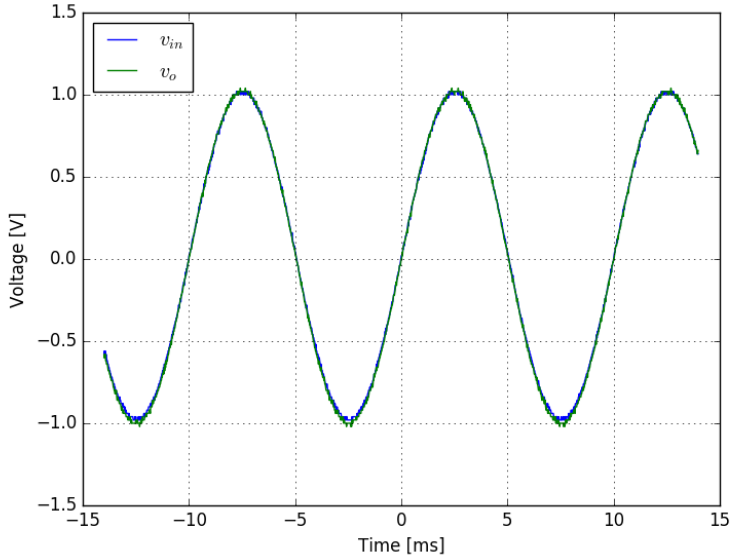


Figure 3.11: Saturated output caused by the maximum current erogated

In the last circuit (3.8) we measured the commond gain, by using

$$A_{CM} = \frac{2v_o}{v_{in1} + v_{in2}}$$

which gave us an unitary gain, as it is evident in the plot.

Experiment 4

Gain in function of the frequency

In a real op-amp the open loop gain (A_{ol}) is a function of the input frequency. In this experience we explored systematically this behaviour using 2 different circuits, one for the lower frequencies and the other for the higher one. After this study we built a non inverting amplifier with ≈ 10 and ≈ 100 gain for measuring its bandwidth.

4.1 Materials

- Operational amplifier uA741
- Resistors, trimmer
- Power supply RIGOL DP831A
- Waveform generator RIGOL DG1032
- Multimeter RIGOL DM3068
- Oscilloscope RIGOL MS02102A

The resistor chosen were $R_1, R_2, R_3 = 10\text{k}\Omega$, $R_4 = 10\Omega$, $R_5 = 100\Omega, R_6 = 1\text{k}\Omega$ with an error of 5% of the value.

4.2 Experimental setup

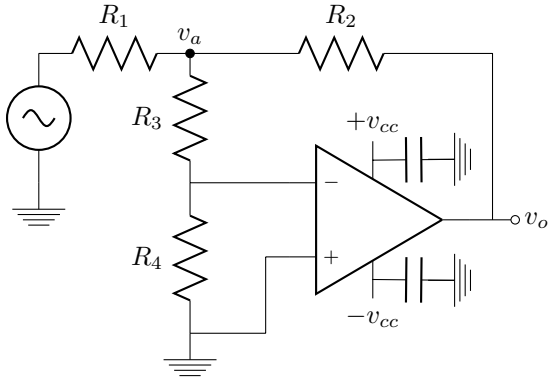


Figure 4.1: A_{ol} measure low frequencies

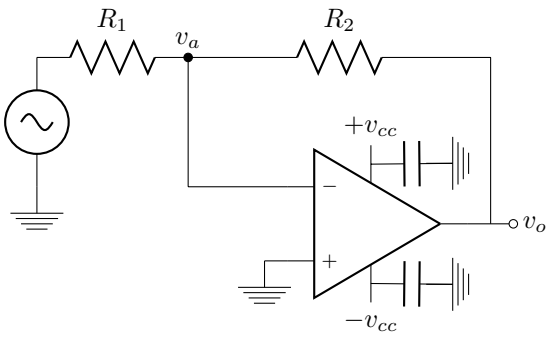


Figure 4.2: A_{ol} measure high frequencies

In this experience we took the measurament in all circuis by changing the frequency of the input, that was a sine wave signal 1 V peak-peak. The voltage chosen is not important, because we are interested

in the ratio between the amplitude of two signal. In the first circuit was used for calculating the gain in the open loop configuration A_{ol} in low frequencies by measuring v_a and v_o. This circuit was chosen for low freqencies instead of the second one, beacause the gain is too high for allowing us to acquiring directly the voltage difference between the two input pins. We didn't measure at lower frequencies than 30 Hz because the noise didn't allow us to make a reliable extimate of the amplitude of the two signals.
In the second circuit we measured v_o and the voltage of the non inverting pin v_a. The frequencies measured went from 10 - 200 kHz, because with high frequencies the absulute value of A_{ol} is low enough.
In the last two circuits we built an non inverting amplifier with gain of 100 and 10.

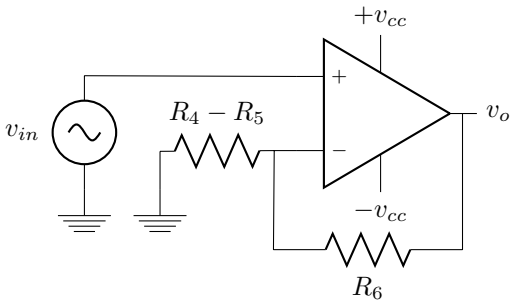
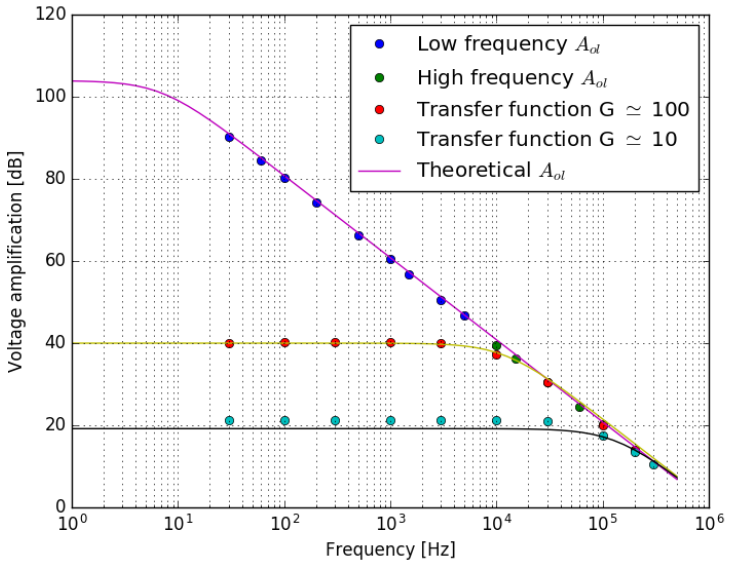


Figure 4.3: Non inverting amplifier

4.3 Data Analysis



In the first circuit we can extimate the open loop gain by using $A_{ol} = -\frac{v_o}{v_a}\frac{R_3+R_4}{R_4}$. In the second circuit we calculated $A_{ol} = -\frac{v_o}{v_a}$.
We can see from the plot that the data appears to be on a straight line, we can also see if that line is compatible with the values in the datasheet. We can compute the theoretical open loop gain with:

$$A_{ol}^{teo}(f) = \frac{A}{1 + j\frac{f}{f_0}}$$

Where $f_0 = 8$ Hz is a parameters available in the datasheet and $A = 1.5 \times 10^5$ was obtained with the best fit, j is the immaginary unit and f is the frequency. We can see from the plot that our data is consistent with the theory and the datasheet.
For the last two circuit we plotted $H = \frac{v_o}{v_{in}}$, the theoretical curve is the following:

$$H(f) = \frac{\frac{A_{ol}}{1+A_{ol}\beta}}{1 + j\frac{f}{(1+A_{ol}\beta)f_0}}$$

Experiment 5

Introducing the comparator

We first built a relaxation oscillator with different periods, then we tested the LM311 comparator and used it for designing a switch that goes on and off depending on the environment light.

5.1 Materials

- Comparator μA741
- Operational amplifier LM311
- Phototransistor OP550A
- Resistors, trimmer, LED, capacitors
- Power supply RIGOL DP831A
- Waveform generator RIGOL DG1032
- Multimeter RIGOL DM3068
- Oscilloscope RIGOL MS02102A

5.2 Experimental setup

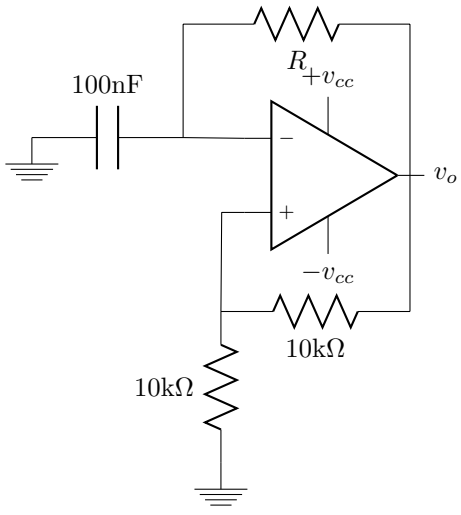


Figure 5.1: Relaxation oscillator

At first we used the μA741 (powered with ± 15 V) as a comparator in order to build a relaxation oscillator producing a square wave from a capacitor charge and discharge: we chose $R_1 = R_2 = 10k\Omega$ and a 0.1 nF capacitor. The circuit has been tested with 5 different values of R in order to have different periods. A measure has been taken also setting the oscilloscope in single mode and then switching on the power supply.
We than tested the LM311 both as non-inverting and inverting comparator using $R_L = 1k\Omega$.
Regarding the Schmitt's trigger, we added to the previous circuit the resistences $R_1 = 10k\Omega$ and $R_2 = 100\Omega$ and analyzed the behaviour at the point when $v_{in} \approx v_{ref}$.

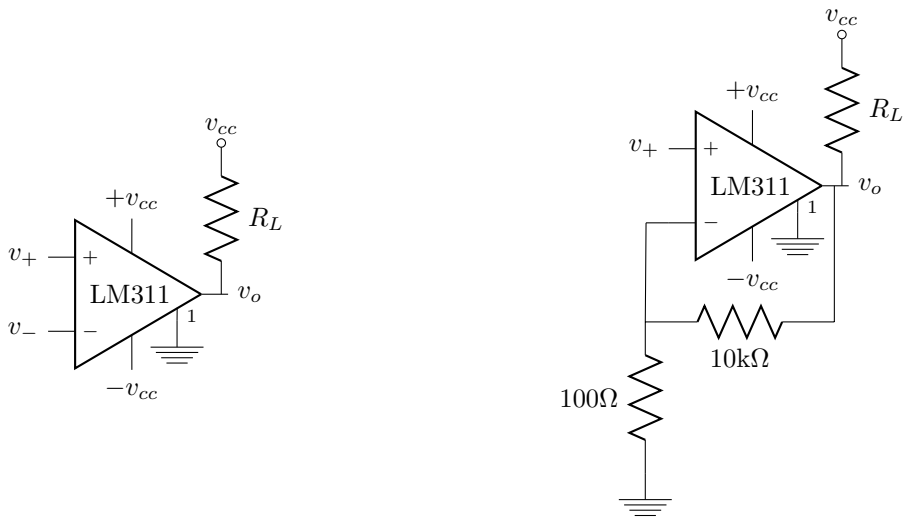


Figure 5.2: Comparator test with and without Schmitt's trigger

At last, we built the twilight switch in circuit 5.3. We used a phototransistor, which give us a costant current based on the light, a op-amp stage for converting the current in voltage, due to the fact that che current of the phototransistor is very small we had to adjust the offset of the op-amp for avoiding sistematic errors. In the last stage we used a comparator for switch a led on and off comparing a voltage reference v_{ref} with the op-amp stage output.

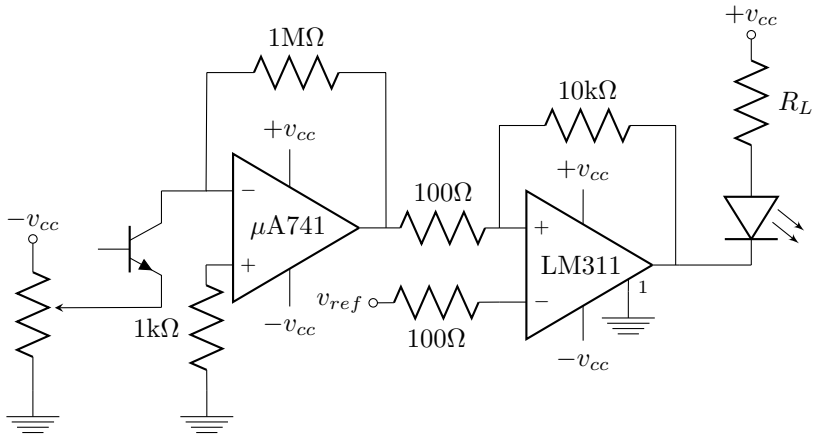


Figure 5.3: Twilight switch

5.3 Data Analysis

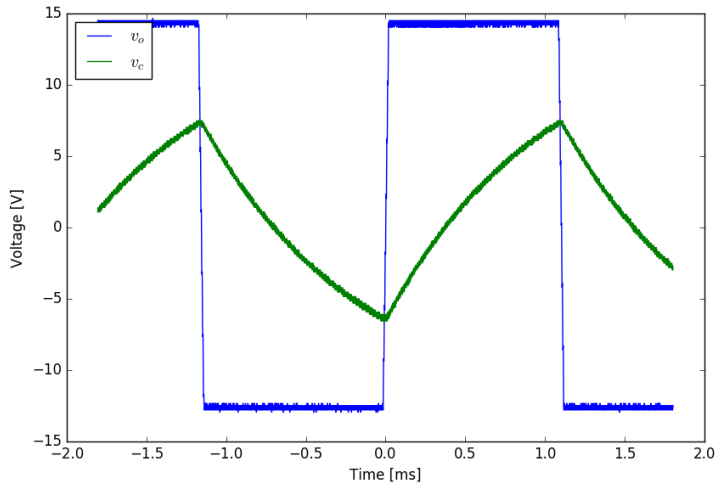


Figure 5.4: op-amp output v_o and capacitor voltage v_c with $R = 10\text{k}\Omega$

The period of the oscillator is related to the resistor R as follows:

$$T = 2RC \log\left(1 + \frac{2R_1}{R_2}\right)$$

where C is the the capacitor and $R_1 = R_2 = 10\text{k}\Omega$. Using the value measured with the multimeter with plot a theoretical curve in funciton of R. We can see that the data are on that line. We've not done a regression because we did not have the error on the periods.

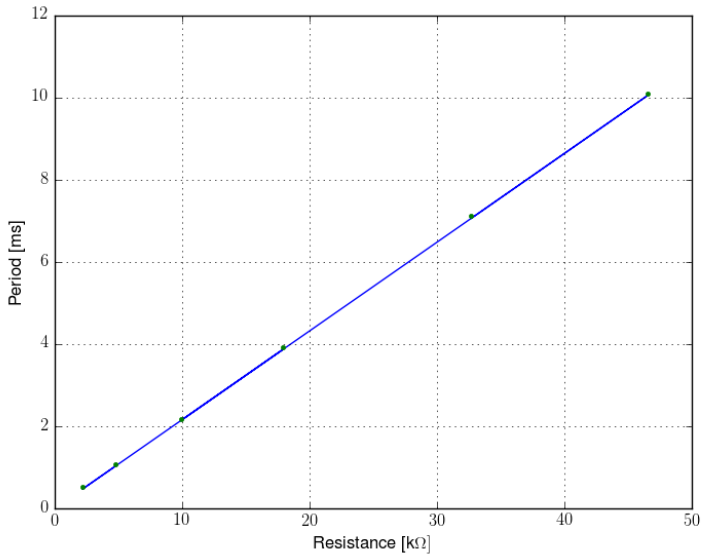


Figure 5.5: Data (green dots) and theoretical curve (blue line)

In the following figures we can see the difference in the comparator output with and without the Schmitt's trigger. If there's not the Schmitt's trigger, the noise can cause a non desired on-off

switching. The Schmitt's trigger raise and lower the threshold of the switching for avoiding this kind of problems.

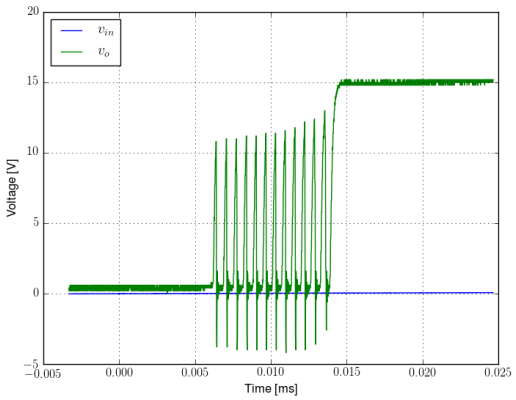


Figure 5.6: Without Schmitt's trigger

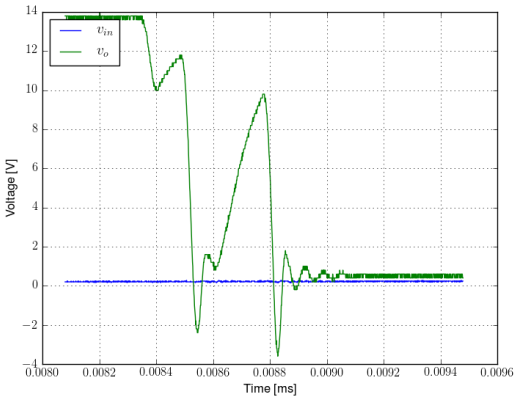
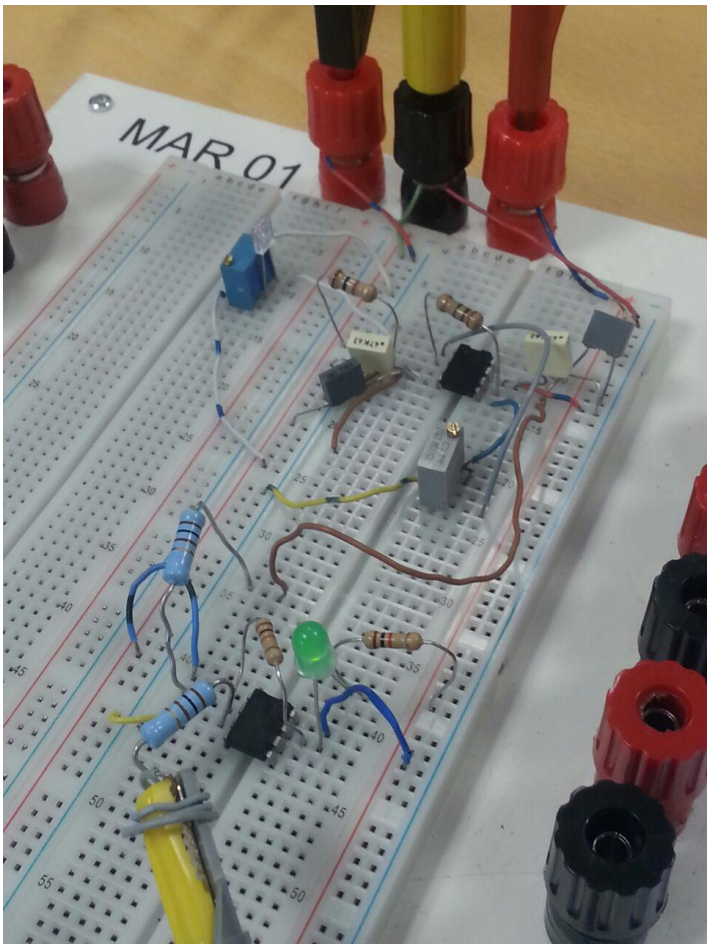


Figure 5.7: With Schmitt's trigger

The Twilight switch worked, it was turning on when we was covering the phototransistor and we were able of choose the threshold for the switching by adjusting the voltage reference v_{ref}. Below a photo of this circuit.



Experiment 6

Building an electronic thermometer

We build and electronic thermometer. This was done by using the PT100, a platinum resistor with a known thermal coefficient α. We made a fixed current pass through the PT100 and we took the voltage on each end of the resistor, we amplified this signal and with an intrumentation amplifier we imposed the final output to be 0 V when the temperature was 0 °C. The objective was to have a voltage that could've been easily converted to a temperature by multipling it to a coefficient $\eta = 10\frac{^\circ C}{\mathrm{V}}$

6.1 Materials

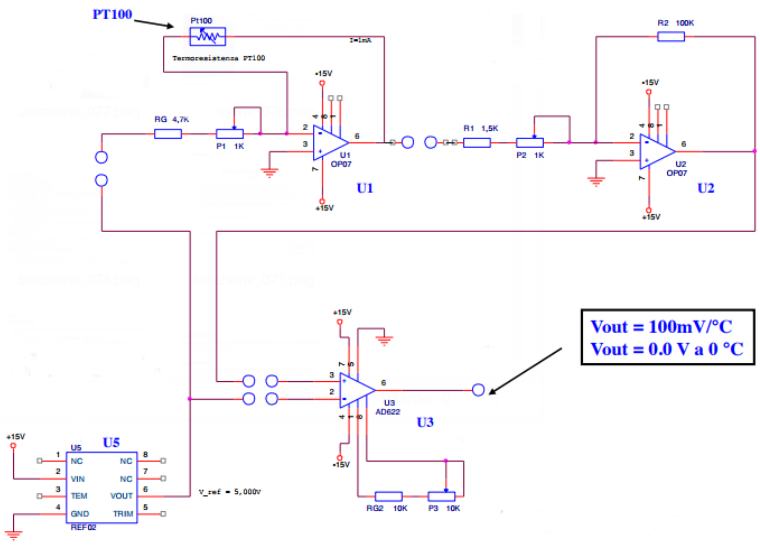
- Operational amplifiers OP07
- Instrumentation amplifier (INA) AD622
- Precision +5V Voltage Reference REF02
- Thermoresistor PT100
- Resistors, trimmers
- Power supply RIGOL DP831A
- Waveform generator RIGOL DG1032
- Multimeter RIGOL DM3068
- Transistor 2N2222

The resistors used were all with an uncertainty of 5%

6.2 Electronic thermometer

Firstly we measured the resistance of the PT100 with two methods. With the standard two wires measure, by adding on each end two 10 Ω resistor to simulate the presence of parassite resisor. We measured $R_t = 13x\Omega$ which converted with $T = \frac{R_t - R_0}{R_0 \alpha}$ [1] gave us $80xx^\circ C$. We then used the 4 wires configuration and meausured $R_t = 10x\Omega$ and the temperaure of $^\circ C$.

[1] R_0 is the PT100's resistance at 0 $^\circ C$ and α is the thermal coefficient, that is around $0.003850^\circ C^{-1}$



For build the thermometer circuit first we turned the resistor's mesurament in a voltage's mesurament, we've done this simply using a fixed current in the PT100. For letting flow a fixed current in the PT100 we needed a highly stable current generator. The one we built needed a stable input voltage, for this reason we used the REF02 that had an output of 4.9993 ± 0.0003 V. Then we measured the current passing through the the PT100 and we made it as close as 1mA by tweaking the trimmer attached to the inverting pin.
For having the output with the format required in the abstract we needed the total gain of the circuit to be $G_{tot} = \frac{100\,\frac{mV}{°C}}{\alpha} = 259.740$. Because we also needed to set the output to 0 mV at 0 °C we decided to first amplify the voltage on the ends of the PT100 by a factor of 50 and then use this output in the differential amplifier, that had a gain of 5.195, this allowed us to take the first amplified signal and compare it with the signal that would had been at $0°C$ (in our case exactly 5V).
For the amplifier stage we used a OP07 in inverting configuration. For setting the gain of the amplifier stage we used an input voltage of around 100 mV and we made the output signal as close as possible to 5 V, by using a trimmer.
In the last stage of the circuit we used AD622 that had to be tested and needed some getting used to, for this reason we built a bridge circuit with attached the AD622. We used two resistors of 100kΩ, one of $1k\Omega$ and one of 100Ω with in series a trimmer, we used also a resistance of 51.1 Ω (1% of uncertainty) to set the gain of the AD622 to 1000 (989.3 to be exact). By changing the resistance of the trimmer we were able to null the output voltage.

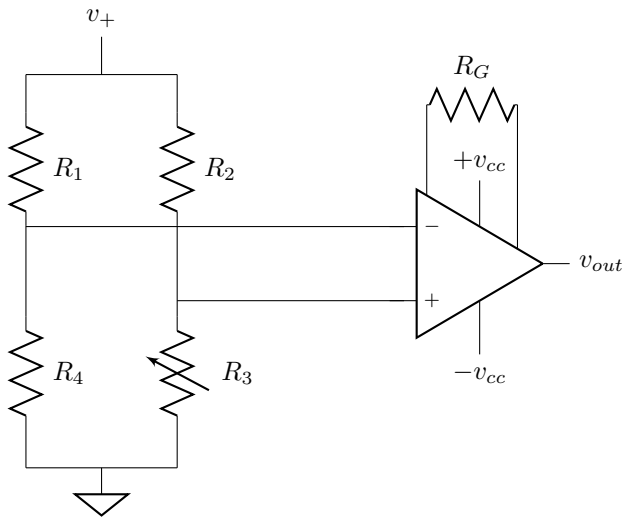
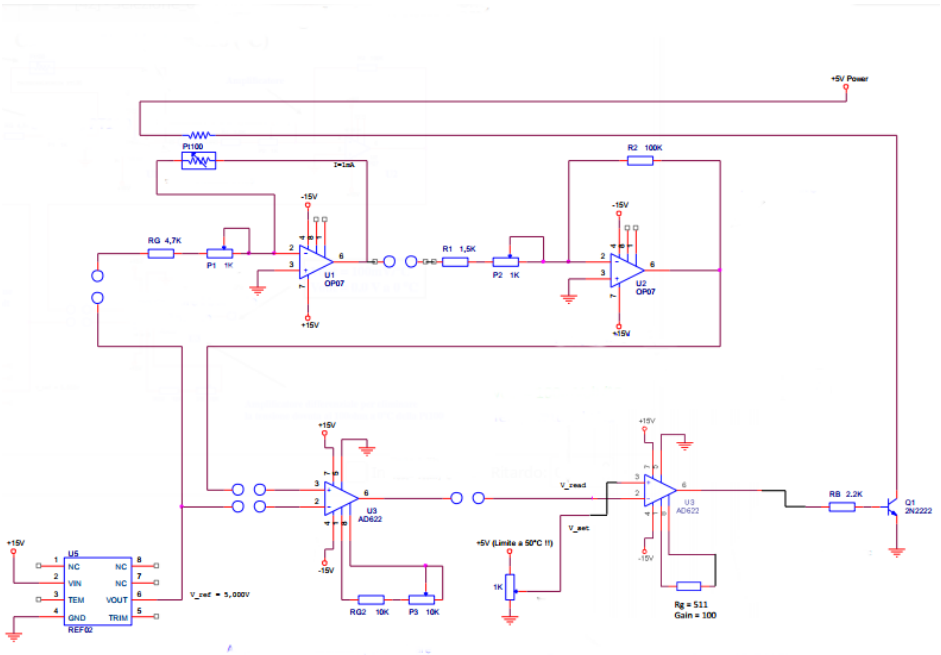


Figure 6.1: Testing bridge

After this test we felt confident to build a differational amplifier with a gain of 5.195, by putting to ground the inverting signal and using a sine wave signal of 100mV on the non-inverting pin and changing the output by tweaking the trimmer attached to the R_G pin.
At last we connected all the circuits together. The signal from the current generator was used as input signal in the amplifier and the output of the amplifier was placed on the non-inverting pin of the differential amplifier and on the inverting pin was placed the voltage generated from the REF02. we connected the output to the multimeter and changed the setting to output 1 °C to for each 100mV in the output. The value visible was about 25 °C and we made sure that it was changing by heating the PT100.

6.3 The P of PID



We connected the output of the thermometer to a differential amplifier with $G = 100$. So we compered the temperature with a reference chosen by us, by connecting the non inverting pin to a trimmer. The output of the INA was connected to the base of a NPN transistor using a resistor in between. The transitor controlled a power circuit made with a small resistence R with a voltage of 5V taken from the agilent generator. The PT100 was placed attached to the small resistor, so we measured the temperature of R. When the temperature set by the trimmer is different frome the one measured with the PT100, the difference is amplified and converted to a current in the power circuit which heat up the resistor until the the difference in temperature is nullified. The current flowing in R is proportional to the temperature difference. The differential amplifier had a saturation voltage of around 10, so the amplification of 100 allowed us to control the temperature on a range of 1 °C (100 mV).
For the current's measure we used a tester ICE placed between R and the transistor. During the test, when we changed the desired temperature using the trimmer, we saw the current raise and then make damped oscillations towards a stable current.

Experiment 7

ECG: Electrocardiogram

In this experience we built and designed an electrocardiogram and tested it on a member of the group.

7.1 Materials

- Operational amplifiers OP07
- Instrumentation amplifier (INA) AD622
- Precision +5V Voltage Reference REF02
- Thermoresistor PT100
- Resistors, trimmers
- Power supply RIGOL DP831A
- Waveform generator RIGOL DG1032
- Multimeter RIGOL DM3068
- A AD622, three OP07, a ISO124
- Three electrodes
- Batteries 9 V

The resistors used were all with an uncertainty of 5%

7.2 Experimental setup

The circuit connected with the patient was all powered by using a battery ± 9.
The signal that we should aquire from the electrodes has a frequency of around 1.5 Hz and an amplitude of ± 1 mV with an offset due to the internal potential of the electrodes of 700 mV. We also need to consider the possible sources of noise caused by the movement of the body and the cables, also by the parasite capacitance and inductance. For these things our circuit need to remove the common potential and annihilate as much as possible the noise without removing signals at 1.5 Hz frequencies.

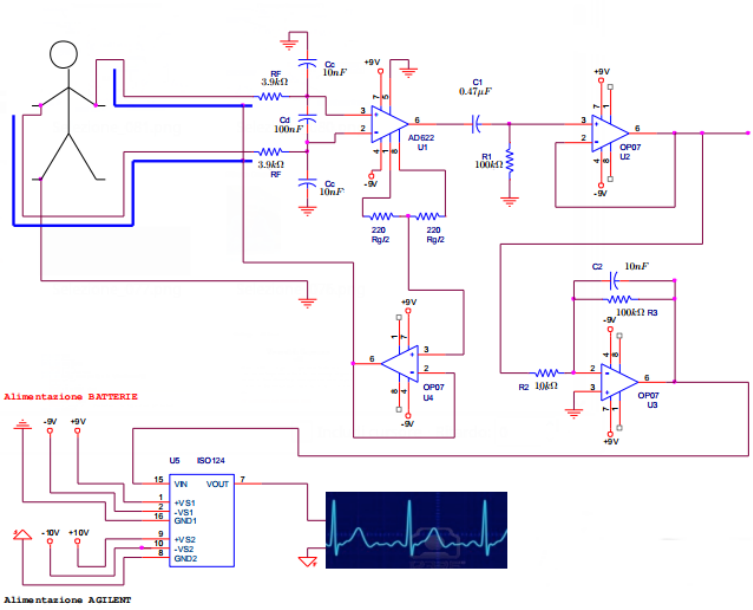


Figure 7.1: Wave measured

The first step was removing high frequency noise by using two low-pass filters on the input by using two resitors and three capacitors.

Than we removed the common signal by using the AD622 with a gain $G = \frac{50.1k\Omega}{440\Omega} + 1 = 116$, where at the denominator there is the resistance of the resistor connecting pin 1 and 8. This resistor is actually built with two resistors in series with half its value. The signal between these two resistors is used in a follower that serves to set the potential of the cable's shield to the same of the wire.

Than we chose to put the signal amplified by the AD622 into a high-pass filter for removing other DC (or almost DC) components and than we used a follower for mismatching the impedance of the circuit.

The penultimate step was taking the signal out of the follower and connecting it to a active low-pass filter.

The last step was decoupling the circuit connected with the patient with the circuit of the oscilloscope, by using an ISO124. This is done for physically separating the power generator and oscilloscope from the the circuit connected with the patient. This was done for avoiding electrocuting the patient in case of mulfunctions.

7.3 Data analysis

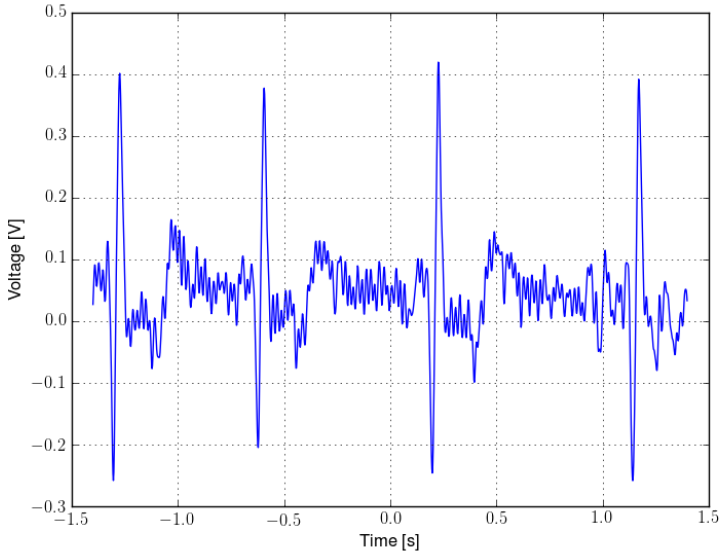


Figure 7.2: Signal measured

The signal acquired with the oscilloscope is in the figure above. Originally we had noise at high frequency, the signal above is smoothed with a running mean algorithm.

Experiment 8

Wien bridge oscillator and digital electronic

In the first part of the experience we built a wien bridge oscillator with an automatic gain control which was made possibile by the changing resistance of a tungsten light. We focused our attention on the wave's quality and the critical time of startup. The second part was about digital electronics, after we got confident with a NAND port we designed a circuit for an house alarm system.

8.1 Materials

- Resistors, trimmers
- A tungsten light
- Power supply RIGOL DP831A
- Waveform generator RIGOL DG1032
- Multimeter RIGOL DM3068
- OP741
- DM74LS244
- DM74LS00

The resistors used were all with an uncertainty of 5%

8.2 Experimental setup

8.2.1 Wien brigde oscillator

For building the wien bridge and have it oscillate it is needed $R_2 = 2R_1$, for this reason we used a trimmer as R_2 and we used in series a resistor of 47Ω with the tungsten light. We have set the trimmer at a resistance around twice the resistance of 47 Ω and the light. This way when we turn on the circuit, the current start flowing in the tungsten resistor increasing its resistance, thanks to the heat produced by the current, and bringing it closer to half R_2. This is, in theory, what is needed for the circuit to oscillate, but it can be seen in the analysis that the circuit took some time for stablizing.

DW/IK	00	01	11	10
00	0	0	0	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

Table 8.1: D = Door, W = Window, I = Infrared, K = Key

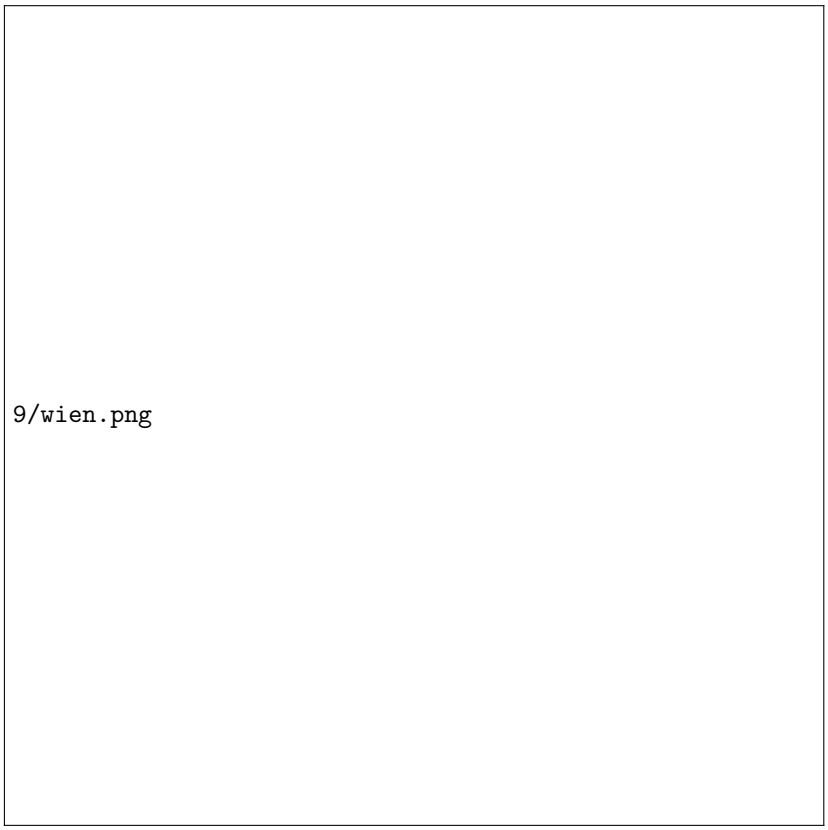


Figure 8.1: Wien bridge

8.2.2 Logic gates

We needed to use some DM74LS00, so the first thing we did was testing it by using it as NAND with the help of DM74LS244 for a visual confirmation. For designing the alarm system we wrote the table of Karnaugh and we minimized it.

The simplified form is $Y = D + W + I\overline{C}$. The problem was that we only had NAND gates so we needed to write OR, AND and NOT with NAND. NOT is the easiest one, because you only need to connect the signal with both inputs of the NAND. AND you get it by negating the output of the NAND. For the OR gate you need to negate both input and use the two signal as input for a NAND.

8.3 Data analysis

In the plot 8.2 we can see how the output oscillates a lot before stabilizing forming a sine wave (as in figure 8.3) of frequency of 1110 Hz that is around the value of :::

Figure 8.2: Starting process of the wien bridge

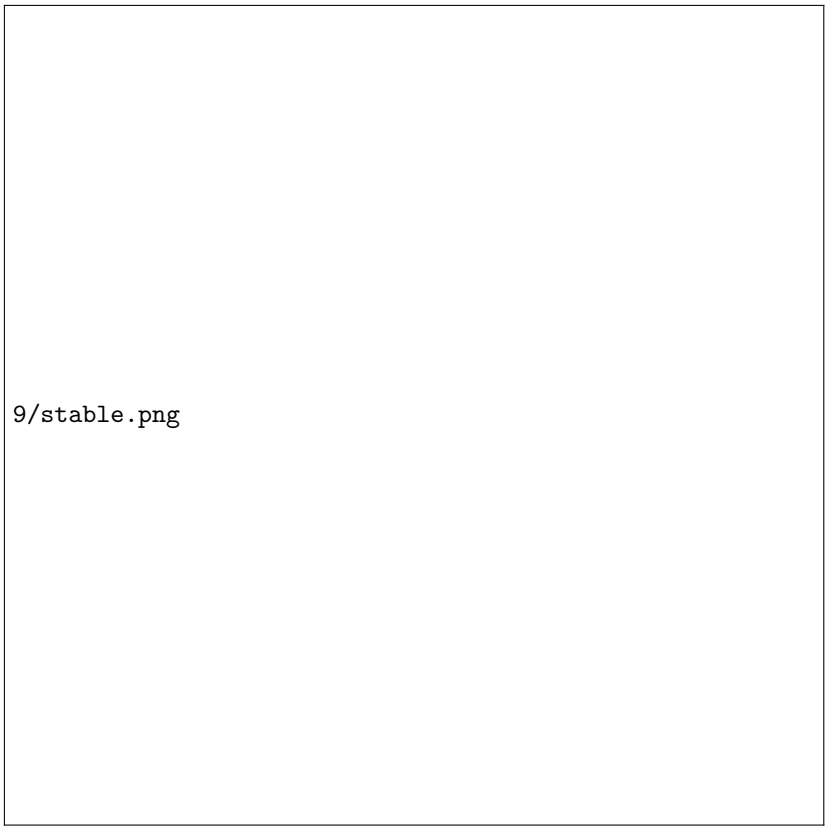


Figure 8.3: Stable state of the wien bridge

We also tested the circuit removing the by-pass capacitors and, as we can see in figure 8.4, the noise is too high for allowing a stable state.

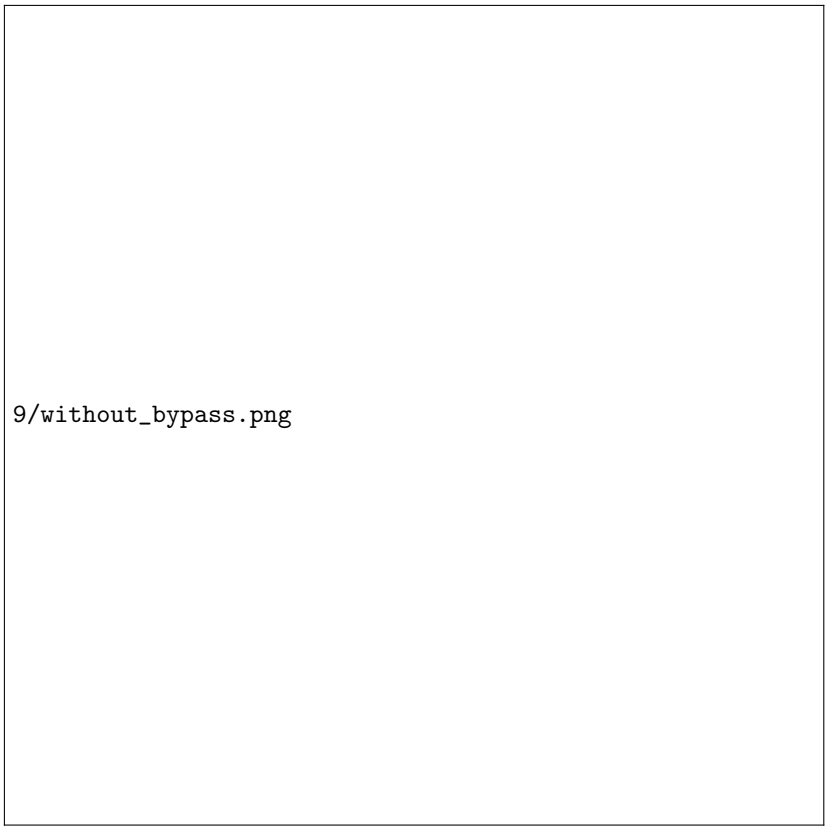


Figure 8.4: Bridge without the by-pass capacitors

Experiment 9

TTL and multiplexer

In this session we first measured the latancy between the input and output signal, then we used a NOT gate with open collector to turn on a LED, thirdly we designed and built an half dulpex with two 3state gates and lastly we projected and implemented a multiplex depultiplex system with 4 signals and two bit of selection.

9.1 Materials

- A resistor
- A LED
- Power supply RIGOL DP831A
- Waveform generator RIGOL DG1032
- Multimeter RIGOL DM3068
- 74LS00
- 74LS05
- 74LS04
- 74LS125

9.2 Experimental setup

For measuring the time propagation of the signal in the 7400 we used the configuration in figure 9.1. As input we used a square-wave with 0-5 V voltage and the frequency of 100kHz.

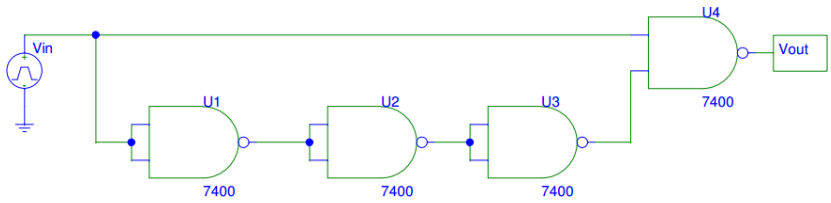


Figure 9.1: The circuit used for measuring the latency in the propagation of a digital input

For switching on and off the LED we used the circuit in 9.2 with a power supply of 9 V and a resistor 1 k Ω.

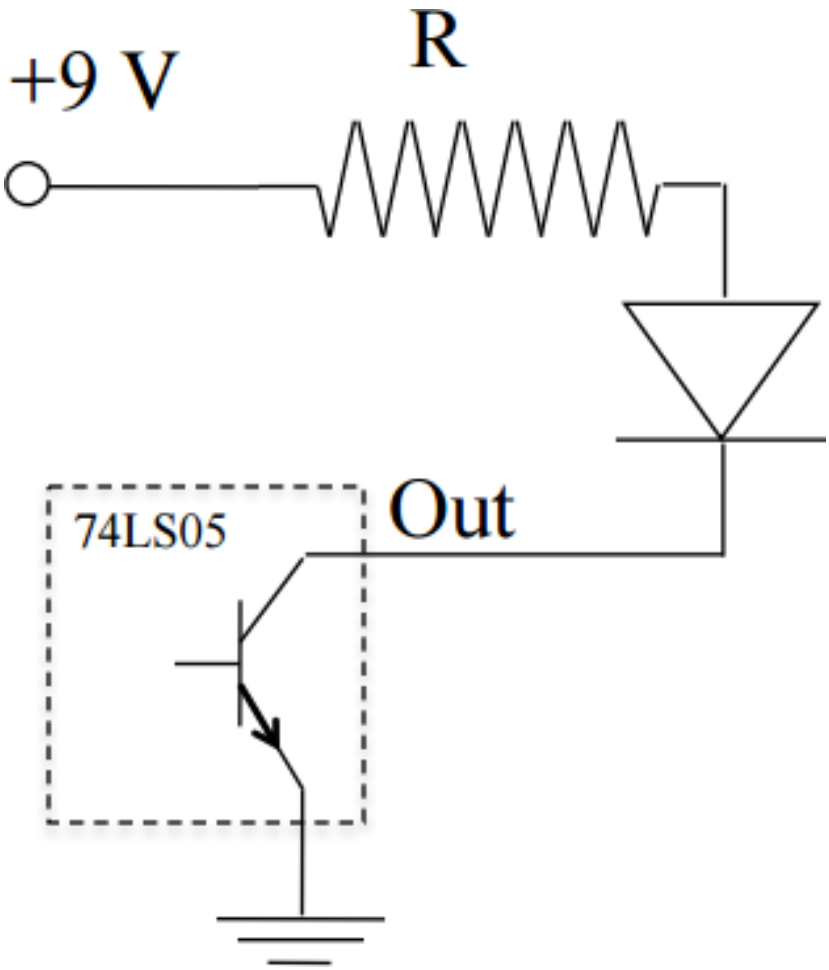


Figure 9.2: NOT TTL Open Collector

For the half duplex we built it as in figure XX, we connected the two input by first passing the signals into a 3state that had the enable bits opposite to one another, so they passed just one singal at the time. It was possible to change signal by changing the voltage in S.

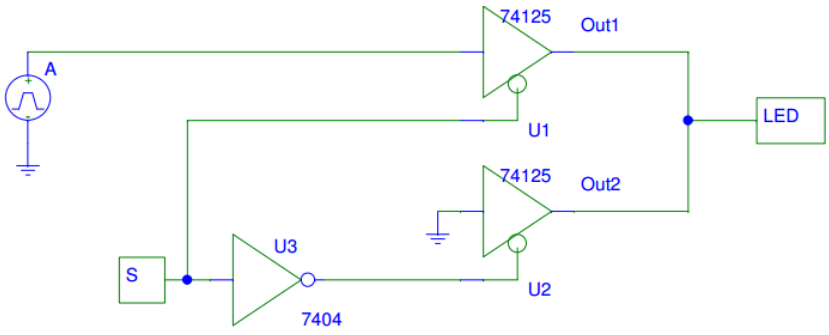


Figure 9.3: Half duplex used for sharing a transmission channel

Lastly we designed a network to pass 4 different signals to all of our friends, we called this network "Canteriphone". First we needed to design a multiplexer to choose between the 4 signals with 2 bits, this was implemented with the circuit 9.4.

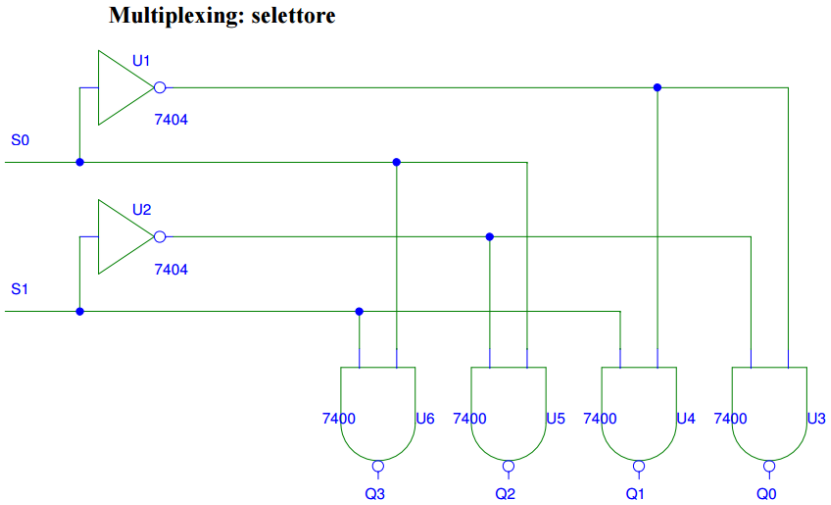


Figure 9.4: The multiplexer used for select one of the four channel

Then we used the signals from the multiplexer to enable and disable 4 3state gates that were connected with the information that we wanted to transmit, this was done in a fashon similar to the half duplex and we can see the circuit in 9.5.

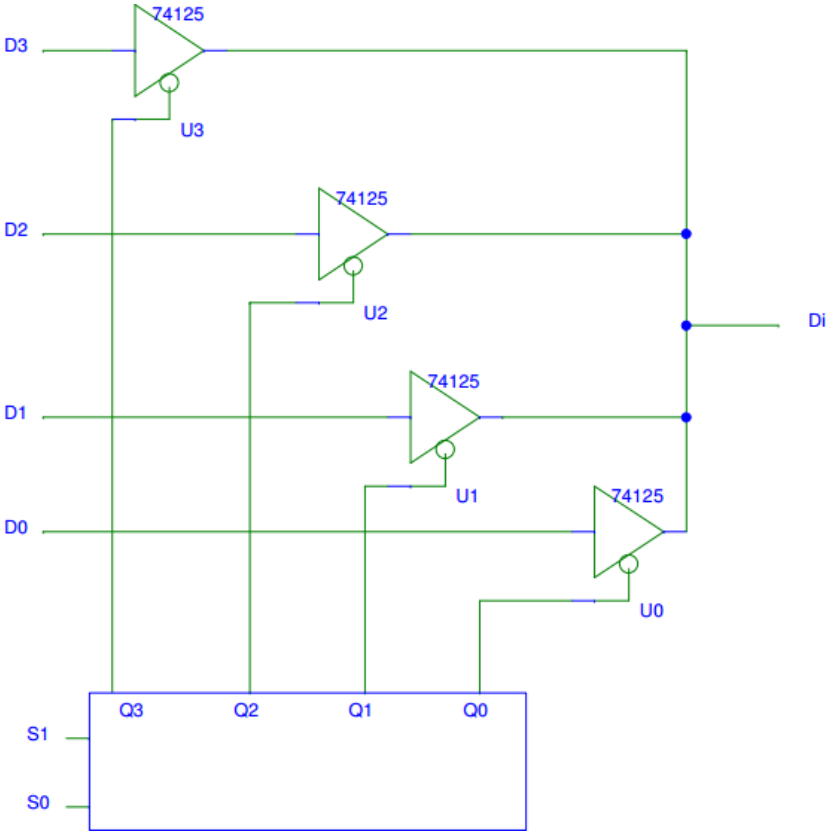


Figure 9.5: The signal from the multiplexer used for blocking and allowing the chosen channel

Then we took the signal from the output of the 3state gates and connected it with our friends with a cable, we also transmitted the two bits that were used to choose the signal, for allowing them to know what channel we were transmitting. Our friends built a multiplexer in 9.4 themself and used the outputs from the multiplexer and the signal transmitted to light a led with the circuit 9.6.

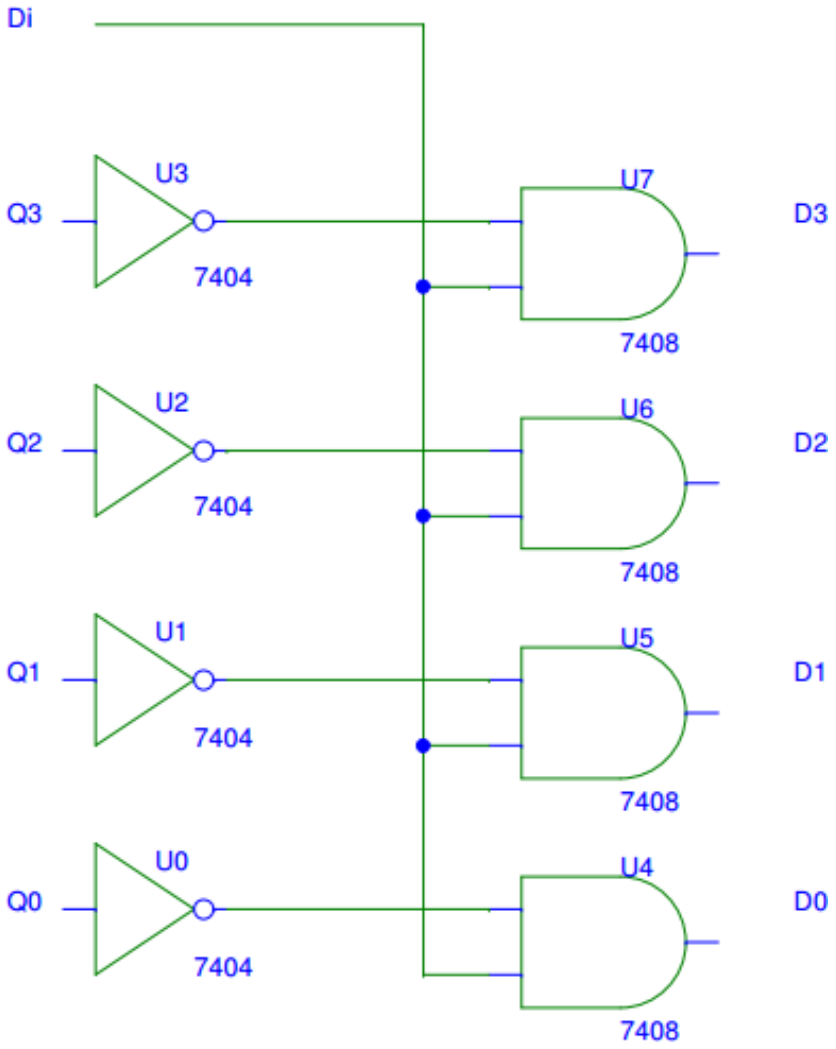


Figure 9.6: De-multiplexer

9.3 Data analysis

In the plot 9.7 we can evaluate the time delay caused by the single gate. We see that the signal from the point it started descending to the point it started going up, it took about 14 ns, that divided by the three gates gives about 4.7 ns per gate. We chose the starting point when the output has a degative derivative, because that is the moment when the first pin recives the signal, and we chose the ending time when the signal invertes direction, bacause that is when the second signal propagated in all the three gates.

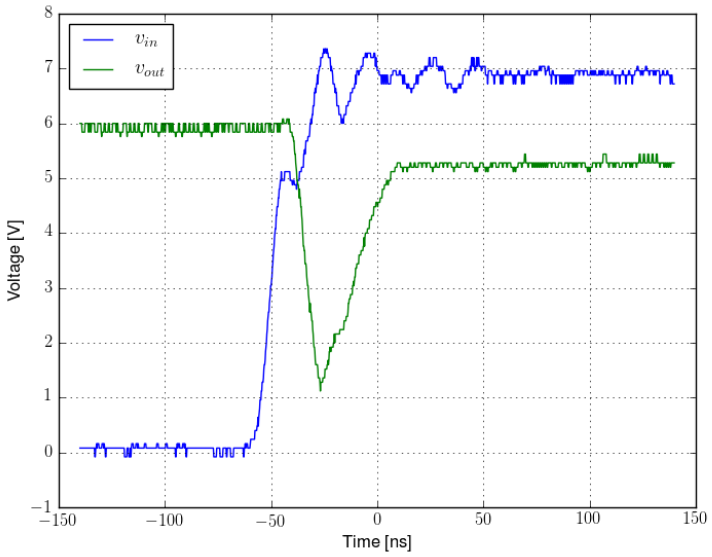


Figure 9.7: The plot shows the delay caused by the propagation of the signal in 3 gates

Experiment 10

System stability analysis and Logic circuits

In the first part of the experience we implemented the cicuits: latch SR, latch SR synchronized (flip flop) and FF type D. All of them by using just NAND and NOT gates. Later we built an anti-bounce latch SR and a circuit that registers an impulsive input by storing it in the memory. Later we used and tested an J-K FF shift register and an 8-bit counter.

10.1 Materials

- Resistors, trimmers
- Power supply RIGOL DP831A
- Waveform generator RIGOL DG1032
- Multimeter RIGOL DM3068
- NAND 74LS00
- NOT 74LS04
- 74LS109
- 74LS191

The resistors used were all with an uncertainty of 5%

10.2 Experimental setup

We built the latch SR as in the figure 10.1 and for visualizing the output we connected Q and $\overline{Q}$ to an 8-led chip.

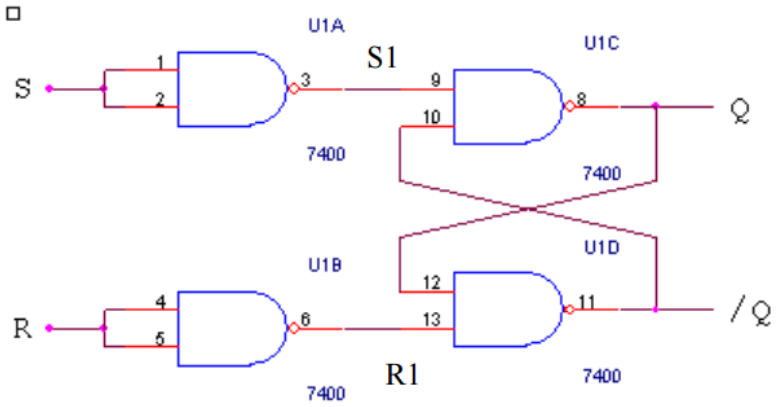


Figure 10.1: Latch SR

Later we modified the circuit as in figure 10.2 and we verified that when EN is low voltage the circuit is in the HOLD configuration, that is it keeps the memory of the previous state.

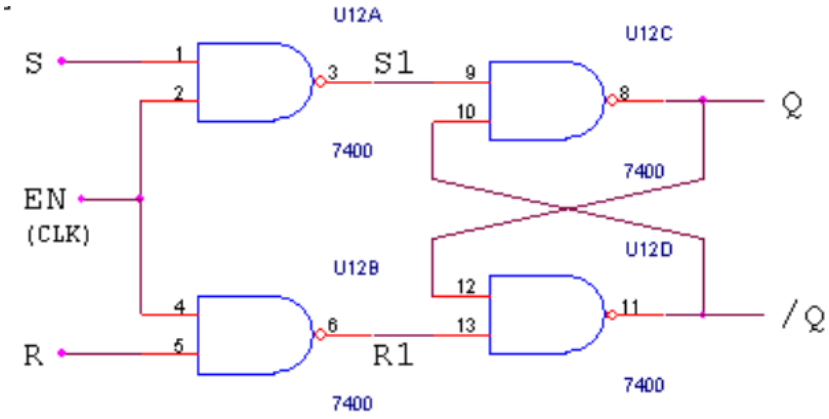


Figure 10.2: Flip-flop built with NAND gates

We modified again the circuit to be an FF type D (figure 10.3) and we verified that every time the EN is on the bit on D is registred in the memory.

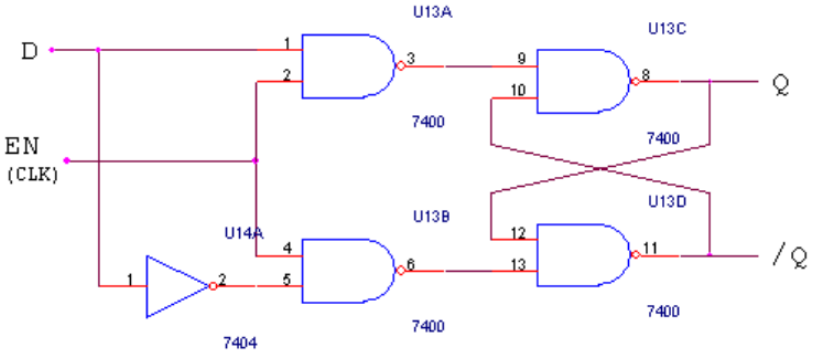


Figure 10.3: FF type D

Then we built a latch SR with an “anti-bounce” configuration (figure 10.4, in particular we made sure the output was changing from LOW to HIGH without too much noise.

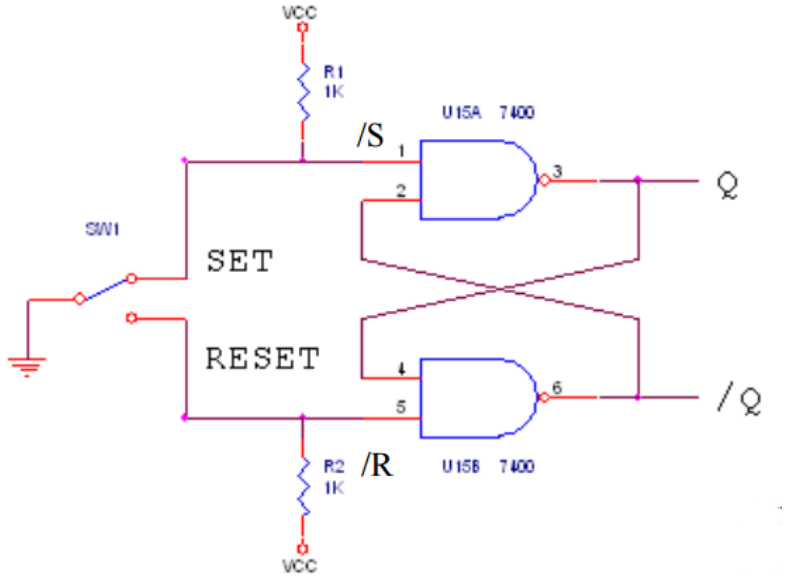


Figure 10.4: Anti bounce circuit

We later built an on/off system (figure 10.5) that had a HIGH output on when we activated SET for a short amount of time and a LOW one when we did the same with REST.

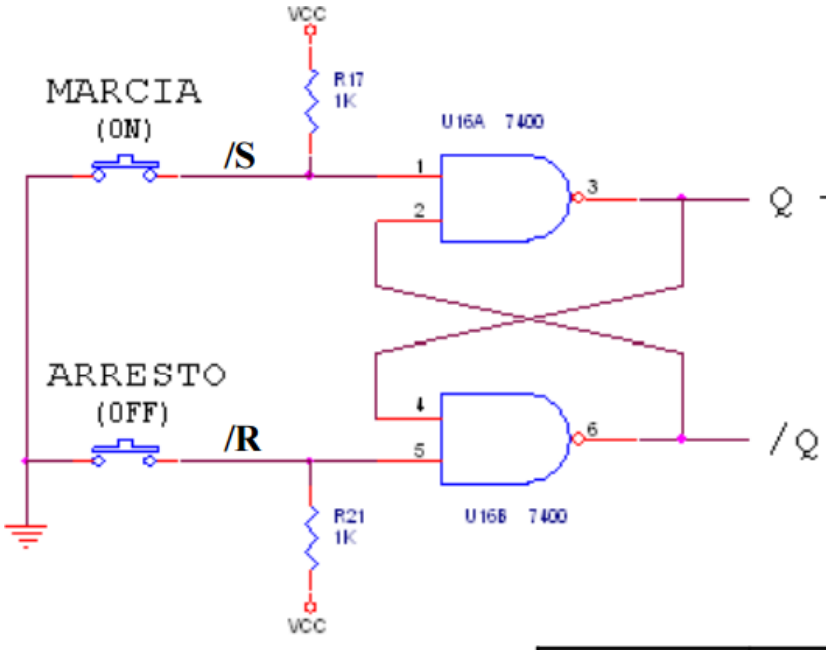


Figure 10.5: On-off circuit

We also built a circuit in 10.6 that gave as output a square wave with frequency that was half or a quarter of the clock, depending on where we took the output. This was done by using two J/K FF connecting the clock with the output of the previous FF or the clock (for the first FF) and connecing J to V_{cc} and K to ground. The frequency of clock used was 10 Hz.

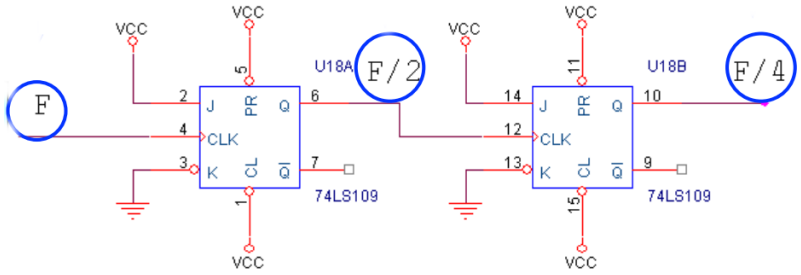


Figure 10.6: Frequency divider

We built the shift register in 10.7 with four J/K FF used as FF type. We connected the FF in circle connecting the output of one with the input of the other. We also used the pin CL and PR to preset the bit in the registers with the help of a capacitor that kept the voltage LOW for a short amount of time. We visualizied the shift register connecting the output of each FF to some LED.

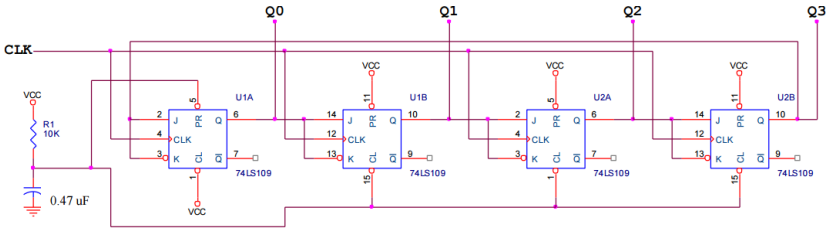


Figure 10.7: Shift register

Laslty we built a counter with two 74LS191 an a D-FF as in figure 10.8. The FF was used to set if we wanted to count up or down by connecting the output to the D / $\overline{U}$. We connected the clock to the elements of the cicuit for setting the frequency of each bit. We used the same method used in the shift register for presetting the bits in the counter. For using an 8 bit system we needed to activate the second 74LS191 just when the bits of the first were all on, this was done by connecting RCD to G of the second one used to enable.

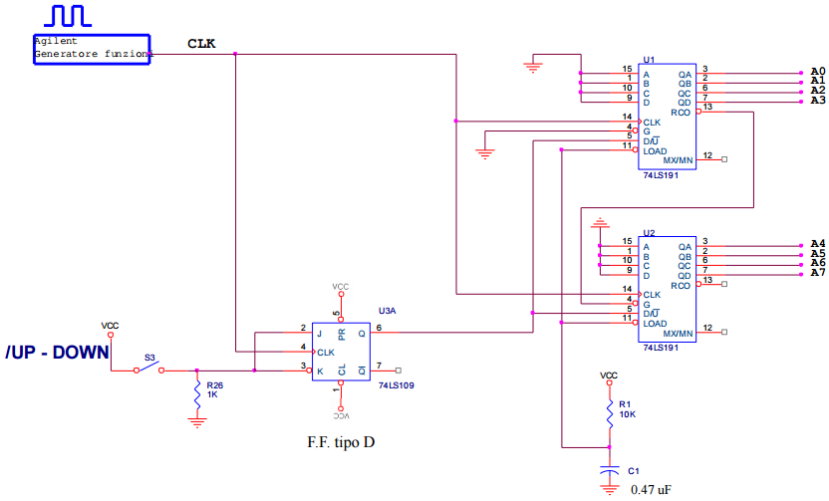


Figure 10.8: 8-bit counter

10.3 Data analysis

We can see in the plot 10.9 that the output of the latch SR is really noisy without the anti bounce expedient.

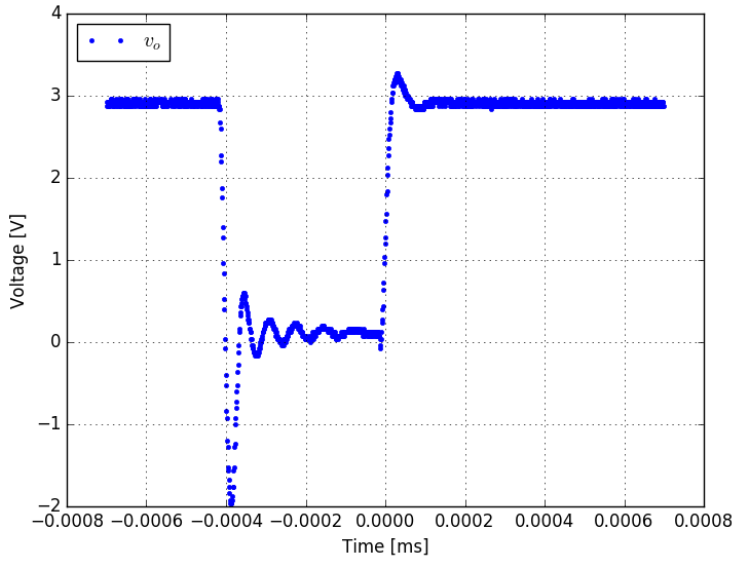


Figure 10.9: Output of a standard latch SR

When we modify as in 10.4 we can see that the output is much more stable.

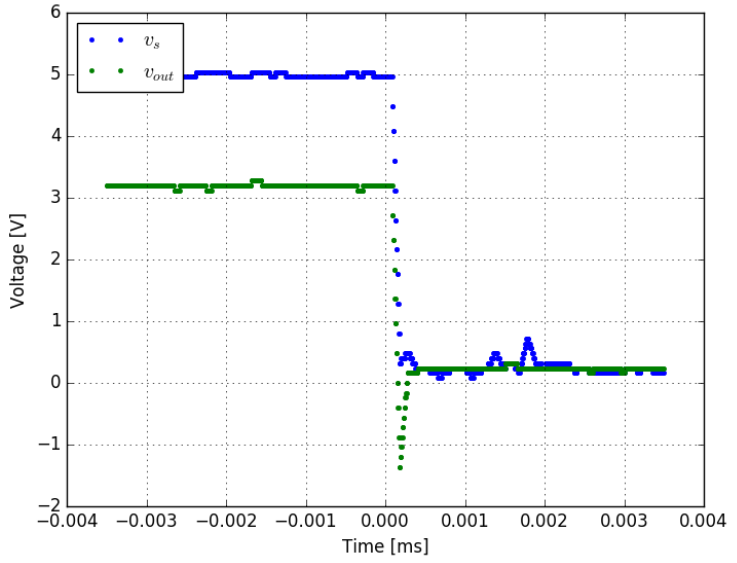


Figure 10.10: Output of a standard latch SR

We can see that in the plots of fequency divider circuit we have the outputs as expected with half and a quarter of the frequency of the clock.

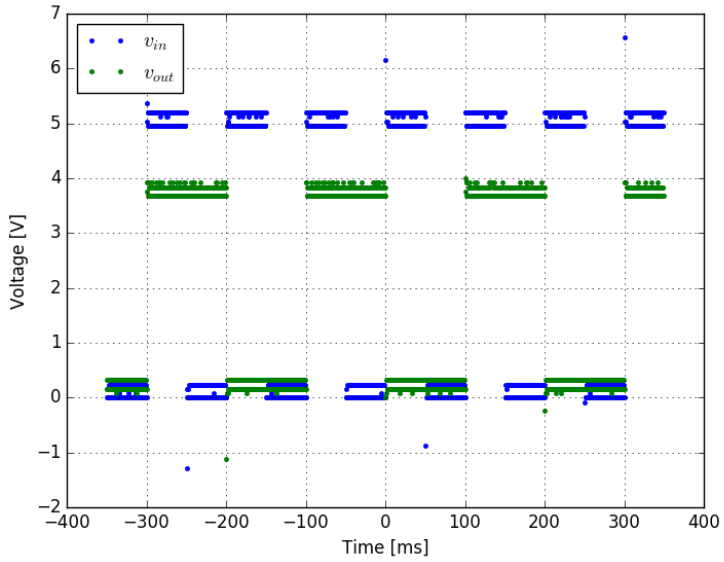


Figure 10.11: Output of frequency divider at half frequency

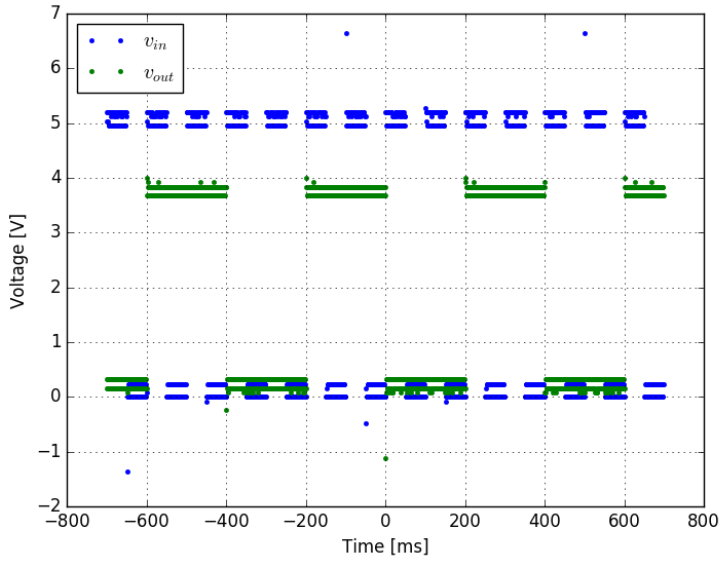


Figure 10.12: Output of frequency divider at quarter frequency

In the counter circuit we used a capacitor for presetting the starting bits. For this reason we measured the voltage at the capacitors ends at the stating time and, as we expected, in the plot 10.13 the voltage slowly goes to the HIGH level

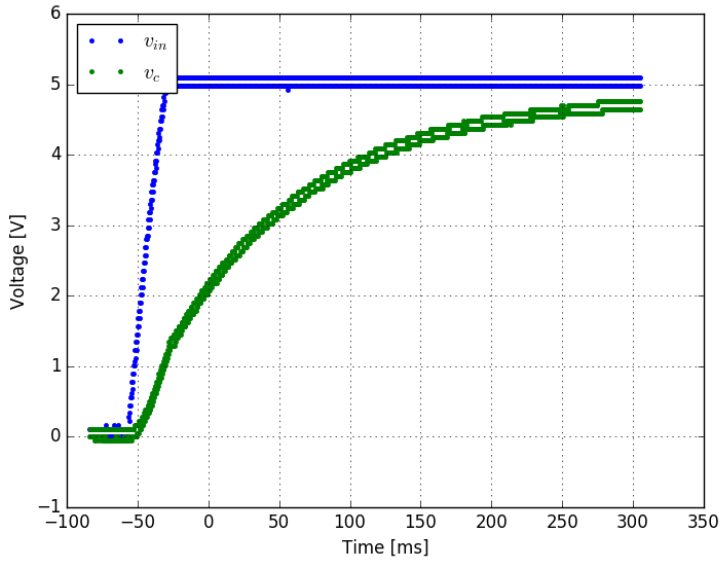


Figure 10.13: In the counting circuit: the voltage of the power supply and the voltage on the ends of the capacitor

Experiment 11

ADC tracking

In this experience we built an 8-bit ADC tracking with the output switching from 0 and 5 volt (TTL logic).

11.1 Materials

- Resistors, capacitors
- Power supply RIGOL DP831A
- 5V power supply NI myDAQ
- Waveform generator RIGOL DG1032
- Multimeter RIGOL DM3068
- Digital counter (from previous experiment)
- DAC08
- 8-bit LED viewer
- Comparator LM311

The resistors used were all with an uncertainty of 5%

11.2 Experimental setup

First of all we tested our DAC08 powering it with ±15V and setting the input current in the $+V_{Ref}$ pin to 2mA: this was acheved by using a 4.4V voltage from the RIGOL power supply and a resistor of 2.2kΩ. In order to clear as much as possible the bias current effects, we used another identical resistor between the $-V_{Ref}$ pin and ground and also added a 10nF capacitor between the COMP pin and -15V to optimize the behavior of the component.
Since we used TTL logic and only one output, we put to ground both the V_{LC} and the $\overline{I_{Out}}$ pins.
At this point we had an output current, but we desired an output voltage: for that reason we added a 2081.7±0.4Ω resistor between the I_{Out} pin and ground.
We than tested the component with various different inputs and measured its resolution.
Once done these measurements we connected the counter circuit from last experiment as the DAC08 input, verifying the output to be a sawtooth signal.
Finally we connected this output to a comparator together with the input voltage to be converted, obtained from the -15V power supply voltage with a 5.6kΩ resistor and a 5kΩ trimmer (therefore freely variable), and used this new output as the $\overline{Up}$/Down counter input, removing the D-FlipFlop being now useless its signal slowing function.
We chose different signals at different frequencies and visualized them with the 8-bit LED viewer. We

verified this way the correct working of the circuit.
0.1μF were added to all the connections with power supply.

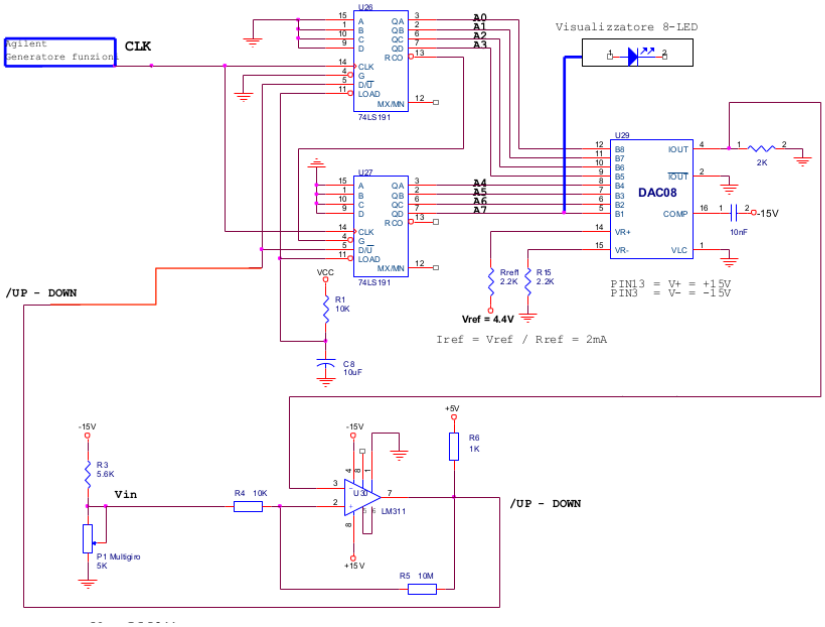


Figure 11.1: Circuit used

11.3 Data Analysis

Once mounted the DAC08, we tested its output with different configurations of the input. The results are shown in table 11.1

Range Fraction	B1	B2	B3	B4	B5	B6	B7	B8	I_{out} (measured)	V_{out} (measured)
FULL RANGE	1	1	1	1	1	1	1	1	1.9870±0.0011 mA	-4.1358±0.0003 V
HALF-SCALE +LSB	1	0	0	0	0	0	0	1	1.0057±0.0006 mA	-2.09378±0.00018 V
HALF-SCALE	1	0	0	0	0	0	0	0	0.9979±0.0006 mA	-2.07775±0.00018 V
HALF-SCALE -LSB	0	1	1	1	1	1	1	1	0.9892±0.0006 mA	-2.05968±0.00018 V
ZERO-SCALE +LSB	0	0	0	0	0	0	0	1	8.08±0.03 μA	-16.807±0.006 mV
ZERO-SCALE	0	0	0	0	0	0	0	0	0.33±0.03 μA	-0.744±0.005 mV

Table 11.1: Test DAC08: measures

Range Fraction	B1	B2	B3	B4	B5	B6	B7	B8	I_{out} (theoretical)	V_{out} (theoretical)
FULL RANGE	1	1	1	1	1	1	1	1	1.992±0.004 mA	-4.147±0.008 V
HALF-SCALE +LSB	1	0	0	0	0	0	0	1	1.008±0.002 mA	-2.098±0.004 V
HALF-SCALE	1	0	0	0	0	0	0	0	1.000±0.002 mA	-2.082±0.004 V
HALF-SCALE -LSB	0	1	1	1	1	1	1	1	0.992±0.002 mA	-2.065±0.004 V
ZERO-SCALE +LSB	0	0	0	0	0	0	0	1	7.8125±0.016 μA	-16.26±0.03 mV
ZERO-SCALE	0	0	0	0	0	0	0	0	0±0 μA	0±0 mV

Table 11.2: Test DAC08: expected values given $I_{Ref} = 2.000 \pm 0.004$mA, $R_{out} = 2081.7 \pm 0.4\Omega$

Comparing the results in these last 2 tables, we can see that the measurements are sufficiently compatible with the expected values (with the only exeption of the zero-scale that theoretically should be zero with no uncertainty at all).
We can as well measure the resolution of our converter: it is actually the least difference that we can distinguish between two different outputs. Making an average, we come to the result of 1LSB = 16.72±0.12 mV, that is distant from its theoretical value of 16.26±0.03 mV of only 3σ.
Then, connected the DAC08 to the counter and verified the signal tracking and "capture" feature of our system, we observed the response to a 0.3V continue input, using a 30Hz clock frequency and setting the oscilloscope time scale to 20ms/div: We got a ladder in the first part, beginning from 0V and approaching to the input voltage with subsequent steps at the clock frequency, each step modifiyng the output of a value equal to the resolution of the circuit. As the output overtook the signal in input, it began decreasing and increasing one step after another, keeping the medium value equal to the input one. We can see the graphic obtained in figure 11.2

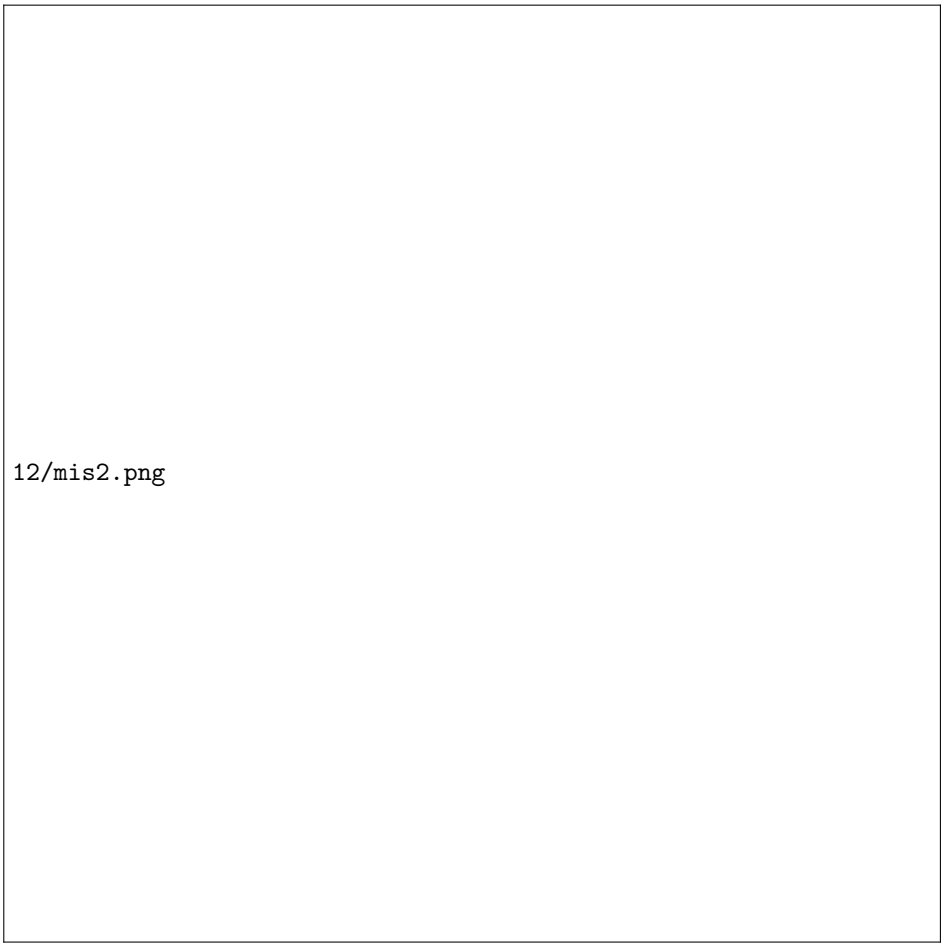


Figure 11.2: signal tracking and "capture" feature of our circuit with a constant input

If we had kept the flip-flop from the previous experiment, once the input signal was reached we would have had 2 steps more both in the increasing and the decreasing stage: this because the change in the direction in which to count would have arrived to the counter one clock pulse after it left the comparator, and not at the same time.

Experiment 12

Digital sampling

We studied how to reconstruct a signal starting from its sampling. We tried different sampling frequency and two different waves then using the Whittaker–Shannon formula we have reconstructed the orginal signal.

12.1 Materials

- Digital sampler (???)

12.2 Experimental setup

The waveform generator and the XXX were connected so we could have use the LabView software for aquiring the data. The sampling frequency and the number of samples were set with the software. As source signal we used a sine wave with frequency 10 Hz and an amplitude pk-pk of 5 V, we sampled this wave with a frequency of 5,10 and 25 Hz. Then we switched wave with a triangular one of 100 Hz and 4 V pk-pk amplitude, this last signal was sampled with a 500 Hz frequency.

12.3 Data analysis

The Whittaker–Shannon formula states that:

$$x(t) = \sum_n x_n \cdot \operatorname{sinc}\left(\frac{t - t_n}{T}\right)$$

where x_n are the data corresponding to the time t_n and T is the sampling period. Appling this formula to our data we obtain the following plot