Università degli studi di Trento

Group **MAR01**

REPORT OF THE EXPERIMENTS PERFORMED IN THE COURSE OF PHYSICS LABORATORY III

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Contents

Experiment 1

Basic circuits with an operational amplifier

In this experiment we have built five different circuits. The first is an open loop circuit with the operational amplifier uA741, the goal was to find the maximum voltage output by the op-amp. The last four circuits are in closed loop configuration with a negative feedback and they consist in a follower, a non inverting amplifier, an inverting amplifier and a weighted summing amplifier. We have measured the input voltage and the output voltage of every circut.

1.1 Materials

- Operational amplifier uA741
- Resistors, nominal value: 100 Ω, 220 Ω
- Power supply RIGOL DP831A
- Waveform generator RIGOL DG1032
- Multimeter RIGOL DM3068
- Oscilloscope AGILENT 54261A

1.2 Experiment setup

In the first four circuits the output of the waveform generator was a sine wave of 100Hz frequency and a peak-peak voltage of 100mV. We measured the waveform input signal v_{in} and the output voltage v_o of the op-amp. The measurements were performed using an oscilloscope triggered externally, the signal acquired is an 8 cycles average. The voltage supply of the op-amp was set to $v_{cc} = 15$V for all the circuits.

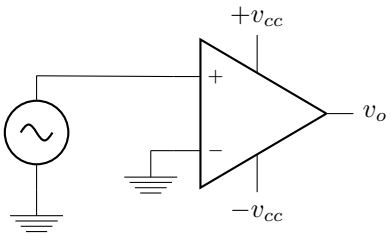


Figure 1.1: Open loop circuit

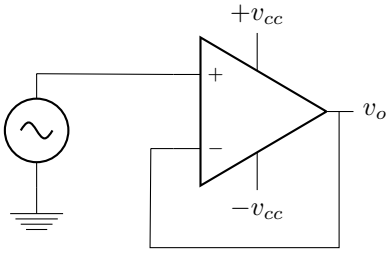


Figure 1.2: Follower

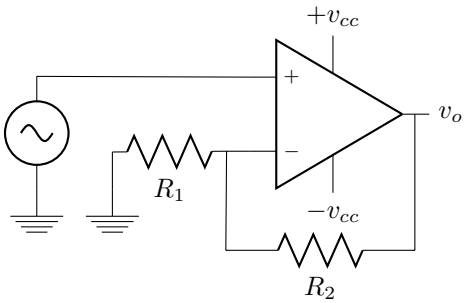


Figure 1.3: Non inverting amplifier

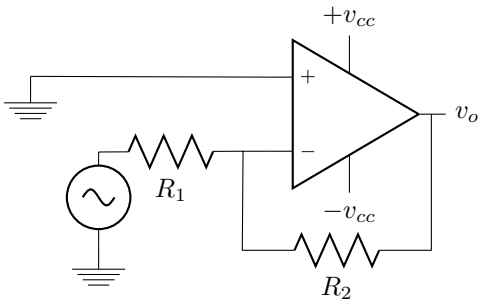


Figure 1.4: Inverting amplifier

For the last circuit we used again a sine wave signal with the same 100Hz frequency but a different peak-peak voltage. The oscilloscope's setting and the measurement taken was the same as before. The values of the resistor are: $R_1 = 99.89 \pm 0.02\,\Omega$, $R_2 = 218.37 \pm 0.04\,\Omega$, $R_3 = 99.89 \pm 0.02\,\Omega$ (the measurement were obtained with the multimeter).

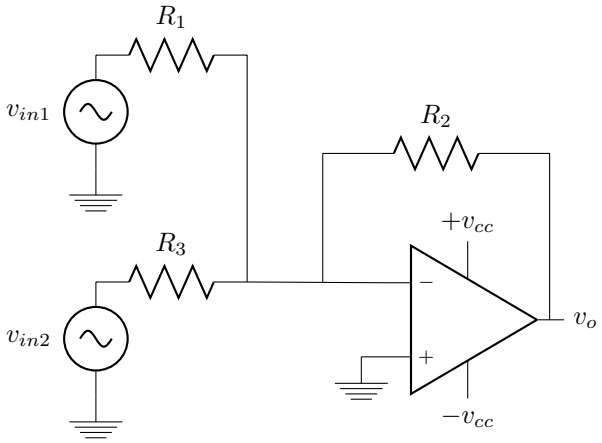


Figure 1.5: Weighted summing amplifier

1.3 Data analysis

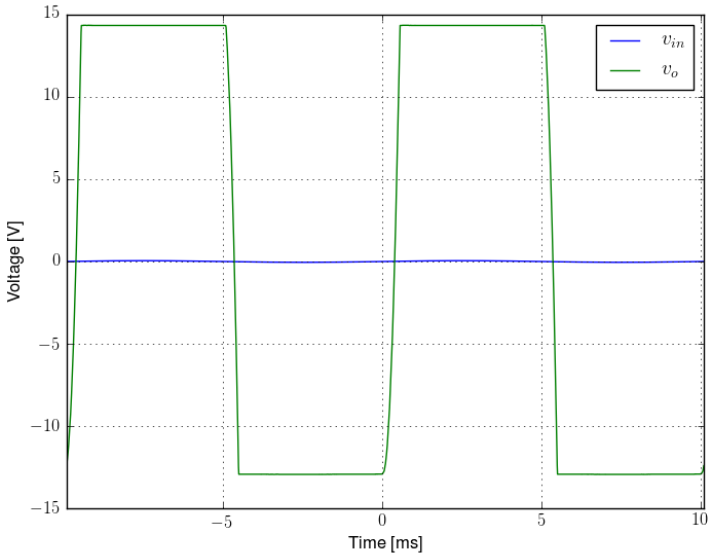


Figure 1.6: Open loop configuration

In the open loop configuration we get an output (visible in figure 1.6) that has a maximum absolute value of 14.35 ± 0.16[1] V and a minimum value of -12.94 ± 0.16[1] V. According to the ideal model we would expect the output to be infinite, as stated by the equation $v_o = A_{ol}(v_+ - v_-)$ where A_{ol} tends to infinity. In the physical case the output voltage is costrained by the saturation voltage that's determined by the voltage applied to the op-amp. The minimum and maximum output values are different in modulus, due to the lack of symmetry between the *npn* and *pnp* trasistors in the final push-pull stage of the op-amp.

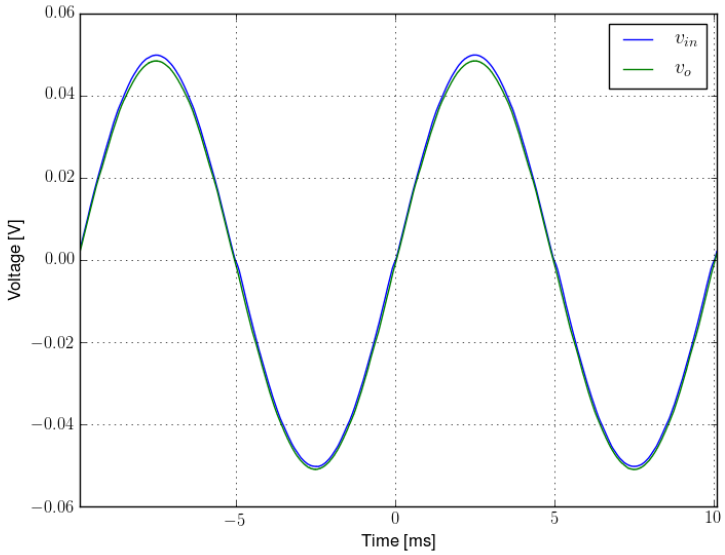


Figure 1.7: Emitter follower

[1]Error based on oscilloscope's 8 bit resolution

Regarding the emitter follower we expect, ideally, an output voltage equal to the input one. Actually we can see in the plot a small discrepancy between the two signals: that is probably determined by the op-amp's offset, as we can see a downward translation in the output, and also by some other non ideal features of the op-amp.

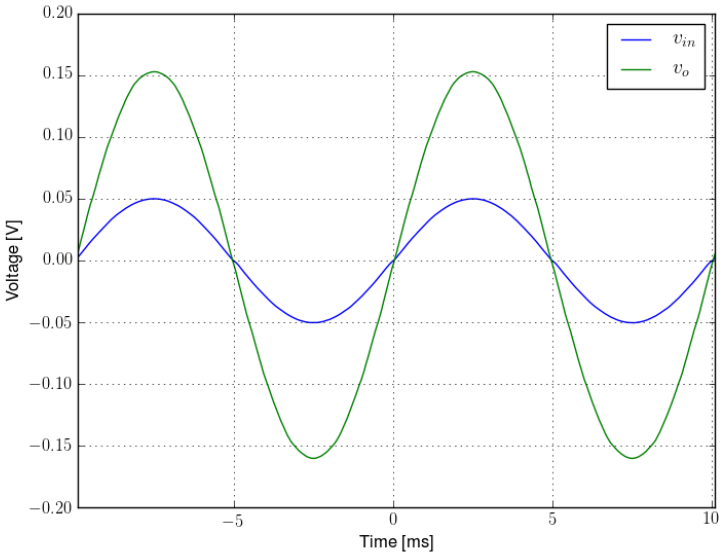


Figure 1.8: Non-inverting amplifier

In the non-inverting amplifier configuration we expect the output voltage to be: $v_o = v_{in}(1 + \frac{R_2}{R_1})$. The theoretical value for the peak-peak output voltage calculated using R_1, R_2 and v_{in} is 320.3 ± 1.9 mV. This prediction is not compatible with the output measured 313.4 ± 0.8 mV of a 3.3σ factor, probably because the op-amp is not ideal.

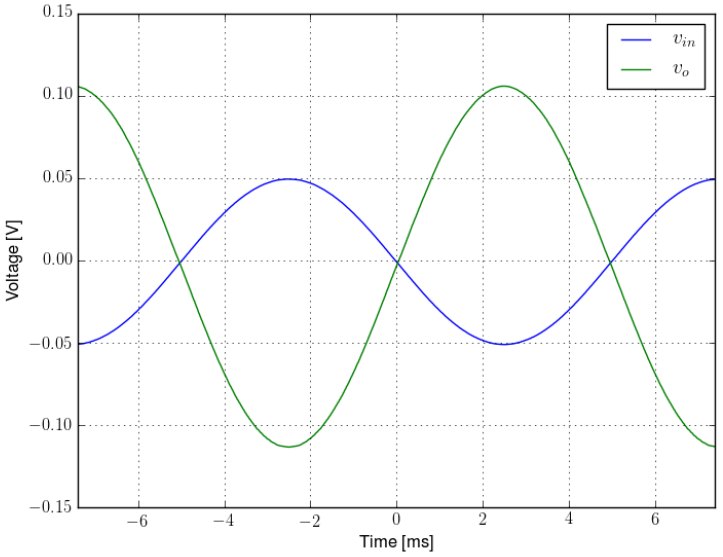


Figure 1.9: Inverting amplifier

In the inverting amplifier the output should be : $v_o = -v_{in}\frac{R_2}{R_1}$. The pk-pk value of the output is 219.4 ± 0.8 mV that is fully compatible with theoretical value 219.8 ± 1.9 mV.

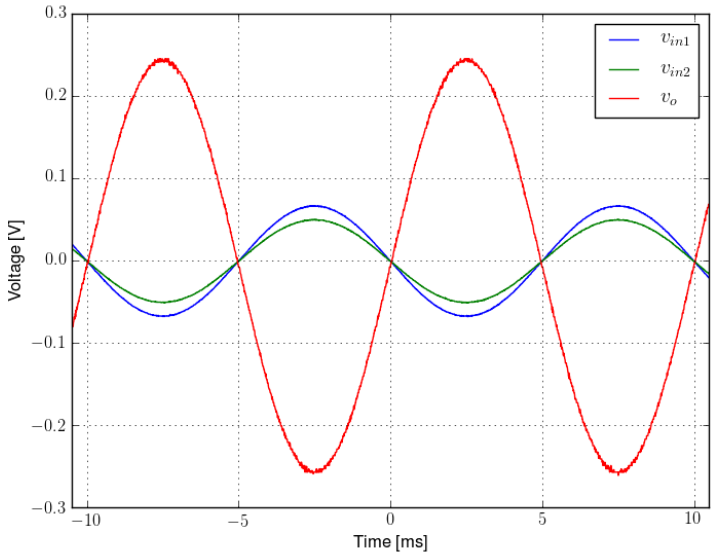


Figure 1.10: Weighted summing circuit

In circuit 1.10 we used two different inputs for aquiring an output voltage: this configuration sums these signals $v_1 = 135.1 \pm 0.8$ mV and $v_2 = 101.3 \pm 0.8$ mV using the resistors R_1 and R_3 as weights, giving as output $v_o = -R_2(\frac{v_1}{R_1} + \frac{v_2}{R_3})$, which gives a pk-pk value of 516.7 ± 2.7 mV. The theory in this case is not compatible with the measurament 506 ± 0.8 mV by a 3.8σ factor, a little more than the previous result, but that's most likely caused by the unavoidable noise in the output.

Experiment 2

Let's get more confident with our little friend op-amp

We designed an inverting amplifier with a gain variable by the use of a trimmer. The second circuit designed was a non-inverting summing amplifier with unitary gain. We then built a current source generator of 1 mA and tested it with various loads. Next we tested the efficacy of the emitter follower configuration in mismatching the source's impedence. At last we designed a differential amplifier with a predetermined gain.

2.1 Materials

- Operational amplifier uA741
- Resistors and trimmers
- Power supply RIGOL DP831A
- Waveform generator RIGOL DG1032
- Multimeter RIGOL DM3068
- Oscilloscope RIGOL MS02102A
- Two capacitors of nominal value of 100nF

2.2 Experiment setup

In each circuit we powered the op-amp with a ±15 V DC voltage and, in order to reduce possible noises, we added two 100nF capacitors connecting the op-amp's pins for the power supply with the ground. The input signal had a frequency of 100 Hz and a peak-peak voltage of 1V except for the differential amplifier. For every specific circuit we designed them as follow:

- Inverting amplifier: we placed a 10kΩ trimmer along the feedback branch in series to a resistor $R_f = 983.9 \pm 0.1\Omega$. In order to have a minimum gain of 5, we used $R_{in} = 199.84 \pm 0.03\Omega$ as in figure (2.1).
- Summing amplifier: caring for the simplest calculations, we used $R_1 = 1484.7 \pm 0.2\Omega \simeq R_2 = 1483.5 \pm 0.2\Omega$ so the equation comes to be $v_o = \frac{v_1 + v_2}{2}\left(1 + \frac{R_4}{R_3}\right)$. In order to obtain as output the inputs sum, we had to choose $R_3 = R_4 = 1001.3 \pm 0.1\Omega$. The inputs v_1 and v_2 are the same 100 Hz, 1 V peak-peak sine wave signal.

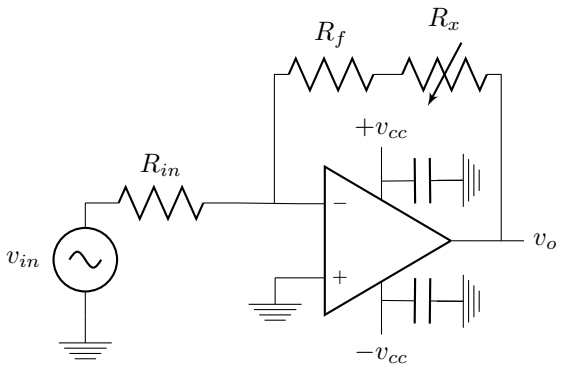


Figure 2.1: Inverting variable amplifier

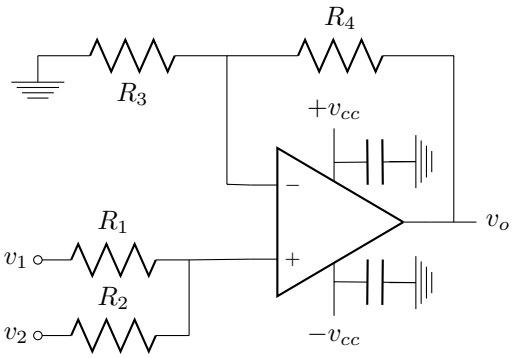


Figure 2.2: Non-inverting summing amplifier, unitary gain

- Emitter follower test: at first we built a circuit without the emitter follower using an input impedence of $R = 100.2 \pm 1\,\text{k}\Omega$ and a load of $R_L = 19.8 \pm 0.2\text{k}\Omega$. Then we added the op-amp stage and compared the output measurements in the 2 different cases.

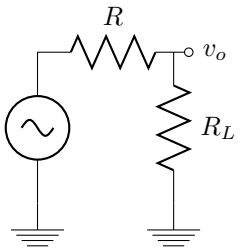


Figure 2.3: Test circuit without follower

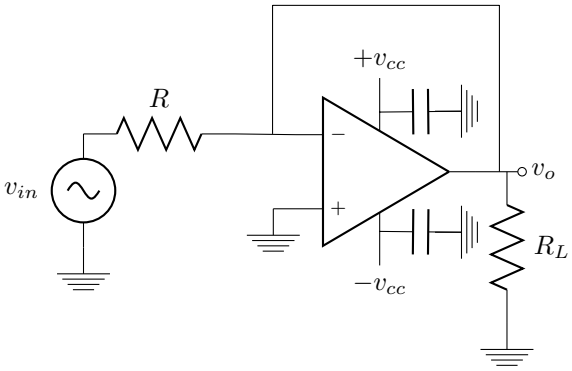


Figure 2.4: Test circuit with follower

- Current generator: the aim of this circuit is to generate a stable fixed current indipendent from the load. We generated a 1mA current using a DC voltage source of 5V and a 4.9693 $\pm$ 0.7kΩ resistor. The load was simulated with a trimmer.
- Differential amplifier: the full equation of the circuit in figure (2.6) is the following:

$$v_o = \frac{R_F}{R_1}\left[\frac{v_b}{1 + R_f/Ry}\left(1 + \frac{R_1}{R_F}\right) - v_a\right]$$

first we set to ground v_b, in this way we were able to set up the gain of the circuit (we chose it to be $A = \frac{R_F}{R_1} = 2$ with $R_F = 3 \pm 0.2\,\text{k}\Omega$ (5% error of nominalvalue)). After that we put the same signal of v_a in v_b with a resistor R_f and a variable resistor R_y made with R_2 in series with a trimmer. We tweaked the trimmer in order to get the output as close to zero as possibile (Figure (2.7)). This means having in the equation $R_f/R_y = R_1/R_F$ so that the new output would exaclty be what we want, i.e. $v_0 = A(v_b - v_a)$. For the amplifier test we used $v_a = 5$V DC and for v_b a sine wave 1V peak-peak 100Hz with an offset of 5V.

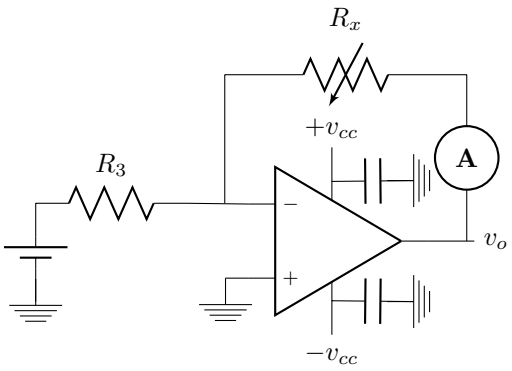


Figure 2.5: Current source generator

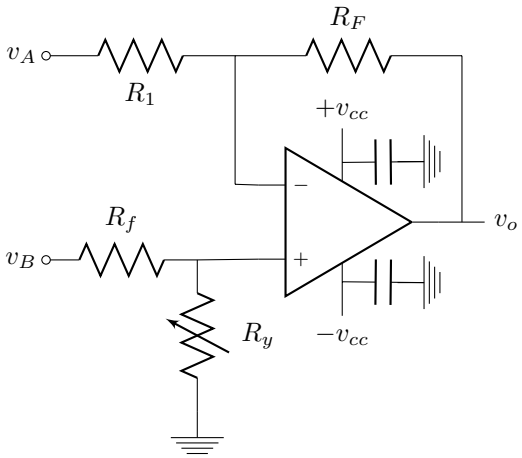


Figure 2.6: differential amplifier

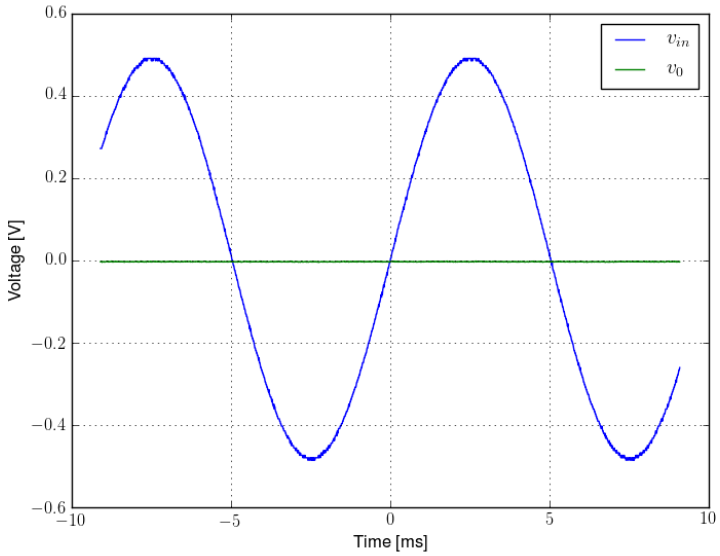


Figure 2.7: Calibration of the differential amplifier

2.3 Data analysis

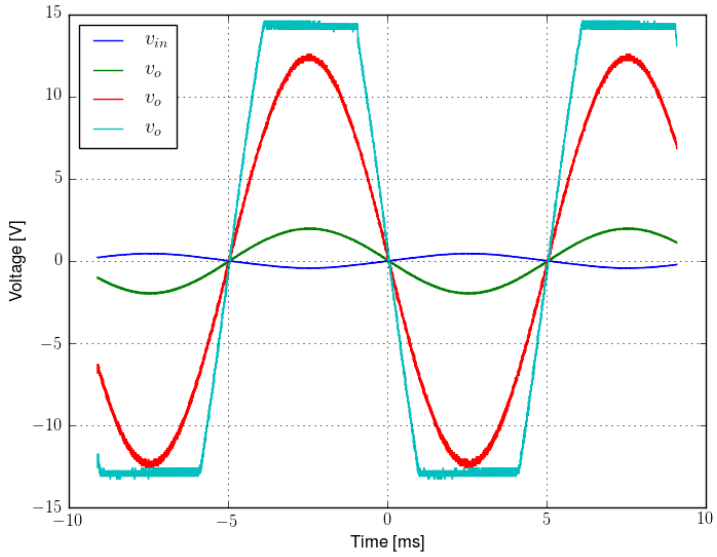


Figure 2.8: Variable amplifier

In the inverting amplifier we used a trimmer in order to vary the gain, in fact the equation is:

$$v_o = -v_{in}\frac{R_f + R_x}{R_{in}}$$

then increasing R_x cause the output to increase linearly. The output voltage is bounded by the op-amps's power supply voltage, it cannot increase further and the signal goes flat, as we can see in figure (2.8) (light blue line), this behavior is called "Clipping". The graphic also shows a discrepance between the absolut value of maximum and minimum voltage during the clipping: this is due to the asimmetry between *pnp* and *npn* transistors in the op-amp's final stage.

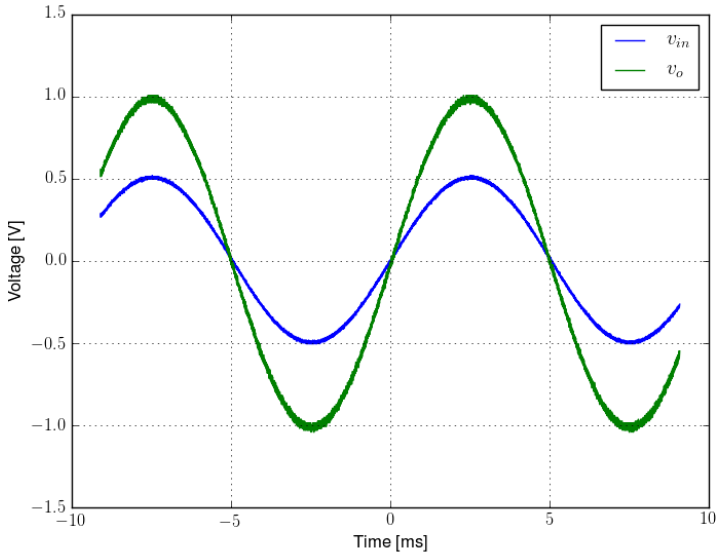


Figure 2.9: Weighted summing amplifier

In the non-inverting summing amplifier circuit we wanted the output to be the simple sum of the signals in entrance, that were identical: it means that the output signal must have double amplitude compared to the input one. The peak-peak voltage's theoretical expectation is 2.0496 ± 0.0009V while the measured one is 2.032 ± 0.001V. The incompatibility is most likely due to the op-amp's non-ideality.

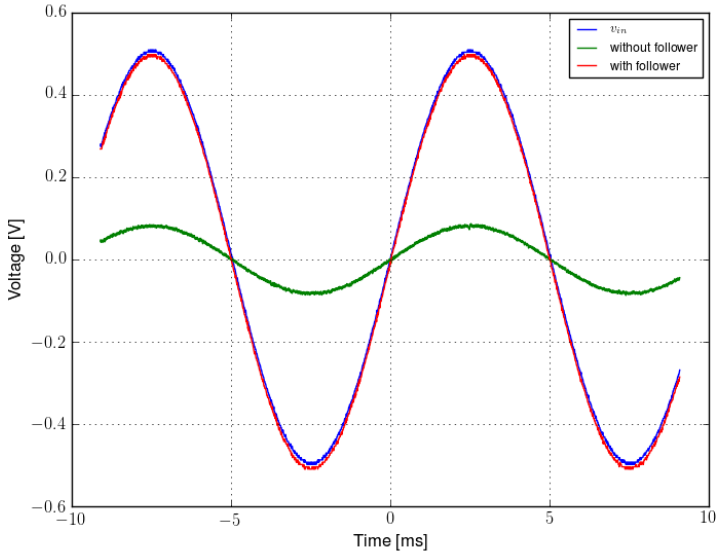


Figure 2.10: Emitter follower comparison

Let's now analyse the differences between a circuit with and without follower stage. We can see in figure (2.10) that using the follower we obtain a replicated signal while without it the signal is much more shrinked due to the input impedence. We can then say that the op-amp has separated the circuit in two different parts, overshadowing to the second any impedence present in the first: this is exactly what we mean by "impedence mismatching".
The difference between the blue and the red line is caused once again by the non-ideality of the op-amp, probably by a non zero offset.

In the current generator circuit we firstly measured the output current $I_m = 1.0045 \pm 0.0006$mA that was compatible with the expected one $I_e = \frac{v_{in}}{R_3} = 1.0062 \pm 0.0020$mA, then we observed the indipendency from the trimmer resistence of the current value: varying the resistance the current value was always the same (at least within its uncertainty).

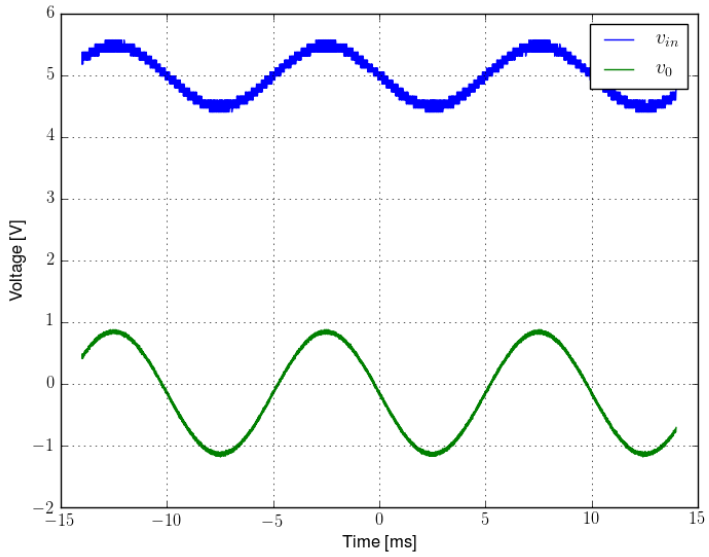


Figure 2.11: Differential amplifier

In the differential amplifier circuit we measured an output cleared from the 5V DC part present in both inputs: the output consisted only in the AC component of the input, but doubled (as we can see in figure (2.11)). This is exactly how we expected the circuit to behave.

Experiment 3

Unfortunately the op-amp is not so ideal

In this set of experiments we dealt with the problems of a real op-amp such as the offset v_{os}, the bias currents i_{b+}, i_{b-}, the slew-rate, the maximum current output and the common gain A_{cm}: we measured all of these parameters. The offset was studied with 3 different circuits and then compensated with a trimmer in the configuration suggested by the op-amp's datasheet. The bias currents were measured in two ways, one for the bias current in the non inverting op-amp input and one for the inverting one. The other parameters were studied simply adjusting the input for the measurement's purpose.

3.1 Materials

- Operational amplifier uA741
- Resistors, trimmers and capacitors
- Power supply RIGOL DP831A
- Waveform generator RIGOL DG1032
- Multimeter RIGOL DM3068
- Oscilloscope RIGOL MS02102A

List of resistors used		
Resistor name	Value [Ω]	Uncertainty [Ω]
$R_{M\Omega}$	982.0×10^3	0.1×10^3
$R_{100k\Omega}$	99.22×10^3	0.01×10^3
$R_{10k\Omega}$	9906.2	1.2
$R_{k\Omega}$	1001.4	0.1
$R_{10\Omega}$	9.963	0.01
$R^*_{10k\Omega}$	9926.4	1.2
$R^*_{10\Omega}$	10.00	0.01

3.2 Experiment setup

In all the circuits we placed on the power supply's pins two capacitors each, one with high capacitace (nominal value 470 ± 23 nF) and one with low capacitance (10.0 ± 0.5 nF). These were used for suppressing the high-frequency noise and contrasting the effect of any eventual change in the power supply voltage, that could move the offset voltage.

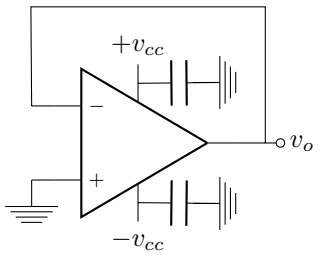


Figure 3.1: Offset voltage's direct measure

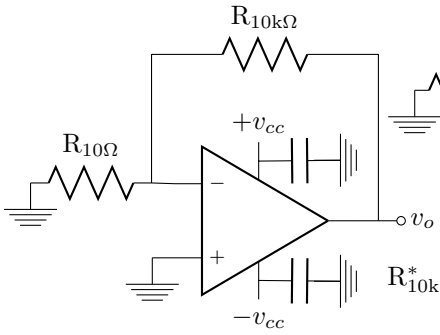


Figure 3.2: Offset voltage's direct measure with gain

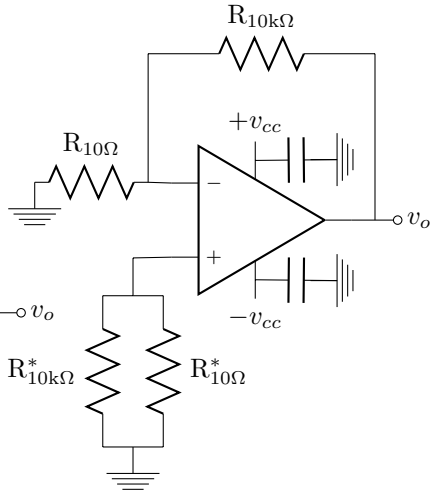


Figure 3.3: Offset voltage's direct measure with gain and bias current correction

In the first circuit we measured v_{os} directly by using the multimeter on the output voltage. We used the second circuit drawn to amplify v_{os}, we measured the amplified signal.
The third circuit is identical to the second except for the added resistors in parallel that connect the non inverting pin to the ground: this was done for removing the bias current influence from the measurament according to the hypothesis that these currents are approximately equal. For this reason these added resistors need to have toghether the same resistance of the parallel between the $R_{10\Omega}$ and $R_{10k\Omega}$ used before. Exploiting this last circuit we removed v_{os} by using a trimmer between op-amp pins 1 and 5, paying attention to connect the central trimmer pin to the negative power supply voltage (according to the uA741 datasheet): we tried to make the output as close to 0 as possible (we used no input voltage in these steps).

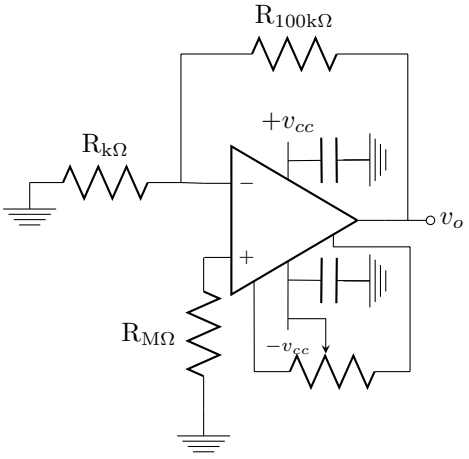


Figure 3.4: Positive bias current measure

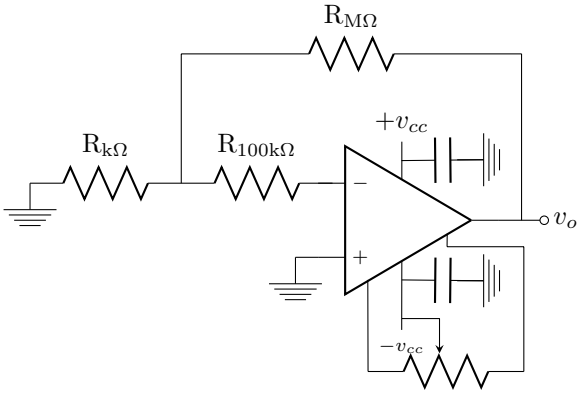


Figure 3.5: Negative bias current measure

The fourth circuit and the fifth are used for measuring the bias currents indirectly basing on how the two currents are related to the output: we use a great resistance ($R_{M\Omega}$) in order to make relevant to a voltage measurement only one bias current with respect to the other.
The sixth circuit was used for measuring the maximum current that the op-amp can erogate. In this configuration the oscilloscope's internal resitor was set to 50Ω.

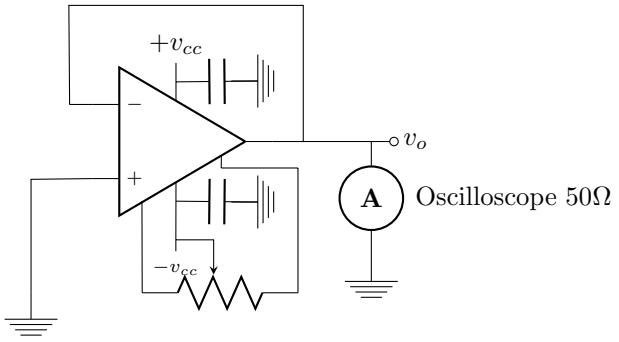


Figure 3.6: Max current measure

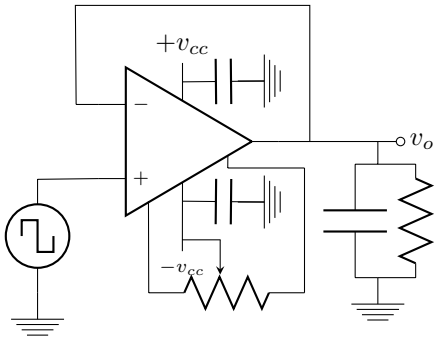


Figure 3.7: Slew rate

With the seventh circuit we measured the slew rate: the load capacitor used was 1 ± 0.05 nF, the resistor 2 ± 0.1 kΩ and the input used a 0-10 V square wave, that allowed us to aquire the image of the raising output.
Finally, the last circuit allowed us to measure the common gain by using the differential amplifier with the same 2V peak-peak sine signal at 100 Hz as the two inputs.

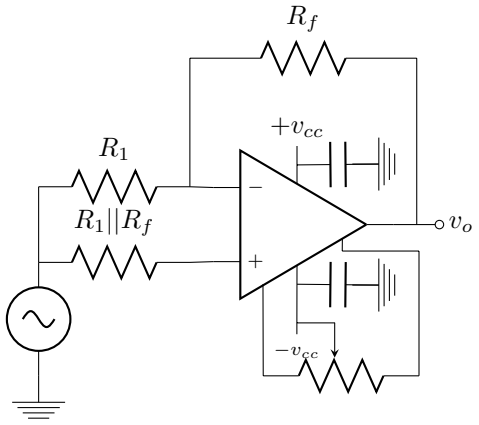


Figure 3.8: Common Gain

3.3 Data analysis

In the emitter follower (3.1) the output measured is -1.484 ± 0.005 mV. Being such a small output we expect to have problems with parassite impedance and other forms of noise, that's why we don't consider this value too reliable. It however gives us an order of magnitude that matches the op-amp datasheet, according to which the absolute typical values are from 1 mV to 5 mV.
In the amplifier (3.2) we can find v_{os} resolving

$$v_{os} = \frac{v_o}{1 + \frac{R_{10\text{k}\Omega}}{R_{10\Omega}}}$$

From the calculation we get $v_{os} = -1.333 \pm 0.001$ mV, which has the same order of magnitude and sign of the previous result.
Then, as stated in the experimental setup, we corrected the circuit (3.3) for compensating the bias currents effect. With the same formula used for the previous amplifier we got an offset voltage of 1.307 ± 0.001 mV.
At this point we compensated the offset through the use of a trimmer (see experimental setup).
Regarding the fourth circuit (3.4), we calculated the current flowing in the non invertent pin by using

$$i_{b+} = -\frac{v_o}{R_{\text{M}\Omega}(1 + \frac{R_{100\text{k}\Omega}}{R_{1\text{k}\Omega}})}$$

The value calculated is -39.042 ± 0.009 nA.
The fifth circuit (3.5) instead leads to the calculation of the current flowing in the invertent pin by using

$$i_{b-} = \frac{v_o}{R_{100\text{k}\Omega}} \frac{R_{\text{k}\Omega}}{R_{\text{M}\Omega}}$$

we obtain the value -39.724 ± 0.009 nA. Now we can compute the bias current $i_b = \frac{|i_{b-}|+|i_{b+}|}{2} = 39.383 \pm 0.006$ nA and the offset current $i_o = ||i_{b-}| - |i_{b+}|| = 0.68 \pm 0.01$ nA.
i_b is less than 100 nA and near the typical value of 10 nA, as the datasheet states, but the offset current is a bit low being around a third of the typical value 2 nA.

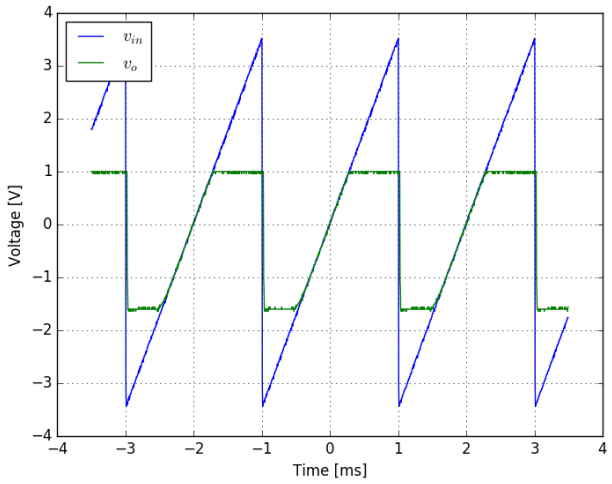


Figure 3.9: Saturated output caused by the maximum current erogated

In the sixth circuit (3.6) we calculated the maximum current erogated by computing the maximum/minimum output voltage over the resistance in the oscilloscope. In the plot it is visible the different absolute value of the maximum and minimum output voltage, that's probably because the op-amp isn't perfectly symmetric in the packaging. So we chose to calculate two different maximum currents: $i_{max} = 0.0201 \pm 0.0001$ A (when the output was positive) and $i_{min} = -0.0328 \pm 0.0001$ (when the output was negative).

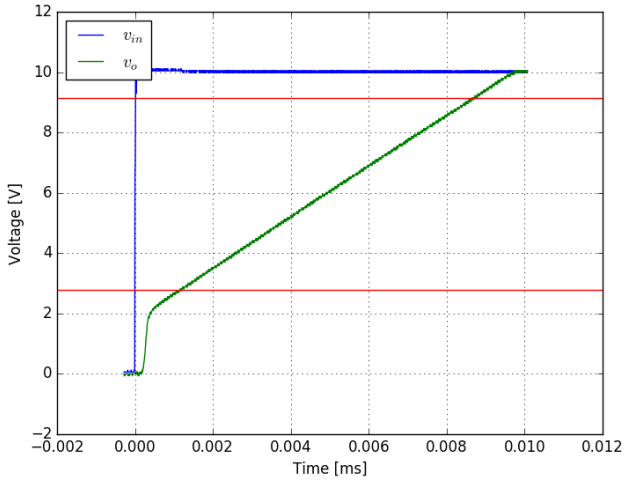


Figure 3.10: Output adjustment after an input change. Red lines are 10% and 90% of the output

In the seventh circuit (3.7) we find that the slew rate ($\frac{\Delta V}{\Delta t}$) of the op-amp used is $0.8332 \pm 0.0026 \frac{\mathrm{V}}{\mu s}$, which is bigger than the typical value $0.5 \frac{\mathrm{V}}{\mu s}$. One possible explanation of this would be that the slew rate depends on the amplitude of the signal: in our experiment the voltage was 50 times larger than the test shown in the datasheet, otherwise we have to conclude that our op-amp, has some difects that cause a larger slew rate.

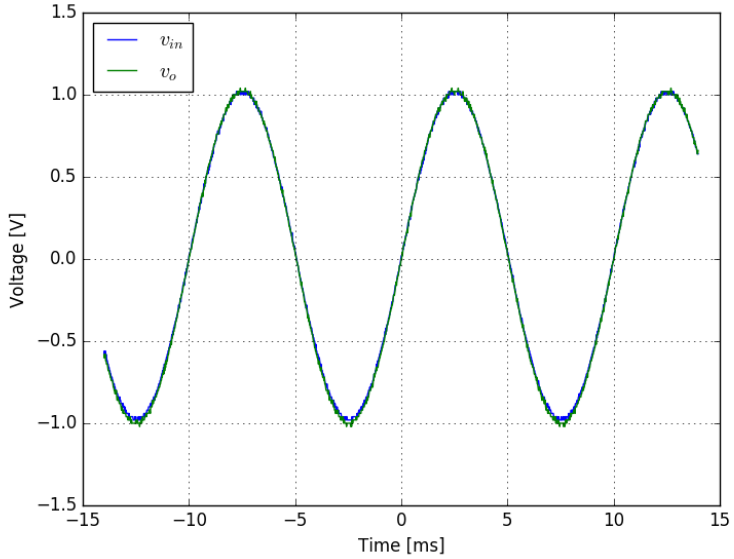


Figure 3.11: Common gain measurement

With the last circuit (3.8) we measured the common gain of our op-amp by solving

$$A_{CM} = \frac{2v_o}{v_{in1} + v_{in2}} = \frac{v_o}{v_{in}}$$

which gave us a unitary gain, 1.01 ± 0.04, as it is evident in the plot. In an ideal situation this parameter should have been zero, in fact the value is pretty low: being the differential gain order of 10^5 at low frequencies, we have a CMRR of 100 db that is quite high, this allows us to neglect the common gain most of the times.

Experiment 4

Gain in function of the frequency

In a real op-amp the open loop gain (A_{ol}) is a function of the input frequency. In this experience we explored systematically this behaviour using 2 different circuits, one for the lower frequencies and the other for the higher ones. After this study we built a non inverting amplifier with ≈ 10 and ≈ 100 gain for measuring its bandwidth.

4.1 Materials

- Operational amplifier uA741
- Resistors, trimmers, capacitors
- Power supply RIGOL DP831A
- Waveform generator RIGOL DG1032
- Multimeter RIGOL DM3068
- Oscilloscope RIGOL MS02102A

The resistor chosen were $R_1, R_2, R_3 = 10\text{k}\Omega$, $R_4 = 10\Omega$, $R_5 = 100\Omega, R_6 = 1\text{k}\Omega$ with an error of 5% of the value.

4.2 Experimental setup

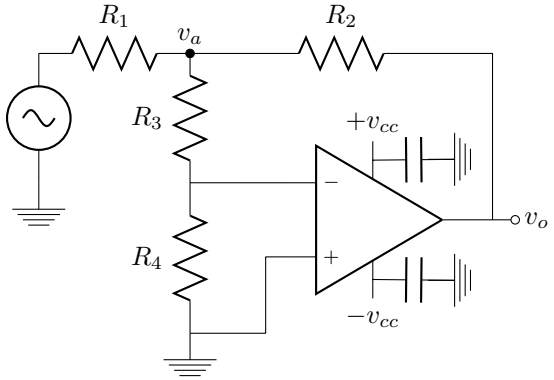


Figure 4.1: A_{ol} measure low frequencies

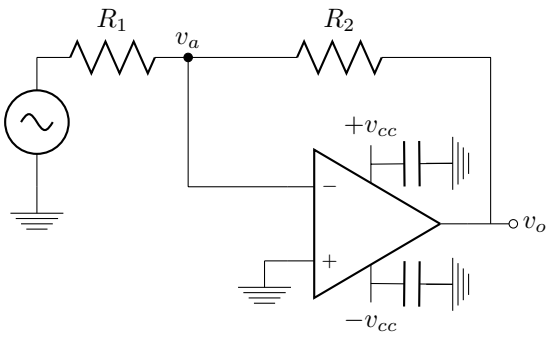


Figure 4.2: A_{ol} measure high frequencies

In this experience we took the measurament in all circuits by changing the frequency of the input, that was a sine wave signal 1 V peak-peak. The voltage chosen is not important, because we are

interested in the ratio between the amplitude of the output and the input signals.
The first circuit was used for calculating the gain in the open loop configuration (A_{ol}) at low frequencies by measuring v_a and v_o. This circuit was chosen for low freqencies instead of the second one, because the gain is too high for us to acquire directly the voltage difference between the two input pins. We didn't measure at frequencies lower than 30 Hz because the noise didn't allow us to make a reliable estimate of the two signals amplitude.
In the second circuit we measured v_o and the voltage of the non inverting pin v_a. The frequencies measured went from 10 kHz to 200 kHz, because with high frequencies the absulute value of A_{ol} is low enough.
In the last two circuits we built a non inverting amplifier (with a compensated offset) with a closed loop gain of 100 and 10, in order to verify the passing bandwidth.

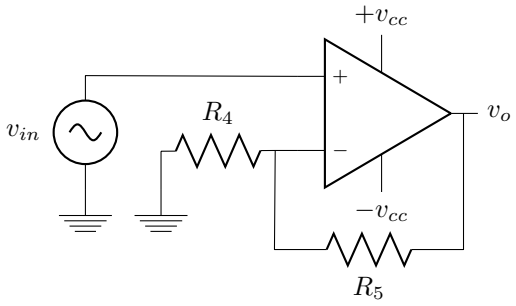


Figure 4.3: Non inverting amplifier

4.3 Data Analysis

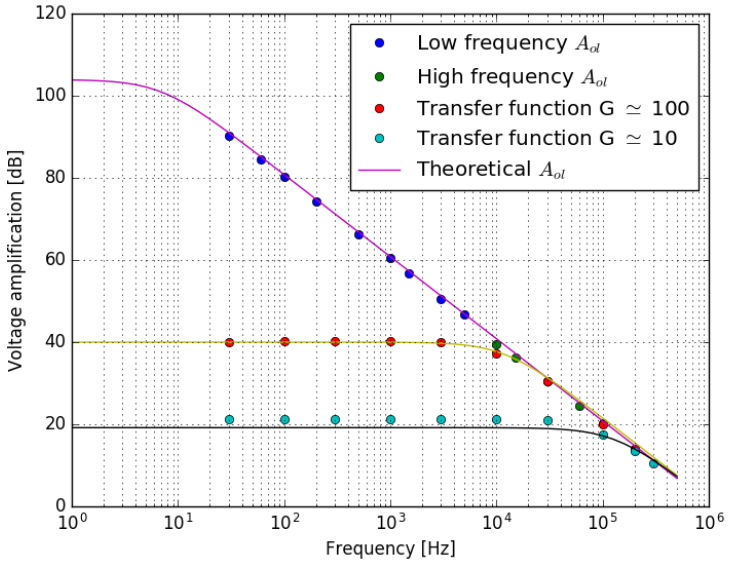


Figure 4.4: Gain as a function of the frequency

Using the first circuit we can estimate from the formula $A_{ol} = -\frac{v_o}{v_a}\frac{R_3+R_4}{R_4}$. The same can be done with the second circuit, but this time the formula comes to be $A_{ol} = -\frac{v_o}{v_a}$.
We can see from the plot that the data appears to be on a straight line and it is also visible that this line is compatible with the values in the datasheet (the continuous line). We can however compute

the theoretical open loop gain with:

$$A_{ol}^{teo}(f) = \frac{A}{1 + j\frac{f}{f_0}}$$

where $f_0 = 8$ Hz is a parameter available in the datasheet and $A = 1.5 \times 10^5$ was obtained with the best fit, j is the immaginary unit and f is the frequency. We can see from the plot that our data is consistent with the theory and the datasheet.
Regarding the last two circuit we plotted $H = \frac{v_o}{v_{in}}$ (the dots in the graph, experimental values), while the theoretical curve has been obtained thanks to the following formula:

$$H(f) = \frac{\frac{A}{1+A\beta}}{1 + j\frac{f}{(1+A\beta)f_0}}$$

where $\beta = \frac{R4}{R5+R4}$.
With a closed loop gain G of 100 we have a cutoff frequency of nearly 10^4 Hz, while with $G = 10$ it becomes 10 times higher, as anticipated. This means that as long as we keep low the gain of our circuit, we can use a wider range of frequencies.

Experiment 5

Introducing the comparator

We first built a relaxation oscillator with different periods, then we tested the LM311 comparator and used it for designing a switch that goes on and off depending on the environment light.

5.1 Materials

- Comparator LM311
- Operational amplifier μA741
- Phototransistor OP550A
- Resistors, trimmers, LED, capacitors
- Power supply RIGOL DP831A
- Waveform generator RIGOL DG1032
- Multimeter RIGOL DM3068
- Oscilloscope RIGOL MS02102A

All resistances and capacitances have an error of 5% of the value.

5.2 Experimental setup

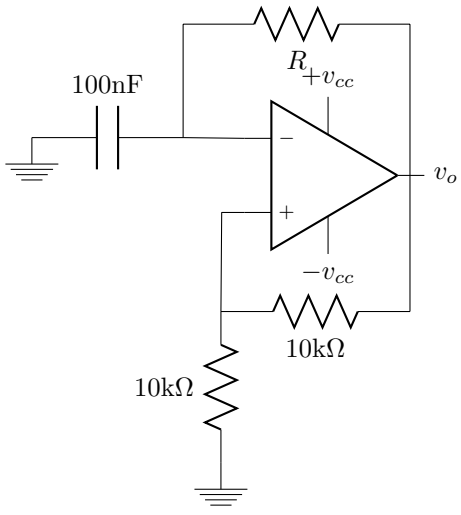


Figure 5.1: Relaxation oscillator

At first we used the μA741 (powered with $\pm$15 V) as a comparator in order to build a relaxation oscillator producing a square wave from a capacitor charge and discharge: we chose $R_1 = R_2 = 10.0 \pm 0.5k\Omega$ and a $100 \pm 5pF$ capacitor. The circuit has been tested with 5 different values of R in order to have different periods. A measure has been taken also setting the oscilloscope in single mode and then switching on the power supply.
We then tested the LM311 both as non-inverting and inverting comparator using $R_L = 1000 \pm 50\Omega$. Regarding the Schmitt's trigger, we added to the previous circuit the resisteors $R_1 = 10.0 \pm 0.5k\Omega$ and $R_2 = 100 \pm 5\Omega$ and analyzed the behaviour at the point when $v_{in} \approx v_{ref}$.

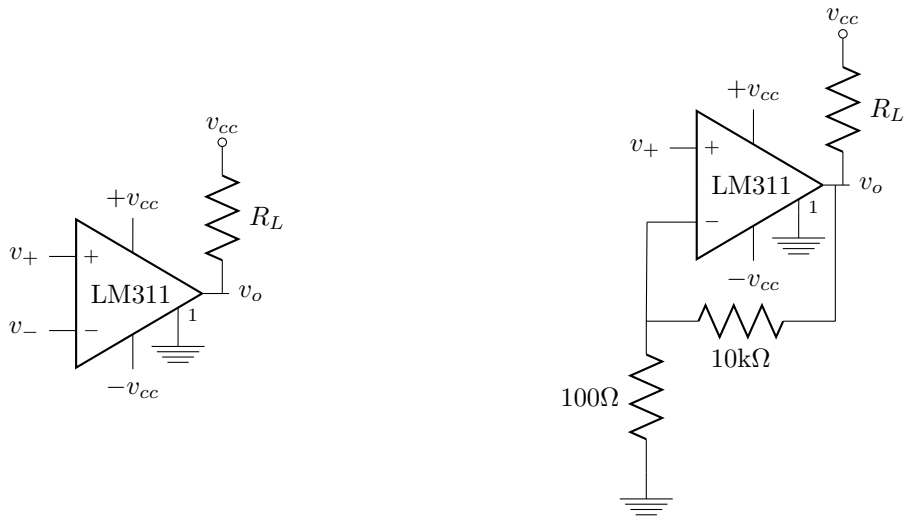


Figure 5.2: Comparator test with and without Schmitt's trigger

At last, we built the twilight switch with circuit 5.3. We used a phototransistor (which gives us a current which intensity is based on the light one) followed by an op-amp stage (for converting the current in voltage): due to the fact that che current from the phototransistor is very small we had to adjust carefully the op-amp offset in order to avoid sistematic errors. In the last stage we used the LM311 comparator to switch a led on and off comparing a reference voltage v_{ref} with the op-amp stage output.

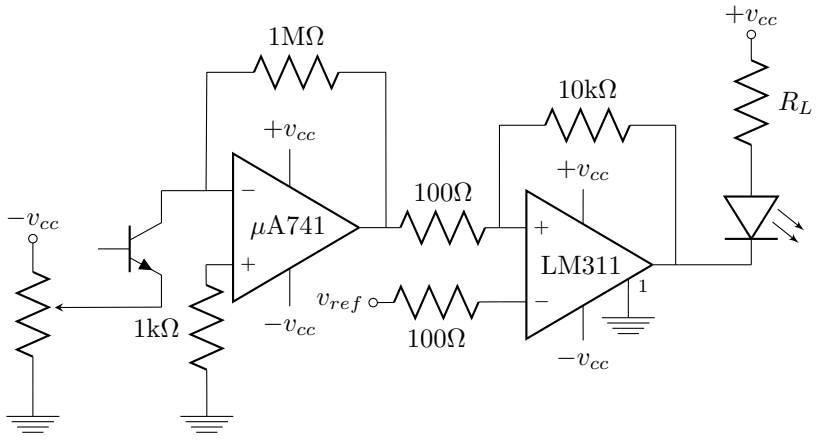


Figure 5.3: Twilight switch

5.3 Data Analysis

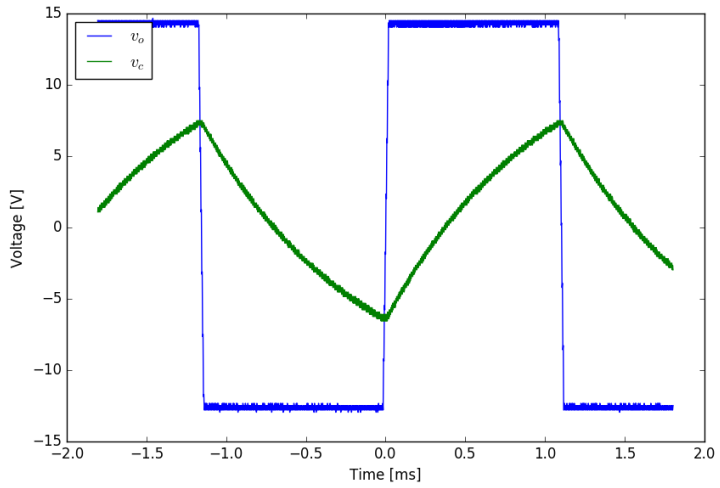


Figure 5.4: op-amp output v_o and capacitor voltage v_c with $R = 10\text{k}\Omega$

The oscillator period is related to the resistor R as follows:

$$T = 2RC \ln\left(1 + \frac{2R_1}{R_2}\right)$$

where C is the capacitor and $R_1 = R_2 = 10\text{k}\Omega$. Using the values measured with the multimeter we plotted a theoretical curve in function of R and we can see that the data are on that line: in fact the slope measured thanks to a linear fit $218.12 \pm 0.06F$ is in perfect accordance with the expected value $220 \pm 3F$ (but we have to admit that only five points don't represent a great pool on which to do a linear regression and statistics, but they do still give an idea). The uncertainties needed for the regression have been provided by the oscilloscope and multimeter resolution.

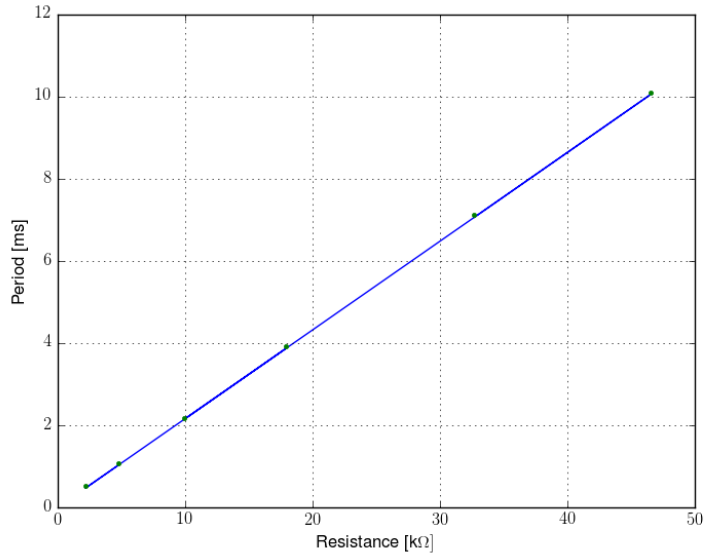


Figure 5.5: Data (green dots) and theoretical curve (blue line)

We then checked our comparator behaviour: it gave an high output when the voltage at the non invertent pin was higher than the other input and a low one when it became lower. The opposit effect happened with the inverting configuration. In the following figures we can see the difference in the comparator output with and without the Schmitt's trigger: when the Schmitt's trigger wasn't present, the noise caused an unwanted on-off repeated toggle. The Schmitt's trigger raises and lowers the threshold everytime it changes the output in order to avoid this problem.

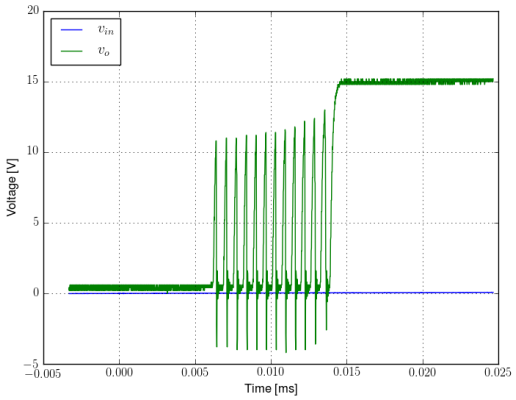


Figure 5.6: Without Schmitt's trigger

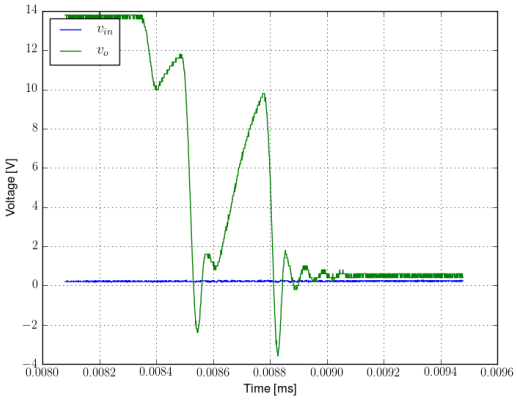


Figure 5.7: With Schmitt's trigger

In the circuit based on the phototransistor we notices that when the light was weaker than a fixed amount it switched on the LED and kept it lighted until the light was increased.
We were also able to choose the threshold for the switching by adjusting the voltage reference v_{ref} using a trimmer.
Below a photo of this circuit.

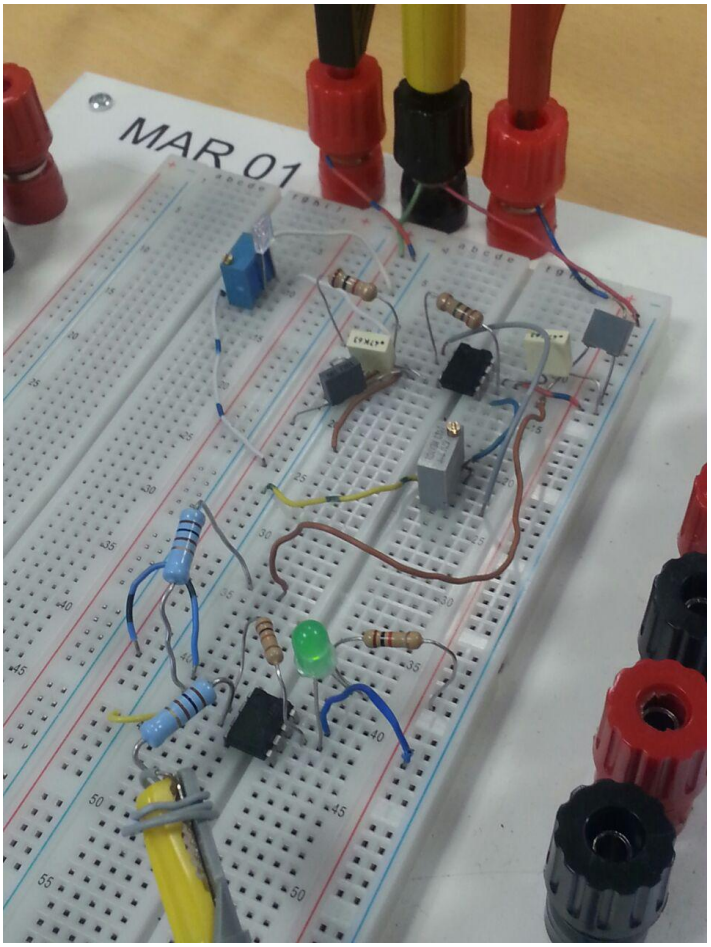


Figure 5.8: Twilight switch circuit

Experiment 6

Building an electronic thermometer and a thermostat

We realized an electronic thermometer. This was achieved by using the PT100, a platinum resistor with a well known thermal coefficient α. We made a fixed current pass through the PT100 so we had the signal represented by a voltage, then we amplified this signal and imposed through a differential amplifier the final output to be 0 V when the temperature was 0 °C. The aim was to have a voltage that could've easily been converted to a temperature by multipling it to a coefficient $\eta = 10\frac{^\circ C}{\mathrm{V}}$.
In the last part we added to this circuit a power step, making it able to heat its surroindings and thus keeping the nearby temperature at a constant value.

6.1 Materials

- Operational amplifiers OP07
- Instrumentation amplifier (INA) AD622
- Precision +5V Voltage Reference REF02
- Thermoresistor PT100
- Resistors, trimmers
- Power supply RIGOL DP831A
- Waveform generator RIGOL DG1032
- Multimeter RIGOL DM3068
- Transistor 2N2222

All the resistors used had an uncertainty of 5% of their nominal value.

6.2 Electronic thermometer

Firstly we measured the PT100 resistance using two different methods: one was the standard two wires measure, obtained by adding on each PT100 end two 10 Ω resistors in order to simulate the presence of parassite wire resistance. We measured $R_t \simeq 132\Omega$ which converted with $T = \frac{R_t - R_0}{R_0 \alpha}$[1] gave us $\simeq 80^\circ C$. We then used the 4 wires configuration and meausured $R_t \simeq 110\Omega$, that means a temperaure of around $26^\circ C$.

[1] R_0 is the PT100's resistance at 0 $^\circ C$ and α is the thermal coefficient, that is around $0.003850^\circ C^{-1}$

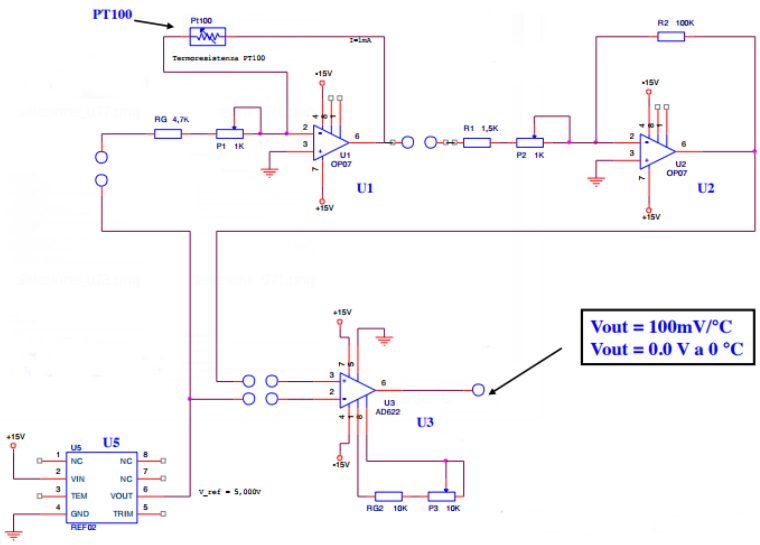


Figure 6.1: full thermometer circuit

In order to build the thermometer circuit we firstly turned the resistor mesurament in a voltage mesurament: this was achieved simply making a fixed current flow into the PT100 and recording the voltage between its ends. We then needed a highly stable current generator, which means a stable input voltage: for this reason we used the REF02 that when powered up gave an output of 4.9993 ± 0.0003 V. Measuring the current flowing through the PT100, we set it as close as possible to 1mA (the best value that limit self-heating) by tuning the trimmer connected to the inverting pin.
Since we wanted a slope of $100\frac{mV}{°C}$ and given that the PT100 had a dependence from temperature of $0.3850\frac{\Omega}{°C}$ with 1 mA of current flowing into it, we need to have a total gain of $G_{tot} = \frac{100\,\frac{mV}{°C}}{0.385\,\frac{mV}{°C}} = 259.74$.
We also needed to set the output to 0 mV at 0 °C, so we decided to first amplify the voltage on the PT100 ends by 50 times and then use this output in a differential amplifier with a gain of 5.195, where the other input should have been the voltage corresponding to $0°C$, i.e. 5V: this allowed us to take the first amplified signal and compare it with the reliable one from REF02.
In the first amplifier stage we used an OP07 in inverting configuration: its gain was set using an input voltage of 100 mV and adjusting a trimmer in order to have as output exactly 5 V.
In the last stage we used the AD622. Since this was the first time we worked with it we did some excercise before the connection to the circuit: we built a bridge to which we connected the AD622. We used two resistors of 100kΩ (R_1 and R_2), one of $1k\Omega$ (R_4) and one of 100Ω in series to a trimmer (R_3), we used also a resistance of 51.1 Ω (1% of uncertainty) to set the gain of the AD622 to 1000. By changing the resistance of the trimmer we were able to nullify the output voltage.

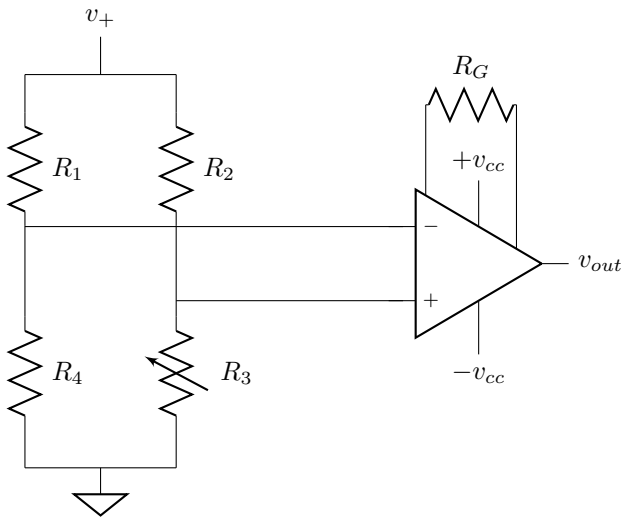
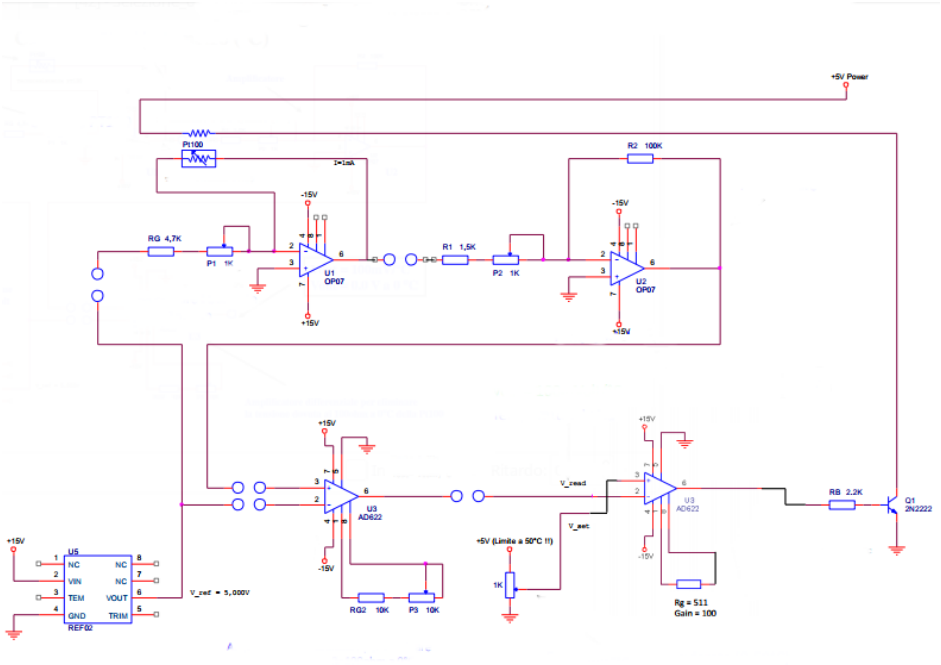


Figure 6.2: Testing bridge

After this test we felt confident to build a differational amplifier with a gain of 5.195 using the AD622: once put to ground the inverting pin and set a sine wave signal of 100mV to the non-inverting one, we changed the output tweaking the trimmer connected to the R_G pin.
After the gain was brought to 5.195 we connected all the circuits together: The signal from the current generator was used as input signal in the amplifier and the output of the amplifier was placed on the non-inverting pin of the differential amplifier, while on the inverting pin was placed the voltage generated from the REF02.
We connected the output to the multimeter and changed the setting in order to make it show 1 °C to each 100mV on the screen. The value measured was around 25 °C and we tested that heating the PT100 caused it to increase.

6.3 The P of PID



We connected the thermometer output to a differential amplifier with $G = 100$ in order to compare it with a reference chosen by us obtained connecting the non inverting pin to a fixed voltage through a trimmer. The INA output was connected as the base input of a NPN transistor using a resistor in between. The transitor controlled a power circuit made with a small resistence $R = 27\Omega$ (0.5 Watt resistor) with a voltage of 5V taken from the agilent generator. The PT100 was placed next to the small resistor, measuring its temperature.
If the temperature set by the trimmer was different from the one measured, that difference was amplified and converted to a current flowing in the power circuit, which would heat up the resistor until the difference in temperature was nullified. The current flowing in R is proportional to the temperature difference. The differential amplifier had a saturation voltage of around 10, so that the amplification of 100 allowed us to control the temperature on a range of 1 °C (100 mV).
For the current's measure we used a tester ICE placed between R and the transistor. During the test, when we changed the desired temperature, we saw the current raise and then making damped oscillations towards a stable current.

Experiment 7

ECG: Electrocardiogram

In this experience we built an electrocardiograph and tested it on a group member.

7.1 Materials

- Operational amplifiers OP07
- Instrumentation amplifier (INA) AD622
- Resistors, trimmers
- Power supply RIGOL DP831A
- Waveform generator RIGOL DG1032
- Multimeter RIGOL DM3068
- Isolation amplifier ISO124
- Three electrodes
- 9 V Batteries

All resistors and capacitors used had an uncertainty of 5% of their value.

7.2 Experimental setup

All the circuit connected with the patient was powered using a 9 V battery: thinking of a real situation in fact, we prevent this way the patient to be exposed to the electrical grid voltage of 220 V in case of any instrumentation malfunctioning.
The signal we wanted to acquire from the electrodes had a frequency of nearly 1.25 Hz and an amplitude from 1 to 4 mV, with an offset of 0.7/0.8 V due to the internal electrodes potential. Obviously any cable or body movement would interfere with the measurement, generating some kind of current, and it is also important to keep in mind the presence of parasite capacitance and inductance. For these reasons our circuit needs to remove the common potential and reduce as much noise as possible, without removing signals at 1.25 Hz frequencies.
During the measure the patient also had to be isolated from earth, otherways the signal would dissipate.

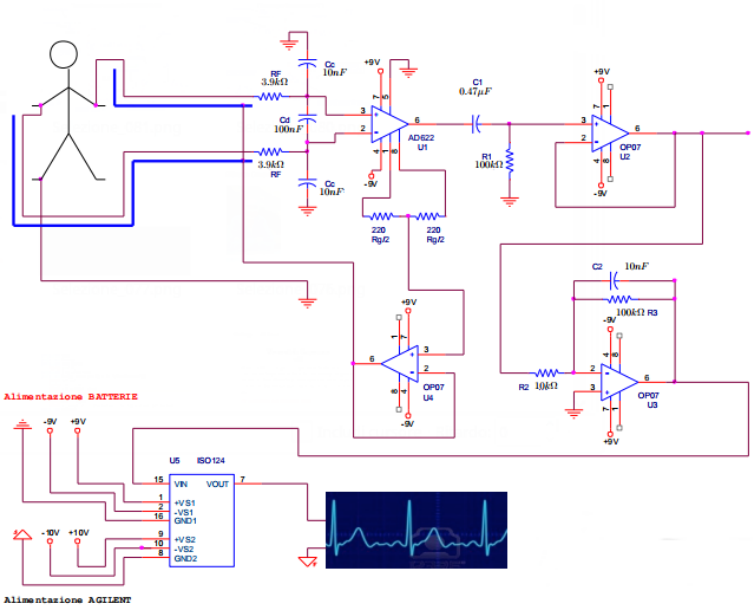


Figure 7.1: Circuit designed

The first step was to remove high frequency noise by using two low-pass filters before the OP07 inputs: this was achieved by the use of two $3.9k\Omega$ resitors (R_F) and three capacitors as shown in figure 7.1 (one connecting the two resistors of 100 nF (C_D), the others of 10 nF (C_C)).
Then we removed the common signal thanks to a differential amplifier, setting this component's gain to $G = \frac{50.1k\Omega}{R_G} + 1 = 116$, where $R_G = 440\Omega$ is the total resistance between pin 1 and 8. This resistance was obtained with two identical resistors in series: this way the voltage between them would have come to be equal to the cable one, so we brought this potential to the coaxial cable shield using a follower for the impedence mismatching. We did this in order to limit the electric dispersion of our signal: if a cable and its shield share the same potential, there will be less electrons that flows from one to the other and so the signal travelling will be better preserved.
After that we put the signal through a high-pass filter in order to remove other components and then we used again a follower for the impedance mismatching. The next step was a second low-pass filter, but active now. At this time we had the signal we needed, except that we wanted to see it with the oscilloscope, powered with undesired 220 V: in order to separate this "dangerous" component from the rest of the circuit we used the isolation amplifier ISO124, which means having two different reference voltages, one for each part of the circuit powered differently. We took a last precaution: since also skin has a resistance that lowers the signal, we cleaned with alcohol the surface where we attached the electrodes aiming to remove the fat and reducing this resistance. Like every other object that produces a ddp, a reference ground voltage was needed for the patient: besides the two electrodes on the wrists, we used also a third one on the left ankle to be connected to the ground of the first part of the circuit, the one powered with $\pm 9V$ (as we said before, we had two different common reference voltages).

7.3 Data analysis

In this experiment there were many noise sources: one could be the patient's body itself, others could instead affect only some parts of the circuit and could be external: this means that the noise could have a component identical in the two input signals but also another different in each of them. In order to reduce as much as possible these noises we used many filters, but even with all those precautions the signal acquired was not completely evident. The result of our measures is shown in figure 7.2

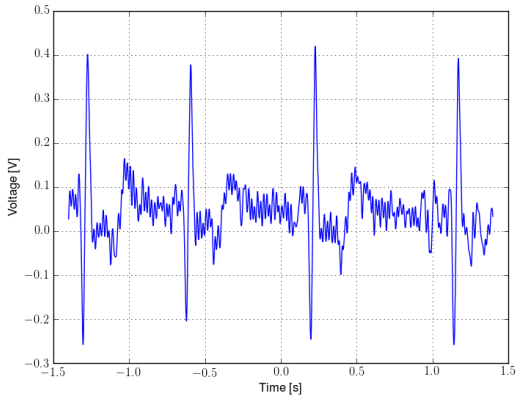


Figure 7.2: Signal measured

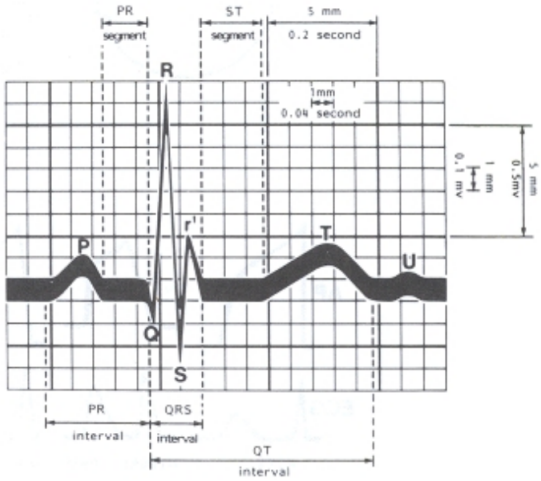


Figure 7.3: Theoretical signal

We can easily see a signal that surely resambles the expected one (see figure 7.3), but is still not clear: fourier trasforming our signal we can analyze the noise frequency composition

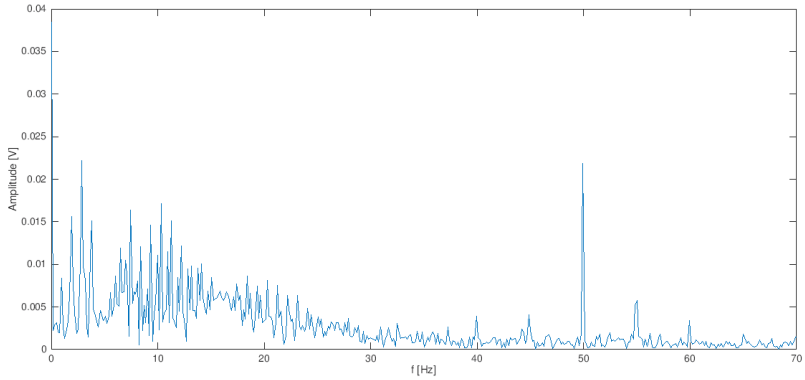


Figure 7.4: Fourier transform of acquired signal

Besides the expected low frequency components, in figure 7.4 we find an evident peak at 50 Hz, a frequency too high for our signal. We can than suppose that with a notch filter at that frequency our measure would have been much less noisy.

Experiment 8

Wien bridge oscillator and digital electronic

In the first part of the experience we built a wien bridge oscillator with an automatic gain control (AGC) which was made possibile by the variable resistance of a tungsten light bulb. We analized the wave's quality and the critical startup time. The second part was about digital electronics: after some exercise with some NAND ports we designed a circuit for an hypotetical rough house alarm system.

8.1 Materials

- Resistors, trimmers, capacitors
- A tungsten light bulb
- Power supply RIGOL DP831A
- Waveform generator RIGOL DG1032
- Multimeter RIGOL DM3068
- uA741
- 8-bit LED viewer
- DM74LS00

The resistors and capacitors used were all with an uncertainty of 5% of their nominal value

8.2 Experimental setup

8.2.1 Wien brigde oscillator

Regarding the band-pass filter in the positive feedback branch, we used two resistors and two capacitors identical in pairs ($R = 10.0 \pm 0.5k\Omega, C = 15.0 \pm 0.7nF$): that way we had a passing frequency of 1060 ± 70 Hz, attenuated by a factor $\frac{1}{3}$. In order to make the wien bridge stably oscillating we then needed a gain factor G of 3 from our op-amp, that means we had to choose $R_2 = 2R_1$: for a better precision we used a $1k\Omega$ trimmer as R_2 and as R_1 a resistor of $47.0 \pm 2.3\Omega$ subsequently followed by a PTC (positive temperature coefficient) tungsten light with a resistance depending on its own temperature.
We set the trimmer to a resistance a little lower than twice 47 Ω, in order to adjust it carefully: once powered the circuit in fact, we raised slowly the trimmer resistance till the output switched from continous 0 V to an oscillating (but unstable) signal.
At this point we placed the light bulb after the 47 Ω resistor: Turning on the circuit, the current would then start to flow in the tungsten resistor increasing its resistance (thanks to the heat produced

by the current), bringing the total one (R_1) till the exact half value of the trimmer one thanks to the thermal inertia.
Our circuit would now auto-oscillate stably, but however the process would have required some time after the power on to equilibrate.

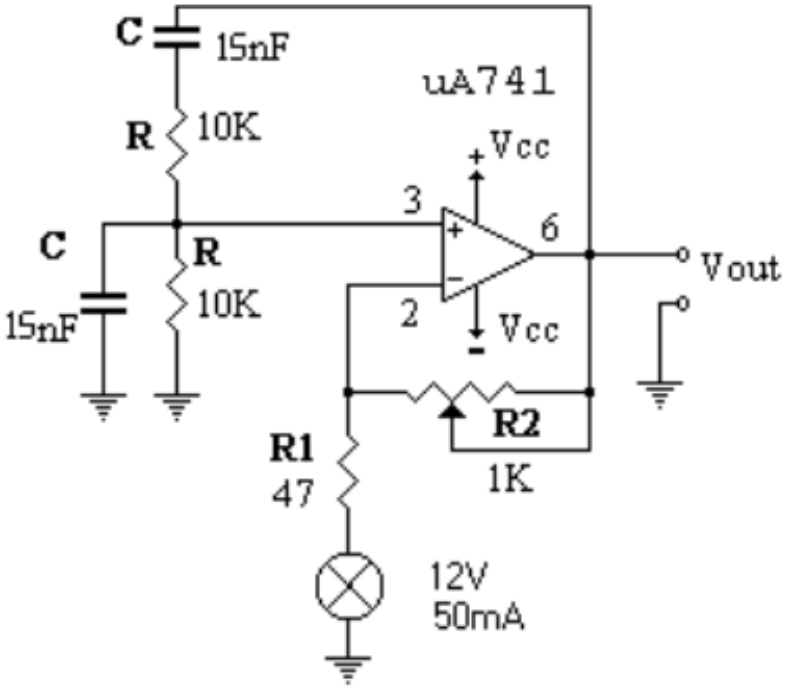


Figure 8.1: Wien bridge

8.2.2 Logic gates

We needed to work with some DM74LS00 components, so firstly we tested them in a NAND configuration with the help of the 8-bit LED viewer for a visual confirmation. For designing the alarm system logic circuit we wrote the desired table of true with which we built the Karnaugh map (table 8.1) and we minimized it.

DW/IK	00	01	11	10
00	0	0	0	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

Table 8.1: D = Door, W = Window, I = Infrared, K = Key

The simplified form found was $Y = D + W + I\overline{K}$. The problem was that we only had NAND gates so we needed to write AND, OR and NOT with NAND: this is how to do it

- NOT is the easiest one, because you only need to connect the signal you want to negate in both NAND inputs
- AND at this point is easy too: it just needs a negation after a simple NAND
- OR is made by negating the inputs of a NAND

Reached these results, we built the circuit and tested it verifing the outputs thanks to the 8-bit LED viewer.

8.3 Data analysis

In figure 8.2 we can see that the output has a transitorial stage that lasts nearly 7.5 s before stabilizing and forming a sine wave (see figure 8.3) of frequency $f_{exp} = 1122.1 \pm 1.4$ Hz: this frequency is actually compatible with the theoretical attended value, $f_{theo} = 1060 \pm 70$ Hz.

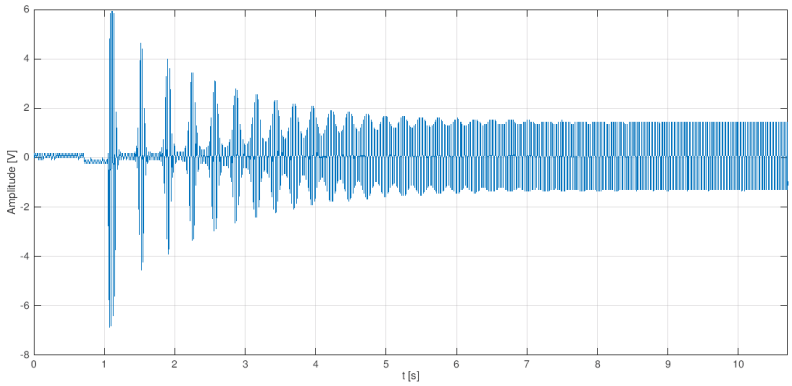


Figure 8.2: Starting process of the wien bridge

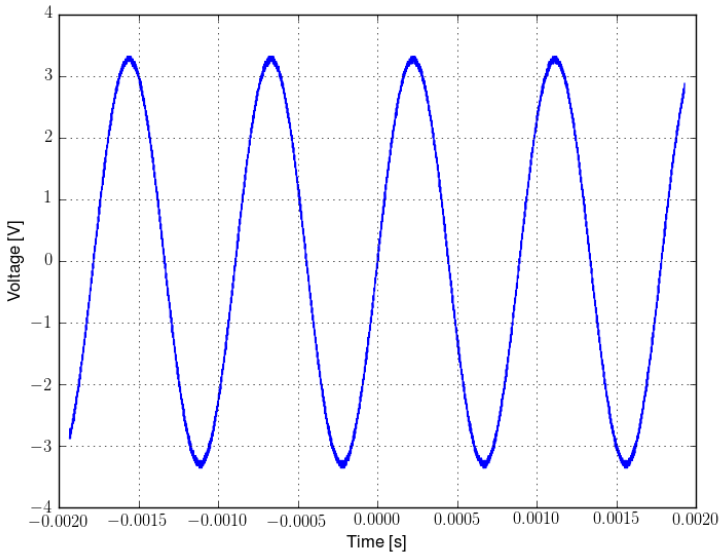


Figure 8.3: Stable state of the wien bridge

We also tested the circuit removing the by-pass capacitors but, as we can see in figure 8.4, the noise is too high for allowing a stable state.

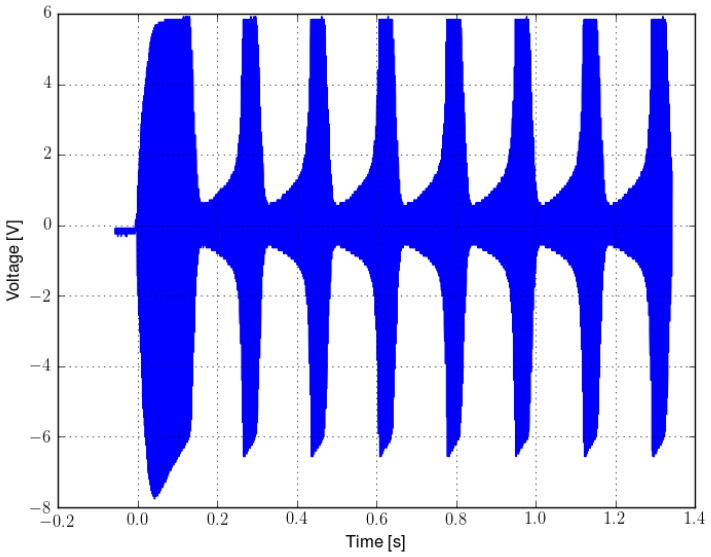


Figure 8.4: Bridge without the by-pass capacitors

Experiment 9

TTL and multiplexer

In this session we first measured the latency between the input and output signal of a 74LS00, then we used a NOT gate with open collector to turn on and off a LED, thirdly we designed and built an half dulpex with two 3state gates and lastly we designed and implemented a multiplexer with 4 signals and two bit of selection.

9.1 Materials

- A resistor
- A LED
- Power supply RIGOL DP831A
- Waveform generator RIGOL DG1032
- Multimeter RIGOL DM3068
- 74LS00
- 74LS05
- 74LS04
- 74LS125

9.2 Experimental setup

In order to measure the time propagation of the signal in the 7400 gate we used the configuration in figure 9.1. As input we used a square wave with 0-5 V voltage and a 100 kHz frequency.

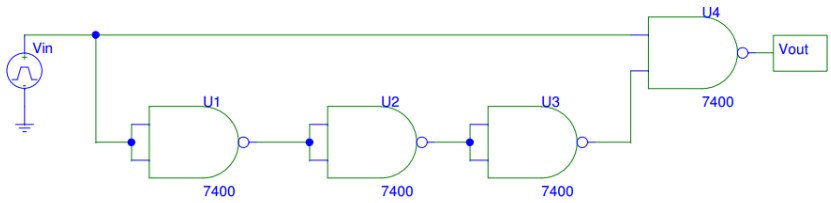


Figure 9.1: The circuit used for measuring the latency in the propagation of a digital input

The NOT gate test was acheved implementing a circuit for switching on and off a LED. The circuit is in figure 9.2 and has a power supply of 9 V: since the voltage drop in the LED and the gate is 1.4 V in total and we must have a 5 mA current flowing, this meant that we needed a pull-up resistor of approximately 1.5 kΩ.

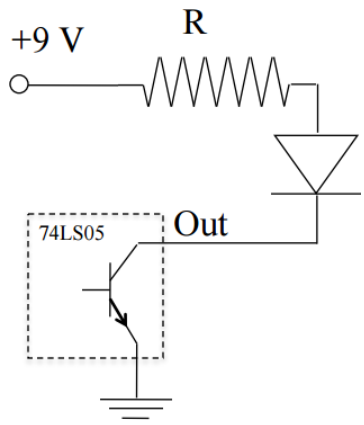


Figure 9.2: NOT TTL Open Collector

we built the half duplex as in figure 9.3. We chose two signals to be transmitted and put each one as the input of a 3-state: the first was a square wave and the other just the ground voltage. We than used an enabling signal to select which of the two had to be transmitted: we connected this directly to the enable pin of a 3-state gate and negated to the same pin of the other gate. We then just put toghether the two gates output and connected them to a LED in order to verify the correct circuit working: actually just one signal passed at any time.

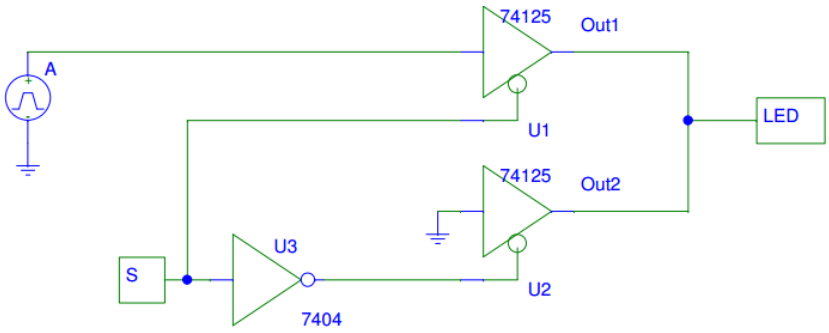


Figure 9.3: Half duplex used for sharing a transmission channel

Lastly we designed a mutiplexer to transmit 4 different signals to another group using again just one wire (plus one for the ground and two for the selection). First we needed to design a 2 bits selector to choose only one among the 4 signals: this was implemented with the circuit in figure 9.4.

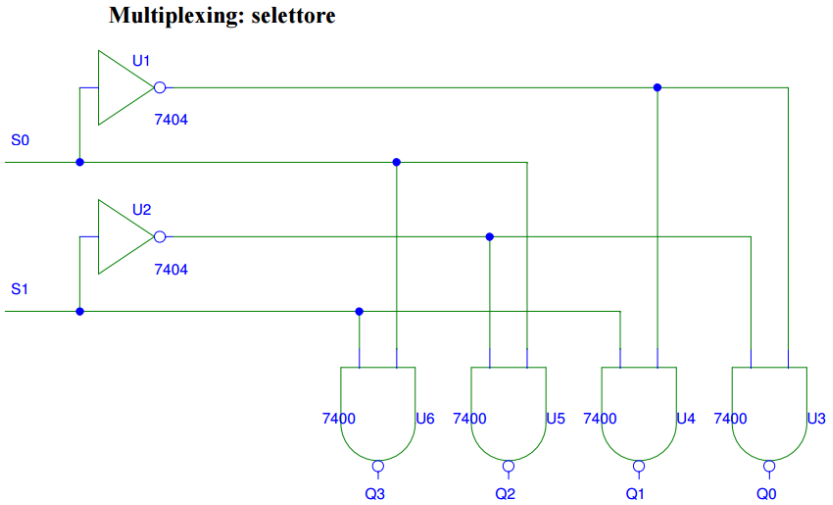


Figure 9.4: The selection circuit: the choice of the enabled channel is made with the 2 bits S0 and S1

Then we used each signal from the selector to enable 4 different 3-state gates, which inputs were our channels D0,D1,D2,D3 with the informations to be transmitted. The 4 outputs had then been put together to be transmitted through only one wire, like we did in the half duplex. This part is shown in figure 9.5.

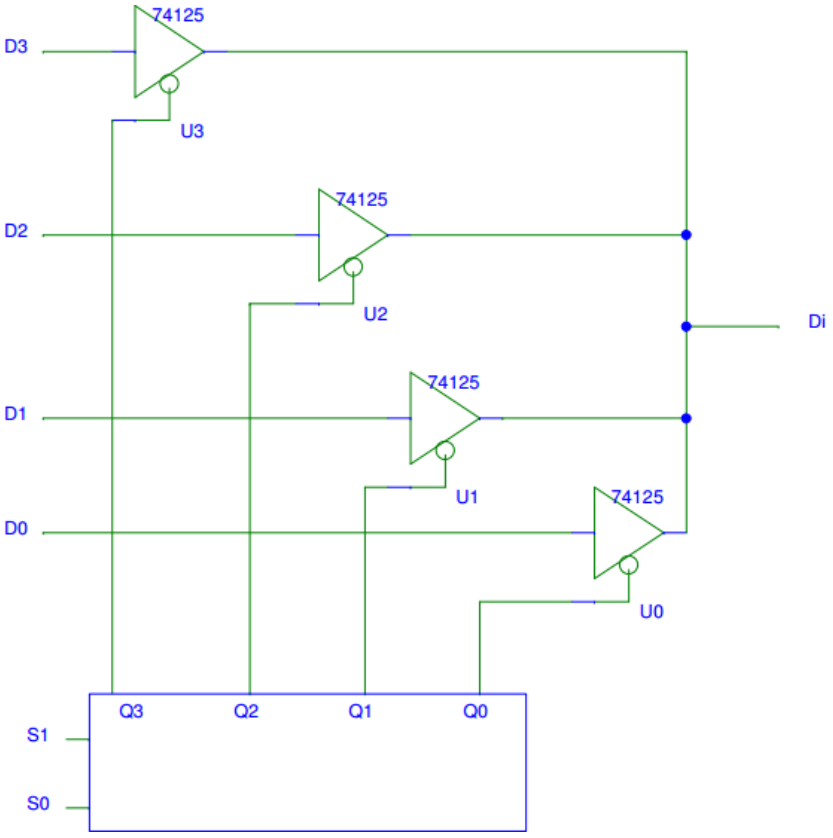


Figure 9.5: The signal from the selector used for blocking and allowing the chosen channel

S0	S1	Channel enabled
0	0	D0
0	1	D1
1	0	D2
1	1	D3

Table 9.1: 2 bits selector logic

We then used a cable to pass to our friends of another group the 3 wires needed for the informations decoding (one with the informations and two for the selection): they were that way able to know which channel was transmitting. The common reference used by the 2 group had to be the same, so we used the earth voltage of the building and successfully trasmitted various signal to the other side of the room.

9.3 Data analysis

From the graph 9.6 we can evaluate the time delay caused by a single gate. We see that the signal took about 14.40 ± 0.08 ns from when it started descending to when it started rising, time that divided by the three gates gives 4.800 ± 0.027 ns per gate: this is an average of the high-to-low ropagation delay and the low-to-high one.
We chose only the part of the signal with a negative derivative because that is the period during which the three gates changes their state.

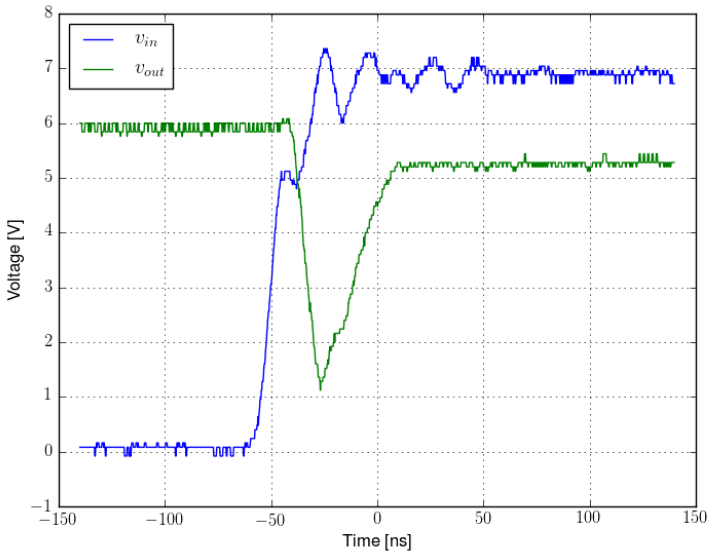


Figure 9.6: The plot shows the delay caused by the propagation of the signal in 3 gates

Experiment 10

Flip flop and sequential logic

In the first part of the experience we implemented the cicuirts: latch SR, latch SR synchronized (flip flop) and a flip flop type D. All of them by using just NAND and NOT gates. Later we built an anti-bounce latch SR and a circuit that registers an impulsive input by storing it in the memory. Later we used a J-K flip flop for building a frequency divider and a shift register. Finally we built an up-down 8-bit counter.

10.1 Materials

- Resistors, trimmers
- Power supply RIGOL DP831A
- Waveform generator RIGOL DG1032
- Multimeter RIGOL DM3068
- NAND 74LS00
- NOT 74LS04
- 74LS109
- 74LS191

The resistors used were all with an uncertainty of 5%

10.2 Experimental setup

We built the latch SR as in the figure 10.1 and for visualizing the output we connected Q and $\overline{Q}$ to an 8-led chip.

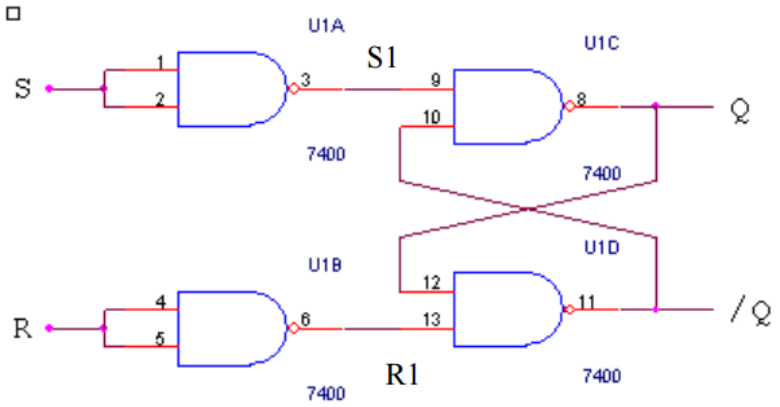


Figure 10.1: Latch SR

Later we modified the circuit as in figure 10.2 and we verified that when EN is low voltage the circuit is in the HOLD configuration, that is it keeps the memory of the previous state.

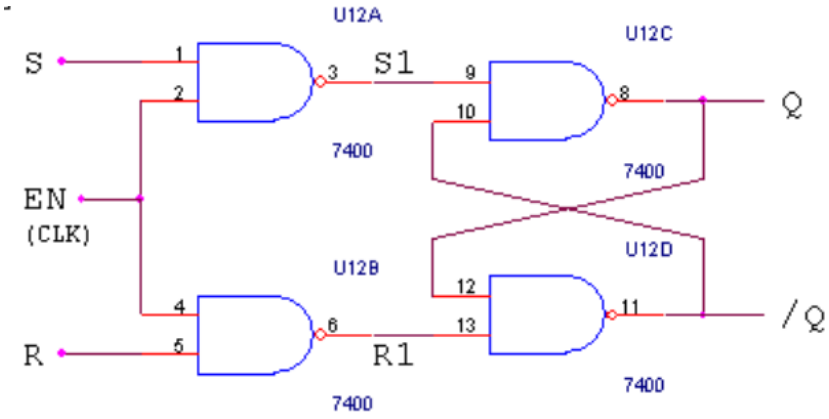


Figure 10.2: Flip-flop built with NAND gates

We modified again the circuit to be a FF type D (figure 10.3) and we verified that every time the EN is on, the bit on D is registred in the memory.

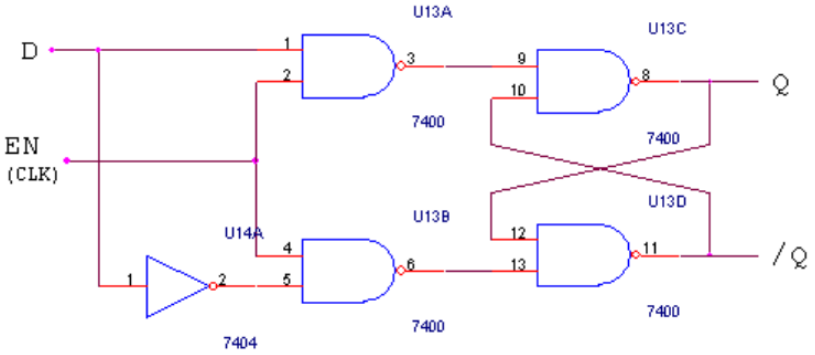


Figure 10.3: Flip flop type D

Then we built a latch SR with an “anti-bounce” configuration (figure 10.4, in particular we made sure the output was changing from LOW to HIGH without too much noise.

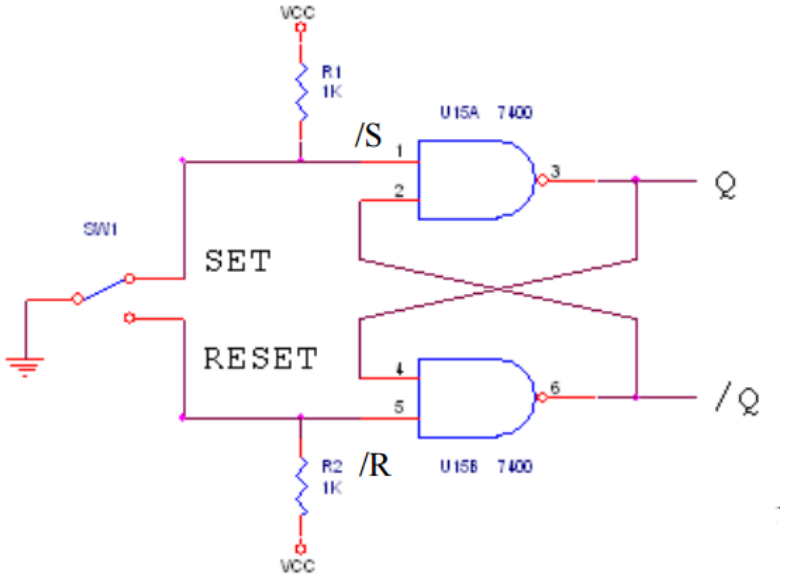


Figure 10.4: Anti bounce circuit

We later built an on/off system (figure 10.5) that had a HIGH output when we activated SET for a short amount of time and a LOW one when we did the same with RESET.

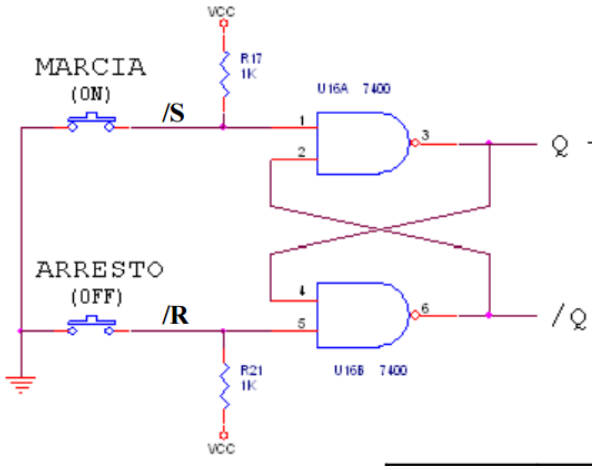


Figure 10.5: On-off circuit

We also built the frequency divider (circuit in 10.6) that gave as output a square wave with frequency that was half or a quarter of the clock, depending on where we took the output. This was done by using two J/K FF connecting the clock with the output of the previous FF or the clock (for the first FF) and connecing J to V_{cc} and K to ground. The frequency of clock used was 10 Hz.

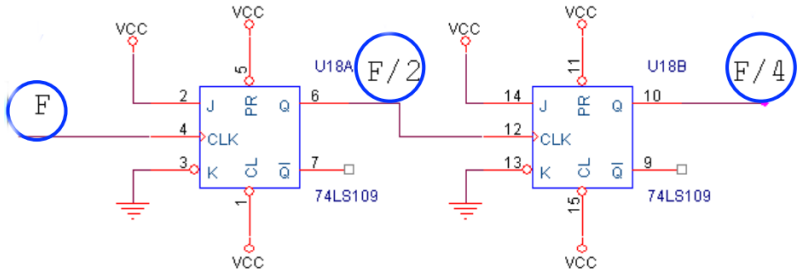


Figure 10.6: Frequency divider

We built the shift register in 10.7 with four J/K FF used as FF type D. We connected the FF in circle connecting the output of one with the input of the other. We also used the pin CL and PR to preset the bit in the registers with the help of a capacitor that kept the voltage LOW for a short amount of time. We visualizied the shift register connecting the output of each FF to some LEDs.

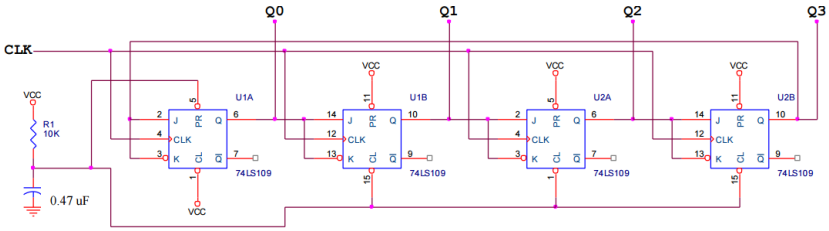


Figure 10.7: Shift register

At last we built a counter with two 74LS191 an a D-FF as in figure 10.8. The FF was used because, as stated in the 74LS191 datasheet, the up/down signal must be on the raising edge of the clock. The FF remember what we chose and transmit it to the clock when this one goes from LOW to HIGH. We used the same method used in the shift register for presetting the bits in the counter. For using an 8 bit system we needed to activate the second 74LS191 just when the bits of the first were all on, this was done by connecting RCD to G of the second one used to enable.

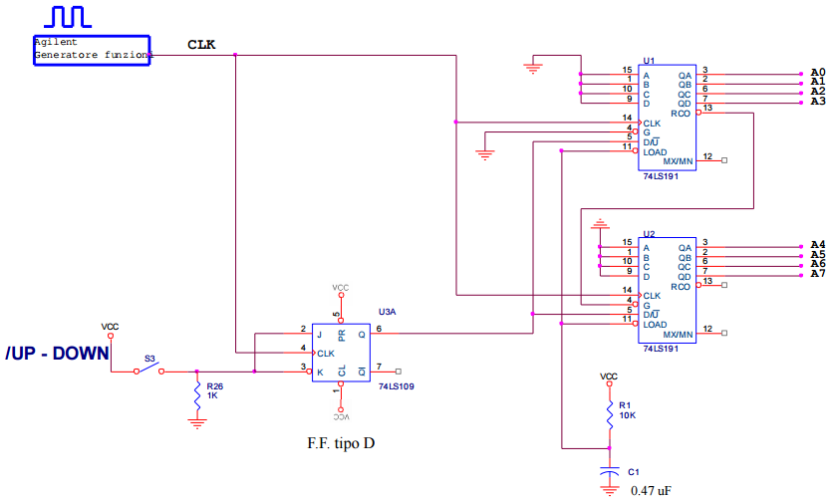


Figure 10.8: 8-bit counter

10.3 Data analysis

We can see in the plot 10.9 that the output of the latch SR is really noisy without the anti bounce expedient.

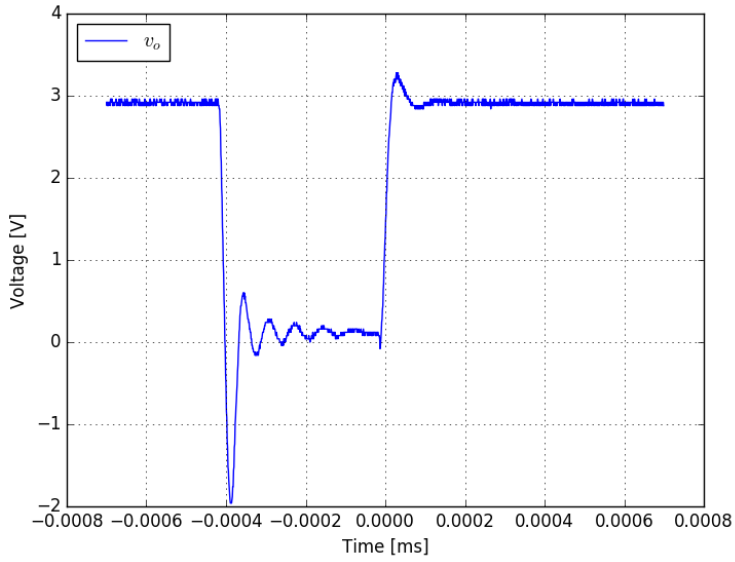


Figure 10.9: Output of a standard latch SR

When we modify as in 10.4 we can see that the output is much more stable.

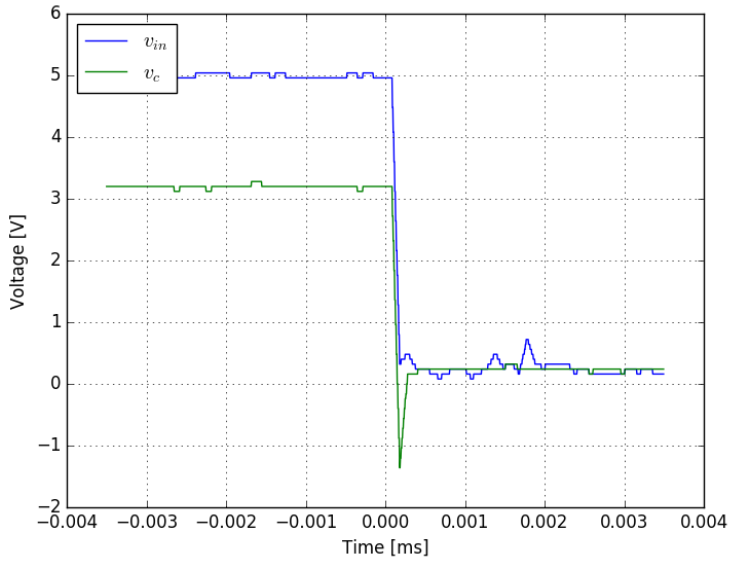


Figure 10.10: Output of a standard latch SR

We can see that in the plots of frequency divider circuit we have the outputs as expected with half and a quarter of the frequency of the clock.

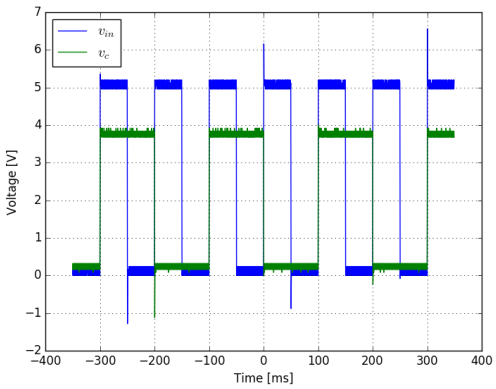


Figure 10.11: Output of frequency divider at half frequency

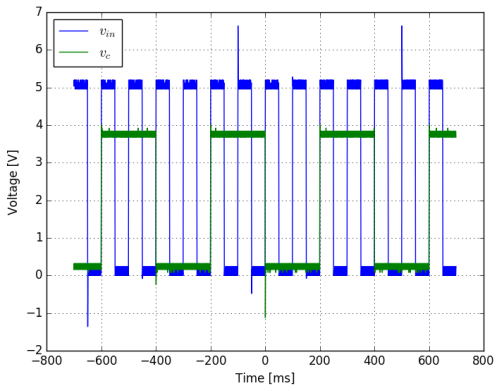


Figure 10.12: Output of frequency divider at quarter frequency

In the counter circuit we used a capacitor for presetting the starting bits. For this reason we measured the voltage at the capacitor's ends at the stating time and, as we expected, in the plot 10.13 the voltage slowly goes to the HIGH level

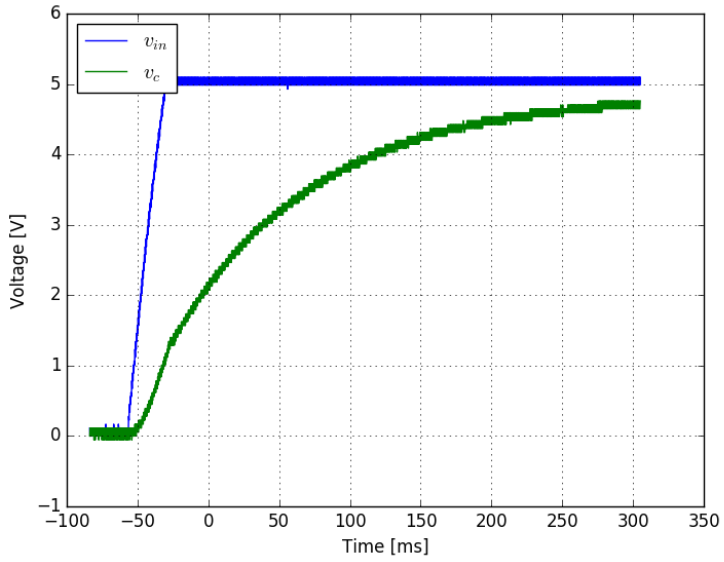


Figure 10.13: In the counting circuit: the voltage of the power supply v_{in} and the voltage on the ends of the capacitor v_c

Experiment 11

ADC tracking

In this experience we built an 8-bit ADC tracking with the output switching from 0 and 5 volt (TTL logic).

11.1 Materials

- Resistors, capacitors
- Power supply RIGOL DP831A
- 5V power supply NI myDAQ
- Waveform generator RIGOL DG1032
- Multimeter RIGOL DM3068
- Digital counter (from previous experiment)
- DAC08
- 8-bit LED viewer
- Comparator LM311

The resistors used were all with an uncertainty of 5%

11.2 Experimental setup

First of all we tested our DAC08 powering it with ±15V and setting the input current in the $+V_{Ref}$ pin to 2mA: this was achieved by tuning the voltage coming from the RIGOL power supply and a resistor of 2.2kΩ. In order to clear as much as possible the bias current effects, we used another identical resistor between the $-V_{Ref}$ pin and ground, we also added a 10nF capacitor between the COMP pin and -15V to optimize the behavior of the component.
Since we used TTL logic and only one output, we put to ground both the V_{LC} and the $\overline{I_{Out}}$ pins.
At this point we had an output current, but we desired an output voltage: for that reason we added a 2081.7±0.4Ω resistor between the I_{Out} pin and ground. We then tested the component with various different inputs and measured its resolution.
Once done these measurements we connected the counter circuit from last experiment as the DAC08 input and we verified the "sawtooth" output of the DAC. Finally we connected this output to a comparator together with the input voltage to be converted, obtained from the -15V power supply voltage with a 5.6kΩ resistor and a 5kΩ trimmer (therefore freely variable), and used this new output as the $\overline{Up}$/Down counter input. We tested the circuit with the D flip flop between the counter and the $\overline{Up}$/Down input and without it. Capacitors 0.1μF were added to all the connections with power supply.

We chose different analog voltage at different clock frequencies and visualized them with the 8-bit LED viewer. In this way we verified the correct working of the circuit.

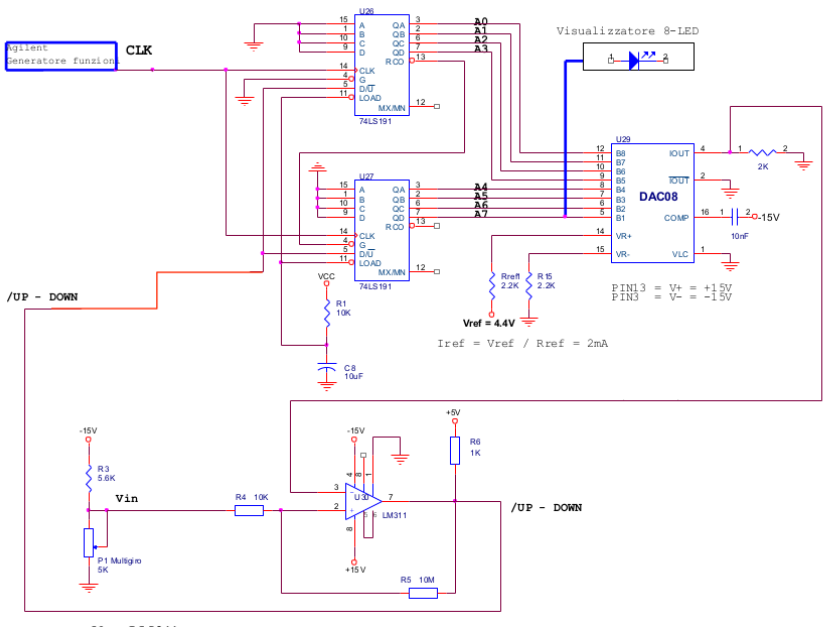


Figure 11.1: Circuit used

11.3 Data Analysis

Once mounted the DAC08, we tested its output with different configurations of the input. The results are shown in table 11.1

Range Fraction	B1	B2	B3	B4	B5	B6	B7	B8	I_{out} (measured)	V_{out} (measured)
FULL RANGE	1	1	1	1	1	1	1	1	1.9870±0.0011 mA	-4.1358±0.0003 V
HALF-SCALE +LSB	1	0	0	0	0	0	0	1	1.0057±0.0006 mA	-2.09378±0.00018 V
HALF-SCALE	1	0	0	0	0	0	0	0	0.9979±0.0006 mA	-2.07775±0.00018 V
HALF-SCALE -LSB	0	1	1	1	1	1	1	1	0.9892±0.0006 mA	-2.05968±0.00018 V
ZERO-SCALE +LSB	0	0	0	0	0	0	0	1	8.08±0.03 μA	-16.807±0.006 mV
ZERO-SCALE	0	0	0	0	0	0	0	0	0.33±0.03 μA	-0.744±0.005 mV

Table 11.1: Test DAC08: measurements

Range Fraction	B1	B2	B3	B4	B5	B6	B7	B8	I_{out} (theoretical)	V_{out} (theoretical)
FULL RANGE	1	1	1	1	1	1	1	1	1.992±0.004 mA	-4.147±0.008 V
HALF-SCALE +LSB	1	0	0	0	0	0	0	1	1.008±0.002 mA	-2.098±0.004 V
HALF-SCALE	1	0	0	0	0	0	0	0	1.000±0.002 mA	-2.082±0.004 V
HALF-SCALE -LSB	0	1	1	1	1	1	1	1	0.992±0.002 mA	-2.065±0.004 V
ZERO-SCALE +LSB	0	0	0	0	0	0	0	1	7.8125±0.016 μA	-16.26±0.03 mV
ZERO-SCALE	0	0	0	0	0	0	0	0	0±0 μA	0±0 mV

Table 11.2: Test DAC08: expected values given $I_{Ref} = 2.000\pm0.004$mA, $R_{out} = 2081.7\pm0.4\Omega$

Comparing the results in these last 2 tables, we can see that the measurements are sufficiently

compatible with the expected values (with the only exeption of the zero-scale that theoretically should be zero with no uncertainty at all).
We can as well measure the resolution of our converter: it is actually the least difference that we can distinguish between two different outputs. Making an average, we come to the result of 1LSB = 16.72±0.12 mV, that is distant from its theoretical value of 16.26±0.03 mV of only 3σ.
Then, connected the DAC08 to the counter and verified the signal tracking and "capture" feature of our system, we observed the response to a 0.3V continue input, using a 30Hz clock frequency and setting the oscilloscope time scale to 20ms/div: We got a ladder in the first part, beginning from 0V and approaching to the input voltage with subsequent steps at the clock frequency, each step modifiyng the output of a value equal to the resolution of the circuit. As the output overtook the signal in input, it began decreasing and increasing one step after another, keeping the medium value equal to the input one. We can see the graphic obtained in figure 11.2

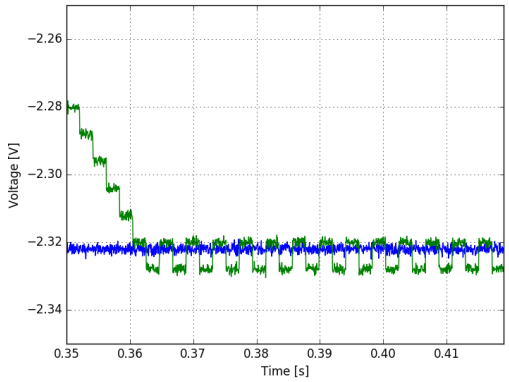


Figure 11.2: signal tracking without flip flop

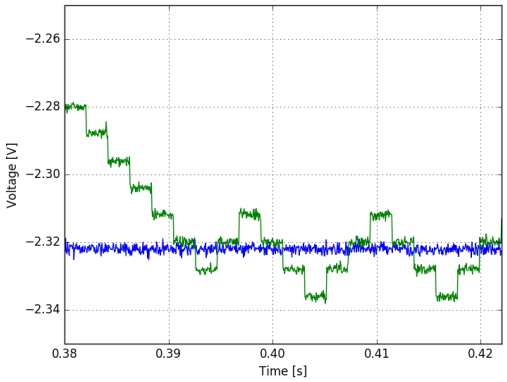


Figure 11.3: signal tracking with flip flop

As we can see in the figure if we keep the flip-flop from the previous experiment, once the input signal was reached we would have had 2 steps more both in the increasing and the decreasing stage: this because the change in the direction in which to count would have arrived to the counter one clock pulse after it left the comparator, and not at the same time.

Experiment 12

Digital sampling

We studied how to reconstruct a signal starting from its sampling. We tried different sampling frequency and two different waves then using the Whittaker–Shannon formula we have reconstructed the orginal signal.

12.1 Materials

- National Instruments myDAQ

12.2 Experimental setup

The waveform generator and the NI myDAQ were connected so we could have use the LabView software for aquiring the data. The sampling frequency and the number of samples were set with the software. As source signal we used a sine wave with frequency 10 Hz and an amplitude pk-pk of 5 V, we sampled this wave with a frequency of 5,10 and 25 Hz. Then we switched wave with a triangular one of 100 Hz and 4 V pk-pk amplitude, this last signal was sampled with a 500 Hz frequency.

12.3 Data analysis

The Whittaker–Shannon formula states that:

$$x(t) = \sum_n x_n \cdot \operatorname{sinc}\left(\frac{t - t_n}{T}\right)$$

where x_n are the data corresponding to the time t_n and T is the sampling period. Appling this formula to our data we obtain the following plot

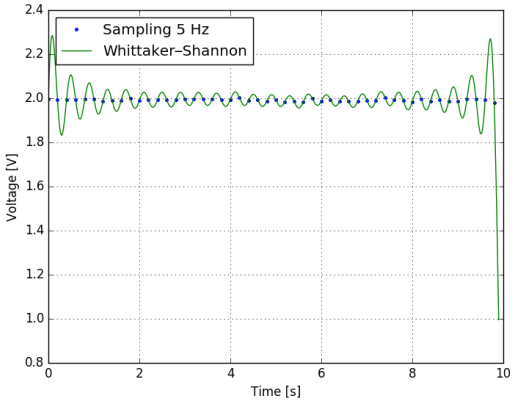


Figure 12.1: Sine input, sampling frequency: 5 Hz

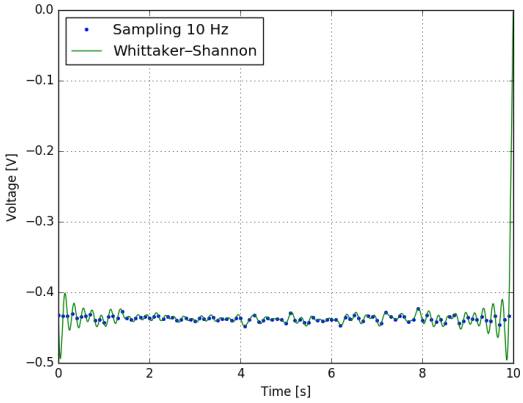


Figure 12.2: Sine input, sampling frequency: 10 Hz

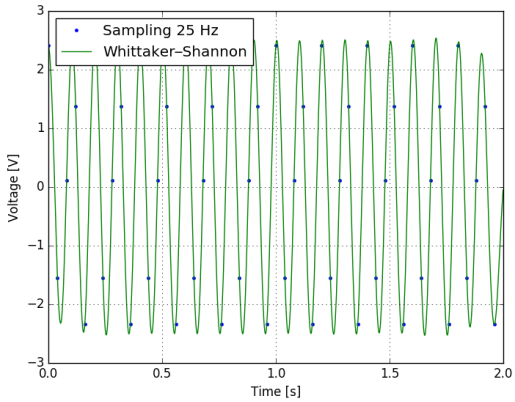


Figure 12.3: Sine input, sampling frequency: 25 Hz

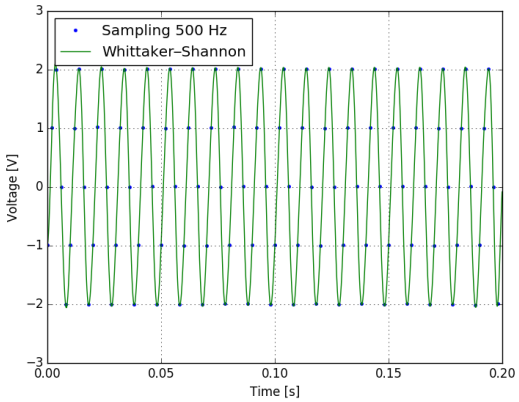


Figure 12.4: Triangular input, sampling frequency: 500 Hz