ANUBHAV KUMAR

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EDUCATION

Technical University of Munich | Germany **October 2022 - March 2025**
Master of Science in Communication and Electronics Engineering | **GPA: 1.9**

Amrita Vishwa Vidyapeetham | India **June 2015 - July 2019**
Bachelor of Science in Electronics and Communication Engineering | **GPA: 1.6**

TECHNICAL SKILLS

- Language: **C** | **C++** | **Verilog** | **SystemVerilog**
- Version Control: **Git** | **Gerrit** | **Perforce**
- Bus Protocols: **AMBA** | **AXI** | **APB** | **UART** | **I2C** | **SPI**
- Architecture: **ARM** | **FPGA** | **RISC-V**
- Interest: **UVM** | **Random Verification** | **Functional Coverage** | **Assertions** | **Formal Verification** | **UPF**

PROFESSIONAL EXPERIENCE

SoC Design Verification Engineer | Master Thesis | Adva Network Security
Munich, Germany | June 2024 - April 2025

- Developed a UVM-based testbench for TRNG IP verification on an Arm-based SoC architecture, incorporating directed and constrained-random stimulus using functional coverage, immediate and concurrent assertions to ensure compliance with security requirements.
- Implemented a class-based SystemVerilog testbench to verify AXI and APB bus protocols for communication between the Processing System (PS) and Programmable Logic (PL), ensuring protocol compliance and functional correctness.
- Performed side-channel injection attacks on the TRNG using instruments such as oscilloscopes, network analyzers, and function generators to evaluate its vulnerability to physical attacks and assess robustness.

Design Verification Engineer | Working Student | Infineon Technologies
Munich, Germany | June 2023 - June 2024

- Developed comprehensive test plans and wrote test cases to verify the functionality and performance of a System on Chip (SoC), ensuring compliance with design specifications and expected behavior.
- Developed testbench setups and executed automated test scripts for directed, random, functional, and stress-testing of the Device Under Test (DUT).
- Proficient in using hardware debugging tools such as oscilloscopes, logic analyzers, and function generators for post-silicon bring-up, signal integrity analysis, and system-level validation.
- Familiar with off-chip communication protocols including UART, SPI, I2C, and Ethernet, with hands-on experience in integration, validation, and debugging of interface-level issues on the DUT.

Embedded Software Engineer | Working Student | Rohde & Schwarz
Munich, Germany | November 2022 - April 2023

- Defined and implemented C++ based data structures to represent software component dependencies at both build-time and run-time for improved traceability and modularity.
- Developed a robust toolset to process and visualize dependency information, enabling efficient debugging and system architecture analysis.
- Automated the generation of configuration files from dependency data to streamline the build and deployment process of software components.

Senior Embedded Software Engineer | Full-time | Honeywell Technology Solutions
Bangalore, India | August 2019 - October 2022

- Security Architect for an ARM-based embedded intrusion panel responsible for obtaining cybersecurity clearance for both software and hardware components prior to market release.
- Contributed to the architecture, design, and implementation of real-time embedded software features for intrusion panels, prioritizing high reliability and security-critical operation.
- Integrated software components with wired and wireless sensors, communication modules, and custom hardware modules in embedded systems.
- Implemented a secure TLS-based WebSocket solution for real-time transmission of critical alarm events from embedded intrusion panels to a central monitoring station.
- Designed a mobile application-based access control panel with secure TLS communication for seamless and secure access to restricted premises.

PUBLICATIONS

- Distance and Energy Aware Device to Device Communication - Apr 2019
- Security Attacks And Their Implications on Time Synchronization In Time-Sensitive Networking - Jul 2024
- Analysis of Technology-Specific Weaknesses of Physical True Random Number Generator Based on Free Running Oscillators - Apr 2025

AWARDS AND CERTIFICATIONS

- **ASIP Designer Hackathon** - Designed and implemented custom RISC-V instructions using Synopsys nML language during the Hackathon (May 2024) to accelerate a target function, optimizing execution efficiency and performance.
- **TUM Science Hackathon** - Developed a trustworthy vehicle insurance platform during the Hackathon (May 2023) by leveraging in-built vehicle sensors to capture driving behavior and accident data for transparent claim assessment.
- **TUM Deutschlandstipendium** - Awarded the scholarship for the academic year 2022–2023 in recognition of outstanding academic performance and significant social contributions.