
Section 31. Introduction (Part III)

HIGHLIGHTS

This section of the manual contains the following major topics:

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31.1 INTRODUCTION

Part III sections of the dsPIC33F Family Reference Manual provide information on modules specific to the low-cost, small pin count, Digital Signal Controllers (DSCs). These devices are ideally suited for low-cost, high-performance motor control, general purpose and audio applications, as well as a variety of sensor applications.

These devices feature many advanced peripherals, such as a Motor Control PWM, 10/12-bit Analog-to-Digital Converter (ADC), 16-bit Digital-to-Analog Converter (DAC), Programmable Cyclic Redundancy Check (CRC), Real-Time Clock and Calendar (RTCC) and a Parallel Master Port (PMP). In addition, these devices feature Peripheral Pins Select functionality, which provides flexibility of mapping any digital peripheral functionality to any desired digital pin.

Part III sections apply to the following dsPIC33F devices (general purpose devices are listed first followed by motor control devices):

- dsPIC33FJ32GP302
- dsPIC33FJ32GP304
- dsPIC33FJ64GP202
- dsPIC33FJ64GP204
- dsPIC33FJ64GP802
- dsPIC33FJ64GP804
- dsPIC33FJ128GP202
- dsPIC33FJ128GP204
- dsPIC33FJ128GP802
- dsPIC33FJ128GP804
- dsPIC33FJ32MC302
- dsPIC33FJ32MC304
- dsPIC33FJ64MC202
- dsPIC33FJ64MC204
- dsPIC33FJ64MC802
- dsPIC33FJ64MC804
- dsPIC33FJ128MC202
- dsPIC33FJ128MC204
- dsPIC33FJ128MC802
- dsPIC33FJ128MC804

Table 31-1 provides a guide to specific information about these devices.

Table 31-1: Family Reference Manual Information Guide

For Information About:	See This Section:
CPU	Part I, Section 2
Data Memory	Part I, Section 3
Program Memory	Part I, Section 4
Flash Programming	Part I, Section 5
Reset	Part I, Section 8
Watchdog Timer and Power-Saving Modes	Part I, Section 9
Timers	Part I, Section 11
Input Capture	Part I, Section 12
Output Compare	Part I, Section 13
Motor Control PWM	Part I, Section 14
Quadrature Encoder Interface (QEI)	Part I, Section 15
Analog-to-Digital Converter (ADC)	Part I, Section 16
Universal Asynchronous Receiver Transmitter (UART)	Part I, Section 17
Serial Peripheral Interface (SPI)	Part I, Section 18
Inter-Integrated Circuit (I ² C™)	Part I, Section 19
Data Converter Interface (DCI)	Part I, Section 20
Enhanced Controller Area Network (ECAN™)	Part I, Section 21
CodeGuard™ Security	Part I, Section 23
Programming and Diagnostics	Part I, Section 24
Device Configuration	Part I, Section 25
Development Tool Support	Part I, Section 26
I/O Ports with Peripheral Pin Select	Part II, Section 30
Interrupts	Part III, Section 32
Audio Digital-to-Analog Converter (DAC)	Part III, Section 33
Comparator	Part III, Section 34
Parallel Master Port (PMP)	Part III, Section 35
Programmable Cyclic Redundancy Check (CRC)	Part III, Section 36
Real-Time Clock and Calendar (RTCC)	Part III, Section 37
Direct Memory Access (DMA)	Part III, Section 38
Oscillator	Part III, Section 39

31.2 REVISION HISTORY

Revision A (October 2007)

This is the initial released revision of this document.