PIC18F2331/2431/4331/4431

PIC18F2331/2431/4331/4431 Data Sheet Errata

In the Device Data Sheet (DS39616**B**), the following clarifications and corrections should be noted. Any silicon issues related to the PIC18F2331/2431/4331/4431 will be reported in a separate silicon errata. Please check the Microchip Web site for any existing issues.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39616**B**), the following clarifications and corrections should be noted.

1. Module: Power-on Reset

The following note has been added to **Section 4.1 "Power-on Reset (POR)"**:

> **Note:** The following decoupling method is recommended:
>
> 1. A 1 μF capacitor should be connected across AVDD and AVSS.
>
> 2. A similar capacitor should be connected across VDD and VSS.

2. Module: Watchdog Timer

In Table 22-2: Summary of Watchdog Timer Registers, the WINEN bit (CONFIG2H<5>) should not be shaded.

3. Module: PWM Equations

In **Section 17.5 "PWM Period"**, Equations 17-1, 17-2 and 17-3 should be corrected as shown.

EQUATION 17-1: PWM PERIOD FOR FREE RUNNING MODE

$$TPWM = \frac{(PTPER + 1) \times PTMRPS}{Fosc/4}$$

EQUATION 17-2: PWM PERIOD FOR UP/DOWN COUNTING MODE

$$TPWM = \frac{(2 \times PTPER) \times PTMRPS}{\frac{Fosc}{4}}$$

EQUATION 17-3: PWM RESOLUTION

$$Resolution = \frac{\log\left(\frac{Fosc}{Fpwm}\right)}{\log(2)}$$

PIC18F2331/2431/4331/4431

4. Module: DC Characteristics

The specifications and parameter numbers for the Brown-out Reset Voltage limits (VBOR, originally parameter D005) in **Section 25.1 "DC Characteristics: Supply Voltage"** of the Device Data Sheet have been changed.

The specifications and parameter numbers have been revised for devices with date codes from 0401xxx to 0420xxx, inclusive.

Specifications and parameter numbers have been revised for specific temperature ranges for date codes from 0421xxx and higher.

The new information is shown in **bold** text.

25.1 DC Characteristics: Supply Voltage
PIC18F2331/2431/4331/4431 (Industrial)
PIC18LF2331/2431/4331/4431 (Industrial, Extended)

PIC18LF2331/2431/4331/4431 (Industrial)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC18F2331/2431/4331/4431 (Industrial, Extended)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Date Codes from 0401xxx to 0420xxx, inclusive							
D005A	VBOR	**Brown-out Reset Voltage**					
		PIC18LF2X31/4X31	Industrial Low Voltage **(-40°C to +85°C)**				
		BORV1:BORV0 = 11	**N/A**	**N/A**	**N/A**	V	**Reserved**
		BORV1:BORV0 = 10	**2.45**	**2.72**	**2.99**	V	
		BORV1:BORV0 = 01	**3.80**	**4.22**	**4.64**	V	
		BORV1:BORV0 = 00	**4.09**	**4.54**	**4.99**	V	
D005B		PIC18F2X31/4X31	Industrial **(-40°C to +85°C)**				
		BORV1:BORV0 = 1x	**N/A**	**N/A**	**N/A**	V	**Reserved**
		BORV1:BORV0 = 01	**3.80**	**4.22**	**4.64**	V	**(Note 2)**
		BORV1:BORV0 = 00	**4.09**	**4.54**	**4.99**	V	**(Note 2)**
D005C		PIC18F2X31/4X31	Extended **(-40°C to +125°C)**				
		BORV1:BORV0 = 1x	**N/A**	**N/A**	**N/A**	V	**Reserved**
		BORV1:BORV0 = 01	**3.80**	**4.22**	**4.64**	V	**(Note 2)**
		BORV1:BORV0 = 00	**4.09**	**4.54**	**4.99**	V	**(Note 2)**

Legend: Shading of rows is to assist in readability of the table.

Note 1:   This is the limit to which VDD can be lowered in Sleep mode, or during a device Reset, without losing RAM data.

2:   **When BOR is on and BORV<1:0> = 0x, the device will operate correctly at 40 MHz for any VDD at which the BOR allows execution.**

25.1 DC Characteristics: Supply Voltage
PIC18F2331/2431/4331/4431 (Industrial)
PIC18LF2331/2431/4331/4431 (Industrial, Extended)

PIC18LF2331/2431/4331/4431 (Industrial)	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial
PIC18F2331/2431/4331/4431 (Industrial, Extended)	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
		Date Codes from 0421xxx and higher					
	VBOR	**Brown-out Reset Voltage**					
D005D		PIC18LF2X31/4X31	Industrial Low Voltage **(-10°C to +85°C)**				
		BORV1:BORV0 = 11	**N/A**	**N/A**	**N/A**	V	**Reserved**
		BORV1:BORV0 = 10	**2.50**	**2.72**	**2.94**	V	
		BORV1:BORV0 = 01	**3.88**	**4.22**	**4.56**	V	
		BORV1:BORV0 = 00	**4.18**	**4.54**	**4.90**	V	
D005F		PIC18LF2X31/4X31	Industrial Low Voltage **(-40°C to -10°C)**				
		BORV1:BORV0 = 11	**N/A**	**N/A**	**N/A**	V	**Reserved**
		BORV1:BORV0 = 10	**2.34**	**2.72**	**3.10**	V	
		BORV1:BORV0 = 01	**3.63**	**4.22**	**4.81**	V	
		BORV1:BORV0 = 00	**3.90**	**4.54**	**5.18**	V	
D005G		PIC18F2X31/4X31	Industrial **(-10°C to +85°C)**				
		BORV1:BORV0 = 1x	**N/A**	**N/A**	**N/A**	V	**Reserved**
		BORV1:BORV0 = 01	**3.88**	**4.22**	**4.56**	V	(Note 2)
		BORV1:BORV0 = 00	**4.18**	**4.54**	**4.90**	V	(Note 2)
D005H		PIC18F2X31/4X31	Industrial **(-40°C to -10°C)**				
		BORV1:BORV0 = 1x	**N/A**	**N/A**	**N/A**	V	**Reserved**
		BORV1:BORV0 = 01	**N/A**	**N/A**	**N/A**	V	**Reserved**
		BORV1:BORV0 = 00	**3.90**	**4.54**	**5.18**	V	(Note 2)
D005J		PIC18F2X31/4X31	Extended **(-10°C to +85°C)**				
		BORV1:BORV0 = 1x	**N/A**	**N/A**	**N/A**	V	**Reserved**
		BORV1:BORV0 = 01	**3.88**	**4.22**	**4.56**	V	(Note 2)
		BORV1:BORV0 = 00	**4.18**	**4.54**	**4.90**	V	(Note 2)
D005K		PIC18F2X31/4X31	Extended **(-40°C to -10°C, +85°C to +125°C)**				
		BORV1:BORV0 = 1x	**N/A**	**N/A**	**N/A**	V	**Reserved**
		BORV1:BORV0 = 01	**N/A**	**N/A**	**N/A**	V	**Reserved**
		BORV1:BORV0 = 00	**3.90**	**4.54**	**5.18**	V	(Note 2)

Legend: Shading of rows is to assist in readability of the table.

Note 1: This is the limit to which VDD can be lowered in Sleep mode, or during a device Reset, without losing RAM data.

2: When BOR is on and BORV<1:0> = 0x, the device will operate correctly at 40 MHz for any VDD at which the BOR allows execution.

PIC18F2331/2431/4331/4431

5. Module: LVD Characteristics

The specifications and parameter numbers for the Low-Voltage Detect thresholds (V_{LVD}, originally parameter D420) in Table 25-2 of the Device Data Sheet have been changed.

The specifications and parameter numbers have been revised for devices with date codes from 0401xxx to 0420xxx, inclusive.

Specifications and parameter numbers have been revised for specific temperature ranges for date codes from 0421xxx and higher.

The new information is shown in **bold** text.

TABLE 25-2: LOW-VOLTAGE DETECT CHARACTERISTICS

PIC18LF2331/2431/4331/4431 (Industrial)			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC18F2331/2431/4331/4431 (Industrial, Extended)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
Date Codes from 0401xxx to 0420xxx, inclusive							
D420A	V_{LVD}	LVD Voltage on V_{DD} Transition High-to-Low	Industrial Low Voltage **(-40°C to +85°C)**				
		PIC18LF2X31/4X31 LVDL<3:0> = 0000	**N/A**	**N/A**	**N/A**	V	Reserved
		LVDL<3:0> = 0001	**N/A**	**N/A**	**N/A**	V	Reserved
		LVDL<3:0> = 0010	**2.08**	**2.26**	**2.44**	V	
		LVDL<3:0> = 0011	**2.26**	**2.45**	**2.65**	V	
		LVDL<3:0> = 0100	**2.35**	**2.55**	**2.76**	V	
		LVDL<3:0> = 0101	**2.55**	**2.77**	**2.99**	V	
		LVDL<3:0> = 0110	**2.64**	**2.87**	**3.10**	V	
		LVDL<3:0> = 0111	**2.82**	**3.07**	**3.31**	V	
		LVDL<3:0> = 1000	**3.09**	**3.36**	**3.63**	V	
		LVDL<3:0> = 1001	**3.29**	**3.57**	**3.86**	V	
		LVDL<3:0> = 1010	**3.38**	**3.67**	**3.96**	V	
		LVDL<3:0> = 1011	**3.56**	**3.87**	**4.18**	V	
		LVDL<3:0> = 1100	**3.75**	**4.07**	**4.40**	V	
		LVDL<3:0> = 1101	**3.93**	**4.28**	**4.62**	V	
		LVDL<3:0> = 1110	**4.23**	**4.60**	**4.96**	V	
D420B		LVD Voltage on V_{DD} Transition High-to-Low	Industrial **(-40°C to +85°C)**				
		PIC18F2X31/4X31 LVDL<3:0> = 1011	**3.56**	**3.87**	**4.18**	V	
		LVDL<3:0> = 1100	**3.75**	**4.07**	**4.40**	V	
		LVDL<3:0> = 1101	**3.93**	**4.28**	**4.62**	V	
		LVDL<3:0> = 1110	**4.23**	**4.60**	**4.96**	V	
D420C		LVD Voltage on V_{DD} Transition High-to-Low	Extended **(-40°C to +125°C)**				
		PIC18F2X31/4X31 LVDL<3:0> = 1011	**3.41**	**3.87**	**4.33**	V	
		LVDL<3:0> = 1100	**3.58**	**4.07**	**4.56**	V	
		LVDL<3:0> = 1101	**3.77**	**4.28**	**4.79**	V	
		LVDL<3:0> = 1110	**4.04**	**4.60**	**5.15**	V	

Legend: Shading of rows is to assist in readability of the table.

  † Production tested at TAMB = 25°C. Specifications over temperature limits ensured by characterization.

TABLE 25-2: LOW-VOLTAGE DETECT CHARACTERISTICS (CONTINUED)

PIC18LF2331/2431/4331/4431 (Industrial)			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC18F2331/2431/4331/4431 (Industrial, Extended)			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
Date Codes from 0421xxx and higher							
D420D	VLVD	LVD Voltage on VDD Transition High-to-Low	Industrial Low Voltage **(-10°C to +85°C)**				
		PIC18LF2X31/4X31 LVDL<3:0> = 0000	N/A	N/A	N/A	V	Reserved
		LVDL<3:0> = 0001	N/A	N/A	N/A	V	Reserved
		LVDL<3:0> = 0010	2.08	2.26	2.44	V	
		LVDL<3:0> = 0011	2.26	2.45	2.65	V	
		LVDL<3:0> = 0100	2.35	2.55	2.76	V	
		LVDL<3:0> = 0101	2.55	2.77	2.99	V	
		LVDL<3:0> = 0110	2.64	2.87	3.10	V	
		LVDL<3:0> = 0111	2.82	3.07	3.31	V	
		LVDL<3:0> = 1000	3.09	3.36	3.63	V	
		LVDL<3:0> = 1001	3.29	3.57	3.86	V	
		LVDL<3:0> = 1010	3.38	3.67	3.96	V	
		LVDL<3:0> = 1011	3.56	3.87	4.18	V	
		LVDL<3:0> = 1100	3.75	4.07	4.40	V	
		LVDL<3:0> = 1101	3.93	4.28	4.62	V	
		LVDL<3:0> = 1110	4.23	4.60	4.96	V	
D420F		LVD Voltage on VDD Transition High-to-Low	Industrial Low Voltage **(-40°C to -10°C)**				
		PIC18LF2X31/4X31 LVDL<3:0> = 0000	N/A	N/A	N/A	V	Reserved
		LVDL<3:0> = 0001	N/A	N/A	N/A	V	Reserved
		LVDL<3:0> = 0010	1.99	2.26	2.53	V	
		LVDL<3:0> = 0011	2.16	2.45	2.75	V	
		LVDL<3:0> = 0100	2.25	2.55	2.86	V	
		LVDL<3:0> = 0101	2.43	2.77	3.10	V	
		LVDL<3:0> = 0110	2.53	2.87	3.21	V	
		LVDL<3:0> = 0111	2.70	3.07	3.43	V	
		LVDL<3:0> = 1000	2.96	3.36	3.77	V	
		LVDL<3:0> = 1001	3.14	3.57	4.00	V	
		LVDL<3:0> = 1010	3.23	3.67	4.11	V	
		LVDL<3:0> = 1011	3.41	3.87	4.34	V	
		LVDL<3:0> = 1100	3.58	4.07	4.56	V	
		LVDL<3:0> = 1101	3.76	4.28	4.79	V	
		LVDL<3:0> = 1110	4.04	4.60	5.15	V	

Legend: **Shading of rows is to assist in readability of the table.**
    †   Production tested at TAMB = 25°C. Specifications over temperature limits ensured by characterization.

TABLE 25-2: **LOW-VOLTAGE DETECT CHARACTERISTICS (CONTINUED)**

PIC18LF2331/2431/4331/4431 (Industrial)			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC18F2331/2431/4331/4431 (Industrial, Extended)			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
		Date Codes from 0421xxx and higher					
D420G	V_LVD	LVD Voltage on VDD Transition High-to-Low	Industrial (-10°C to +85°C)				
		PIC18F2X31/4X31 LVDL<3:0> = 1101	3.93	4.28	4.62	V	
		LVDL<3:0> = 1110	4.23	4.60	4.96	V	
D420H		LVD Voltage on VDD Transition High-to-Low	Industrial (-40°C to -10°C)				
		PIC18F2X31/4X31 LVDL<3:0> = 1101	3.76	4.28	4.79	V	Reserved
		LVDL<3:0> = 1110	4.04	4.60	5.15	V	
D420J		LVD Voltage on VDD Transition High-to-Low	Extended (-10°C to +85°C)				
		PIC18F2X31/4X31 LVDL<3:0> = 1101	3.94	4.28	4.62	V	
		LVDL<3:0> = 1110	4.23	4.60	4.96	V	
D420K		LVD Voltage on VDD Transition High-to-Low	Extended (-40°C to -10°C, +85°C to +125°C)				
		PIC18F2X31/4X31 LVDL<3:0> = 1101	3.77	4.28	4.79	V	Reserved
		LVDL<3:0> = 1110	4.05	4.60	5.15	V	

Legend: **Shading of rows is to assist in readability of the table.**
† Production tested at TAMB = 25°C. Specifications over temperature limits ensured by characterization.

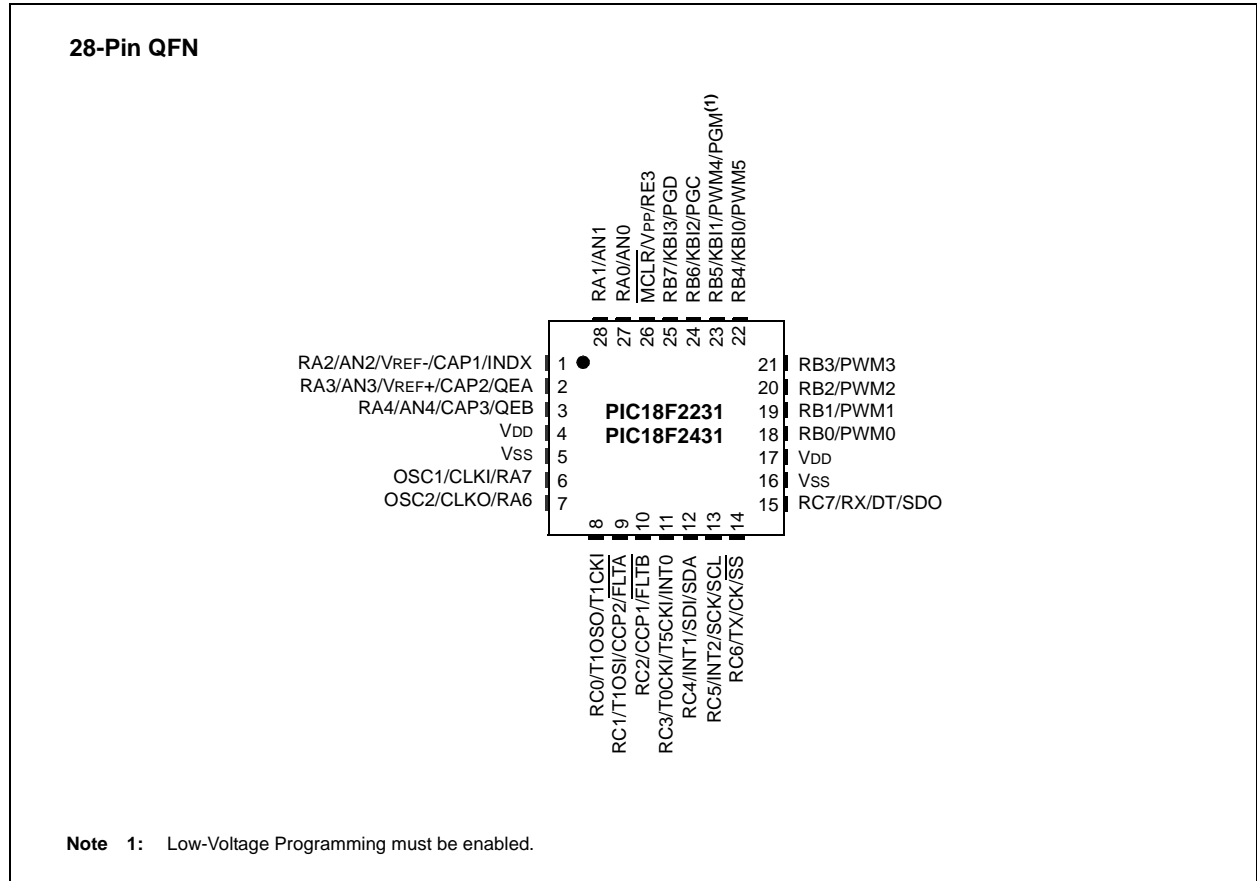## 6. Module: 28-Pin QFN Diagram

A 28-pin QFN package has been introduced for the PIC18F2331 and PIC18F2431 devices. The Device Data Sheet has been updated as follows:

- The **Pin Diagram** section (page 3) has been updated to include the new 28-pin QFN package.

FIGURE 1:   28-PIN QFN DIAGRAM

- The Packages information in Table 1-1 (page 9) and Table B-1 (page 379) has been updated to include a reference to the 28-pin QFN. The new text is shown in **bold**.

TABLE 1:

Features	PIC18F2331	PIC18F2431	PIC18F4331	PIC18F4431
Packages	28-pin SDIP 28-pin SOIC **28-pin QFN**	28-pin SDIP 28-pin SOIC **28-pin QFN**	40-pin DIP 44-pin TQFP 44-pin QFN	40-pin DIP 44-pin TQFP 44-pin QFN

PIC18F2331/2431/4331/4431

- A new column with pin number information for the 28-pin QFN package has been added to Table 1-2 (pages 12-14). New information is shown in **bold** text.

TABLE 1-2: **PIC18F2331/2431 PINOUT I/O DESCRIPTIONS**

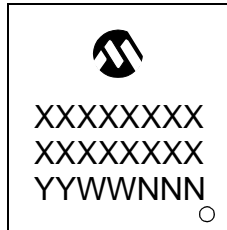| Pin Name	Pin Number		Pin Type	Buffer Type	Description
	DIP, SOIC	QFN			
MCLR/VPP/RE3	1	**26**			Master Clear (input) or programming voltage (input).
MCLR			I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP			P		High-voltage ICSP programming enable pin.
RE3			I	ST	Digital input. Available only when MCLR is disabled.
OSC1/CLKI/RA7	9	**6**			Oscillator crystal or external clock input.
OSC1			I	ST	Oscillator crystal input or external clock source input. ST buffer when configured in RC mode, CMOS otherwise.
CLKI			I	CMOS	External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.)
RA7			I/O	TTL	General purpose I/O pin.
OSC2/CLKO/RA6	10	**7**			Oscillator crystal or clock output.
OSC2			O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO			O	—	In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6			I/O	TTL	General purpose I/O pin.
					PORTA is a bidirectional I/O port.
RA0/AN0	2	**27**			
RA0			I/O	TTL	Digital I/O.
AN0			I	Analog	Analog input 0.
RA1/AN1	3	**28**			
RA1			I/O	TTL	Digital I/O.
AN1			I	Analog	Analog input 1.
RA2/AN2/VREF-/CAP1/INDX	4	**1**			
RA2			I/O	TTL	Digital I/O.
AN2			I	Analog	Analog input 2.
VREF-			I	Analog	A/D reference voltage (Low) input.
CAP1			I	ST	Input capture pin 1.
INDX			I	ST	Quadrature Encoder Interface index input pin.
RA3/AN3/VREF+/CAP2/QEA	5	**2**			
RA3			I/O	TTL	Digital I/O.
AN3			I	Analog	Analog input 3.
VREF+			I	Analog	A/D reference voltage (High) input.
CAP2			I	ST	Input capture pin 2.
QEA			I	ST	Quadrature Encoder Interface channel A input pin.
RA4/AN4/CAP3/QEB	6	**3**			
RA4			I/O	TTL	Digital I/O.
AN4			I	Analog	Analog input 4.
CAP3			I	ST	Input capture pin 3.
QEB			I	ST	Quadrature Encoder Interface channel B input pin.

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
O = Output
OD = Open-Drain (no diode to VDD)
CMOS = CMOS compatible input or output
I = Input
P = Power

TABLE 1-2:   PIC18F2331/2431 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	DIP, SOIC	QFN			
					PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/PWM0	21	**18**			
RB0			I/O	TTL	Digital I/O.
PWM0			O	TTL	PWM output 0.
RB1/PWM1	22	**19**			
RB1			I/O	TTL	Digital I/O.
PWM1			O	TTL	PWM output 1.
RB2/PWM2	23	**20**			
RB2			I/O	TTL	Digital I/O.
PWM2			O	TTL	PWM output 2.
RB3/PWM3	24	**21**			
RB3			I/O	TTL	Digital I/O.
PWM3			O	TTL	PWM output 3.
RB4/KBI0/PWM5	25	**22**			
RB4			I/O	TTL	Digital I/O.
KBI0			I	TTL	Interrupt-on-change pin.
PWM5			O	TTL	PWM output 5.
RB5/KBI1/PWM4/PGM	26	**23**			
RB5			I/O	TTL	Digital I/O.
KBI1			I	TTL	Interrupt-on-change pin.
PWM4			O	TTL	PWM output 4.
PGM			I/O	ST	Low-Voltage ICSP™ Programming entry pin.
RB6/KBI2/PGC	27	**24**			
RB6			I/O	TTL	Digital I/O.
KBI2			I	TTL	Interrupt-on-change pin.
PGC			I/O	ST	In-Circuit Debugger and ICSP programming clock pin.
RB7/KBI3/PGD	28	**25**			
RB7			I/O	TTL	Digital I/O.
KBI3			I	TTL	Interrupt-on-change pin.
PGD			I/O	ST	In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
             ST   = Schmitt Trigger input with CMOS levels   I   = Input
             O   = Output   P   = Power
             OD = Open-Drain (no diode to V$_{DD}$)

TABLE 1-2:   PIC18F2331/2431 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	DIP, SOIC	QFN			
RC0/T1OSO/T1CKI	11	**8**			PORTC is a bidirectional I/O port.
RC0			I/O	ST	Digital I/O.
T1OSO			O	—	Timer1 oscillator output.
T1CKI			I	ST	Timer1 external clock input.
RC1/T1OSI/CCP2/FLTA	12	**9**			
RC1			I/O	ST	Digital I/O.
T1OSI			I	CMOS	Timer1 oscillator input.
CCP2			I/O	ST	Capture 2 input, Compare 2 output, PWM 2 output.
FLTA			I	ST	Fault interrupt input pin.
RC2/CCP1/FLTB	13	**10**			
RC2			I/O	ST	Digital I/O.
CCP1			I/O	ST	Capture 1 input/Compare 1 output/PWM 1 output.
FLTB			I	ST	Fault interrupt input pin.
RC3/T0CKI/T5CKI/INT0	14	**11**			
RC3			I/O	ST	Digital I/O.
T0CKI			I	ST	Timer0 alternate clock input.
T5CKI			I	ST	Timer5 alternate clock input.
INT0			I	ST	External interrupt 0.
RC4/INT1/SDI/SDA	15	**12**			
RC4			I/O	ST	Digital I/O.
INT1			I	ST	External interrupt 1.
SDI			I	ST	SPI™ data in.
SDA			I/O	ST	I^{2}C™ data I/O.
RC5/INT2/SCK/SCL	16	**13**			
RC5			I/O	ST	Digital I/O.
INT2			I	ST	External interrupt 2.
SCK			I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL			I/O	ST	Synchronous serial clock input/output for I^{2}C mode.
RC6/TX/CK/SS	17	**14**			
RC6			I/O	ST	Digital I/O.
TX			O	—	USART asynchronous transmit.
CK			I/O	ST	USART synchronous clock (see related RX/DT).
SS			I	TTL	SPI slave select input.
RC7/RX/DT/SDO	18	**15**			
RC7			I/O	ST	Digital I/O.
RX			I	ST	USART asynchronous receive.
DT			I/O	ST	USART synchronous data (see related TX/CK).
SDO			O	—	SPI data out.
Vss	8, 19	**5, 16**	P	—	Ground reference for logic and I/O pins.
VDD	7, 20	**4, 17**	P	—	Positive supply for logic and I/O pins.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
 ST   = Schmitt Trigger input with CMOS levels   I   = Input
 O   = Output   P   = Power
 OD   = Open-Drain (no diode to VDD)

• 28-pin QFN details have been added to
Section 27.1 "Package Marking Information"
(page 373).

27.1   Package Marking Information

28-Lead QFN   Example

```
XXXXXXXX                    18F2431
XXXXXXXX                    -I/MM
YYWWNNN                     0410017
        ○                          ○
```

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:		In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

*   Standard PICmicro device marking consists of Microchip part number, year code, week code, and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

PIC18F2331/2431/4331/4431

• 28-pin QFN packaging details have been added
  to **Section 27.2 "Package Details"** (page 374).

28-Lead Plastic Quad Flat No Lead Package (MM) 6x6x0.9 mm Body (QFN-S) – With 0.40 mm Contact Length (Saw Singulated)
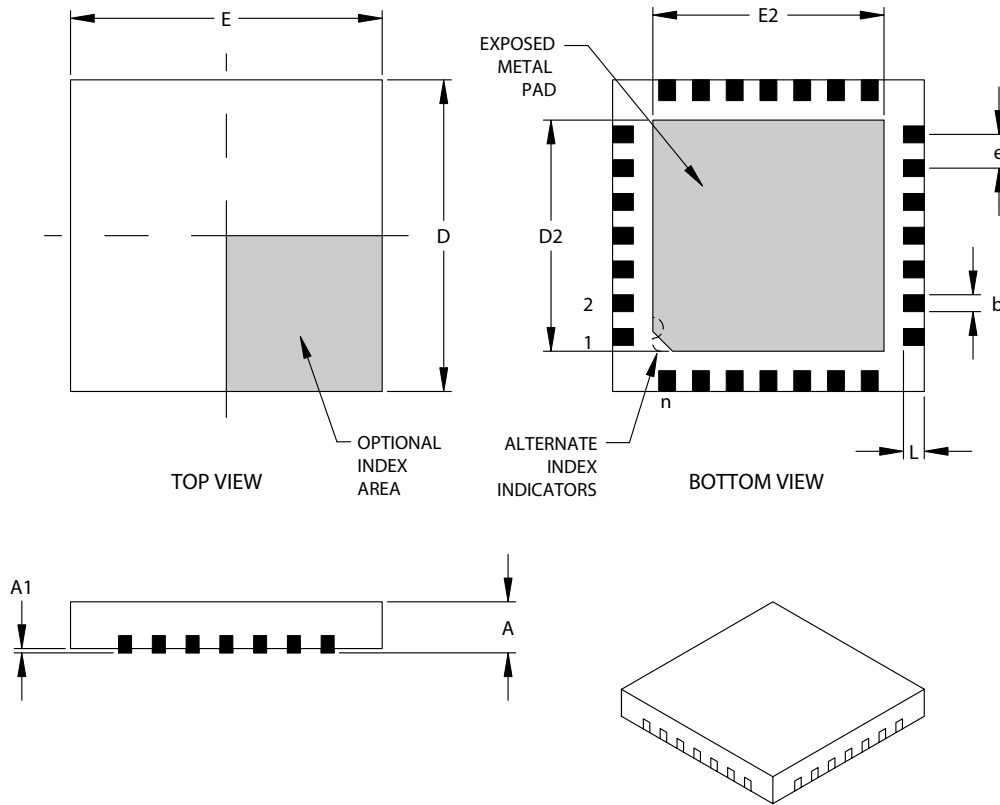
Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	e		.026 BSC			0.65 BSC	
Overall Height	A	.031	.035	.039	0.80	0.90	1.00
Standoff	A1	.000	.001	.002	0.00	0.02	0.05
Overall Width	E	.232	.236	.240	5.90	6.00	6.10
Exposed Pad Width	E2	.169	.175	.177	4.30	4.45	4.50
Overall Length	D	.232	.236	.240	5.90	6.00	6.10
Exposed Pad Length	D2	.169	.175	.177	4.30	4.45	4.50
Lead Width	b	.013	.015	.017	0.33	0.38	0.43
Lead Length	L	.012	.016	.020	0.30	0.40	0.50

*Controlling Parameter

Notes:
   JEDEC equivalent: MO-220

Drawing No. C04-124   Revised 05/24/04

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REVISION HISTORY

<u>Rev A Document (06/2005)</u>
First revision of this document. Data Sheet Clarification issues 1 (Power-on Reset), 2 (Watchdog Timer), 3 (PWM Equations), 4 (DC Characteristics), 5 (LVD Characteristics), and 6 (28-Pin QFN Diagram).

NOTES:

Note the following details of the code protection feature on Microchip devices:

• Microchip products meet the specification contained in their particular Microchip Data Sheet.

• Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.

• There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.

• Microchip is willing to work with the customer who is concerned about the integrity of their code.

• Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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