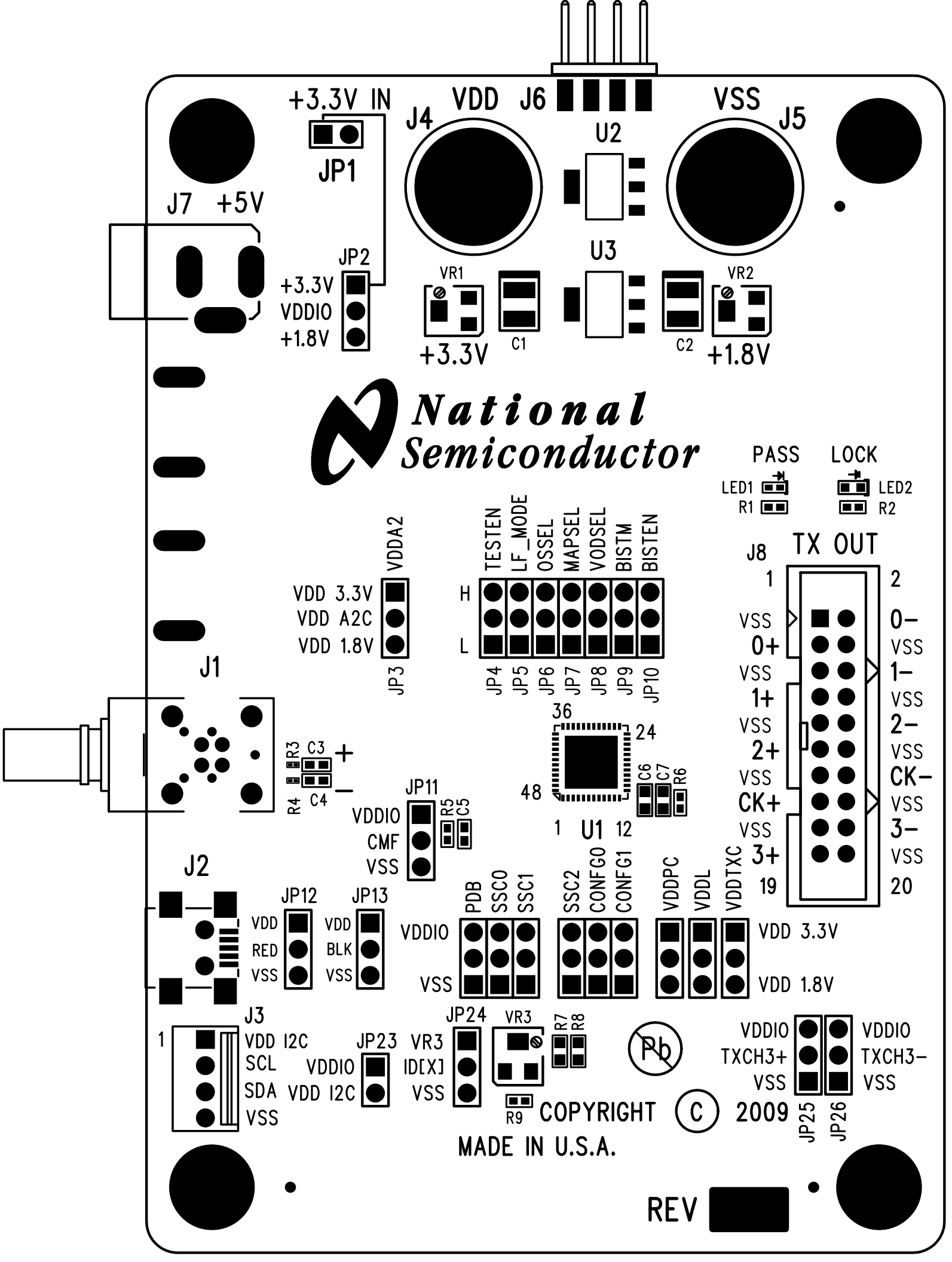
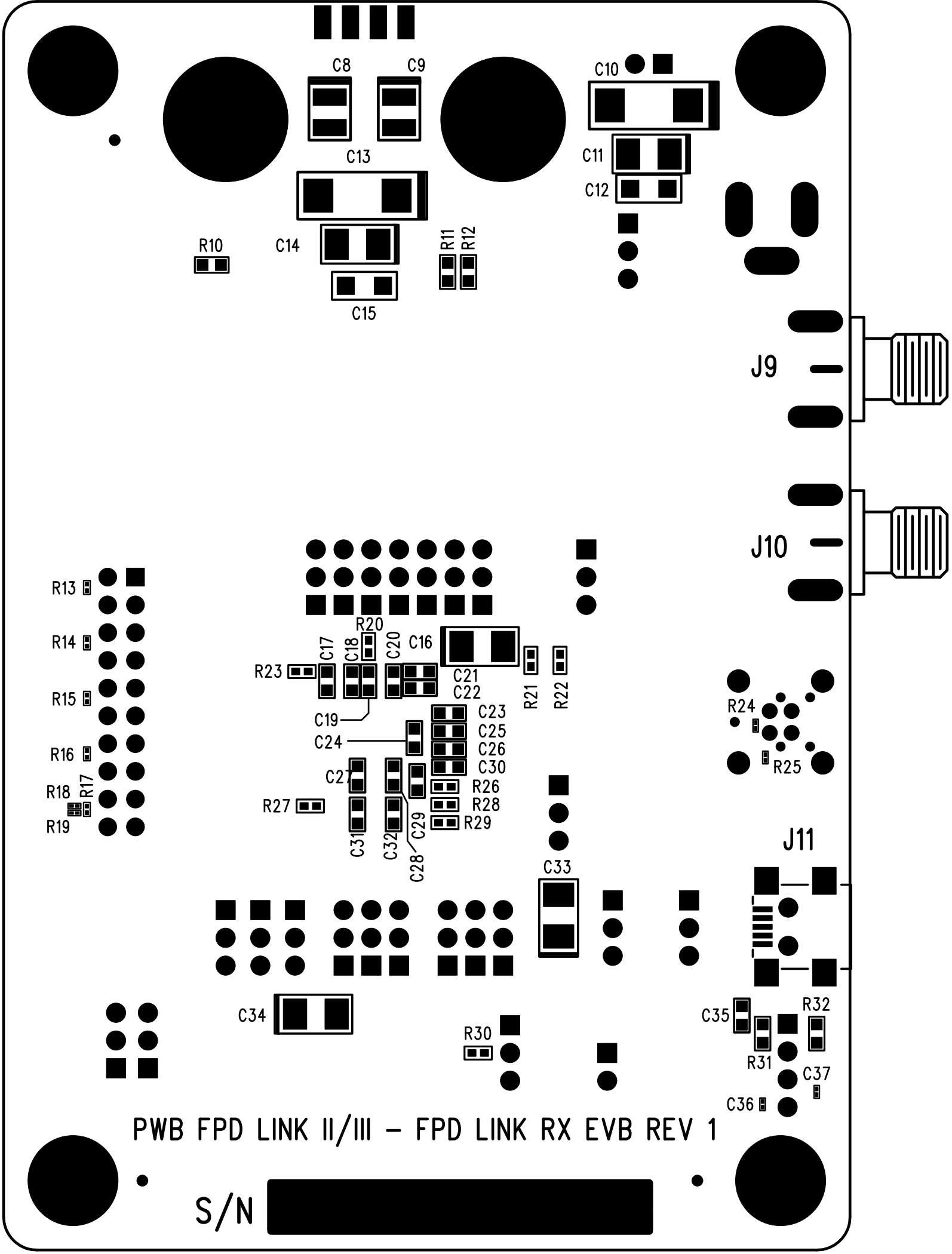
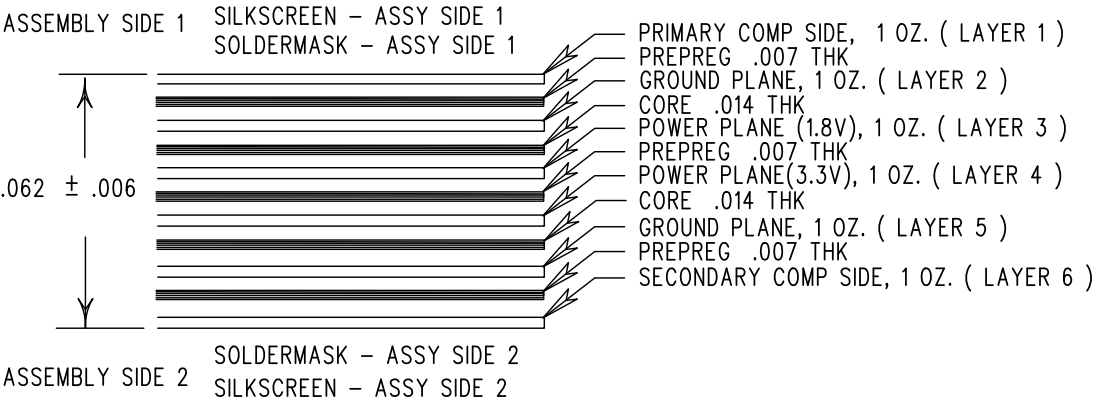
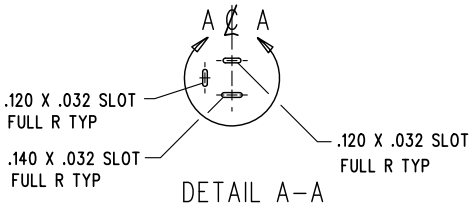

+3.3V IN
JP1
VDD
J4
J6
VSS
J5
U2
U3
J7 +5V
JP2
+3.3V
VDDIO
+1.8V
VR1
C1
+3.3V
C2
VR2
+1.8V
National
Semiconductor
PASS
LOCK
LED1
R1
LED2
R2
VDDA2
VDD 3.3V
VDD A2C
VDD 1.8V
JP3
TESTEN
LF_MODE
OSSEL
MAPSEL
VODSEL
BISTM
BISTEN
H
L
JP4
JP5
JP6
JP7
JP8
JP9
JP10
J8
TX OUT
J1
R3
C3
+
R4
C4
–
36
24
48
1
U1
12
C6
C7
R6
JP11
VDDIO
CMF
VSS
R5
C5
J2
JP12
JP13
VDD
RED
VSS
VDD
BLK
VSS
PDB
SSC0
SSC1
SSC2
CONFG0
CONFG1
VDDPC
VDDL
VDDTXC
VDDIO
VSS
VDD 3.3V
VDD 1.8V
J3
1
VDD I2C
SCL
SDA
VSS
JP23
VDDIO
VDD I2C
JP24
VR3
ID[X]
VSS
VR3
R7
R8
R9
Pb
VDDIO
TXCH3+
VSS
VDDIO
TXCH3–
VSS
JP25
JP26
COPYRIGHT
C
2009
MADE IN U.S.A.
REV


C8
C9
C10
C11
C12
C13
C14
C15
R10
R11
R12
J9
J10
R13
R14
R15
R16
R17
R18
R19
R20
C16
C17
C18
C19
C20
C21
C22
C23
C24
C25
C26
C27
C28
C29
C30
C31
C32
R21
R22
R23
R24
R25
R26
R27
R28
R29
C33
J11
C34
C35
R30
R31
R32
C36
C37
PWB FPD LINK II/III – FPD LINK RX EVB REV 1
S/N



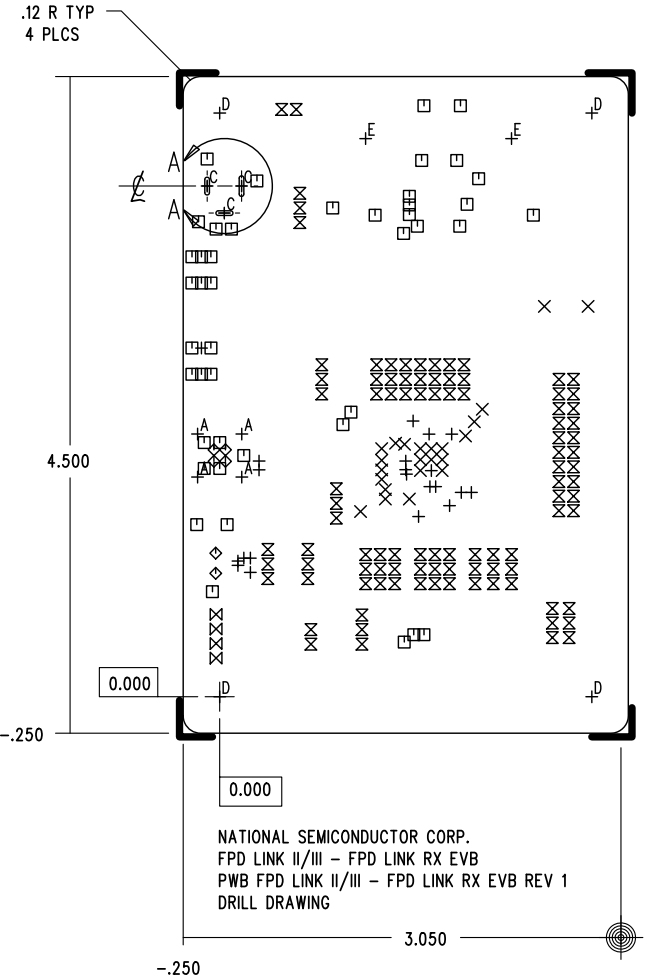
HOLE CHART				
CODE	SIZE	QTY	PLATED	TOL
+	0.006	21	YES	± .003
×	0.010	23	YES	± .003
□	0.016	44	YES	± .003
◇	0.036	6	YES	± .003
⧖	0.040	96	YES	± .003
⋈	0.043	4	YES	± .003
A	0.065	4	YES	± .003
B	—	—		
C	0.032	3	YES	± .003
D	0.156	4	YES	± .004
E	0.265	2	YES	± .005

THRU HOLE SLOT – SEE DETAIL A–A



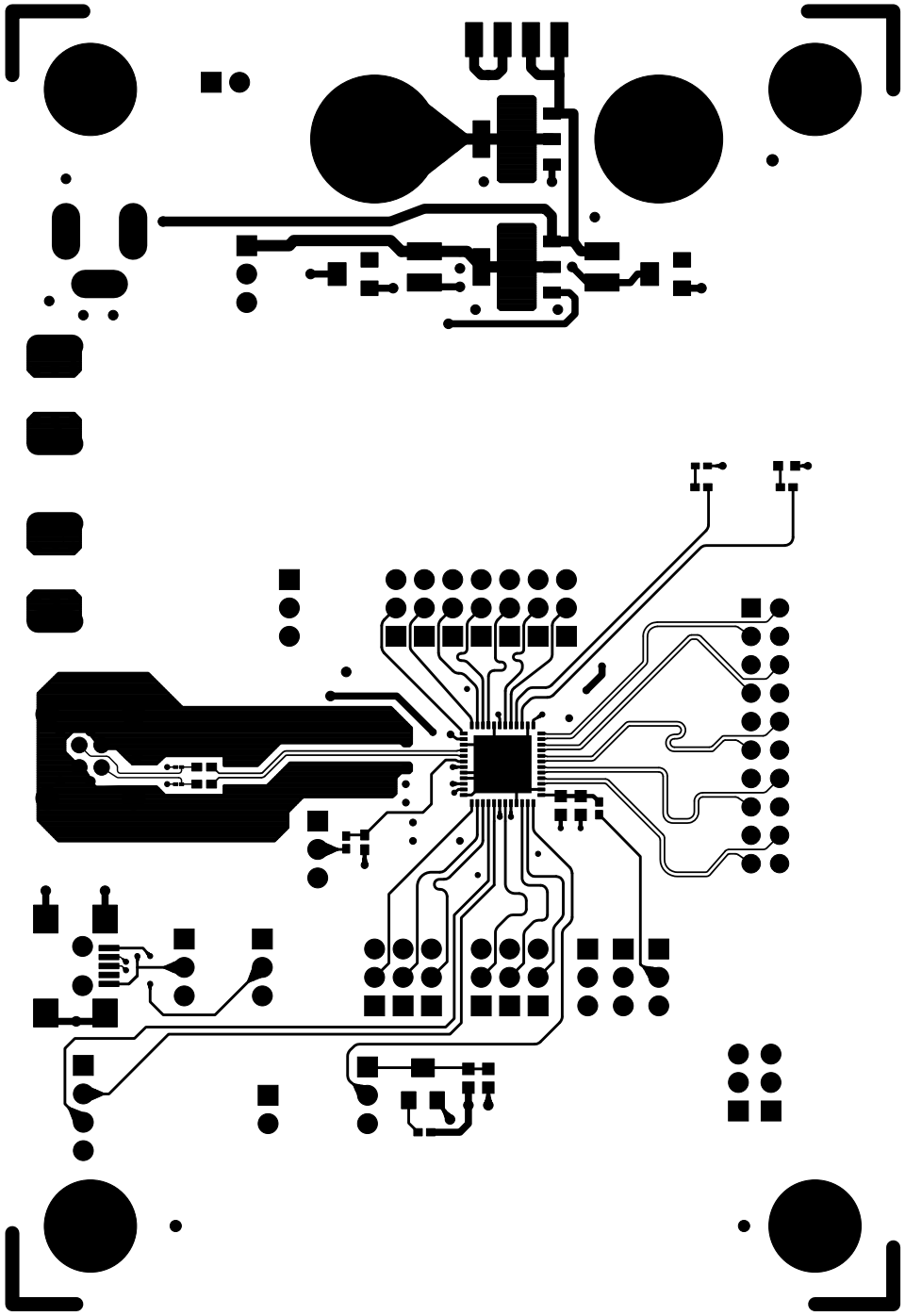
DETAIL A–A

SCALE 1:1 ROT 90° CW
NOTE: .032 DRILL AT SLOT CENTER
PER NC DRILL FILE

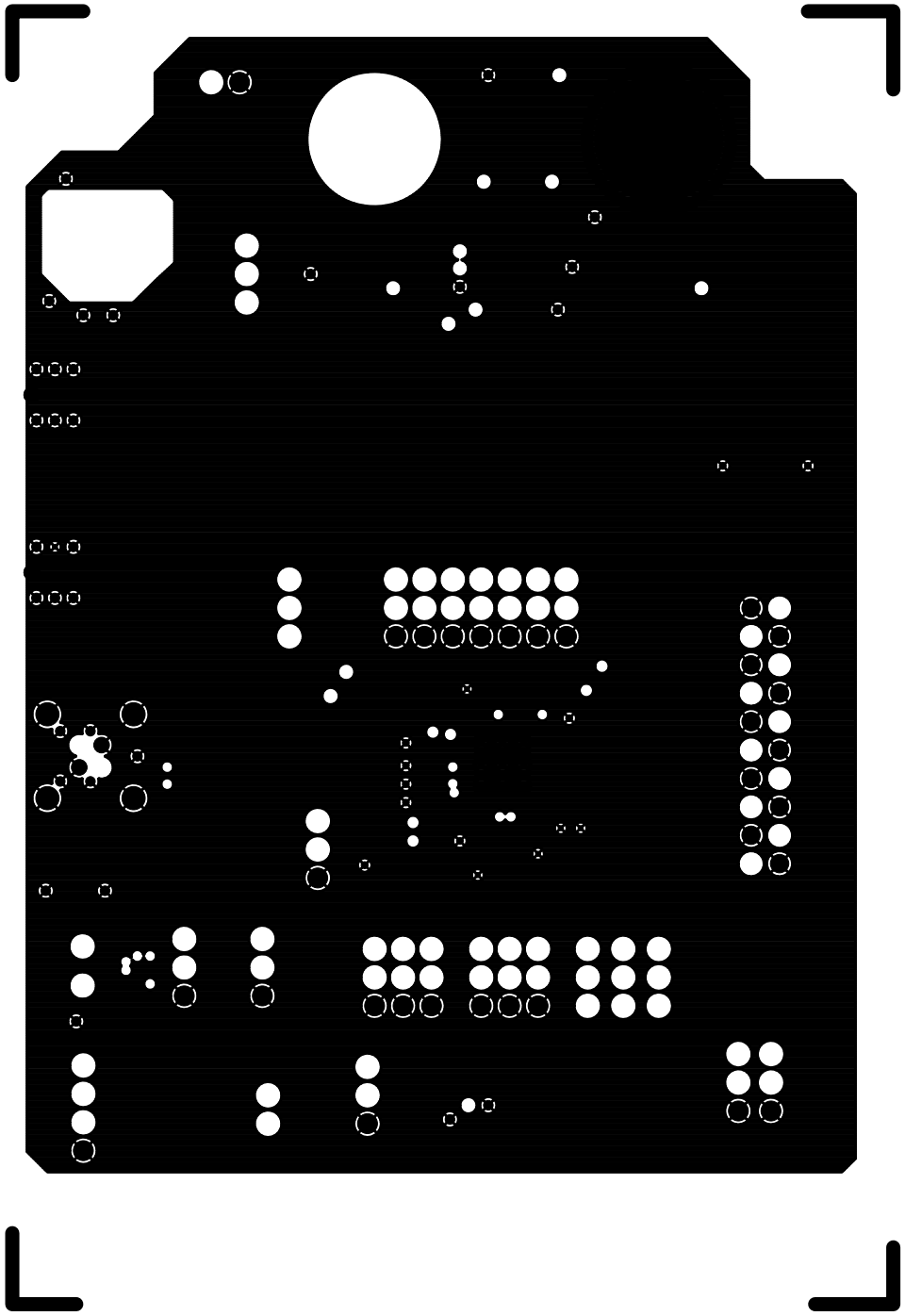


NOTES: UNLESS OTHERWISE SPECIFIED

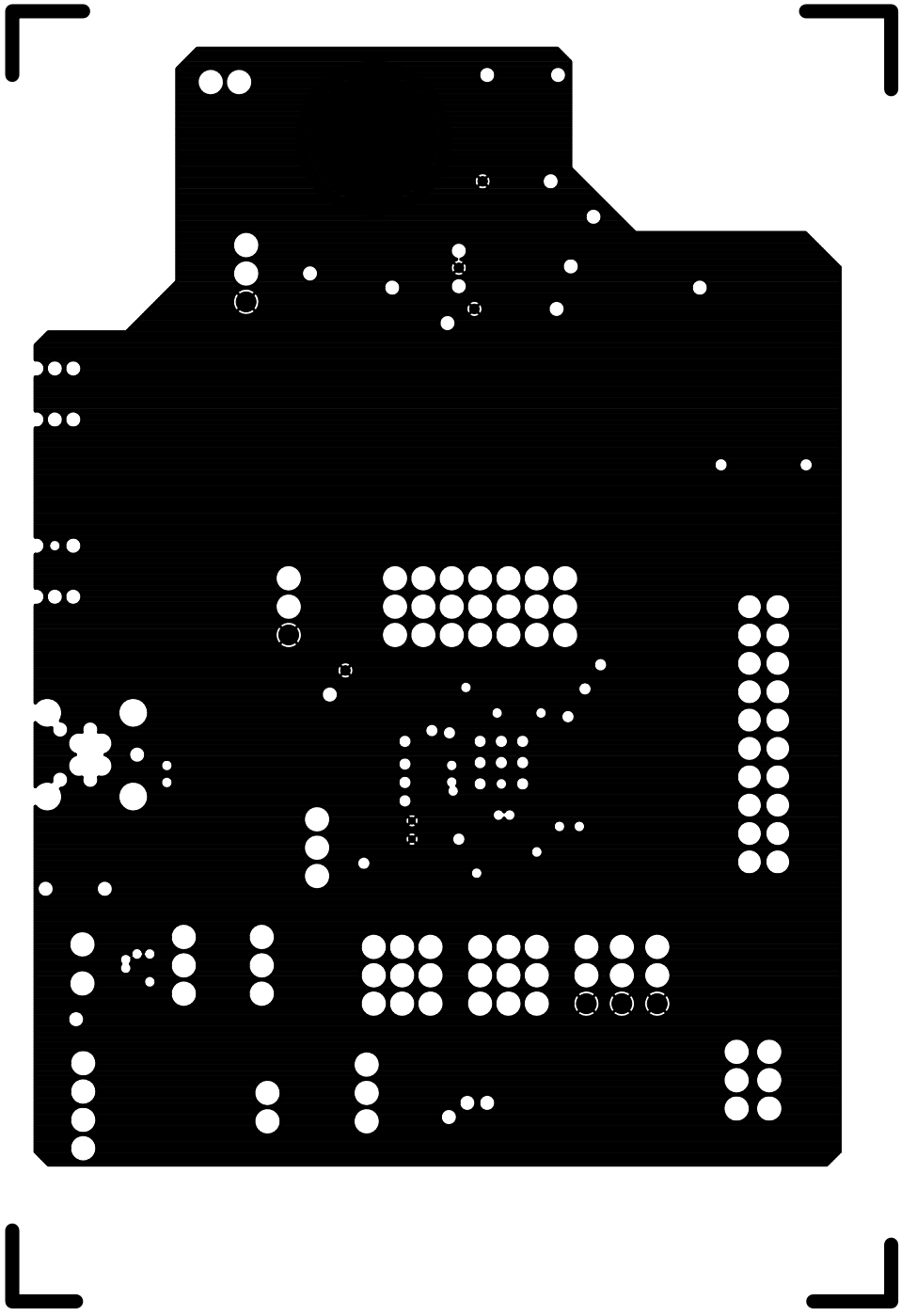
1. PRIMARY COMPONENT SIDE IS SHOWN.
2. DELETED.
3. FABRICATE USING MASTER FILM FPD LINK II/III – FPD LINK RX EVB REV 1. USE GERBER FILE A679BOA.PHO FOR BOARD ROUTE.
4. ACCEPTABILITY SHALL BE BASED ON IPC–A–600, CLASS 2
5. MATERIAL: BASE MATERIAL IS ISOLA 410 OR FR–370HR, COLOR GREEN, 0.050 INCH NOM. THICKNESS. COPPER CLADDING SHALL BE 1 OZ.
6. PLATING: ALL HOLES AND CONDUCTIVE SURFACES SHALL BE PLATED WITH A MIN. OF .001 INCH COPPER. EXPOSED PADS / TRACES SHALL BE PLATED .000030 MIN GOLD OVER NICKEL, .000150 MIN.
7. FABRICATION TOLERANCES:
   END PRODUCT CONDUCTOR WIDTHS AND LAND DIAMETERS SHALL NOT VARY MORE THAN .002 INCH FROM THE 1:1 DIMENSIONS OF THE MASTER PATTERN. THE CONDUCTIVE PATTERN SHALL BE POSITIONED SO THAT THE LOCATION OF ANY LAND SHALL BE WITHIN .010 INCH DIAMETER TO THE TRUE POSITION OF THE HOLE IT CIRCUMSCRIBES THE MINIMUM ANNULAR RING SHALL BE .002 INCH. BOW AND TWIST SHALL NOT EXCEED .010 INCH PER INCH.
8. SOLDERMASK BOTH SIDES PER IPC–SM–840, TYPE A, CLASS B. COLOR–GREEN. THERE SHALL BE NO SOLDERMASK ON ANY LAND.
9. SILKSCREEN THE LEGEND ON BOTH SIDES USING NON CONDUCTIVE EPOXY INK, COLOR–WHITE. THERE SHALL BE NO INK ON ANY LAND.
10. THE .00975 TRACES (LAYER 1 & 6) TO BE 50 OHM SINGLE ENDED AND THE .00575 TRACES (LAYER 1 & 6) TO BE 100 OHM DIFFERENTIAL IMPEDANCE AND THE DIELECTRIC REFERENCED IN BOARD STACK DETAIL IS SUGGESTED. HOWEVER, TRACE WIDTHS AND OR DIELECTRIC THICKNESS MAY BE MICRO–MODIFIED IN ORDER TO FABRICATE BOARDS TO THE REQUIRED IMPEDANCE NOMINALS TO A TOLERANCE OF +/– 10%.
11. PCB MUST BE MADE OF US RECOGNIZED MATERIAL AND TRACEABLE FOR 94V–0 MINIMUM FLAMMABILITY RATING AND MANUFACTURED BY A UL RECOGNIZED PRINTED CIRCUIT BOARD SUPPLIER. PCB MUST BE PERMANENTLY MARKED WITH UL RECOGNIZED MANUFACTURER'S LOGO AND TYPE CODE AS DESIGNATED IN THE UL RECOGNIZED DIRECTORY.



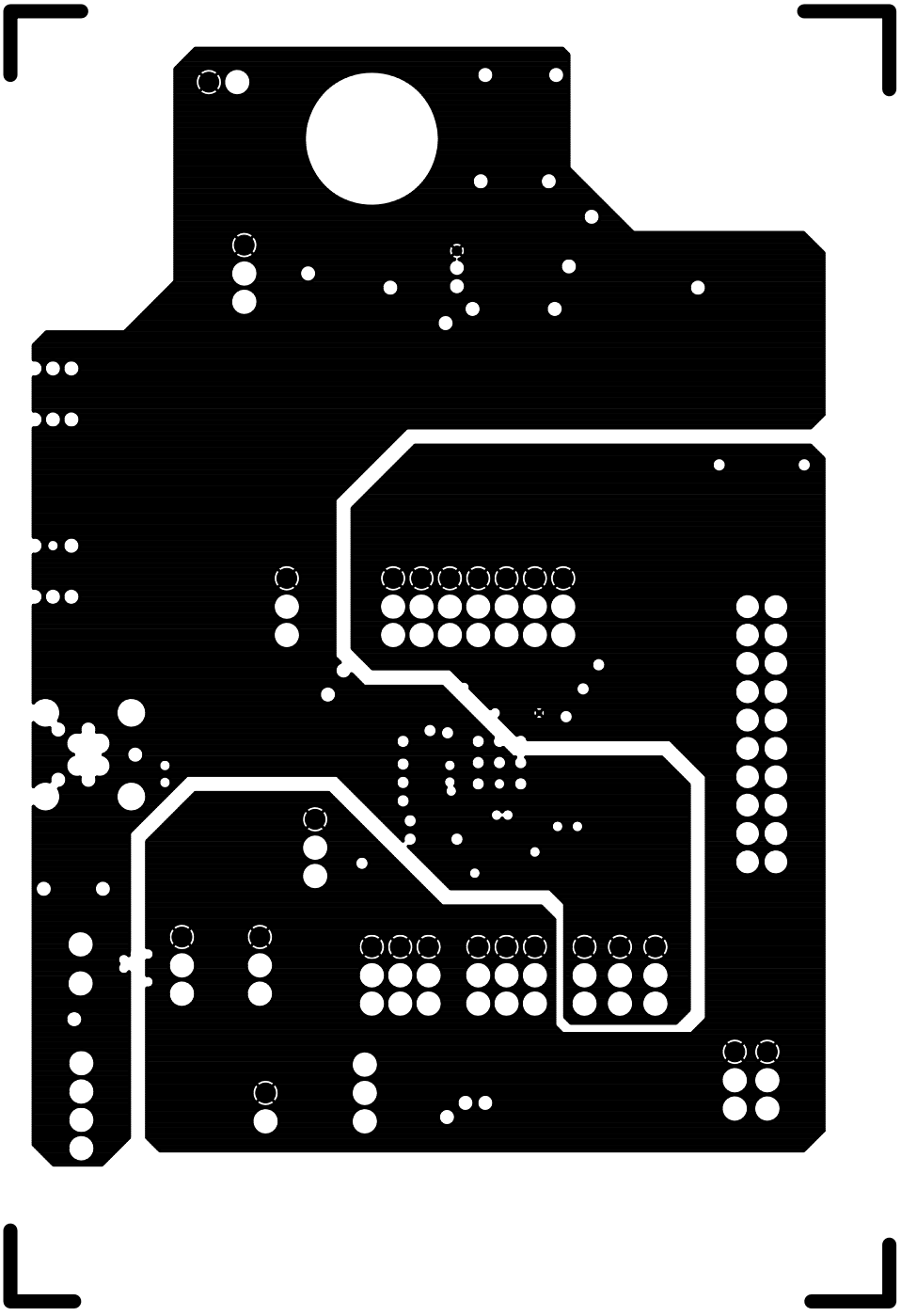
NATIONAL SEMICONDUCTOR CORP.
FPD LINK II/III – FPD LINK RX EVB
PWB FPD LINK II/III – FPD LINK RX EVB REV 1
PRIMARY COMP SIDE – LAYER 1



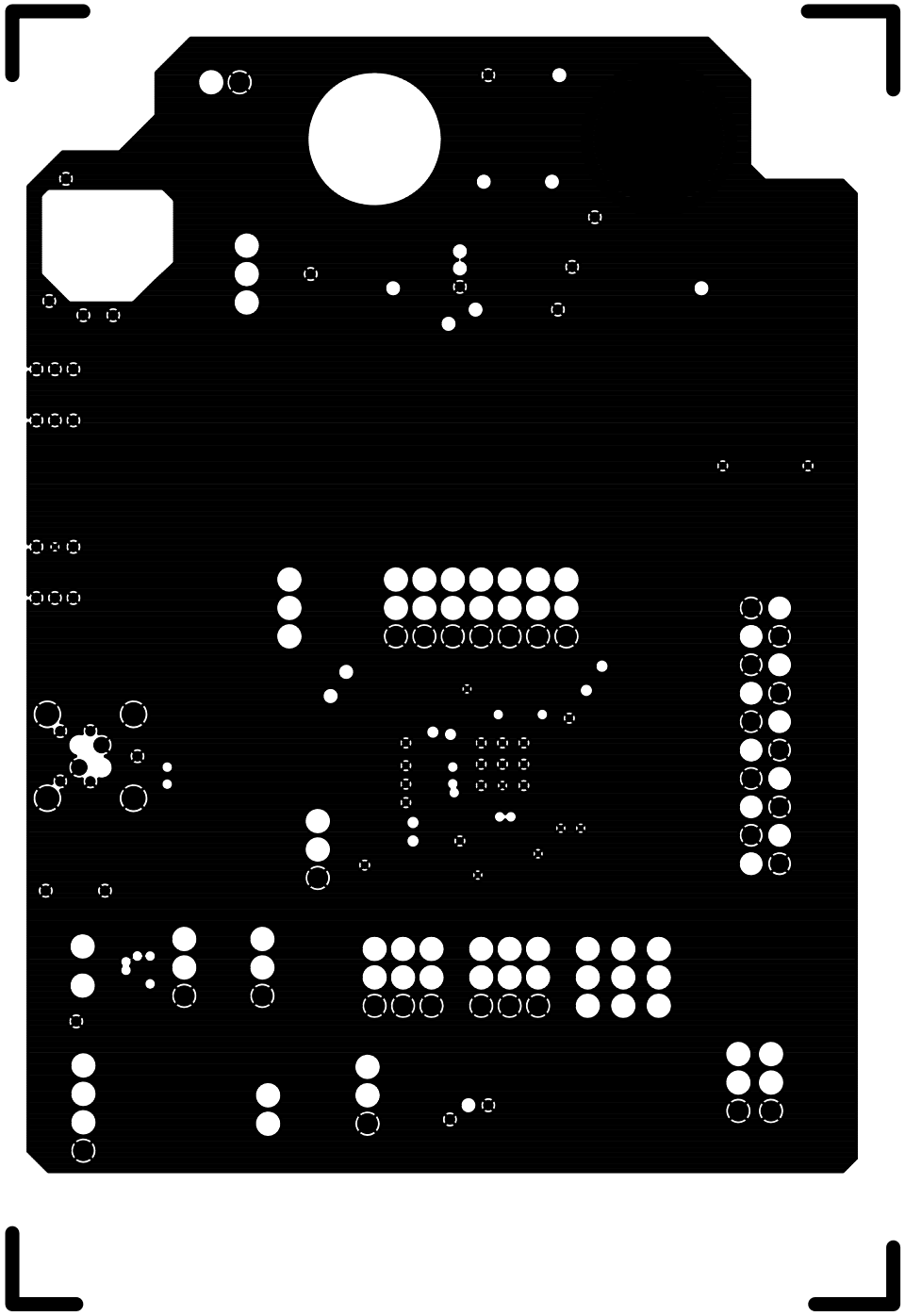
NATIONAL SEMICONDUCTOR CORP.
FPD LINK II/III – FPD LINK RX EVB
PWB FPD LINK II/III – FPD LINK RX EVB REV 1
GROUND PLANE – LAYER 2



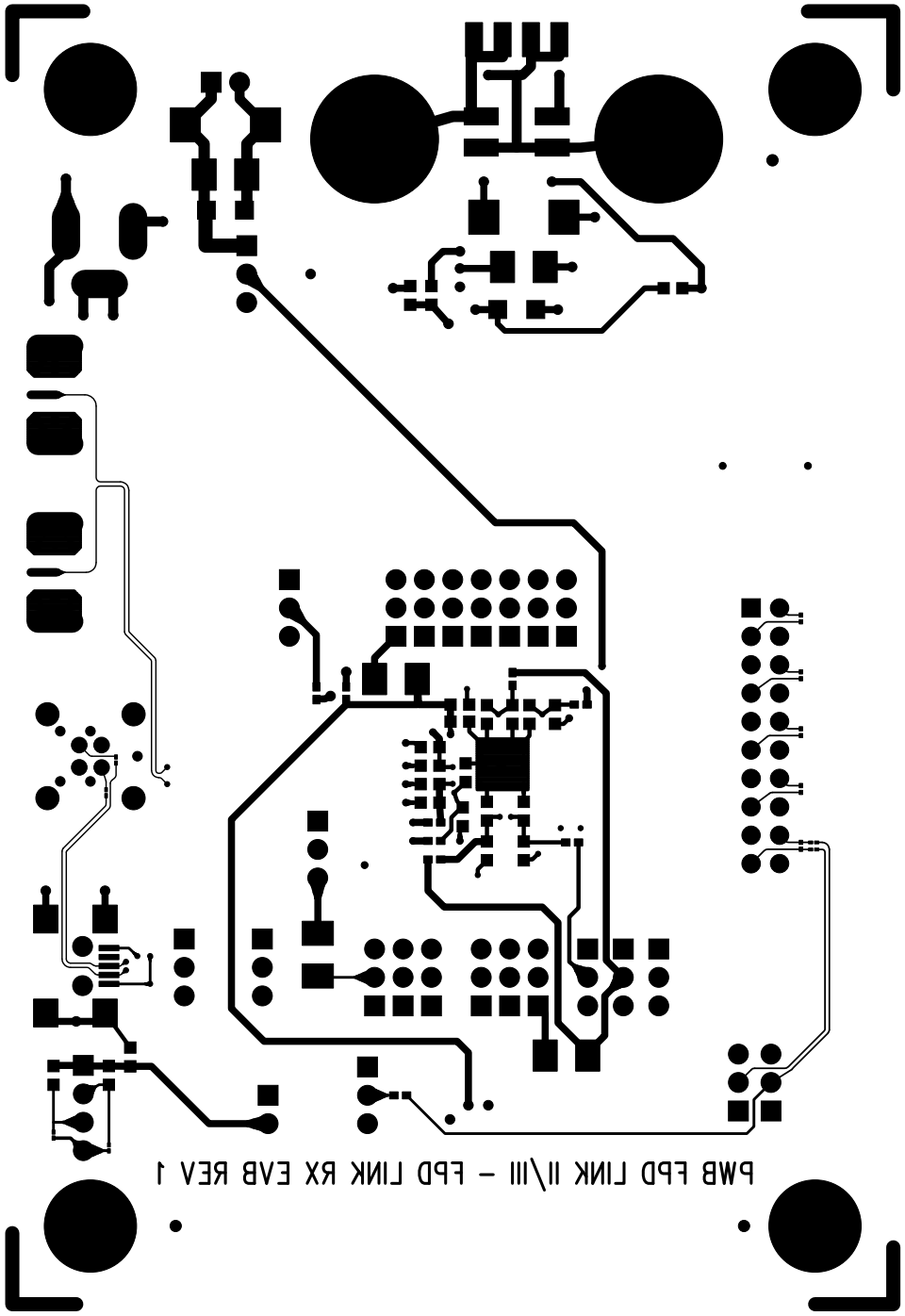
NATIONAL SEMICONDUCTOR CORP.
FPD LINK II/III – FPD LINK RX EVB
PWB FPD LINK II/III – FPD LINK RX EVB REV 1
POWER PLANE (1.8V) – LAYER 3



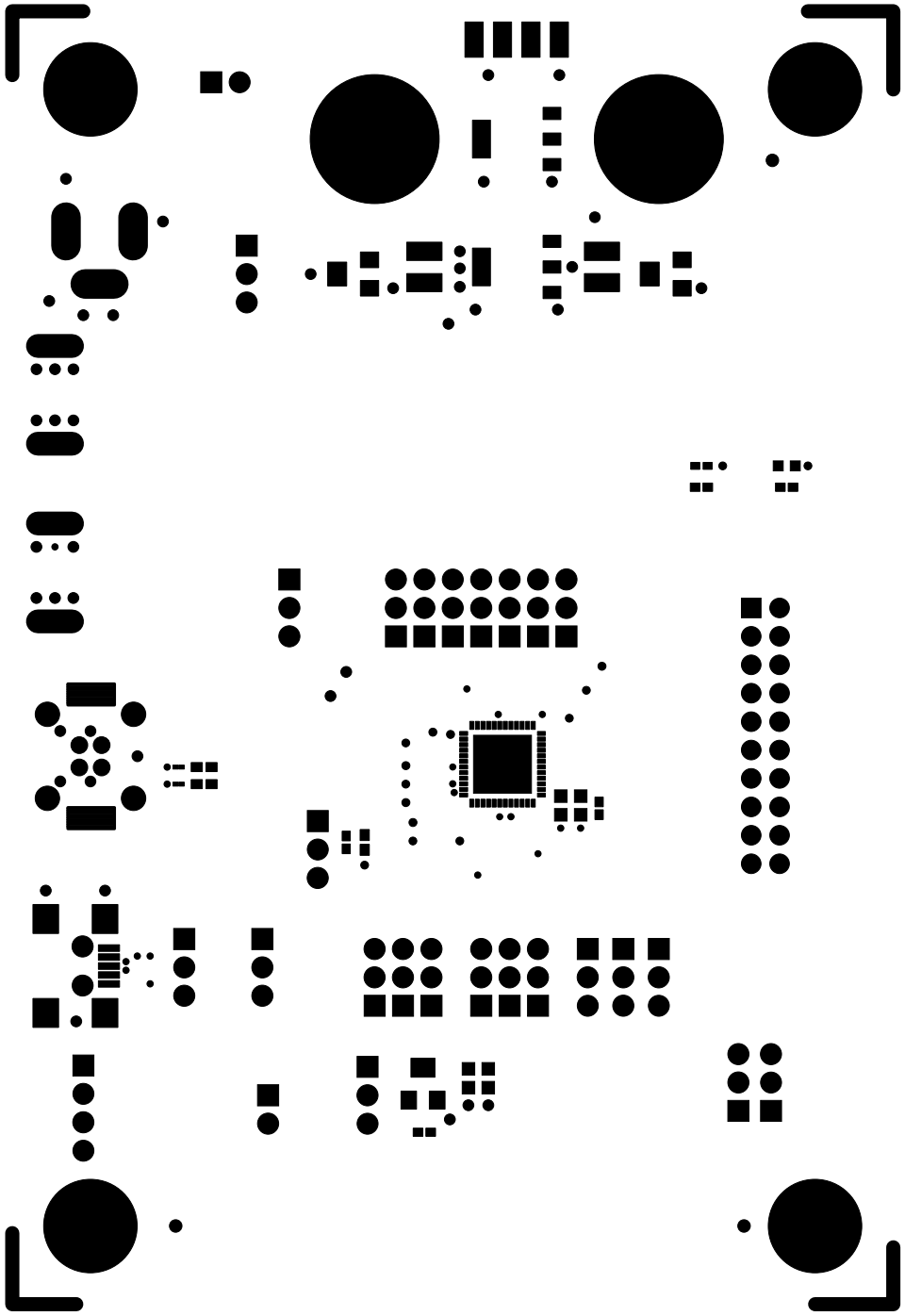
NATIONAL SEMICONDUCTOR CORP.
FPD LINK II/III – FPD LINK RX EVB
PWB FPD LINK II/III – FPD LINK RX EVB REV 1
POWER PLANE (3.3V) – LAYER 4



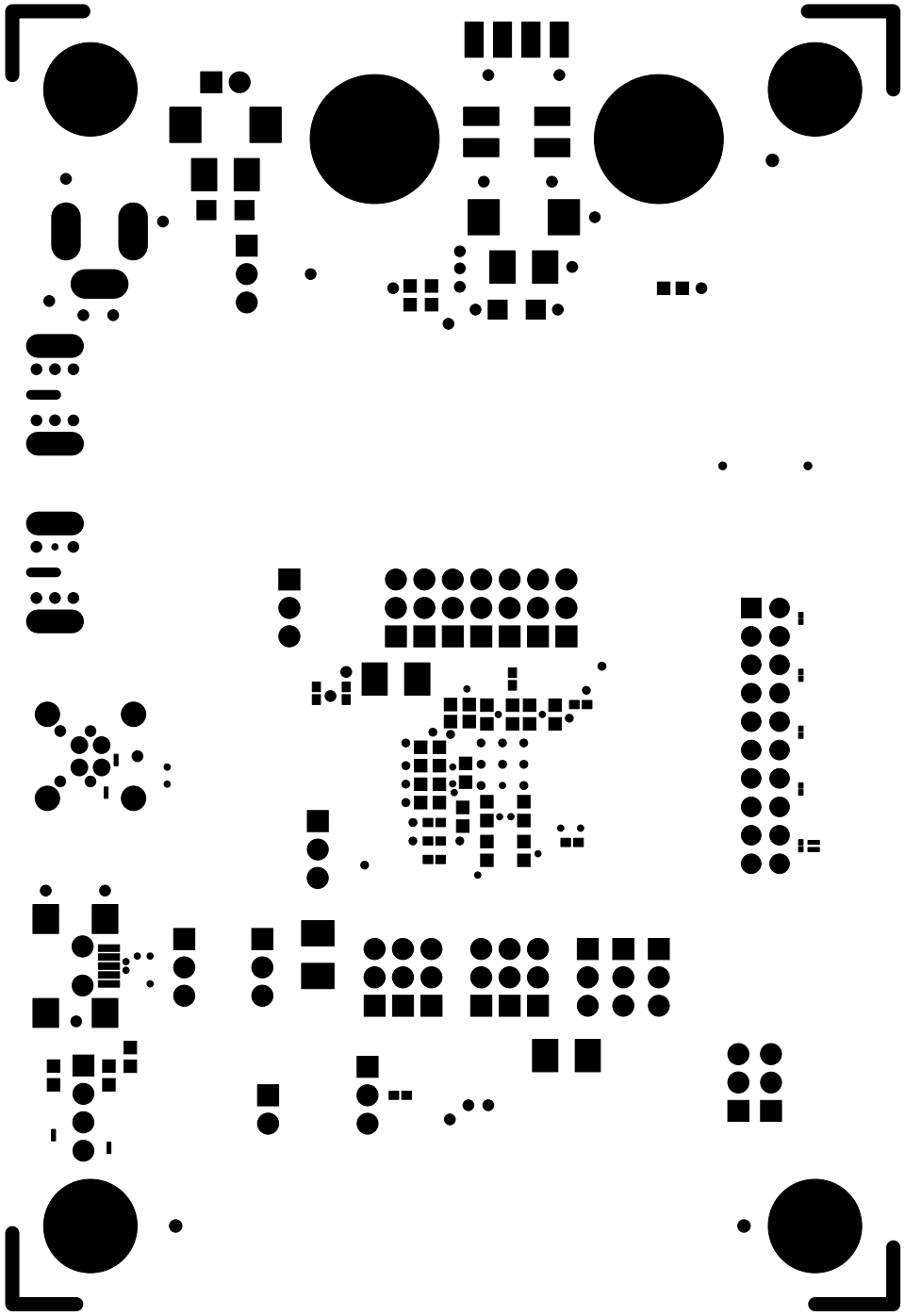
NATIONAL SEMICONDUCTOR CORP.
FPD LINK II/III – FPD LINK RX EVB
PWB FPD LINK II/III – FPD LINK RX EVB REV 1
GROUND PLANE – LAYER 5



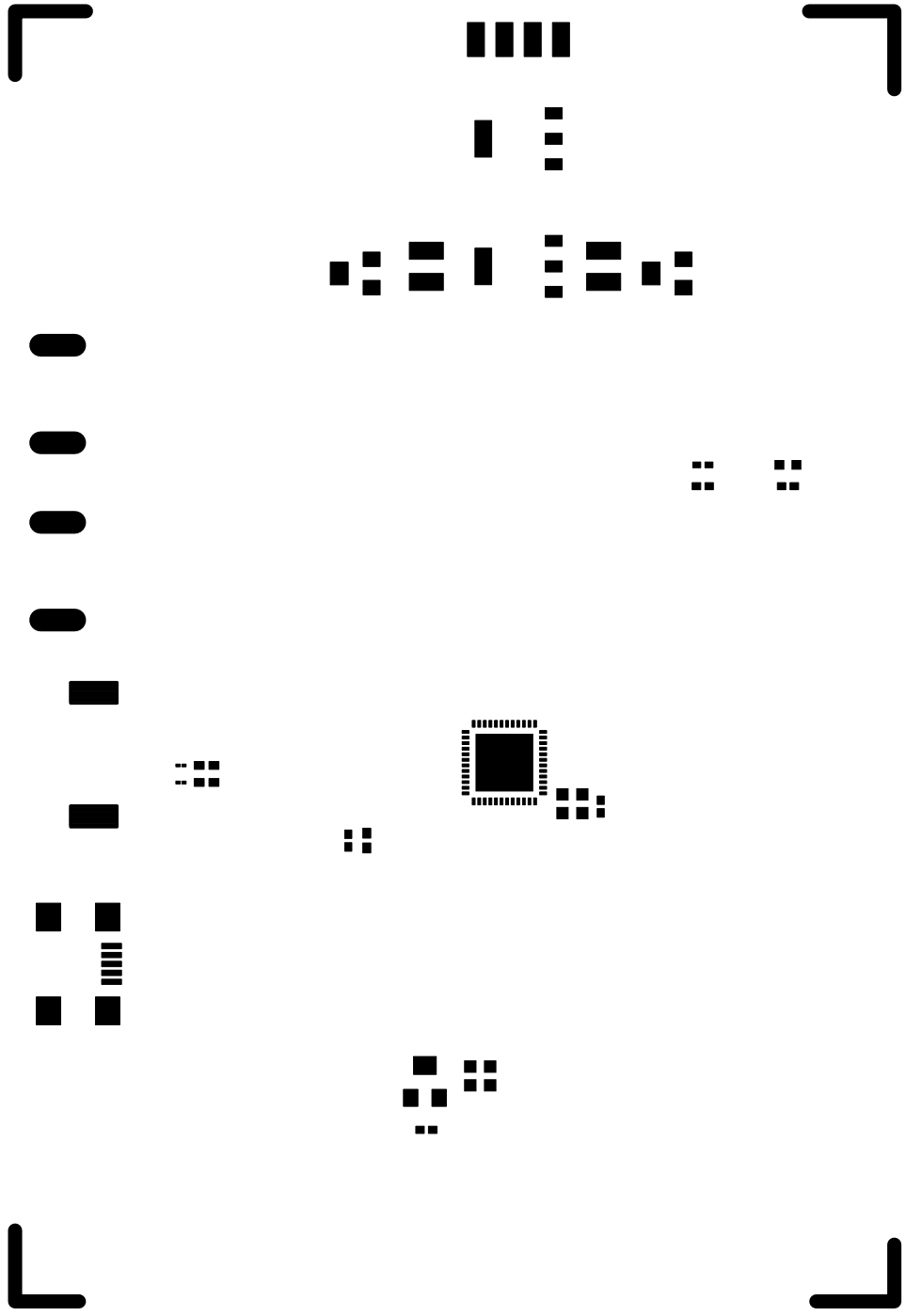
NATIONAL SEMICONDUCTOR CORP.
FPD LINK II/III – FPD LINK RX EVB
PWB FPD LINK II/III – FPD LINK RX EVB REV 1
SECONDARY COMP SIDE – LAYER 4



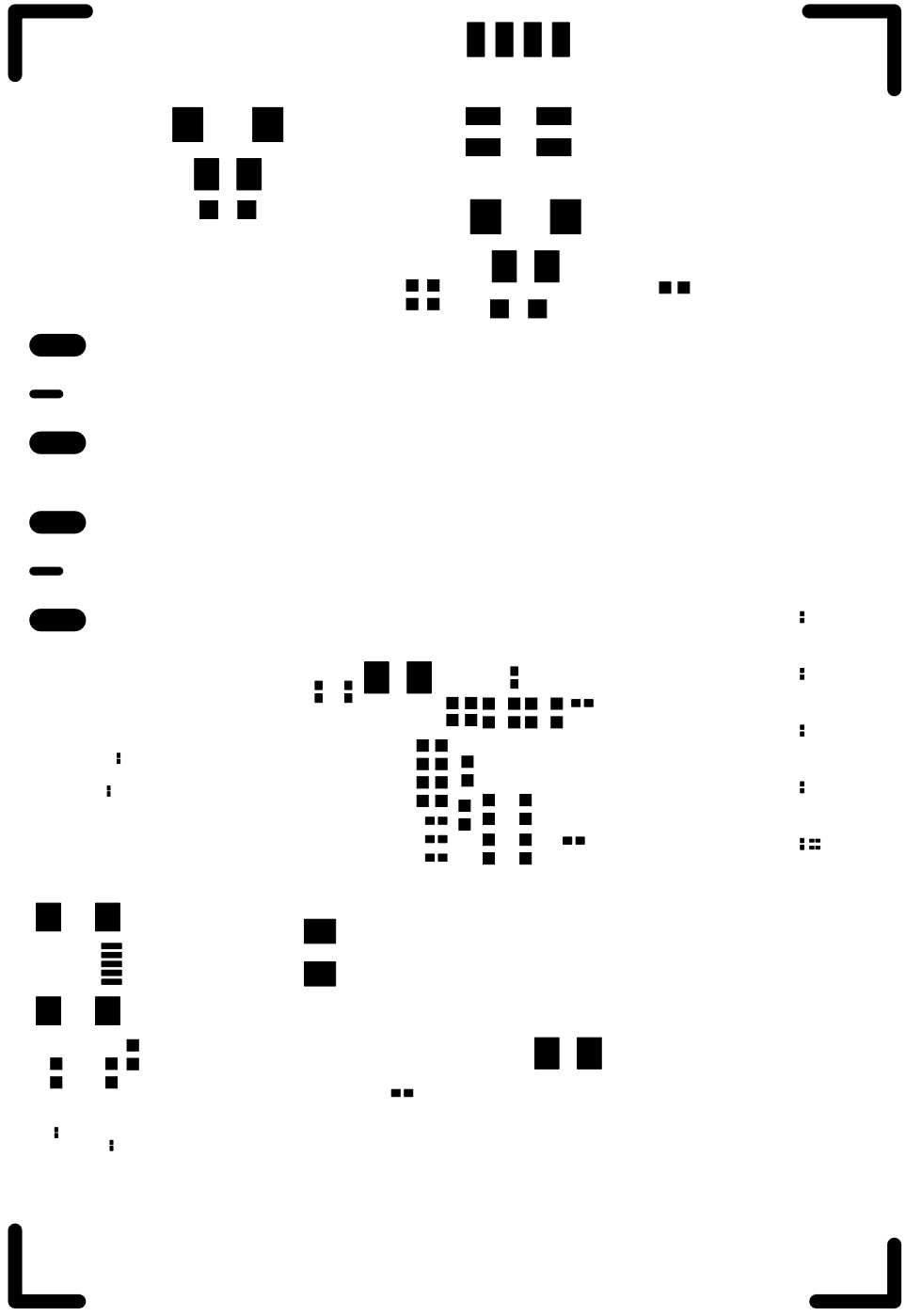
NATIONAL SEMICONDUCTOR CORP.
FPD LINK II/III – FPD LINK RX EVB
PWB FPD LINK II/III – FPD LINK RX EVB REV 1
PRIMARY COMP SIDE – SOLDER MASK (LAYER 1)



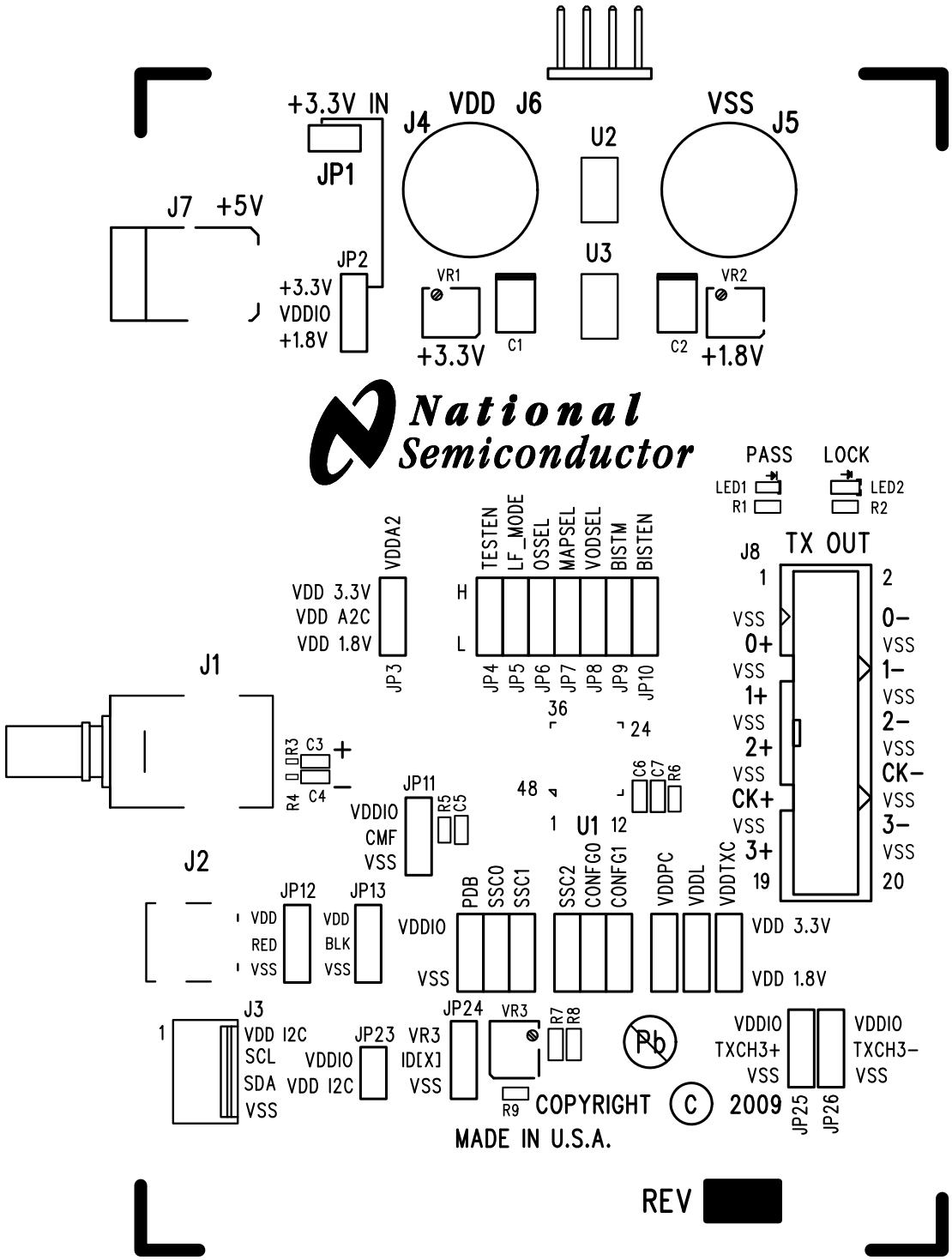
NATIONAL SEMICONDUCTOR CORP.
FPD LINK II/III – FPD LINK RX EVB
PWB FPD LINK II/III – FPD LINK RX EVB REV 1
SECONDARY COMP SIDE – SOLDER MASK (LAYER 4)



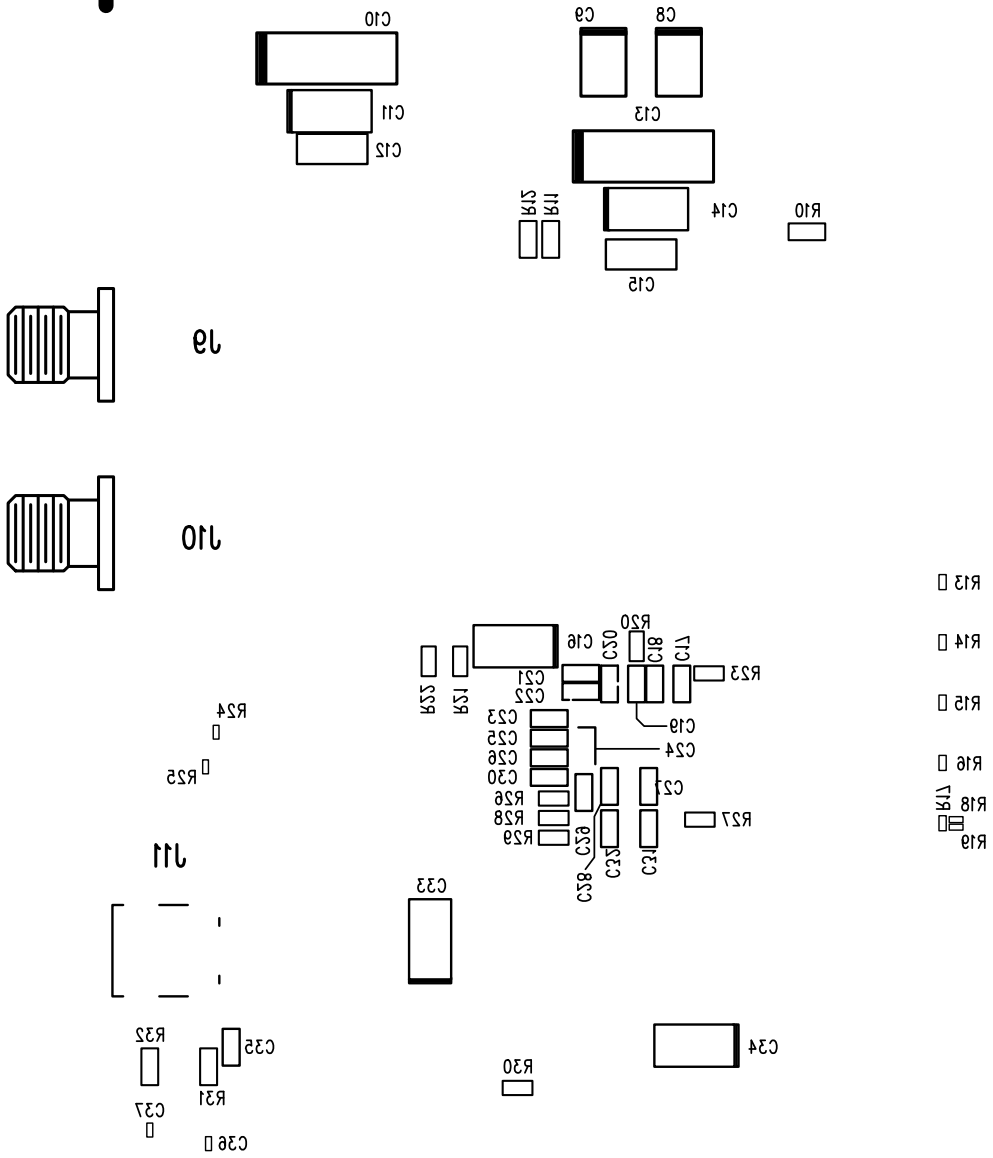
NATIONAL SEMICONDUCTOR CORP.
FPD LINK II/III – FPD LINK RX EVB
PWB FPD LINK II/III – FPD LINK RX EVB REV 1
PRIMARY COMP SIDE – SOLDER PASTE MASK



NATIONAL SEMICONDUCTOR CORP.
FPD LINK II/III – FPD LINK RX EVB
PWB FPD LINK II/III – FPD LINK RX EVB REV 1
SECONDARY COMP SIDE – SOLDER PASTE MASK



NATIONAL SEMICONDUCTOR CORP.
FPD LINK II/III – FPD LINK RX EVB
PWB FPD LINK II/III – FPD LINK RX EVB REV 1
PRIMARY COMP SIDE – SILKSCREEN (LAYER 1)



NATIONAL SEMICONDUCTOR CORP.
FPD LINK II/III – FPD LINK RX EVB
PWB FPD LINK II/III – FPD LINK RX EVB REV 1
SECONDARY COMP SIDE – SILKSCREEN (LAYER 4)