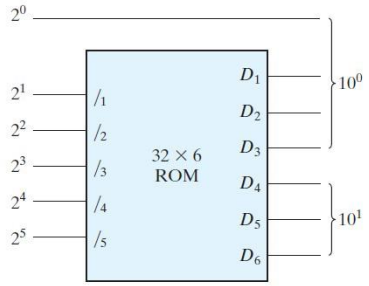
EE2001-Tutorial 9
Date: 10th April 2018
Memory and Programmable Logic

1) (a) Using 64 × 8 ROM chips with an enable input, construct a 512 × 8 ROM with eight chips and a decoder.
(b) A ROM chip of 4,096 × 8 bits has two chip select inputs and operates from a 5-V power supply. How many pins are needed for the integrated circuit package? Draw a block diagram, and label all input and output terminals in the ROM.

2) The 32 × 6 ROM, together with the 2^0 line, as shown, converts a six-bit binary number to its corresponding two-digit BCD number. For example, binary 100001 converts to BCD number 011 0011 (decimal 33). Specify the truth table for the ROM.



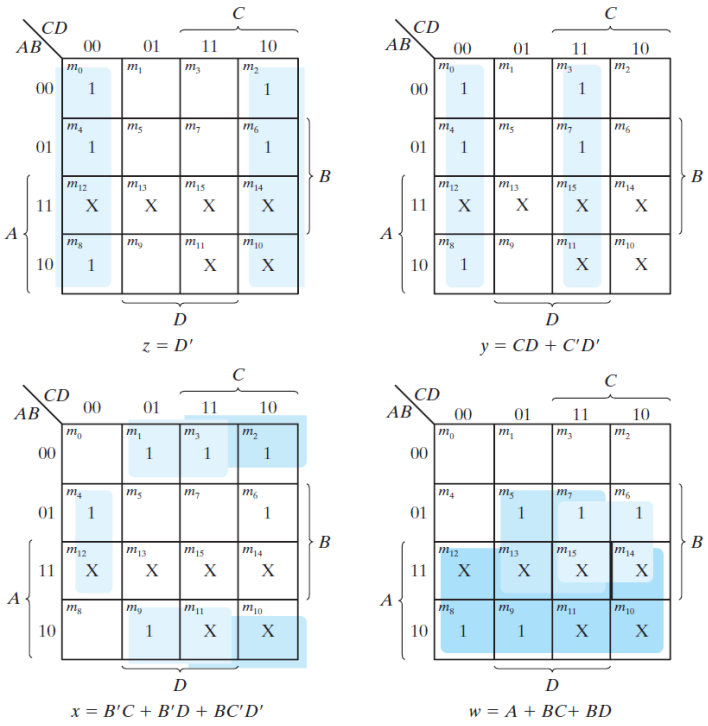
3) Specify the size of a ROM (number of words and number of bits per word) that will accommodate the truth table for the following combinational circuit components:
(a) a binary multiplier that multiplies two 4-bit binary words,
(b) a 4-bit adder–subtractor,
(c) a quadruple two-to-one-line multiplexer with common select and enable inputs, and
(d) a BCD-to-seven-segment decoder with an enable input.

4) Tabulate the PLA programming table for the four Boolean functions listed below. Minimize the numbers of product terms.
(a) A(x, y, z) = Σ(1, 3, 5, 6)
(b) B(x, y, z) = Σ(0, 1, 6, 7)
(c) C(x, y, z) = Σ(3, 5)
(d) D(x, y, z) = Σ(1, 2, 4, 5, 7)

5) Tabulate the truth table for an 8 × 4 ROM that implements the following Boolean functions:
(a) A(x, y, z) = Σ(0, 3, 4, 6)
(b) B(x, y, z) = Σ(0, 1, 4, 7)
(c) C(x, y, z) = Σ(1, 5)
(d) D(x, y, z) = Σ(0, 1, 3, 5, 7)
Considering now the ROM as a memory. Specify the memory contents at addresses 1 and 4.

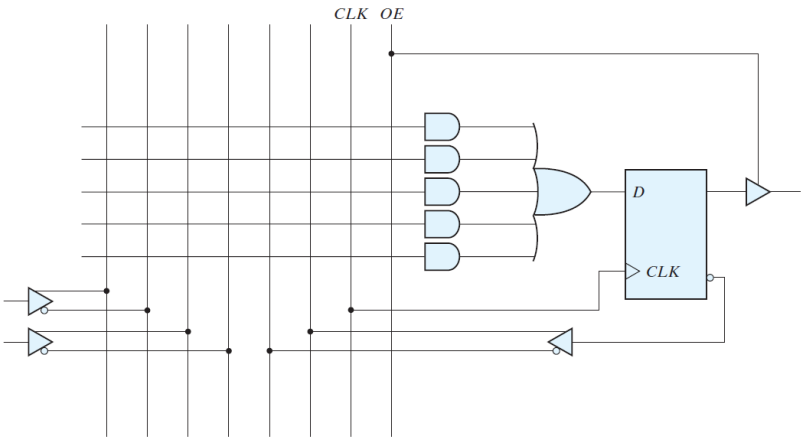
6) (a) Derive the PLA programming table for the combinational circuit that squares a three-bit number. Minimize the number of product terms.
(b) Derive the ROM programming table for the combinational circuit that squares a 4-bit number. Minimize the number of product terms.

7) List the (a) PLA and (b) PAL programming tables for the BCD to excess-3 code converter whose Boolean functions are simplified as shown.



8) Draw a PLA circuit to implement the functions
(a) F1 = A'B + AC + A'BC'
(b) F2 = (AC + AB + BC)'

9) Using the given registered macrocell, show the fuse map for a sequential circuit with two inputs x and y and one flip-flop A described by the input equation
D_A = x XOR y XOR A



10) Modify the given PAL diagram by including three clocked D-type flip-flops between the OR gates and the outputs (as in a registered macrocell). The diagram should conform with the block diagram of a sequential circuit. The modification will require three additional buffer–inverter gates and six vertical lines for the flip-flop outputs to be connected to the AND array through programmable connections.

Using the modified registered PAL diagram, show the fuse map that will implement a three-bit binary counter with an output carry.