EE2016 Microprocessors Theory and Lab

Tutorial 2 (Classes on 5, 6 & 9th of Aug. 2019)

July-Nov 2018, EE Dept, IIT Madras.

1 Fill in the blanks

1. What is the difference between ROTATE right, shift-right and arthmetic shift right? Explain with neat diagrams.
2. Draw the block diagram for Execution Unit and explain its components
3. What is the purpose of flag register?
4. Does the control lines are ALWAYS directed from CU to EU? If it is not, just give an example to counter the above.
5. How does the number of I/O lines in Von Neumann and Harvard architecture compare?

2 Problems

1. Given a set of n $(= 2^m)$ registers (each of (word) length l bits) for some $m = 0, 1, 2, \ldots,$
   (a) What is the minimum number of address bits necessary to pick an unique register from the above set?
   (b) Evolve an addressing scheme which uses minimum bus size. Show the digital circuit derived indicating the TT if any, at all used in the design.
   (c) Give an overall block diagram indicating the various units used in (b) above viz., register bank, address bus, data bus and control lines / bus. Indicate size of each bus.
   (d) Explain how the steps involved in instruction MOV Rd, Rs when executed, by using the above block diagram. Here, Rd & Rs are registers of size l bits. Identify the physical path of the digital signal journey.
   (e) Show the timing diagram of execution of the instruction in (d).
2. What is the size of (General Purpose) register memory (part of CU) in AVR? (Mention its size in terms of Bytes and its arrangement). What is the role of registers R26 through R31?
3. Consider the internal registers (internal to CU of a processor) of size l bits each and 'm' of them are available. If consecutive two such registers are used as a pointer to external memory (which might hold code or data), what would be the maximum number of memory words it could uniquely address?