EE2001-Tutorial 4
Date: 15th February 2018
More Combinational Logic

1) (i) Construct a 5-to-32-line decoder with four 3-to-8-line decoders with enable and a 2-to-4-line decoder.
Use block diagrams for the components.
(ii) Construct a 4-to-16-line decoder with five 2-to-4-line decoders with enable.

2) A combinational circuit is specified by the following three Boolean functions:
$F_1(A, B, C) = \Sigma(1, 4, 6)$
$F_2(A, B, C) = \Sigma(3, 5)$
$F_3(A, B, C) = \Sigma(2, 4, 6, 7)$
Implement the circuit with a decoder constructed with NAND gates and NAND or AND gates connected to the decoder outputs. Use a block diagram for the decoder. Minimize the number of inputs in the external gates.

3) Using a decoder and external gates, design the combinational circuit defined by the following three Boolean functions:

(a) $F_1 = x'yz' + xz$
$F_2 = xy'z' + x'y$
$F_3 = x'y'z' + xy$

(b) $F_1 = (y' + x)z$
$F_2 = y'z' + x'y + yz'$
$F_3 = (x + y)z$

4) (i) Design a four-input priority encoder with input D_0 having the highest priority and input D_3 the lowest priority.
(ii) Specify the truth table of an octal-to-binary priority encoder. Provide an output V to indicate that at least one of the inputs is present. The input with the highest subscript number has the highest priority. What will be the value of the four outputs if inputs D_2 and D_6 are 1 at the same time?

5) (i) Construct a 16 x 1 multiplexer with two 8 x 1 and one 2 x 1 multiplexers. Use block diagrams.
(ii) Implement a full adder with two 4 x 1 multiplexers.

6) An 8 x 1 multiplexer has inputs A, B, and C connected to the selection inputs S_2, S_1 and S_0 respectively. The data inputs I_0 through I_7 are as follows:
(a) $I_1 = I_2 = I_7 = 0$; $I_3 = I_5 = 1$; $I_0 = I_4 = D$ and $I_6 = D'$.
(b) $I_1 = I_2 = 0$; $I_3 = I_7 = 1$; $I_4 = I_5 = D$ and $I_0 = I_6 = D'$.
Determine the Boolean function that the multiplexer implements.

7) Implement the following Boolean function with a 4 x 1 multiplexer and external gates.
(a) $F_1(A, B, C, D) = \Sigma(1, 3, 4, 11, 12, 13, 14, 15)$
(b) $F_2(A, B, C, D) = \Sigma(1, 2, 5, 7, 8, 10, 11, 13, 15)$

Connect inputs A and B to the selection lines. The input for the 4 data lines will be functions of variables C and D. These functions may have to be implemented with external gates.

8) Implement a 4-bit ripple carry subtractor using four Full Adder blocks.

9) Design a single bit comparator circuit that compares two single-bit numbers in such a way that you can use n-such blocks in order to compare two n-bit numbers.

10) Design a 8 x 1 MUX using a 3X8 decoder and tristate gates.