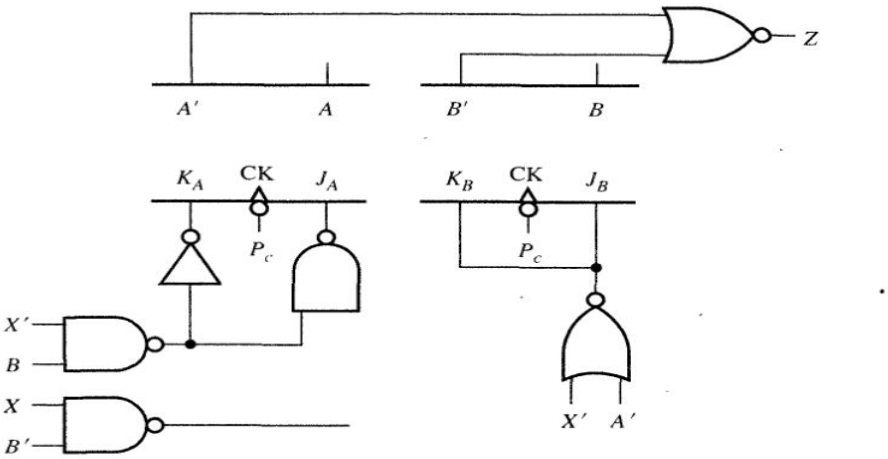
Tutorial 5

1.Design a 3-bit counter which counts in the sequence:
001, 011, 010, 110, 111, 101, 100, 001,...
a) Use clocked D flip-flops.
b) Use clocked T flip-flops.

2.Repeat above Problem for the sequence using clocked JK flip-flops.
001, 100, 101, 111, 110, 010, 011, 001,...

3.Using clocked T flip-flops design a decade counter which counts in the 6-3-1-1 code sequence

4. (a) For the following sequential network, find the next-state equation or map for each flip-flop.
Using these next-state equations or maps,
construct a (Moore) state table and graph for the network.
(b) What is the output sequence when the input sequence is X ~ 01100?
(c) Draw a timing diagram for the input sequence in (b). Show Pc, X, A, B,
and Z. Assume that the input changes between clock pulses.



5.Design a four-bit shift register with parallel load using D flip-flops. There are two control inputs: shift and load . When shift = 1, the content of the register is shifted by one position New data are transferred into the register when load = 1 and shift = 0. If both control inputs are equal to 0, the content of the register does not change.

6.A flip-flops has a 3 ns delay from the time the clock edge occurs to the time the output is complemented. What is the maximum delay in a 10-bit binary ripple counter that uses these flip-flops? What is the maximum frequency at which the counter can operate reliably?

7.Design a serial 2's complementer with a shift register and a flip-flop. The binary number is shifted out from one side and it's 2's complement shifted into the other side of the shift register