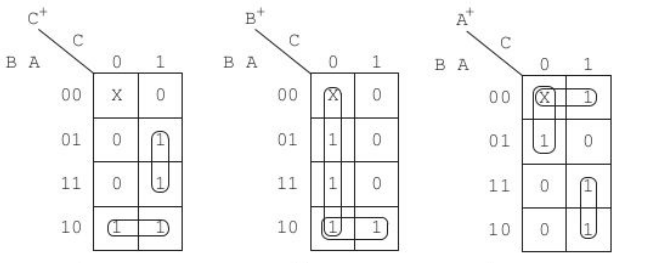
Tutorial 5 Solutions

1.Design a 3-bit counter which counts in the sequence:
001, 011, 010, 110, 111, 101, 100, 001,...
a) Use clocked D flip-flops.
b) Use clocked T flip-flops.

sol:

(a)

CBA	$C^+B^+A^+$
0 0 0	X X X
0 0 1	0 1 1
0 1 0	1 1 0
0 1 1	0 1 0
1 0 0	0 0 1
1 0 1	1 0 0
1 1 0	1 1 1
1 1 1	1 0 1



$C^+ = C\,A + B\,A'$

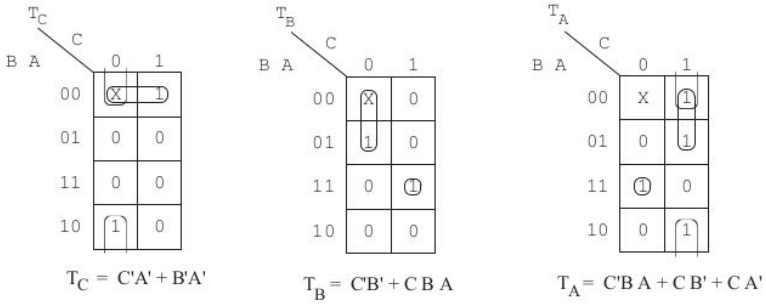
$B^+ = C' + B\,A'$

$A^+ = C'B' + C\,B + B'A'$

$A^+ = C'B' + C\,B + C\,A'$

For D flip-flop: 000 goes to 011 because $D_C D_B D_A = 011$

(b)



$T_C = C'A' + B'A'$

$T_B = C'B' + C\,B\,A$

$T_A = C'B\,A + C\,B' + C\,A'$

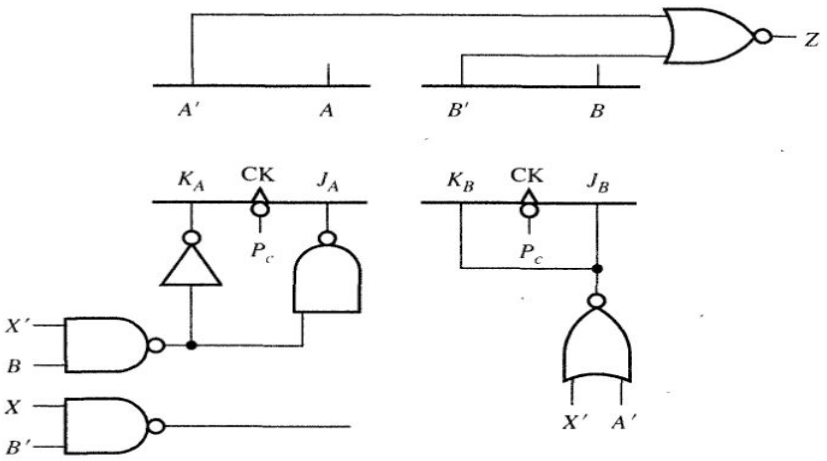
For T flip-flop: 000 goes to 110 because $T_A T_B T_C = 110$

2.Repeat above Problem for the sequence using clocked JK flip-flops.
001, 100, 101, 111, 110, 010, 011, 001,...

Sol:

J_A = B', K_A = BC'; J_B = AC, K_B = A'C; J_C = A' + B', K_C = A'B' + AB

4. (a) For the following sequential network, find the next-state equation or map for each flip-flop.
Using these next-state equations or maps,
construct a (Moore) state table and graph for the network.
(b) What is the output sequence when the input sequence is X = 01100?
(c) Draw a timing diagram for the input sequence in (b). Show Pc, X, A, B,
and Z. Assume that the input changes between clock pulses.



sol:

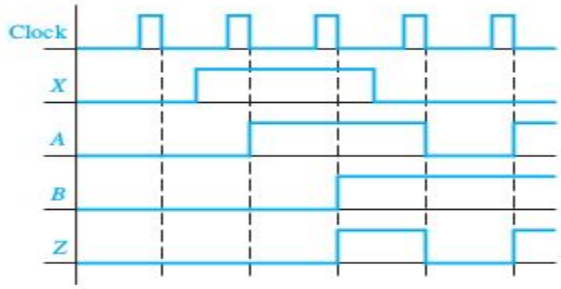
(a) $A^+ = A(B' + X) + A'(BX' + B'X)$ $\quad B^+ = AB'X + B(A' + X')$

Present State AB	Next State (A^+B^+) x = 0	x = 1	Z
00	00	10	0
01	11	01	0
11	01	10	1
10	10	11	0

This is a Moore machine.

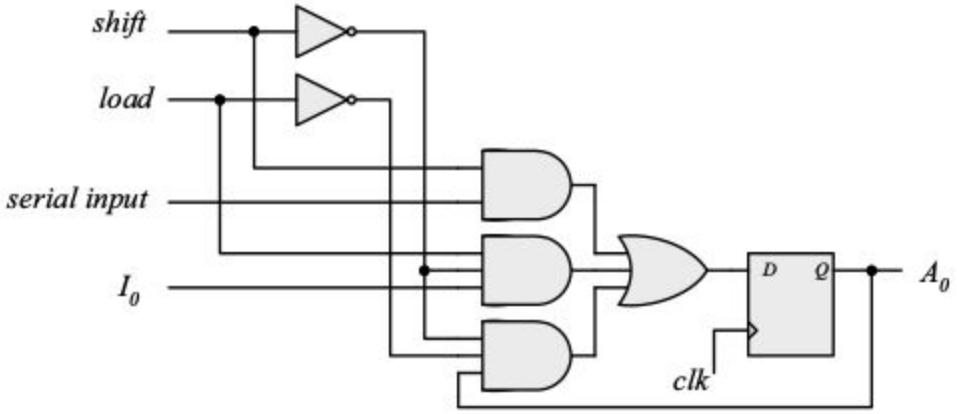
(b) $Z = (0)00101$

(c)



5.Design a four-bit shift register with parallel load using D flip-flops. There are two control inputs: shift and load . When shift = 1, the content of the register is shifted by one position New data are transferred into the register when load = 1 and shift = 0. If both control inputs are equal to 0, the content of the register does not change

sol:



6.A flip-flops has a 3 ns delay from the time the clock edge occurs to the time the output is complemented. What is the maximum delay in a 10-bit binary ripple counter that uses these flip-flops? What is the maximum frequency at which the counter can operate reliably?

sol:The worst case is when all 10 flip-flops are complemented.
The maximum delay is 10 x 3ns = 30 ns.
The maximum frequency is 10^9 /30 = 33.3 MHz

7.Design a serial 2's complementer with a shift register and a flip-flop. The binary number is shifted out from one side and it's 2's complement shifted into the other side of the shift register?

sol:

Note that y = x if Q = 0, and y = x' if Q = 1. Q is set on the first 1 from x.
Note that x ⊕ 0 = x, and x ⊕ 1 = x'.