Solutions to EE2016F19 Jan 16

Note Title 09/10/2019

1. impolly is impossible, while in interrupts it is possible

2. advantage of interrupt over polling is that CPU could be used most efficiently while interfacing with a peripheral

3. RETI. enables the interrupt again, after its execution, so that interrupts can happen

4. locations wherein the corresponding ISR is placed (or pointers to the ISR).

5. is to store the PC, content registers,

6. setting the I bit of the SREG register (status register)

7. global interrupt enabling is SEI

CLI (check this?)

Refer Muzidi & ammen.

EE2016 F19 Tut 6

Problem #1

1(a) Case A:

Time taken for peripheral (I/O) operation: $T_{33} = T_{REQ} + N_1 T_{INS} + T_{RES}$

$= 10 \times 6 T_{clk} + 6 N_1 T_{clk} + 3 T_{clk}$

$= (63 + 6N_1) T_{clk}$ secs.

Total time required for whole program $= 99 \times 6 T_{clk} + T_{33}$

$= 99 \times 6 T_{clk} + 10 \times 6 T_{clk} + N_1 \times 6 T_{clk} + 3 T_{clk}$ secs

$T^{net} = (99 \times 6 + 60 + 3 + 6N_1) T_{clk}$ secs

Total # of clk cycles (T_{clk}) required $= (594 + 63 + 6N_1)$

$= (657 + 6N_1)$ clock periods or clock cycles

1(a) Case B:

instructions executed concurrently during 33rd instruction execution $= \left\lfloor \frac{N_1 T_{INS}}{N_2 T_{INS} + T_{chk}} \right\rfloor \times N_2$

(K_{poll} cycles; $= K_{poll} \cdot N_2$)

Hence total time $T^{net}_{poll} = 32 \times 6 T_{clk} + T_{33} + (6 - K_{poll}) T_{INS}$

Note: K_{poll} is # of polling cycles & at each cycle, CPU executes N_2 instructions

$$T_{poll_j}^{net} = 192\,T_{clk} + (63+6N_1)T_{clk} + (67-K_{poll})6T_{clk}$$

$$= (255+6N_1+402-6K_{poll})T_{clk}$$

$$T_{poll_j}^{net} = (657+6N_1-6K_{poll})T_{clk}$$

1(a) (Case iii) Interrupt

$$T_{interrupt}^{net} = 32\times6T_{clk} + T_{33} + (67-N_1)6T_{clk}$$

$$= 192\,T_{clk} + (63+6N_1)T_{clk} + (402-6N_1)T_{clk}$$

$$T_{interrupt}^{net} = 657\,T_{clk}$$

1(a) (Case iv) DMA

$$T_{33} = (63+6N_1)T_{clk}$$

# of instructions executed concurrently during 33rd instruction execution $\Big\}\, K_{DMA} \triangleq \left\lfloor \frac{T_{REQ} + N_1 T_{INS} + T_{RES}}{T_{INS}} \right\rfloor$

$$T_{DMA}^{net} = 32\times6T_{clk} + \underbrace{4T_{clk} + T_{33}}_{T_{33,DMA}} + (67-K_{DMA})6T_{clk}$$

$$= (192+67+6N_1+402-6K_{DMA})T_{clk}$$

$$= (261+6N_1-6K_{DMA})T_{clk}$$

where $K_{DMA} = \left\lfloor \frac{T_{REQ} + N_1 T_{INS} + T_{RES}}{T_{INS}} \right\rfloor$

1(b) Observe that $K_{DMA} > N_1 > K_{poll}$

Hence $T^{net}_{DMA} < T^{net}_{interrupt} < T^{net}_{poll} < T^{net}$

1(c) Case A: is clearly ruled out.

Case B (Polling): K_{poll} denotes # of instructions after 33 has been correctly executed.

$$K_{poll} = \left\lfloor \frac{N_1 T_{INS}}{N_2 T_{INS} + T_{Chk}} \right\rfloor$$

and K^{th} instruction would not be executed (in polling scheme) when N_1, N_2 satisfy the following inequality:

$$(K-33)\,6\,T_{Clk} > K_{poll} \cdot N_2 \times 6\, T_{Clk}$$

or $$(K-33) > \left\lfloor \frac{N_1 T_{INS}}{N_2 T_{INS} + T_{Chk}} \right\rfloor N_2$$