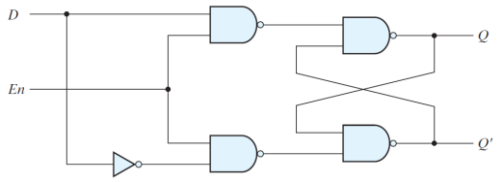
EE2001-Tutorial 5
Date: 27th February 2018
Synchronous Sequential Logic

1) The D Flip Flop is constructed with four NAND gates and an inverter. Consider the following three other ways for obtaining a D Flip Flop. In each case, draw the logic diagram and verify the circuit operation. (a) Use NOR gates for the SR latch part and AND gates for the other two. An inverter may be needed. (b) Use NOR gates for all four gates. Inverters may be needed. (c) Use four NAND gates only (without an inverter). This can be done by connecting the output of the upper gate (the gate that goes to the SR latch) to the input of the lower gate (instead of the inverter output).



2) (a) Construct a JK flip-flop using a D flip-flop, a 2x1 multiplexer, and an inverter.
(b) Show that the characteristic equation for the complement output of a JK flip-flop is

$$Q'(t + 1) = J'Q' + KQ$$

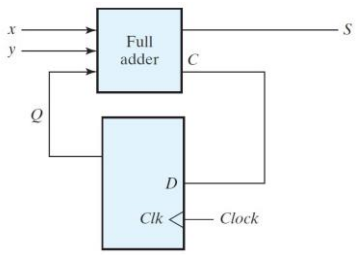
3) A PN flip-flop has four operations: clear to 0, no change, complement and set to 1, when inputs P and N are 00, 01, 10, and 11, respectively.
(a) Tabulate the characteristic table.
(b) Derive the characteristic equation.
(c) Tabulate the excitation table.
(d) Show how the PN flip-flop can be converted to a D flip-flop.

4) A sequential circuit with two D flip-flops A and B, two inputs, x and y ; and one output z is specified by the following next-state and output equations:

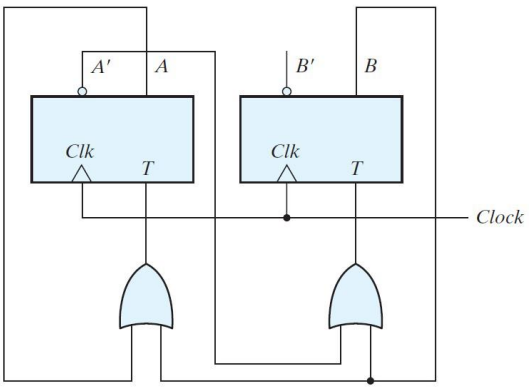
$$A(t + 1) = xy' + xB; \quad B(t + 1) = xA + xB'; \quad z = A$$

(a) Draw the logic diagram of the circuit.
(b) List the state table for the sequential circuit.
(c) Draw the corresponding state diagram.

5) A sequential circuit has one flip-flop Q, two inputs x and y, and one output S . It consists of a full-adder circuit connected to a D flip-flop, as shown below. Derive the state table and state diagram of the sequential circuit.



6) Derive the state table and the state diagram of the sequential circuit shown below. Explain the function that the circuit performs.



7) A sequential circuit has two JK flip-flops A and B and one input x . The circuit is described by the following flip-flop input equations:

$J_A = x$; $K_A = B$

$J_B = x$; $K_B = A'$

(a) Derive the state equations A (t + 1) and B (t + 1) by substituting the input equations for the J and K variables.

(b) Draw the state diagram of the circuit.

8) A sequential circuit has two JK flip-flops A and B, two inputs x and y, and one output z. The flip-flop input equations and circuit output equation are:

$J_A = Bx + B'y'$; $K_A = B'xy'$

$J_B = A'x$; $K_B = A + xy'$

$z = Ax'y' + Bx'y'$

(a) Draw the logic diagram of the circuit.

(b) Tabulate the state table.

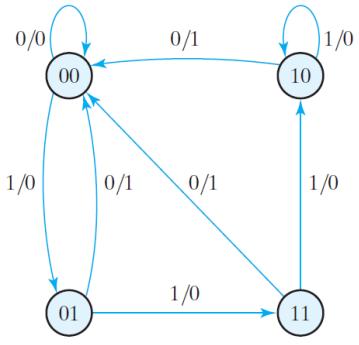
(c) Derive the state equations for A and B.

9) For the circuit described by the state diagram given below

(a) Determine the state transitions and output sequence that will be generated when an input sequence of 010110111011110 is applied to the circuit and it is initially in the state 00.

(b) Find all of the equivalent states and draw a simpler, but equivalent, state diagram.

(c) Using D flip-flops, design the equivalent machine described by the state diagram in (b).



10) For the given state table (a) draw the corresponding state diagram. (b) Tabulate the reduced state table. (c) Draw the state diagram corresponding to the reduced state table. (d) Starting from state a, and the input sequence 01110010011, determine the output sequence for (i) the state table and (ii) the reduced state table. Show that the same output sequence is obtained for both.

	Next State		Output	
Present State	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0