Name: _____ Roll Number: _____

EE2001 Quiz II

Monday, 02/04/18

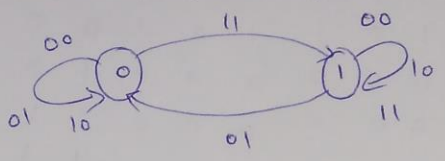
Closed book, 50 mins, 20 points

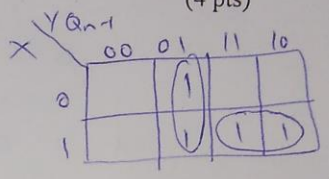
Remember...

- *Make reasonable assumptions when in doubt. However, you should show all steps and justify assumptions for full credit.* ***Provide final answers ONLY in the space provided.***

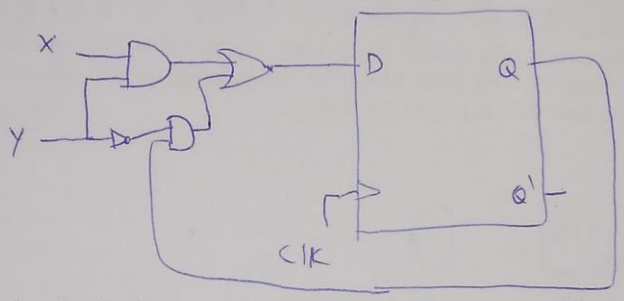
1. Draw the state diagram for a Flip-Flop which has two inputs X and Y and two outputs Q and Q'. When Y = 0, the output Q_n is equal to the previous state Q_{n-1} and when Y =1, Q_n = X. Realize the Flip-Flop using a D Flip-Flop and some gates. (4 pts)

X	Y	Q_{n-1}	Q_n
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

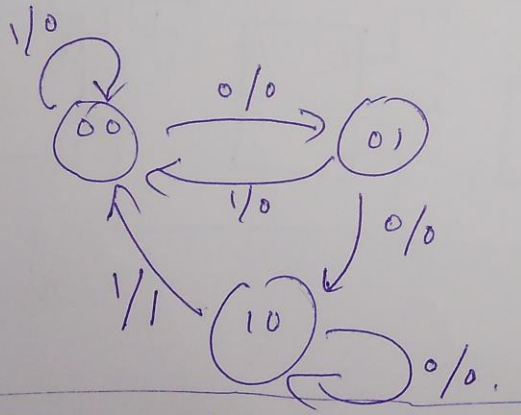


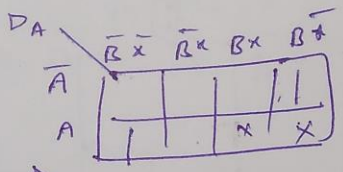


$Q_n = XY + Q_{n-1}Y'$

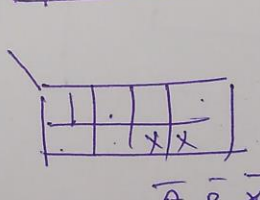


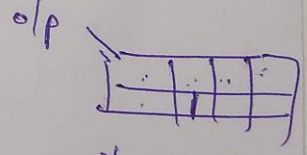
2. Design and draw the circuit of a synchronous single input single output system such that the output Z = 1 with every occurrence of an input 1 following a string following a string of at least two consecutive 0 inputs. At all other times, the output Z = 0. (4 pts)





$D_A = \bar{x}(A + B)$



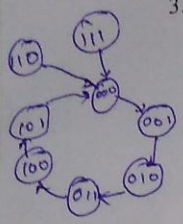


$o/p = A\bar{B}x$.

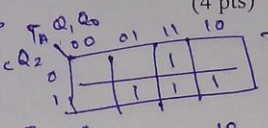
A	B	x	A^+	B^+	o/p	D_A	D_B
0	0	0	0	1	0	0	1
0	0	1	0	0	0	0	0
0	1	0	1	0	0	1	0
0	1	1	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
						x	x

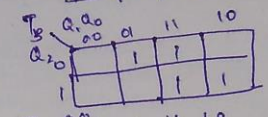
Name: _____ Roll Number: _____

3. Design and draw the circuit of a synchronous mod-6 counter which counts from 000 in the binary sequence. Also, if any unused state occurs, the output goes to 000 at the next clock pulse. (4 pts)



Present state			Next state			D-Flip-flop input			T-Flip flop input		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	D_A	D_B	D_C	T_A	T_B	T_C
0	0	0	0	0	1	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0	0	1	1
0	1	0	0	1	1	0	1	1	0	0	1
0	1	1	1	0	0	1	0	0	1	1	1
1	0	0	1	0	1	1	0	1	0	0	1
1	0	1	0	0	0	0	0	0	1	0	1
1	1	0	0	0	0	0	0	0	1	1	0
1	1	1	0	0	0	0	0	0	1	1	1



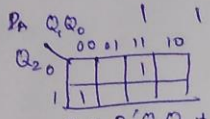


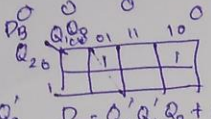
JK flip flop:

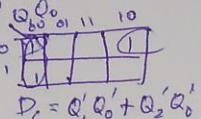
$J_A = Q_1Q_0$ $K_A = Q_1'Q_0'$

$J_B = Q_2'Q_0$ $K_B = Q_2'Q_0'$

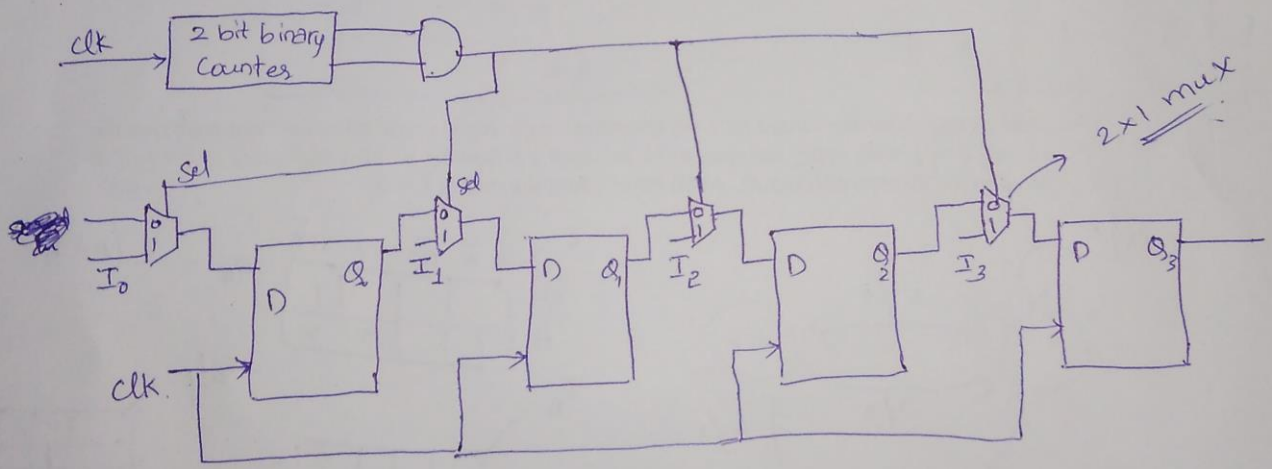
$J_C = Q_2Q_1$ $K_C = 1$





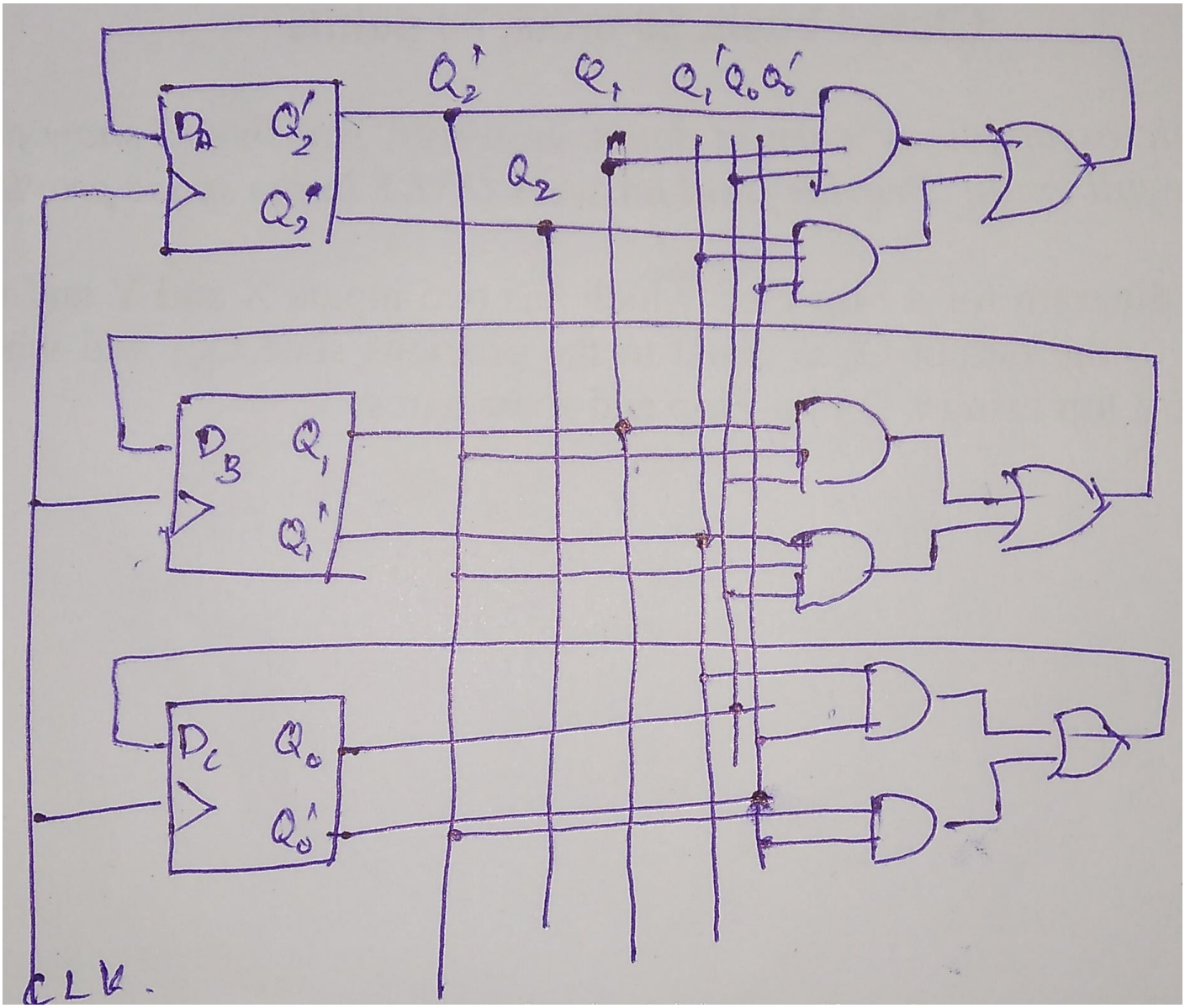


4. Draw the circuit of a system which loads 4-bit parallel data once in every 4 clock pulses and outputs them as 4-bit serial data. The design **must** include generation of appropriate control signals to load data at proper intervals. (4 pts)



5. (a) Consider a 16 M x 8 memory constructed using the above element. The number of address lines and the input/output data lines required are 24 and 8 respectively. (2pts)

(b) The number of AND gates required for the decoder in the above memory is 2^{24} for 1-D addressing and 2^{13} for 2-D addressing (2pts)


Q_2'
Q_1
$Q_1'Q_0Q_0'$
D_A
Q_2
Q_2'
Q_2
D_B
Q_1
Q_1'
D_C
Q_0
Q_0'
CLK.