EE2001-Tutorial 10
Date: 24th April 2018
ASMD Charts and Asynchronous Sequential Circuits

1) A logic circuit with active-low synchronous reset has two control inputs x and y. If x is 1 and y is 0, register R is incremented by 1 and control goes to a second state. If x is 0 and y is 1, register R is cleared to zero and control goes from the initial state to a third state. Otherwise, control stays in the initial state.
Draw (i) a block diagram showing the controller, datapath unit (with internal registers), and signals, and (ii) the portion of an ASMD chart starting from an initial state.

2) Draw the ASMD charts for the following state transitions:
(a) If x = 1, control goes from state S1 to state S2 ; if x = 0, generate a conditional operation R <= R + 2 and go from S1 to S2 .
(b) If x = 1, control goes from S1 to S2 and then to S3; if x = 0, control goes from S1 to S3.
(c) Start from state S1; then if xy = 11, go to S2; if xy = 01 go to S3; and if xy = 10, go to S1; otherwise, go to S3.

3) Construct a block diagram and an ASMD chart for a digital system that counts the number of people in a room. The one door through which people enter the room has a photocell that changes a signal x from 1 to 0 while the light is interrupted. They leave the room from a second door with a similar photocell that changes a signal y from 1 to 0 while the light is interrupted. The datapath circuit consists of an up–down counter with a display that shows how many people are in the room.

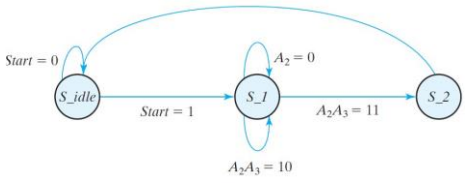
4) Draw a block diagram and an ASMD chart for a circuit with two eight-bit registers RA and RB that receive two unsigned binary numbers. The circuit performs the subtraction operation

$$RA \leftarrow RA - RB$$

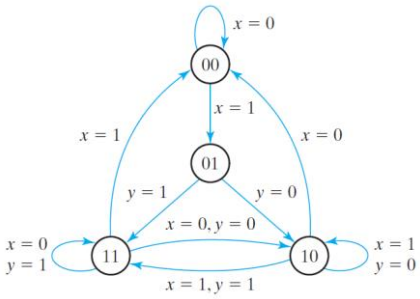
Set a borrow flip-flop to 1 if the answer is negative.

5) Design a digital circuit with three 16-bit registers AR, BR and CR that perform the following operations:
(a) Transfer two 16-bit signed numbers (in 2's-complement representation) to AR and BR.
(b) If the number in AR is negative, divide the number in AR by 2 and transfer the result to register CR.
(c) If the number in AR is positive but nonzero, multiply the number in BR by 2 and transfer the result to register CR.
(d) If the number in AR is zero, clear register CR to 0.

6) Design the controller whose state diagram is given. Use one flip-flop per state.



7) The state diagram of a control unit is shown. It has four states and two inputs x and y. Draw the equivalent ASM chart. Design the controller corresponding to the statediagram. Use D flip-flops.



8) Derive the transition table for the asynchronous sequential circuit of Fig. P9-2. Determine the sequence of internal states Y1Y2 for the following sequence of inputs x1x2: 00, 10, 11, 01, 11, 10, 00

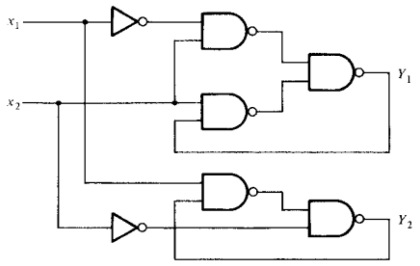


FIGURE P9-2

9) An asynchronous sequential circuit is described by the following excitation and output functions:

$$Y = x_1x_2' + (x_1 + x_2')y$$

$$z = y$$

(a) Draw the logic diagram of the circuit.
(b) Derive the transition table and output map.
(c) Obtain a 2-state flow table.

10) Convert the flow table of Fig. P9-5 into a transition table by assigning the following binary values: a=00, b=11, c=01.
(a) Assign values to the extra fourth state to avoid critical races.
(b) Assign outputs to the don't-care states to avoid momentary false outputs.
(c) Derive the logic diagram of the circuit.

	x_1x_2 = 00	01	11	10
a	(a), 0	b, –	c, –	(a), 1
b	a, –	(b), 0	(b), 0	c, –
c	a, –	b, –	(c), 1	(c), 0

FIGURE P9-5

11) Investigate the transition table of Fig. P9-6 and determine all race conditions and whether they are critical or non-critical.
Also determine if there are any cycles.

y_1y_2 \ x_1x_2	00	01	11	10
00	10	(00)	11	10
01	(01)	00	10	10
11	01	00	(11)	(11)
10	11	00	(10)	(10)

FIGURE P9-6

12) For the asynchronous sequential circuit shown in Fig. P9-9:
(a) Derive the Boolean functions for the outputs of the two SR latches Y_1 and Y_2. Note that the S input of the second latch is $x_1'y_1'$.
(b) Derive the transition table and output map of the circuit.

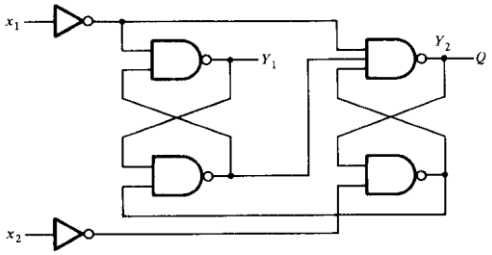


FIGURE P9-9