# EE2016 Microprocessors Theory and Lab

Tutorial 1 (Classes on 29, 30 & 31st of July 2019)

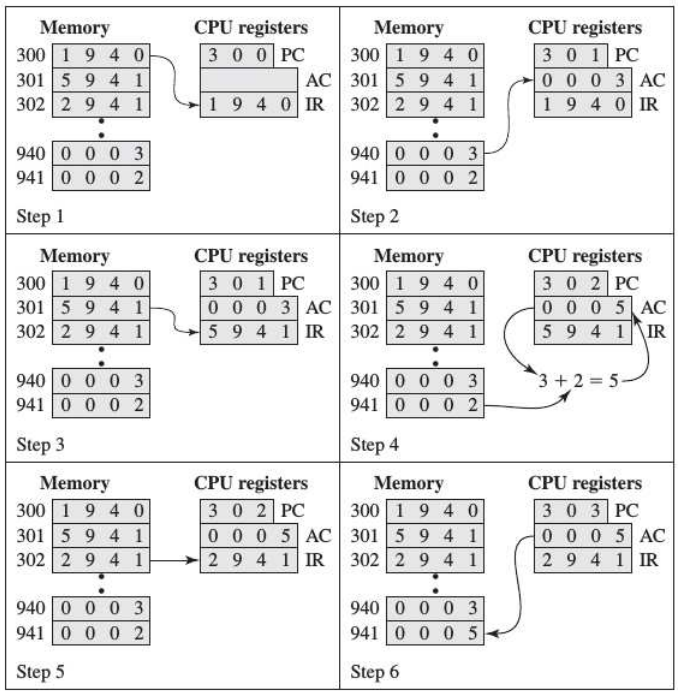
July-Nov 2019, EE Dept, IIT Madras.

## 1 Fill in the blanks

1. The harware realization of multiplier in a microcontroller / microprocessor is a ..... (architectural / organizational) issue.
2. Data bus is always ..... (unidirections / bidirectional) and address bus is ..... (unidirections / bidirectional)
3. Major difference between the microcontroller and a microprocessor is ..... .....
4. In the Von Neumann architecture discussed in the class the MBR handles a word of length ..... (20 or 40). IR ..... IBR ..... MAR ..... and finally PC .....
5. Output of IR is a part of ..... (address / control / data bus).
6. Issues or performance measures of whether a hardware multiplier implementation or software realization of multiplier algorithm are ....., ....., ....., and .....
7. Which of the following is (are) volatile? (a) SRAM, (b) EEPROM (c) DRAM (d) NV-RAM

## 2 Answer the following

1. Browse in the internet for a commercial processor which has also FPGA.
2. What is the difference between computer organization and architecture?
3. Describe the Von Neumann architecture with a block diagram and explain its operation.
4. What is the major difference between Von Neumann architecture and Harvard architecture?
5. Recall the van Neumann computer introduced in the class. The following Fig gives the execution of instructions, in which MAR & MBR are implicit.




(a) Explicitly mention the role of MAR & MBR and quantitatively evaluate its value in each clock cycle.

(b) What is the role of AC here?

6. What is the major, superficial cycle or infinite loop of operations a microcontroller or microprocessor would be there ALWAYS?

7. How are registers built out of flip-flips? Show the control lines and data lines.