



## Department of Electrical Engineering, Indian Institute of Technology Madras

Course title	Digital Systems & Lab - A slot										Course No	EE2001			
Department	Electrical Engineering	New Credits	L	T	E	P	O	C	TH	Old Credits	L	T	P		
			3	1		6	6	16	6		16	3	1	3	
Offered for	B.Tech 2nd year										Status	Modified			
Faculty	Ananth Krishnan, T G Venkatesh, Vinita Vasudevan										Type	Lab			
Pre-requisite											To take effect from	16-10-2018			
Submission date	Date of approval by DCC		Date of approval by BAC							Date of approval by Senate					
08-10-2018															

### Objectives:

At the end of this course, the student should be able to: 1. understand number systems 2. implement and analyse digital systems based on combinational and sequential logic 3. understand and design state machines 4. design systems using RTL

### Course Contents:

1. Introduction to Digital Systems and Boolean Algebra Binary, octal and hexadecimal number systems; Truth table; Basic logic operation and logic gates. Basic postulates and fundamental theorems of Boolean algebra; Canonical (SOP and POS) forms 2. Logic Minimization and Implementation Minterm and Maxterm expansions; - Karnaugh-maps, essential prime implicants, incompletely specified functions, NAND and NOR implementation, Quine-McCluskey method; Switch level representation and realization using transistors Logic families – TTL, CMOS 3. Combinational Logic Multi level gate circuits, Decoders, encoders, multiplexers and demultiplexers and their applications; Parity circuits and comparators; Representation of signed numbers; Adders, Ripple carry. Introduction to HDL (VHDL/Verilog), HDL description of combinational circuits 4. Sequential Logic Latches and flip-flops: SR-latch, D-latch, D flip-flop, JK flip-flop, T flip-flop; Setup and Hold parameters, timing analysis; Registers and counters; Shift register; Ripple counter, Synchronous counter design using D, T, and JK flip flops. HDL description of sequential circuits 5. State Machine Design State machine as sequential controller; Moore and Mealy state machines; Derivation of state graph and tables; Sequence detector state table reduction using Implication table; state assignment, logic realization; equivalent state machines, Designing state machine using ASM charts. state machine modeling based on HDL 6. Memory and Programmable Logic Devices ROM and RAM; Sequential PLDs and their applications; State- machine design with sequential PLDs; FPGAs 7. Register transfer language: Notation, HDL features for RTL, Digital design at the RTL level, Simple design of a microcontroller using RTL 8. Advanced Topics Asynchronous Sequential Machines, Static and Dynamic hazards; race free design; testing digital circuits.

Syllabus: Laboratory Experiments on design of combinational circuits including adders and magnitude comparators; realization using multiplexers and other approaches; identification of critical path Design of sequential circuits including flip-flops, counters and registers Digital to analog converter design and study of characteristics Experiments on motor control using flip-flops and gates Introduction to hardware description languages and simulation of simple circuits

### Text Books:

1. Morris. M. Mano, Michael D. Ciletti, Digital Design, Fourth Edition, Prentice-Hall India. 2008.
2. Charles. H. Roth, Jr., Fundamentals of Logic Design, Fifth Edition, Thomson Brooks /Cole, 2005.
3. S. Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, Second Edition, Pearson Education, 2004.

### Reference Books:

1. S. Brown and Z. Vranesic, Fundamentals of digital logic with Verilog design, Third Edition, McGraw-Hill, 2013.
2. Charles. H. Roth, Jr., Digital System Design using VHDL, Indian Edition, Thomson Brooks /Cole, 2006.
3. Mohammad A. Karim, Xinghao Chen, Digital Design, CRC press 2008.
4. J.F. Wakerly, Digital Design: Principles and Practices, Fourth Edition, Prentice Hall, 2005