EE2016 Microprocessors Theory and Lab, July-Nov 2019

Tutorial 5a (Classes in week 26 - 30.9.19: Memory Mapping)

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Problems

1. For a processor which has 64KB address space with 2KB Internal Memory (M0) with peripherals as given in table

Peripheral type	**Notation**	**Memory Size**	
Memory Module	M1	16 KB	
Memory Module	M2	8 KB	
Keyboard	KBD	128 B	
Mouse	MSE	128 B	
Mic	MIC	256 B	
Speaker	SPK	512 B	
Communication Controller	COM	1 KB	
USB	USB1	1 KB	
USB	USB2	1 KB	
Scanner	SCN	2 KB	
Printer RAM	PRN	16 KB	
Monitor	MNTR	16 KB	

   (a) Design an I/O memory map, for the cases
      i. with regular mapping
      ii. with M1 starting immediately after M0 (is it a regular mapping?)

   (b) Obtain expression for chip select for each of the devices / peripherals. Implement it using logic gates. Show the digital circuitry.

   (c) Suppose '*scanner*' is not there in the table. Can one have (i) regular mapping (ii) a single contiguous place corresponding to all the unmapped memory area?

   (d) Suppose '*16 KB memory*' is not there in the table. Can one have (i) regular mapping (ii) a single contiguous place corresponding to all the unmapped memory area?

   (e) Following are the constraints
      i. M0 always starts at location 0000 (H).
      ii. As far as possible, design such that all of the peripherals, memory modules (internal memory inclusive) are accommodated (with unmapped area in one contiguous place - which could be used to accommodate single large memory in future).