Tutorial 3

1 .Construct a 16 - 1 multiplexer with two 8 - 1 and one 2 - 1 multiplexers. Use block diagrams.

2. An 8 - 1 multiplexer has inputs A , B , and C connected to the selection inputs S2,S1,S0 respectively. The data inputs i0 through i7 are as follows:
i1 =i2 = i7 = 0; i3 =i5 = 1; i0 = i4 = D ; and i6 = D'
Determine the Boolean function that the multiplexer implements.

3. a)Realize the function A'C + A'B'D' + ACD+A'BD using an 8-to-1 MUX with control inputs A, C, and D.
b)Repeat part a using a 4-to-1 MUX. Select the control inputs to minimize the number of added gates.

4. Construct a 5-to-32-line decoder with four 3-to-8-line decoders with enable and a 2-to-4 Line decoder. Use block diagrams for the components.

5. Using a decoder and external gates, design the combinational circuit defined by the following three Boolean functions:

F1 = x'yz' + xz
F2 = xy'z' + x'y
F3 = x'y'z' + xy

6. Specify the truth table of an octal-to-binary priority encoder. Provide an output V to indicate that at least one of the inputs is present. The input with the highest subscript number has the highest priority. What will be the value of the four outputs if inputs D_2 and D_6 are 1 at the same time?

7. An ABCD-to-seven-segment decoder is a combinational circuit that converts a decimal digit in BCD to an appropriate code for the selection of segments in an indicator used to display the decimal digit in a familiar form. The seven outputs of the decoder (a, b, c, d, e, f, g) select the corresponding segments in the display, as shown in Fig. P4.9(a) . The numeric display chosen to represent the decimal digit is shown in Fig. P4.9(b) . Using a truth table and Karnaugh maps, design the BCD-to-seven-segment decoder using a minimum number of gates. The six invalid combinations should result in a blank display.

(a) Segment designation (b) Numerical designation for display

8. Design a 3 bit odd parity generator and odd parity checker.
9. Design a network of AND and OR gates to convert from 8-4-2-1 BCD code to 6-3-1-1 code.