Model Answers.

Name: Roll Number:

EE2001 Quiz I

Monday, 19/02/18

Closed book, 50 mins, 20 points

Remember...

- *Make reasonable assumptions when in doubt. However, you should show all steps in additional sheets and justify assumptions for full credit.* ***Provide final answers ONLY in the space provided.***

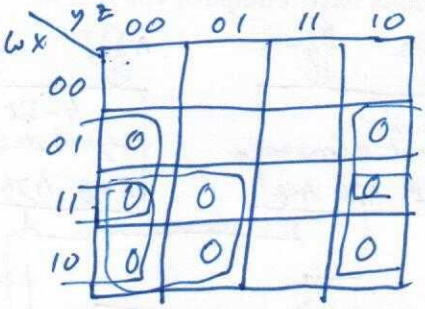
1. In a particular number system of base r, the roots of the equation $5x^2 + 50x + 125 = 0$ are given by $x = -8$ and $x = -5$. The value of r is . 13 (2 pts)

$(x+8)(x+5) = 0 \Rightarrow x^2 + 13x + 40 = 0 \Rightarrow 5x^2 + 65x + 200 = 0.$

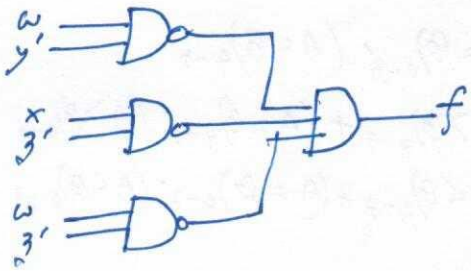
$5r = 65 \Rightarrow r = 13$; Also, $1\times13^2 + 2\times13 + 5 = 200$. (Confirmed).

2. Simplify the following Boolean function and implement the same using NAND-AND gates:

$F(w, x, y, z) = \Pi\,(4, 6, 8, 9, 10, 12, 13, 14)$ (3 pts)

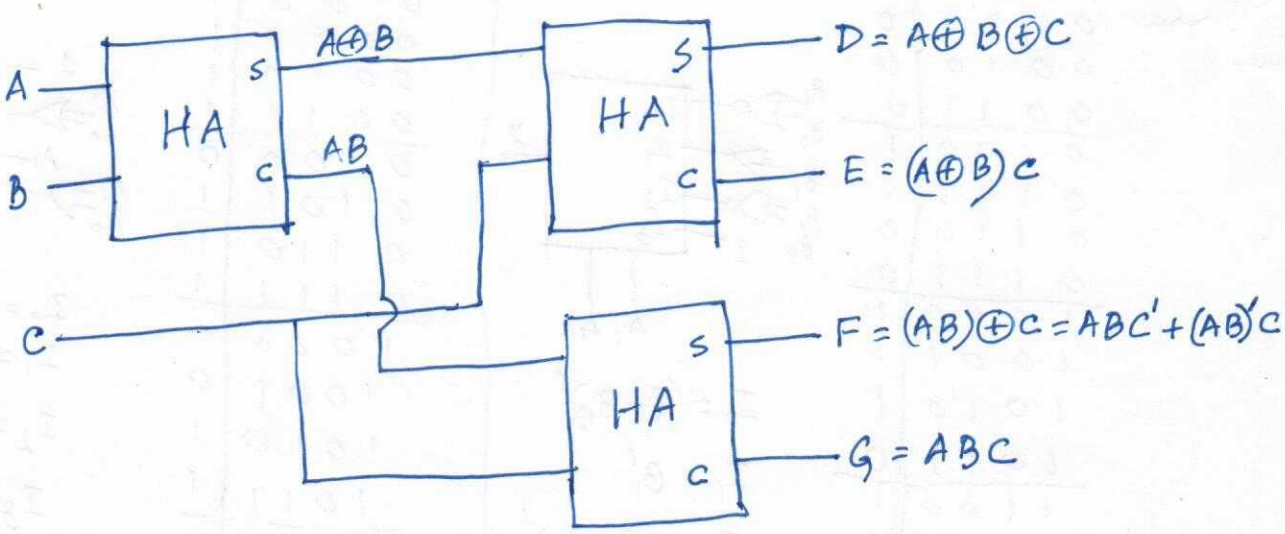


$F' = wy' + xz' + wz'$



3. Implement the following Boolean functions using ONLY three half-adder circuits: (4 pts)

(i) D = A ⊕B⊕C (ii) E = A'BC + AB'C (iii) F = ABC' + (A' + B')C (iv) G = ABC



4. (a) Obtain Boolean expressions for the carry bits (C_1, C_2, C_3, C_4) of a 4-bit carry look ahead adder.

$C_1 = G_0 + P_0 C_0$

$C_2 = G_1 + P_1 G_0 + P_1 P_0 C_0$

$C_3 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0$

$C_4 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_0$

$G_i = A_i B_i$

$P_i = A_i \oplus B_i$

(b) Assuming that the exclusive-OR gate has a propagation delay of 20 ns and all other gates have propagation delay of 10 ns, the total propagation delay for this 4-bit adder is ..60 ns..

1 Ex-OR for generating G's and P's + 2 Gates for generating carries + 1 Ex-OR for Sum output

(c) If two such 4-bit adders are connected to realize an 8-bit adder, the total propagation delay is ....80 ns.... (1+2+2 pts)

For the CLA for higher order bits, C_4 is available after 40 ns.

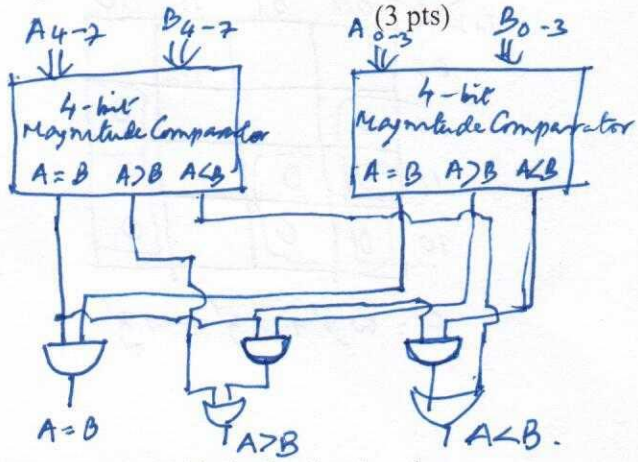
Delay = 40 ns + 20 ns (to generate all C's) + 20 ns for Sum o.p's.

5. Design and draw the circuit of an 8-bit magnitude comparator realized using two 4-bit magnitude comparators and a few gates. The magnitude comparators have 3 outputs, viz. A = B, A > B and A < B. (3 pts)

$(A=B) = (A=B)_{0-3} \cdot (A=B)_{4-7}$

$(A>B) = (A>B)_{4-7} + (A=B)_{4-7} \cdot (A>B)_{0-3}$

$(A<B) = (A<B)_{4-7} + (A=B)_{4-7} \cdot (A<B)_{0-3}$

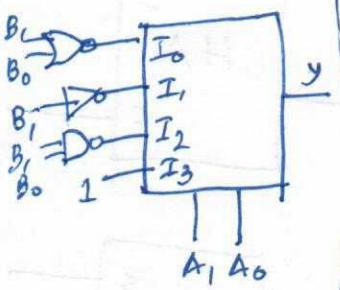


6. Two 2-bit binary numbers A = A_1A_0 and B = B_1B_0 are fed into a 4-bit logic circuit, whose output is 1 only if A ≥ B. Design and draw the circuit using one 4 x 1 MUX and some gates. (3 pts)

A_1A_0	B_1B_0	Y
0 0	0 0	1
0 0	0 1	0
0 0	1 0	0
0 0	1 1	0
0 1	0 0	1
0 1	0 1	1
0 1	1 0	0
0 1	1 1	0
1 0	0 0	1
1 0	0 1	1
1 0	1 0	1
1 0	1 1	0
1 1	0 0	1
1 1	0 1	1
1 1	1 0	1
1 1	1 1	1

OR

B_1B_0	A_1A_0	Y
0 0	0 0	1
0 0	0 1	1
0 0	1 0	1
0 0	1 1	1
0 1	0 0	0
0 1	0 1	1
0 1	1 0	1
0 1	1 1	1
1 0	0 0	0
1 0	0 1	0
1 0	1 0	1
1 0	1 1	1
1 1	0 0	0
1 1	0 1	0
1 1	1 0	0
1 1	1 1	1

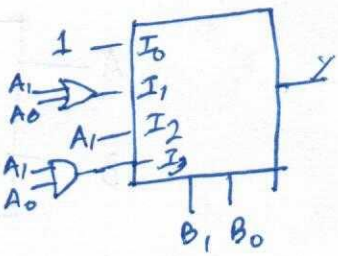


$I_0 = (B_1 + B_0)'$

$I_1 = B_1'$

$I_2= (B_1 \cdot B_0)'$

$I_3 = 1$



$I_0 = 1$

$I_1 = A_1 + A_0$

$I_2 = A_1$

$I_3 = A_1 \cdot A_0$