

# EE2016 Microprocessors Theory and Lab, July - Nov 2019

## Tutorial 7: Memory Map

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### Problems

1. Design an IO/memory map for the processor which has 64KB address space and requires 2KB Internal Memory (M0), 16 KB EEPROM (M1) and 8KB RAM (M2). Additionally, attach a 2KB Keyboard Controller (P1) and a 4KB printer Controller (P2). First place M0, M1, M2 as well as P1 and P2 at suitable locations in memory space, with M0 starting at location 0000(H), such that all devices use the lower 32KB of IO/memory space and have regular mapping. Then obtain expression for chip select for each of the devices.
2. Design an IO/memory map for the processor which has 32KB address space and requires 4KB Internal Memory (M0), 8KB external memory (M1), 16KB Network Controller (P1) and 3 KB Keyboard Controller (P2). First place M0, M1 as well as P1 and P2 at suitable locations in memory space, with M0 starting at location 0000(H). Then obtain expression for chip select for each of the devices.
3. Design an IO/memory map for the processor which has 64KB address space and requires 2KB Internal Memory (M0), 2 KB EEPROM (M1) and 8KB RAM (M2). Additionally, attach a 2KB Keyboard Controller (P1) and a 4KB printer Controller (P2). First place M0, M1, M2 as well as P1 and P2 at suitable locations in memory space, with M0 starting at location 0000(H) and M1 at location 0C00(H). Then obtain expression for chip select for each of the devices.
4. Create a memory map for a processor with 16 address lines that need to connect to M1 – 4KB and M2 – 512 Bytes with M2 starting at location 0080 (H).