Tutorial 4 Solutions

5.10 A sequential circuit has two JK flip-flops A and B, two inputs x and y, and one output z. The flip-flop input equations and circuit output equation are

$$J_A = Bx + B'y' \qquad K_A = B'xy'$$
$$J_B = A'x \qquad K_B = A + xy'$$
$$z = Ax'y' + Bx'y'$$

(a) Draw the logic diagram of the circuit.
(b) Tabulate the state table.
(c)* Derive the state equations for A and B.

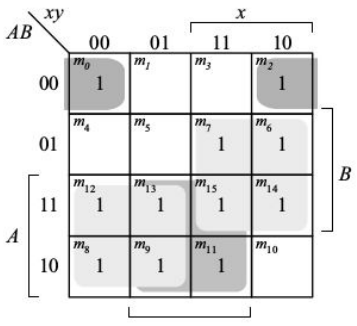
sol:

5.10 **(a)** $J_A = Bx + B'y'$ $\quad J_B = A'x$
$K_A = B'xy'$ $\quad K_B = A + xy'$ $\quad z = Axy + Bx'y'$

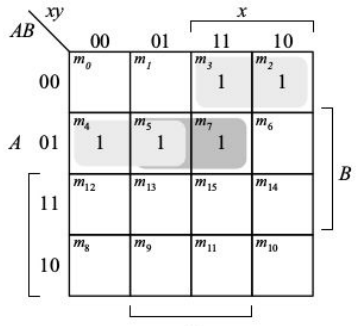
(b)

Present state A	Present state B	Inputs x	Inputs y	Next state A	Next state B	Output z	FF Outputs J_A	FF Outputs K_A	FF Outputs J_A	FF Outputs J_B
0	0	0	0	1	0	0	1	0	0	0
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	1	0	1	1	1	1
0	0	1	1	0	1	0	0	0	1	0
0	1	0	0	0	1	1	0	0	0	0
0	1	0	1	0	1	0	0	0	0	0
0	1	1	0	1	0	0	1	0	1	0
0	1	1	1	1	1	0	1	0	1	0
1	0	0	0	1	0	0	1	0	0	1
1	0	0	1	1	0	0	0	0	0	1
1	0	1	0	0	0	0	1	1	0	1
1	0	1	1	1	0	0	0	0	0	1
1	1	0	0	1	0	1	0	0	0	1
1	1	0	1	1	0	0	0	0	0	1
1	1	1	0	1	0	0	1	0	0	1
1	1	1	1	1	0	1	1	0	0	1

(c)



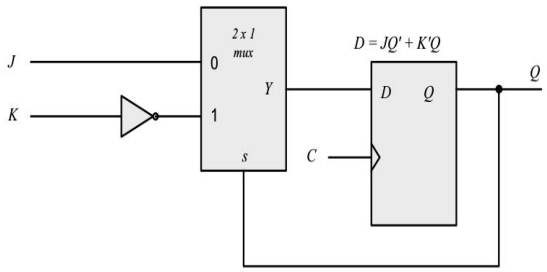
$A(t+1) = Ax' + Bx + Ay + A'B'y'$



$B(t+1) = A'B'x + A'B'(x' + y)$

5.2) Construct a JK flip flop using a D flip flop, 2 x 1 mux and an inverter
sol:

5.2



5.8* Derive the state table and the state diagram of the sequential circuit shown in Fig. P5.8. Explain the function that the circuit performs. (HDL—see Problem 5.36.)

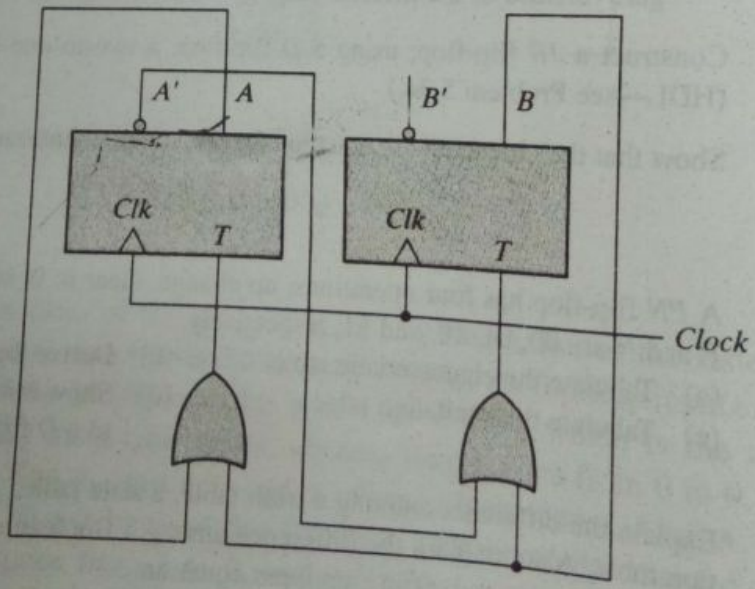


FIGURE P5.8

sol:

5.8 A counter with a repeated sequence of 00, 01, 10.

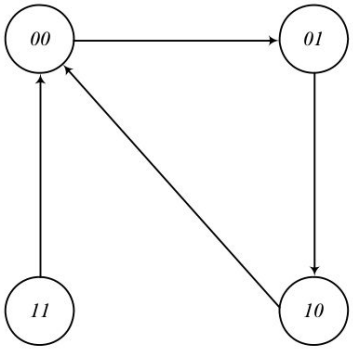
Present state A	Present state B	Next state A	Next state B	FF Inputs T_A	FF Inputs T_B
0	0	0	0	0	1
0	1	1	0	1	1
1	0	0	0	1	0
1	1	0	0	1	1

$T_A = A + B$

$T_B = A' + B$

Repeated sequence:

$\rightarrow 00 \rightarrow 01 \rightarrow 10 \rightarrow$



5.4 A *PN* flip-flop has four operations, no change, clear to 0, set 1 and complement, when inputs *P* and *N* are 00, 01, 10, and 11, respectively.

(a) Tabulate the characteristic table.

(b)* Derive the characteristic equation.

(c) Tabulate the excitation table.

(d) Show how the *PN* flip-flop can be converted to a *D* flip-flop.

sol:

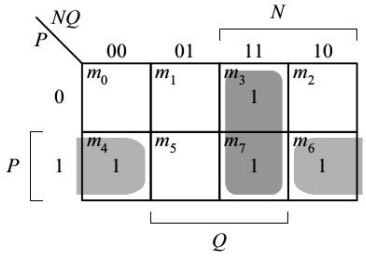
5.4

(a)

P	N	Q(t + 1)
0	0	0
0	1	Q(t)
1	0	Q'(t)
1	1	1

(b)

P	N	Q(t)	Q(t + 1)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1



$Q(t+1) = PQ' + NQ$

(c)

Q(t)	Q(t+1)	P	N
0	0	0	x
0	1	1	x
1	0	x	0
1	1	x	1

(d) Connect P and N together.

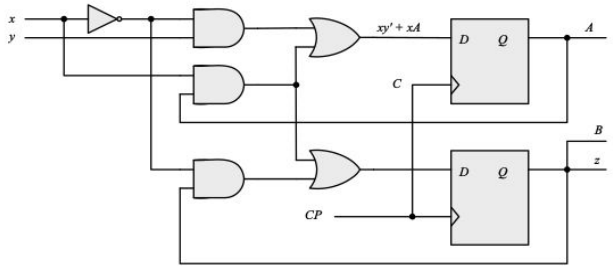
5.6 A sequential circuit with two D flip-flops A and B, two inputs x and y, and one output z is specified by the following next-state and output equations (HDL—see Problem 5.35):

$$A(t+1) = x'y + xB$$
$$B(t+1) = x'A + xB$$
$$z = A$$

(a) Draw the logic diagram of the circuit.
(b) List the state table for the sequential circuit.
(c) Draw the corresponding state diagram.

sol:

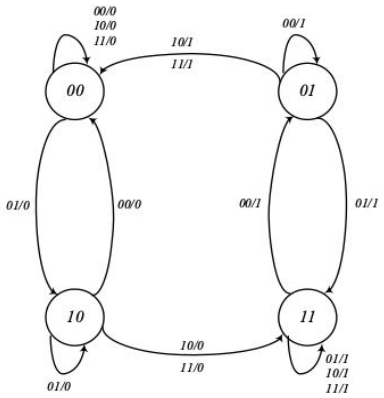
5.6 **(a)**



(b)

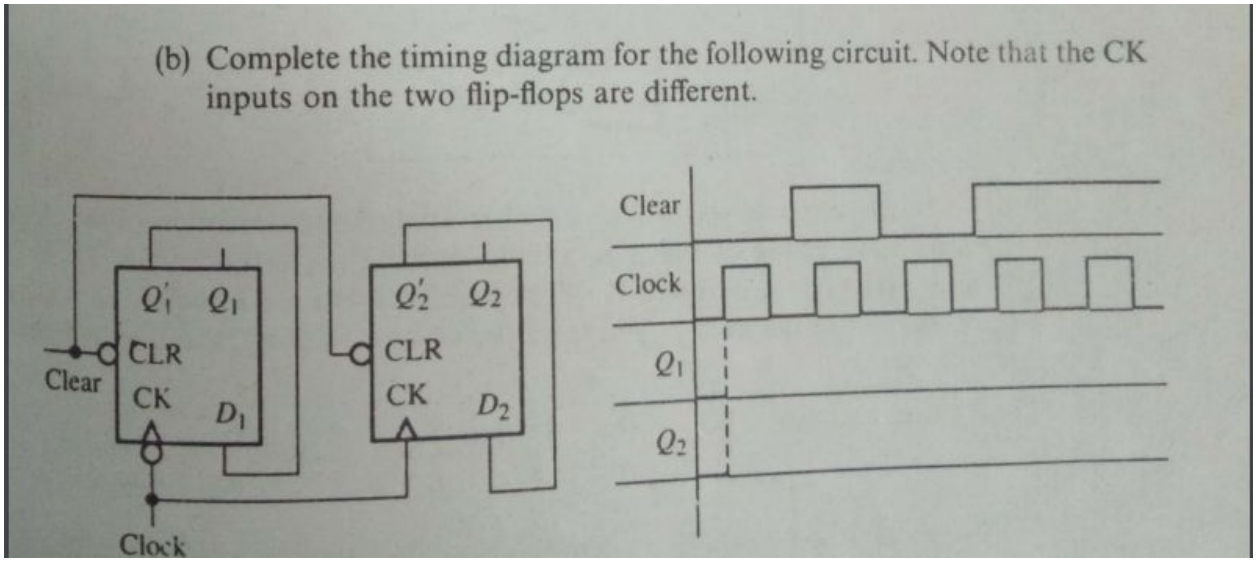
Present state		Inputs		Next state		Output
A	B	x	y	A	B	z
0	0	0	0	0	0	0
0	0	0	1	1	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	1	1
0	1	0	1	1	1	1
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	0	0	0
1	0	0	1	1	0	0
1	0	1	0	1	1	0
1	0	1	1	1	1	0
1	1	0	0	0	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

(c)

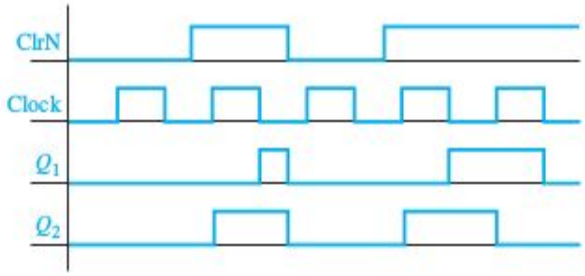


11.13 b)

(b) Complete the timing diagram for the following circuit. Note that the CK inputs on the two flip-flops are different.



sol:

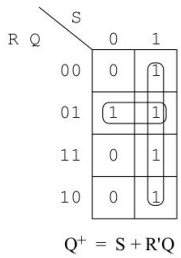


11.15 A set-dominant flip-flop is similar to the reset-dominant flip-flop of Problem 11.14 except that the input combination $S = R = 1$ sets the flip-flop. Repeat Problem 11.14 for a set-dominant flip-flop.

sol:

11.15 (a)

$S\,R\,Q$	Q^+
0 0 0	0
0 0 1	1
0 1 0	0
0 1 1	0
1 0 0	1
1 0 1	1
1 1 0	1
1 1 1	1



11.15 (b) A set-dominant FF from an S-R FF—The arrangement will ensure that when $S = R = 1$, $S_1 = 1$, $R_1 = 0$, and $Q^+ = 1$.