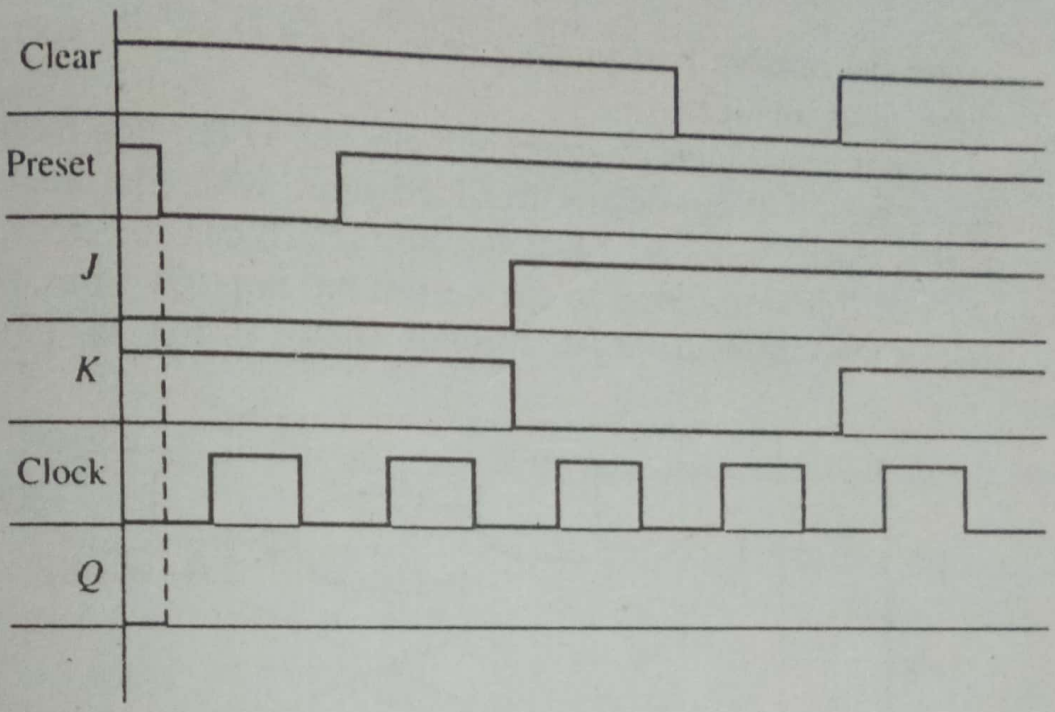
11.12 A gated latch (G-L flip-flop) behaves as follows: If $G = 0$, the flip-flop does not change state. If $G = 1$, the next state of the flip-flop is equal to the value of L.

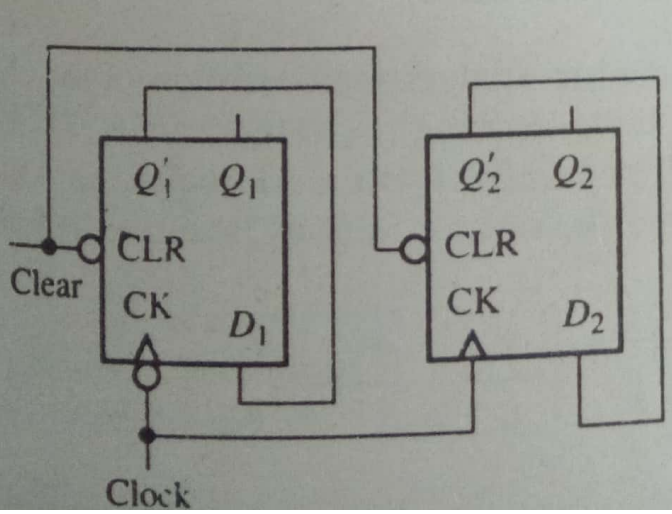
(a) Derive the characteristic (next-state) equation for the flip-flop.

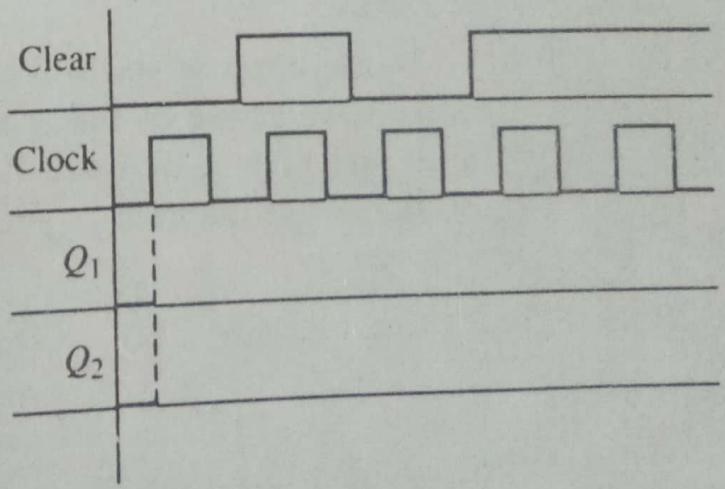
(b) Show how an S-R flip-flop can be converted to a G-L flip-flop by adding gate(s) and inverters(s). *Hint:* What values must S and R have so that the flip-flop will be set and reset at the proper time when $G = 1$? How can you prevent the flip-flop from changing state when $G = 0$?

11.13 (a) Complete the following timing diagram for the flip-flop of Fig. 11–20.



(b) Complete the timing diagram for the following circuit. Note that the CK inputs on the two flip-flops are different.





11.15 A set-dominant flip-flop is similar to the reset-dominant flip-flop of Problem 11.14 except that the input combination $S = R = 1$ sets the flip-flop. Repeat Problem 11.14 for a set-dominant flip-flop.

5.2 Construct a *JK* flip-flop, using a *D* flip-flop, a two-to-one-line multiplexer, and an inverter. (HDL—see Problem 5.34.)

5.3 Show that the characteristic equation for the complement output of a *JK* flip-flop is

$$Q'(t+1) = J'Q' + KQ$$

5.4 A *PN* flip-flop has four operations, no change, clear to 0, set 1 and complement, when inputs *P* and *N* are 00, 01, 10, and 11, respectively.

(a) Tabulate the characteristic table.
(b)* Derive the characteristic equation.
(c) Tabulate the excitation table.
(d) Show how the *PN* flip-flop can be converted to a *D* flip-flop.

5.5 Explain the differences among a truth table, a state table, a characteristic table, and an excitation table. Also, explain the difference among a Boolean equation, a state equation, a characteristic equation, and a flip-flop input equation.

5.6 A sequential circuit with two *D* flip-flops *A* and *B*, two inputs *x* and *y*, and one output *z* is specified by the following next-state and output equations (HDL—see Problem 5.35):

$$A(t+1) = x'y + xB$$
$$B(t+1) = x'A + xB$$
$$z = A$$

(a) Draw the logic diagram of the circuit.
(b) List the state table for the sequential circuit.
(c) Draw the corresponding state diagram.

5.8* Derive the state table and the state diagram of the sequential circuit shown in Fig. P5.8. Explain the function that the circuit performs. (HDL—see Problem 5.36.)

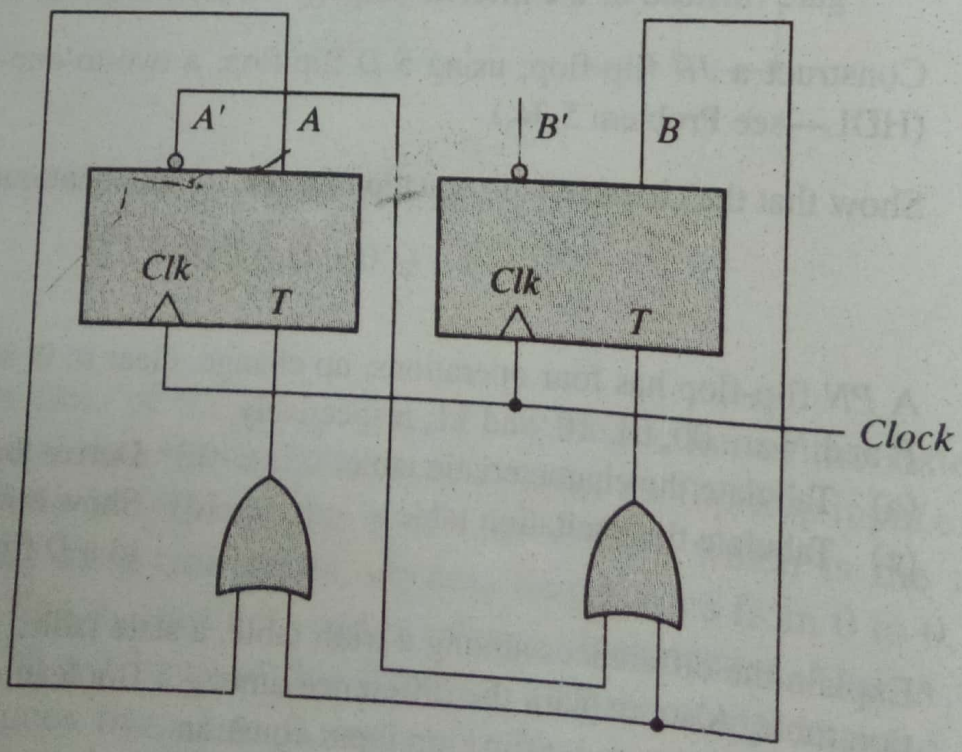


FIGURE P5.8

5.10 A sequential circuit has two *JK* flip-flops *A* and *B*, two inputs *x* and *y*, and one output *z*. The flip-flop input equations and circuit output equation are

$$J_A = Bx + B'y' \qquad K_A = B'xy'$$
$$J_B = A'x \qquad K_B = A + xy'$$
$$z = Ax'y' + Bx'y'$$

(a) Draw the logic diagram of the circuit.
(b) Tabulate the state table.
(c)* Derive the state equations for *A* and *B*.