Tutorial 6 (Extra Questions) Solutions

1. A sequential network has two inputs (Xu X2) and one output (Z). The output remains a constant value unless one of the following input sequences occurs:
(a) The input sequence XXX2 = 01, 00 causes the output to become 0.
(b) The input sequence XXX2 = 11, 00 causes the output to become 1.
(c) The input sequence XtX2 = 10, 00 causes the output to toggle.
Derive a Moore state table and state graph.

sol:

This should be solved in the same way as Example 3 on FLD p. 406. Assign a state to each possible input (00, 01, 11, 10) with an output of 0, and another state to each input with an output of 1. This gives eight states.
See FLD p. 657 for the state table.

State	Z = 0
S_0	Last input was 00
S_1	Last input was 01
S_2	Last input was 11
S_3	Last input was 10

State	Z = 1
S_4	Last input was 00
S_5	Last input was 01
S_6	Last input was 11
S_7	Last input was 10

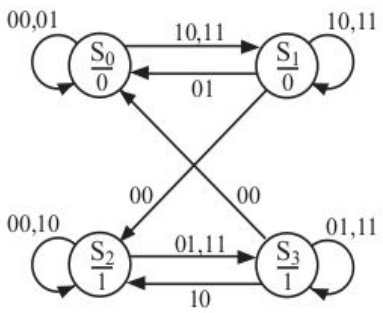
Each input takes you to the state defined by that input (e.g. an input of 01 takes you to either S_1 or S_5). The only thing in question is whether the output is 0 or 1. Determine the output by checking whether the last two inputs correspond to the three input sequences.

Alternate Solution: Notice that when $Z = 0$, "causes the output to become 0" is the same as remaining constant, and "causes the output to become 1" is the same as toggling the output. The situation is similar when $Z = 1$. So we can use only four states, as follows:

State	Meaning
S_0	Z= 0 and last input was either 00 or 01
S_1	$Z = 0$ and last input was either 10 or 11
S_2	$Z = 1$ and last input was either 00 or 10
S_3	$Z = 1$ and last input was either 01 or 11

State	Next State $X_1X_2 = 00$	01	11	10	Z
S_0	S_0	S_0	S_1	S_1	0
S_1	S_2	S_0	S_1	S_1	0
S_2	S_2	S_3	S_3	S_2	1
S_3	S_0	S_3	S_3	S_2	1

Note: The state table with 8 states reduces to this 4-state table using methods in Unit 15.



2.A sequential network has one input (X) and one output (Z). Draw a Mealy state graph for each of the following cases:

(a) The output is Z = 1 iff the total number of I's received is divisible by 3.
(Note: 0, 3, 6, 9,... are divisible by 3).

(b) The output is Z = 1 iff the total number of I's received is divisible by 3 and the total number of O's received is an even number greater than zero (9 states are sufficient).

sol:

a:Typical input and output sequence:

X = 0 0 1 0 0 1 1 0 0 0 1 1 0 1 0 0 1 ...

Z = 1 1 0 0 0 0 1 1 1 1 0 0 0 1 1 1 0 …

State	Meaning
S_0	Number of 1's is divisible by three
S_1	Number of 1's is one more than divisible by 3
S_2	Number of 1's is two more than divisible by 3

b:Typical input and output sequence:

X = 0 0 0 0 1 1 1 1 0 0 0 1 1 0 1 1 1 1 ...

Z = 0 1 0 1 0 0 1 0 0 0 0 0 0 1 0 0 1 0 …

State	Meaning
S_0	Number of 1's is divisible by three, no 0's
S_1	Number of 1's is one more than divisible by 3, no 0's
S_2	Number of 1's is two more than divisible by 3, no 0's
S_3	Number of 1's is divisible by three, number of 0's is odd
S_4	Number of 1's is one more than divisible by 3, number of 0's is odd
S_5	Number of 1's is two more than divisible by 3, number of 0's is odd
S_6	Number of 1's is divisible by three, number of 0's is even and < 0
S_7	Number of 1's is one more than divisible by 3, number of 0's is even and < 0
S_8	Number of 1's is two more than divisible by 3, number of 0's is even and < 0

3.A sequential circuit has two inputs and two outputs. The inputs (X 1 and X 2) represent a 2-bit binary number, N. If the present value of N is greater than the previous value, then Z 1 is 1. If the present value of N is less than the previous value, then Z 2 is 1. Otherwise, Z 1 and Z 2 are 0. When the first pair of inputs is received, there is no previous value of N, so we cannot determine whether the present N is greater than or less than the previous value; therefore, the "otherwise" category applies.

(a) Find a Mealy state table or graph for the circuit (minimum number of states, including starting state, is five).

(b) Find a Moore state table for the circuit (minimum number of states is 11).

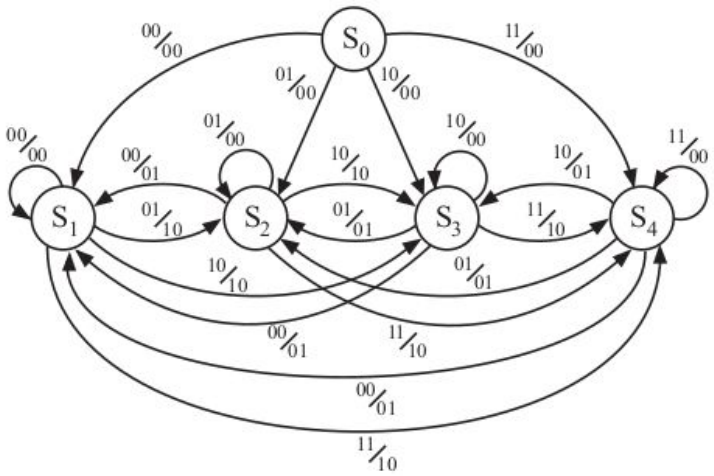
Sol:

(a) Typical input and output sequence:

$X_1 = 1\ 0\ 0\ 1\ 0\ 0\ 1\ 1\ 1\ 0\ \ldots$
$X_2 = 1\ 0\ 0\ 0\ 1\ 1\ 0\ 0\ 1\ 1\ \ldots$
$Z_1 = 0^*0\ 0\ 1\ 0\ 0\ 1\ 0\ 1\ 0\ \ldots$
$Z_2 = 0^*1\ 0\ 0\ 1\ 0\ 0\ 0\ 0\ 1\ \ldots$
* Regardless of any value of N.

See FLD p. 657 for state table.

State	Meaning
S_0	Reset
S_1	Previous input was 00
S_2	Previous input was 01
S_3	Previous input was 10
S_4	Previous input was 11



(b) Similar to part (a), but we need a separate state for each possible output and previous input.

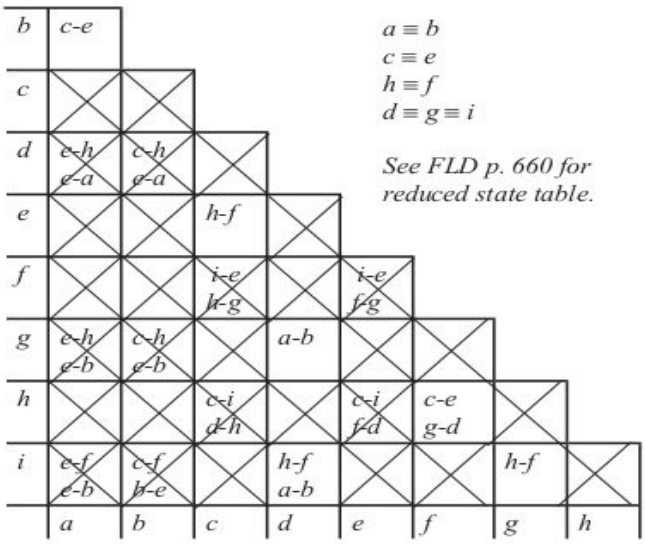
See FLD p. 658 for state table.

State	Meaning
S_0	Reset state / current output is = 00
S_1	Previous input was 00 / current output is = 00
S_2	Previous input was 00 / current output is = 01
S_3	Previous input was 01 / current output is = 10
S_4	Previous input was 01 / current output is = 00
S_5	Previous input was 01 / current output is = 01
S_6	Previous input was 10 / current output is = 10
S_7	Previous input was 10 / current output is = 00
S_8	Previous input was 10 / current output is = 01
S_9	Previous input was 11 / current output is = 10
S_{10}	Previous input was 11 / current output is = 00

4.Reduce the following state table to a minimum number of states.

Present State	Next State $X = 0$	1	Present Output (Z)
a	e	e	1
b	c	e	1
c	i	h	0
d	h	a	1
e	i	f	0
f	e	g	0
g	h	b	1
h	c	d	0
i	f	b	1

Sol:



5.Reduce the following state table to a minimum number of states:

(a)	$XY = 00$	01	11	10	Z
a	a	c	e	d	0
b	d	e	e	a	0
c	e	a	f	b	1
d	b	c	c	b	0
e	c	d	f	a	1
f	f	b	a	d	1

Sol:

(a) Set don't care to 0 so $S_2 \equiv S_4 \equiv S_5$:

Present State	Next State X=0	Next State 1	Output $X=0$	Output $X=1$
S_0	S_1	S_2	0	0
S_1	S_3	S_2	1	1
S_2	S_2	S_2	0	1
S_3	S_2	S_2	1	1

Set don't care to 0 so $S_1 \equiv S_3 \equiv S_4$:

Present State	Next State X=0	Next State 1	Output $X=0$	Output $X=1$
S_0^1	S_1^1	S_5^1	0	0
S_1^1	S_1^1	S_2^1	1	1
S_2^1	S_2^1	S_1^1	0	1
S_5^1	S_5^1	S_2^1	0	1

6.Circuits N and M have the state tables that follow.
(a) Without first reducing the tables, determine whether circuits N and M are equivalent.
(b) Reduce each table to a minimum number of states, and then show that N is equivalent to M by inspecting the reduced tables.

	M		
	$X=0$	1	
S_0	S_3	S_1	0
S_1	S_0	S_1	0
S_2	S_0	S_2	1
S_3	S_0	S_3	1

	N		
	$X=0$	1	
A	E	A	1
B	F	B	1
C	E	D	0
D	E	C	0
E	B	D	0
F	B	C	0

sol:

(a)

Straight Binary Assignment	Equivalent State Assignments (any three)				
	$c_2 \leftrightarrow c_3$	$c_1 \leftrightarrow c_3$	$c_1 \leftrightarrow c_2$	$c_1 \rightarrow c_3 \rightarrow c_2 \rightarrow c_1$	$c_1 \rightarrow c_2 \rightarrow c_3 \rightarrow c_1$
000	000	000	000	000	000
001	001	100	010	010	100
010	100	010	001	100	001
011	101	110	011	110	101
100	010	001	100	001	010
101	011	101	110	011	110
110	110	011	101	101	011
111	111	111	111	111	111

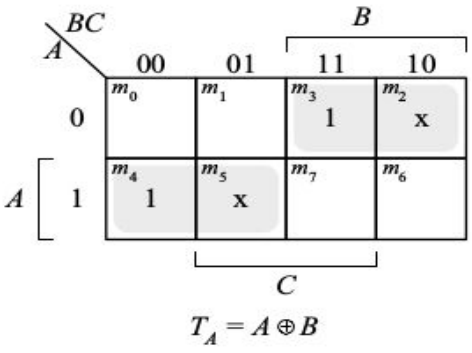
(b) Many state assignments are not equivalent to the straight binary assignment, for example:

111	111	etc.
101	001	
110	010	
100	011	
011	100	
010	101	
001	000	
000	110	

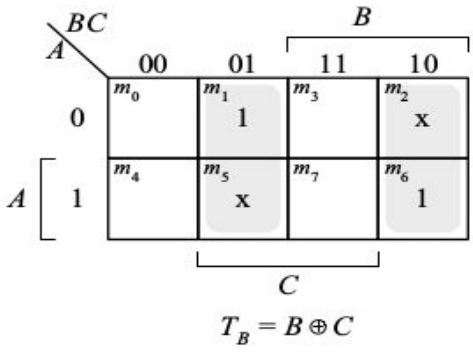
7.Design a counter with T flip-flops that goes through the following binary repeated sequence: 0, 1, 3, 7, 6, 4. Show that when binary states 010 and 101 are considered as don't care conditions, the counter may not operate properly. Find a way to correct the design.

sol:

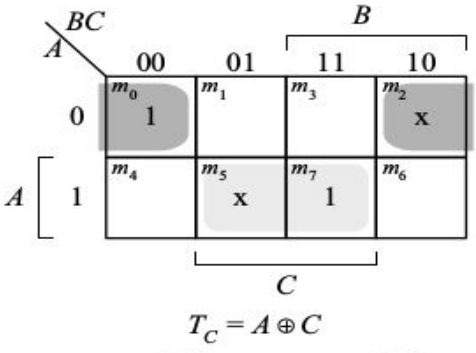
Present state ABC	*Next state ABC*	*Flip-flop inputs* T_A	T_B	T_C
000	001	0	0	1
001	011	0	1	0
010	xxx	x	x	x
011	111	1	1	0
100	000	1	1	0
101	xxx	x	x	x
110	100	0	1	0
111	110	0	0	1



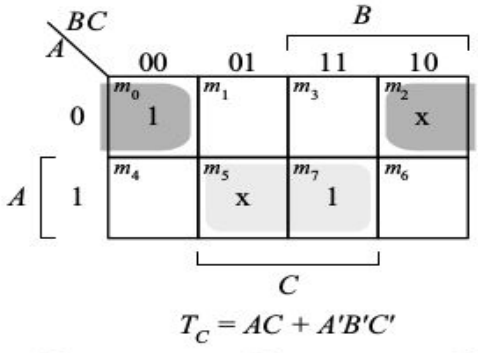
$T_A = A \oplus B$



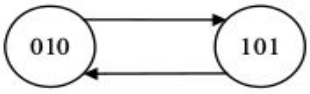
$T_B = B \oplus C$



$T_C = A \oplus C$



$T_C = AC + A'B'C'$



No self-correcting

Self-correcting