EE2016F19 Microprocessor Theory and Lab

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EE Dept – *IIT Madras 2018*

Course Information

- Course Information
  - Credit Scheme
  - Syllabus
  - Reference
    - William Stallings, “Computer Architecture and Organization:
    - Ppt Slides
  - Regular lab sessions and project
  - A quiz and Endsem (Theory)

Course Information

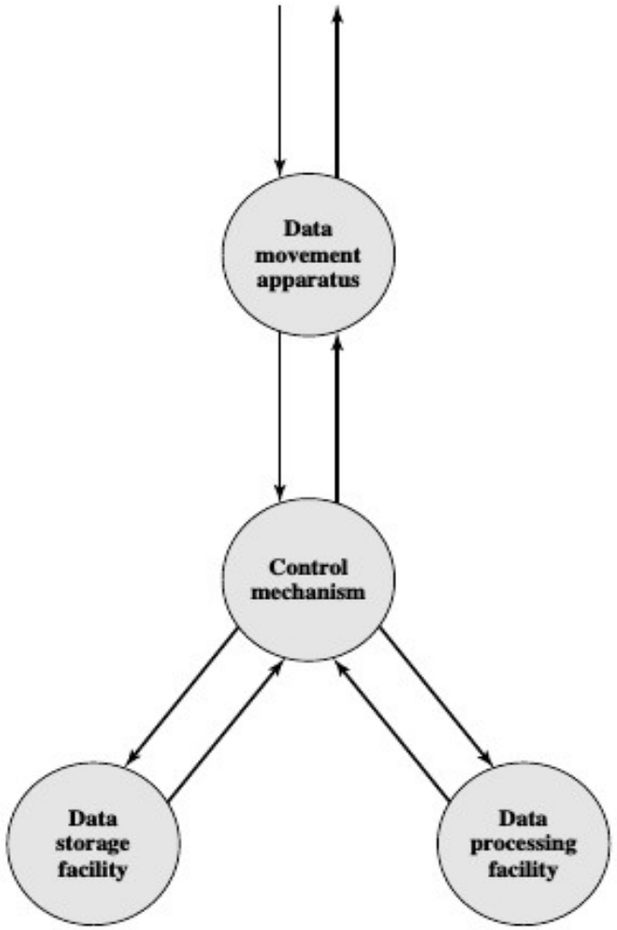
- Course Information

- Positioning of EE2016
  - Physics--> Electronics-->Digital Circuits--> Digital Systems--> EE2016
  - Future Courses
    - VLSI Design --> Algorithms for VLSI Design
    - VLSI Technology

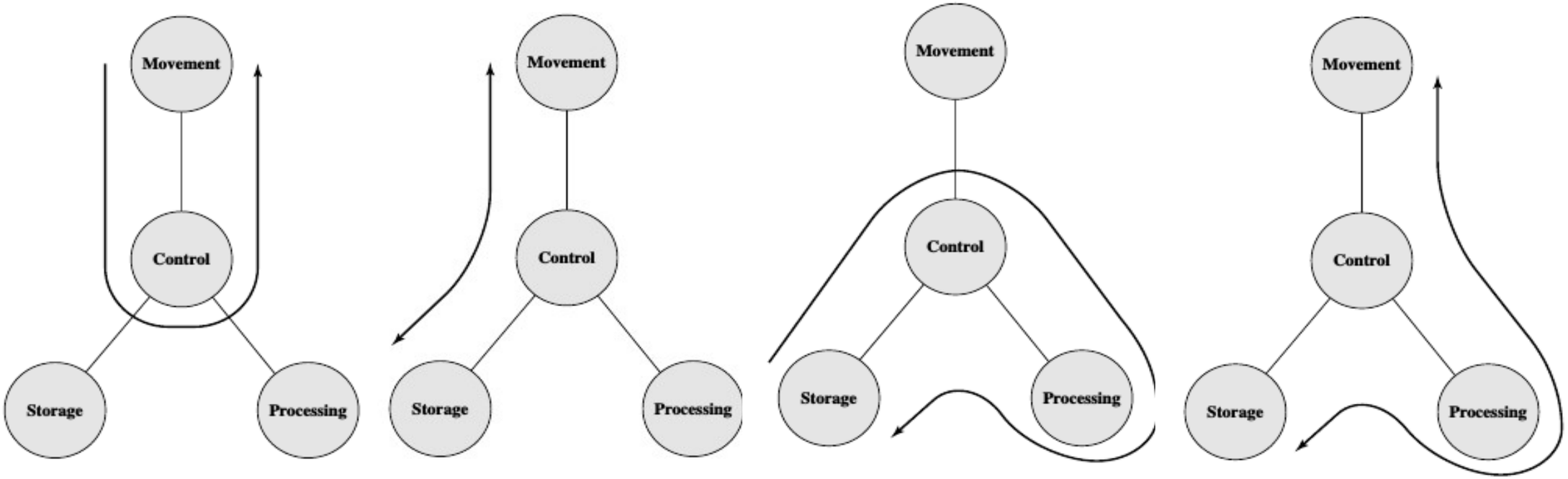
Lecture 1: Overview

- Overview of Microprocessors
  - Architecture and Organization
    - Difference?
  - Computer
  - Main frame, work station, server, microcomputer, microprocessor, embedded processor & systems and microcontroller in that order.

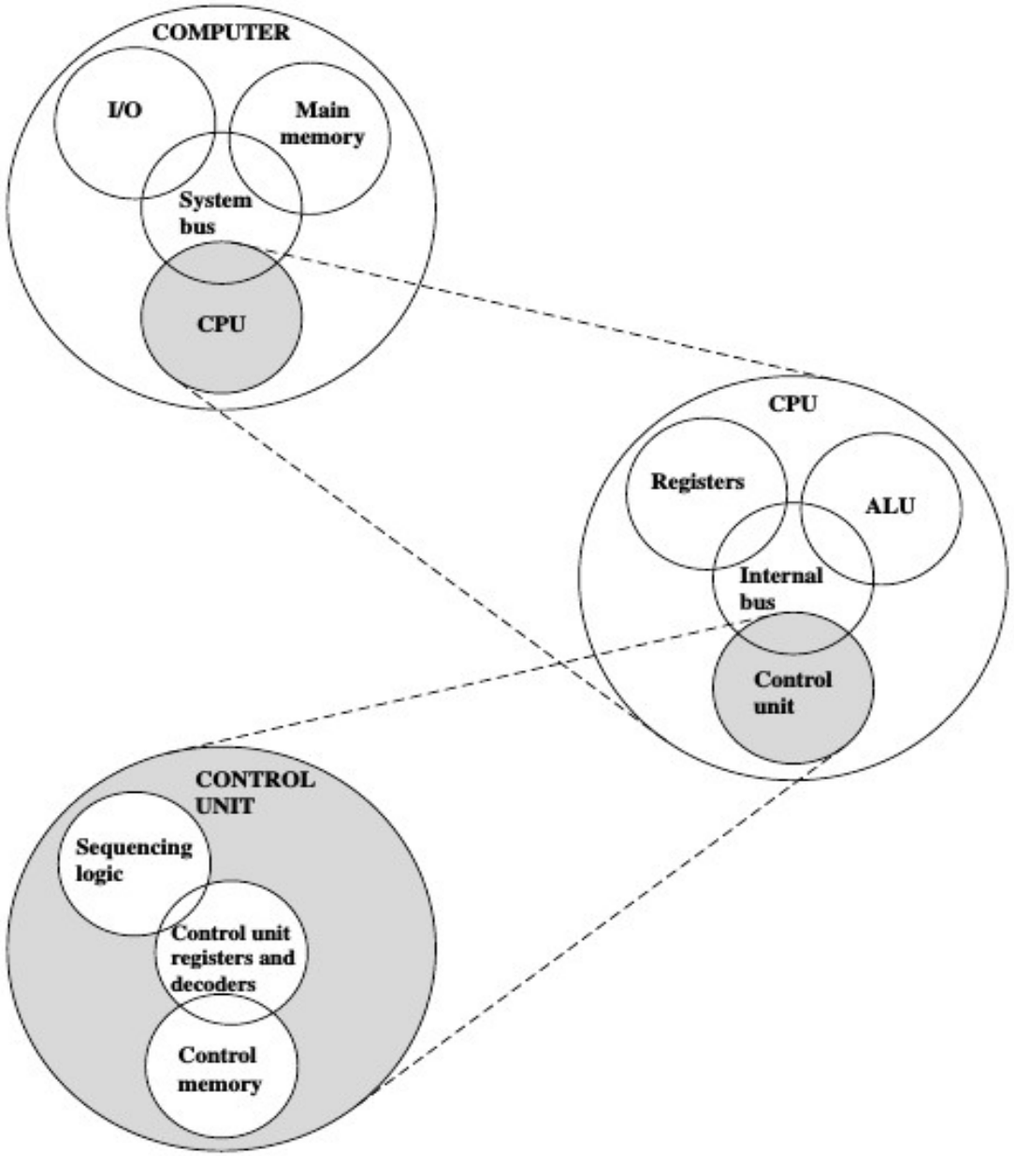
Computer Model



Possible Computer Operation Cycle



Computer: Top Level



Lecture 1: Overview

- Theory
  - Generic Microprocessor
  - In this course
    - Lab
      - Atmel Atmega 6 (16 bit processor)
      - ARM processor (ARM7)
  - Recall Digital Systems – Basics
    - Universal GATEs
    - Combinational Circuits
    - Sequential Circuits
    - Max-Min Representations
    - Flip-flops
    - Counters

Microprocessors

- Theory

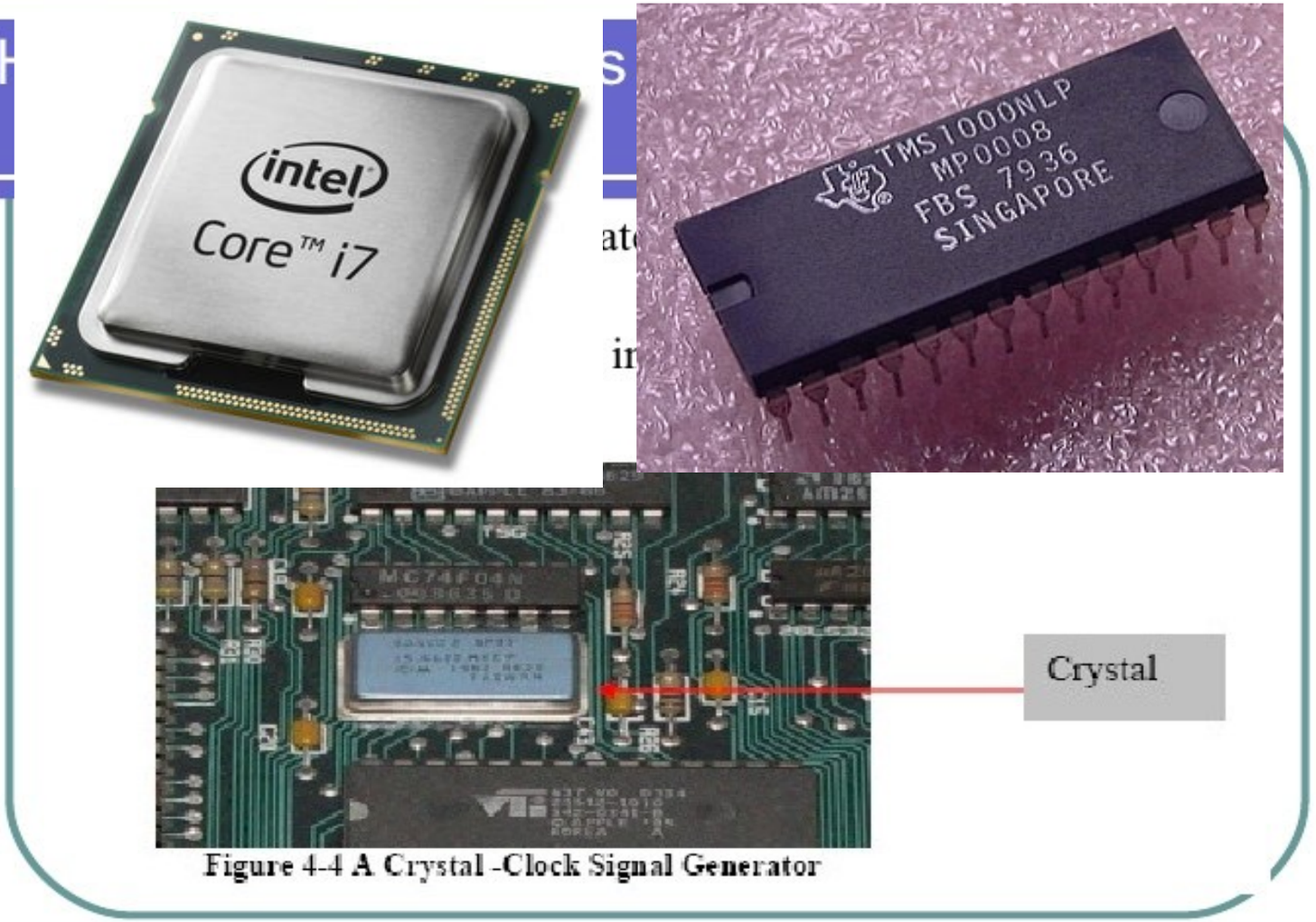
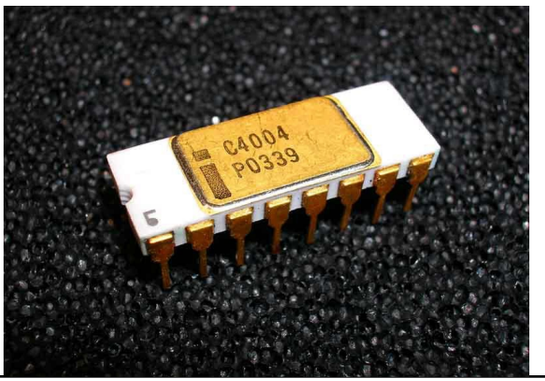
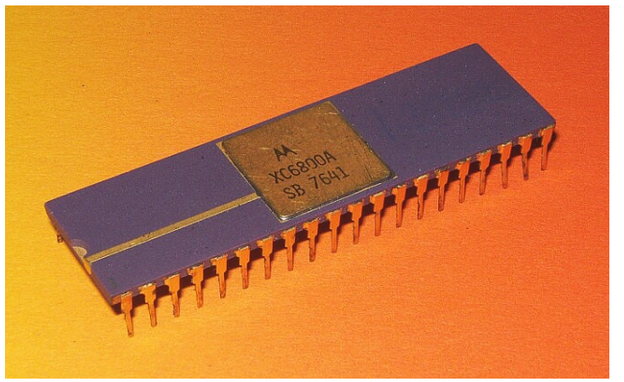


Figure 4-4 A Crystal -Clock Signal Generator

Microprocessor

- A Microprocessor
  - Is a multi-purpose clock driven, register based digital IC that accepts binary input processes it according to instructions stored in memory and provides results as output.
    - Combines combinational and sequential logic
    - Operate on numerals and symbols represented in binary numeral systems.
  - Before microprocessors, small computers were built using racks of circuit boards.



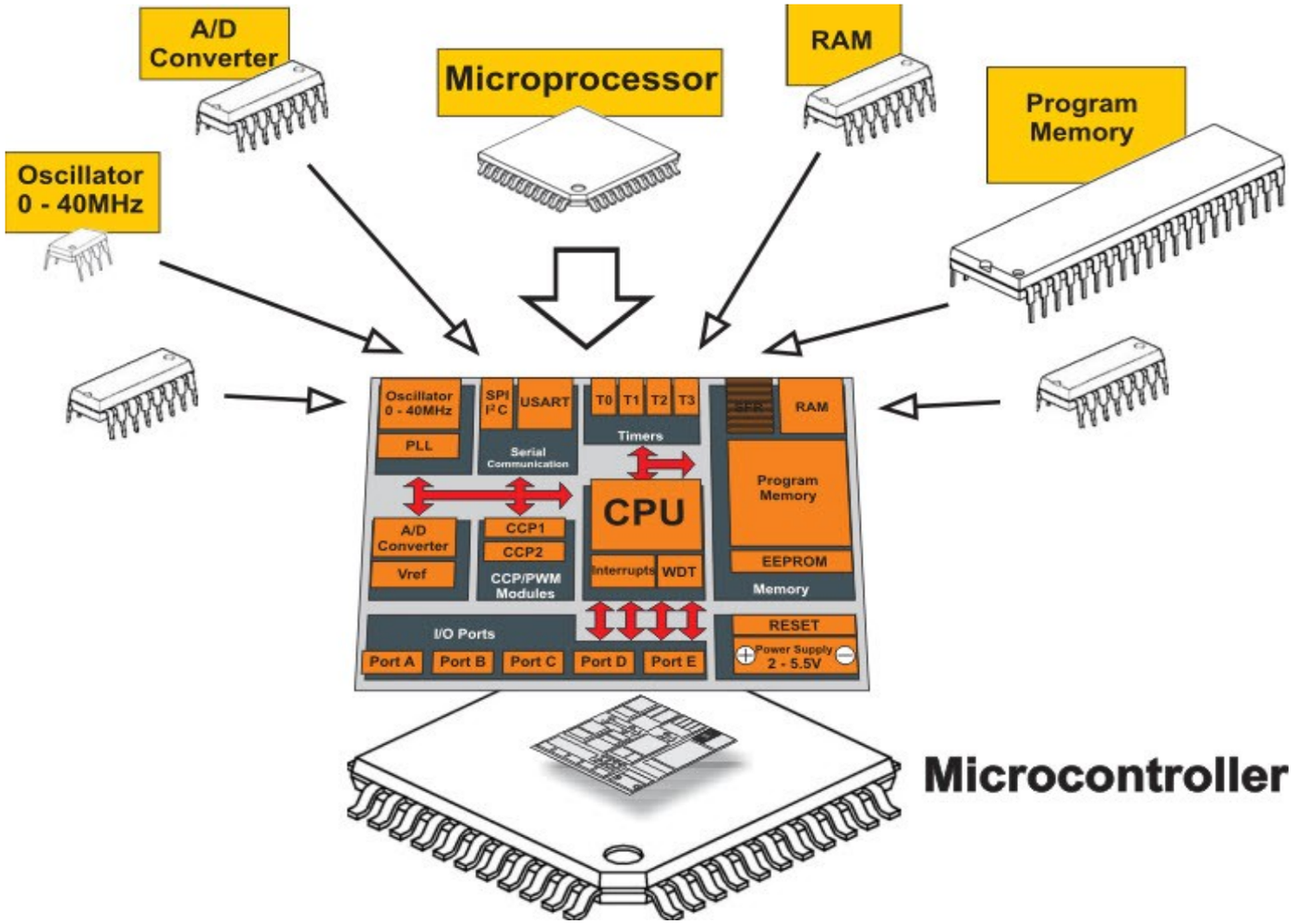


Microprocessor

- A Microprocessor
  - Computing machines of decreasing computing power: Main frame (parallel), work station (multicore), server (multicore), CPU (desktop), microcomputer, microprocessor, embedded processor & systems, microcontroller, wearables in that order.
  - 1943: Computers, 1968's microcontrollers
- Theory
  - Generic Microprocessor
  - In this course
    - Lab
      - Atmel Atmega 6 (16 bit processor)
      - ARM processor (ARM7)

MicroController Architecture

- Microcontroller

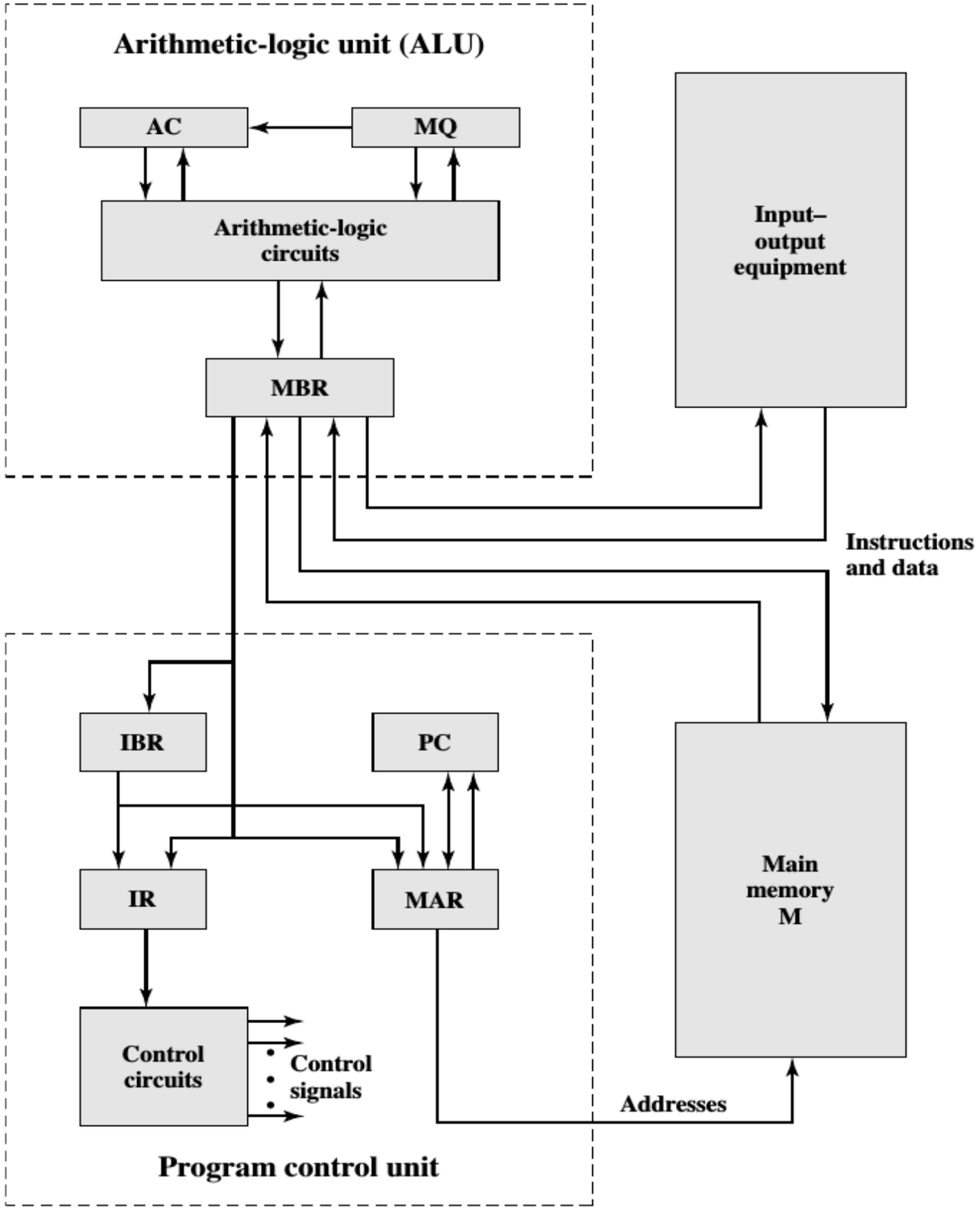


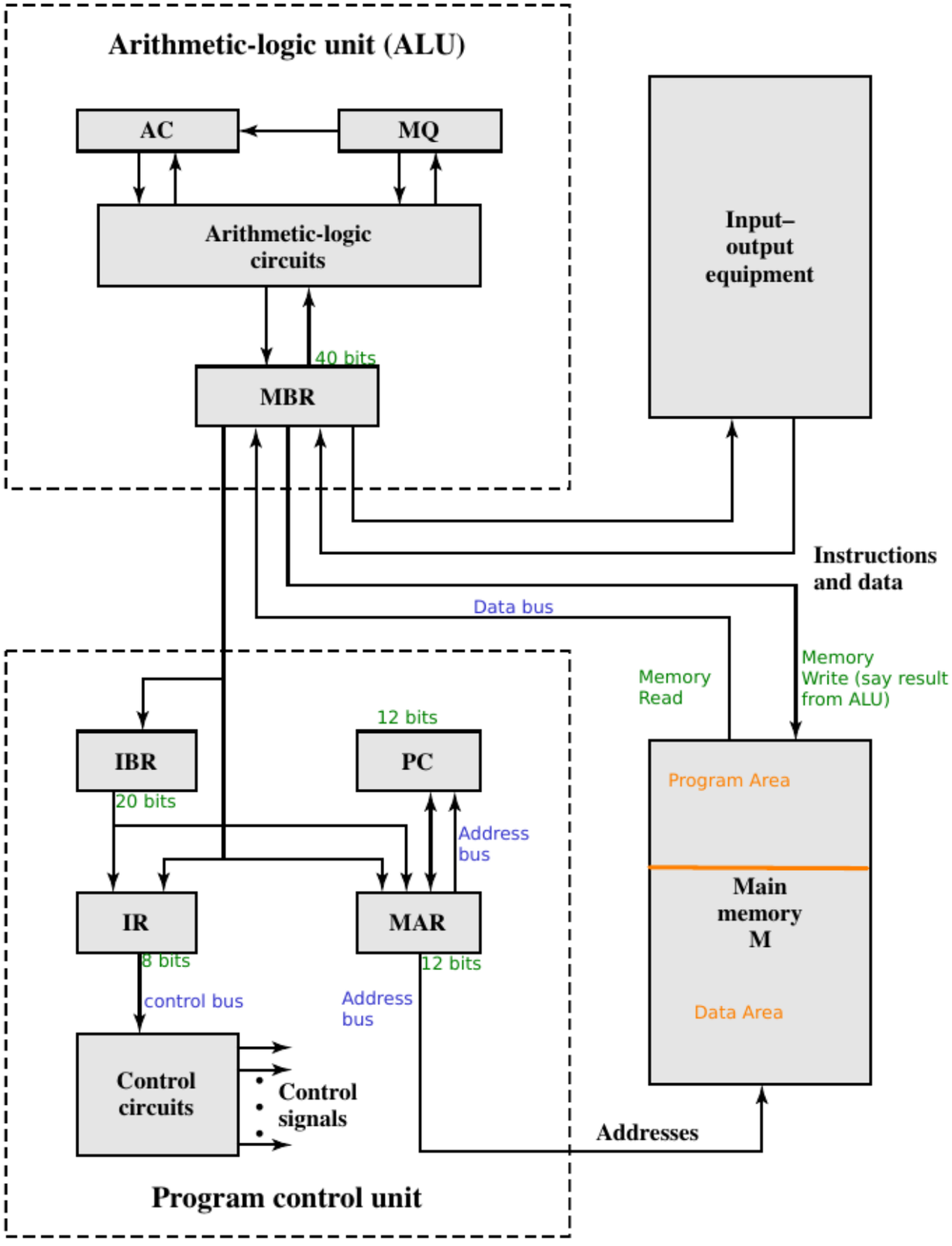
Microprocessor Vs Microcontroller

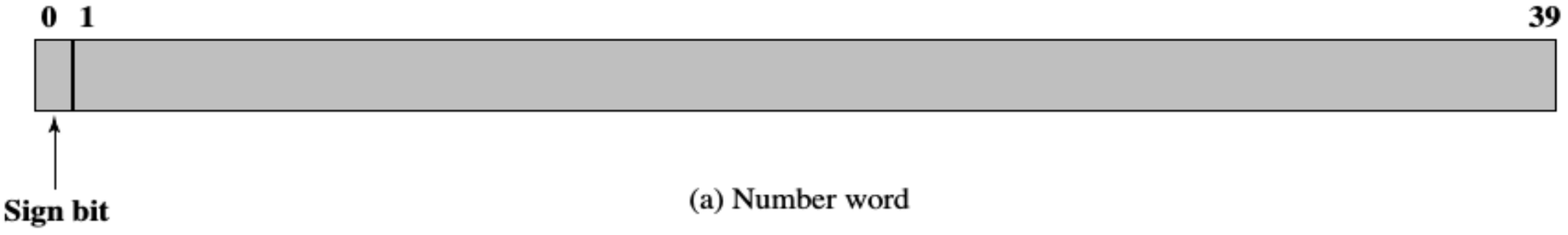
- Microprocessor
  - Provides mainly the CPU
  - Without RAM, ROM and peripherals
  - General purpose computation: could be used for anything from simple to more memory / computationally intensive applications
- Microcontroller
  - A complete computer despite designed optimally for a specific task
    - This means RAM & ROM / EPROM are all built-in
  - Metal oxide semiconductor technology --> cheaper
  - Processing speed lower
  - Power consumption is lesser

Microprocessor Vs Microcontroller

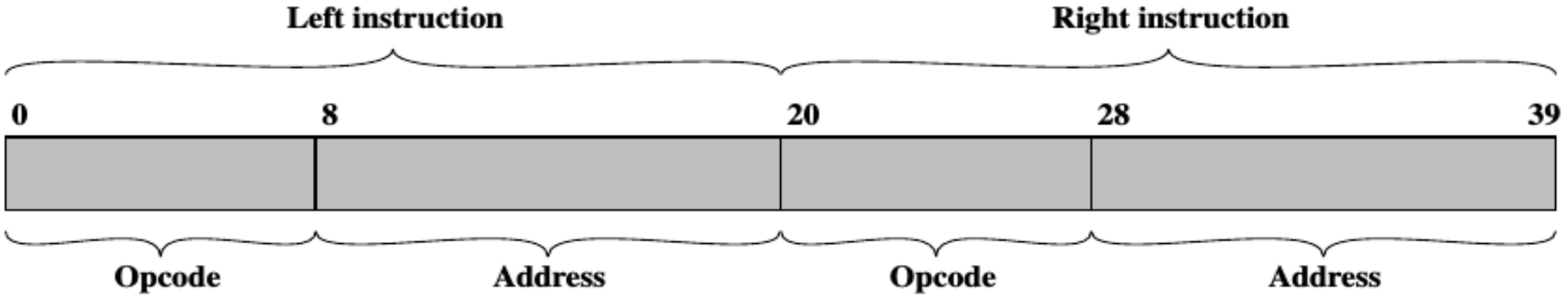
- Atmel Atmega8 is a microcontroller while ARM is a microprocessor
- ARM is a microprocessor architectural design
  - (not a physical processor, its called core) which ARM holdings inc, gives licence to others.
  - Manufacturer could fabricate either a microprocessor or microcontroller.
- Main Architectural Difference
  - Microcontrollers are based on Harvard architecture where program memory and data memory are separate
  - while microprocessors are based on von Neumann model where program and data are stored in same memory module.

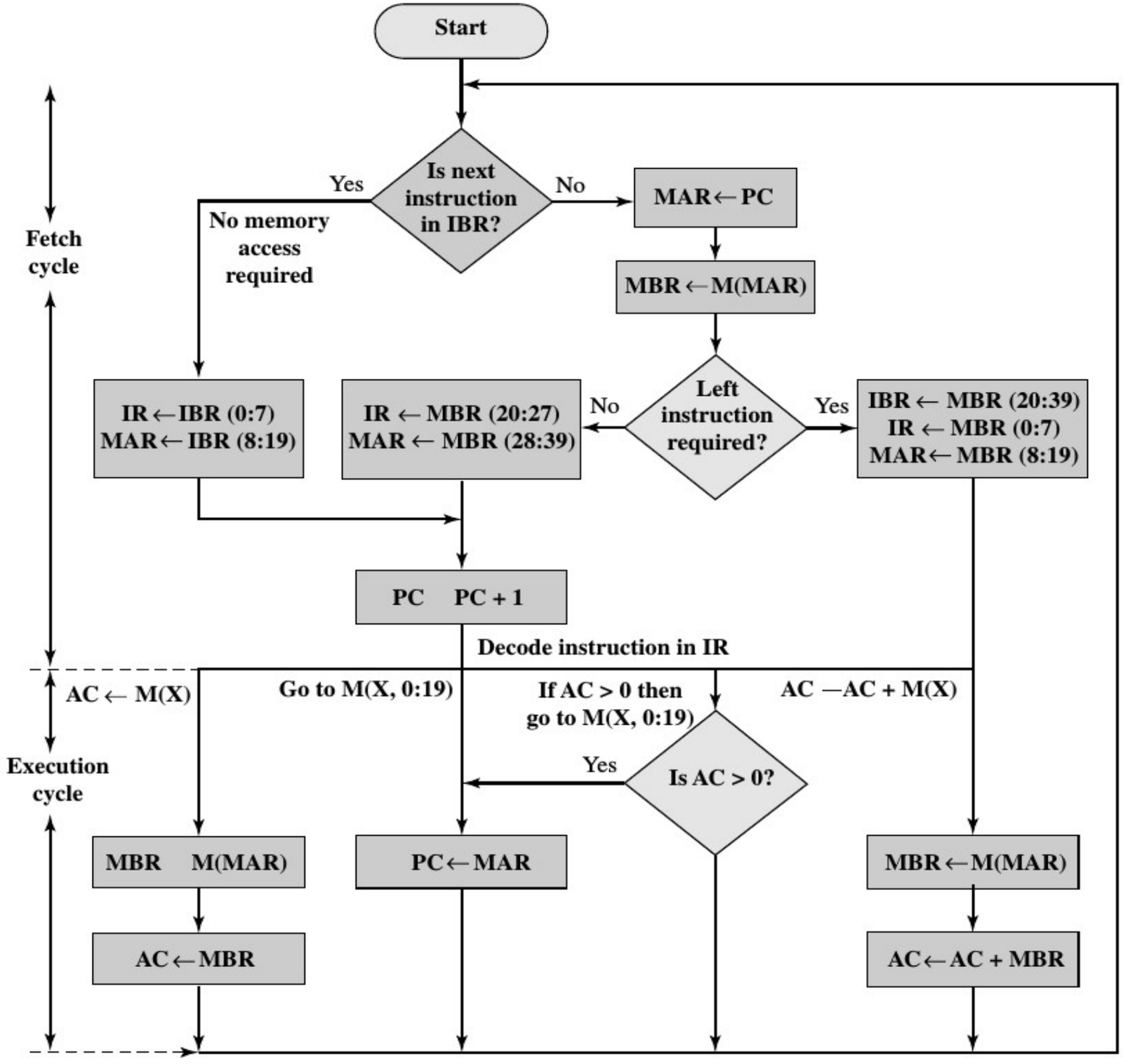

Arithmetic-logic unit (ALU)
AC
MQ
Arithmetic-logic circuits
MBR
Input–output equipment
Instructions and data
IBR
PC
IR
MAR
Main memory M
Control circuits
Control signals
Addresses
Program control unit

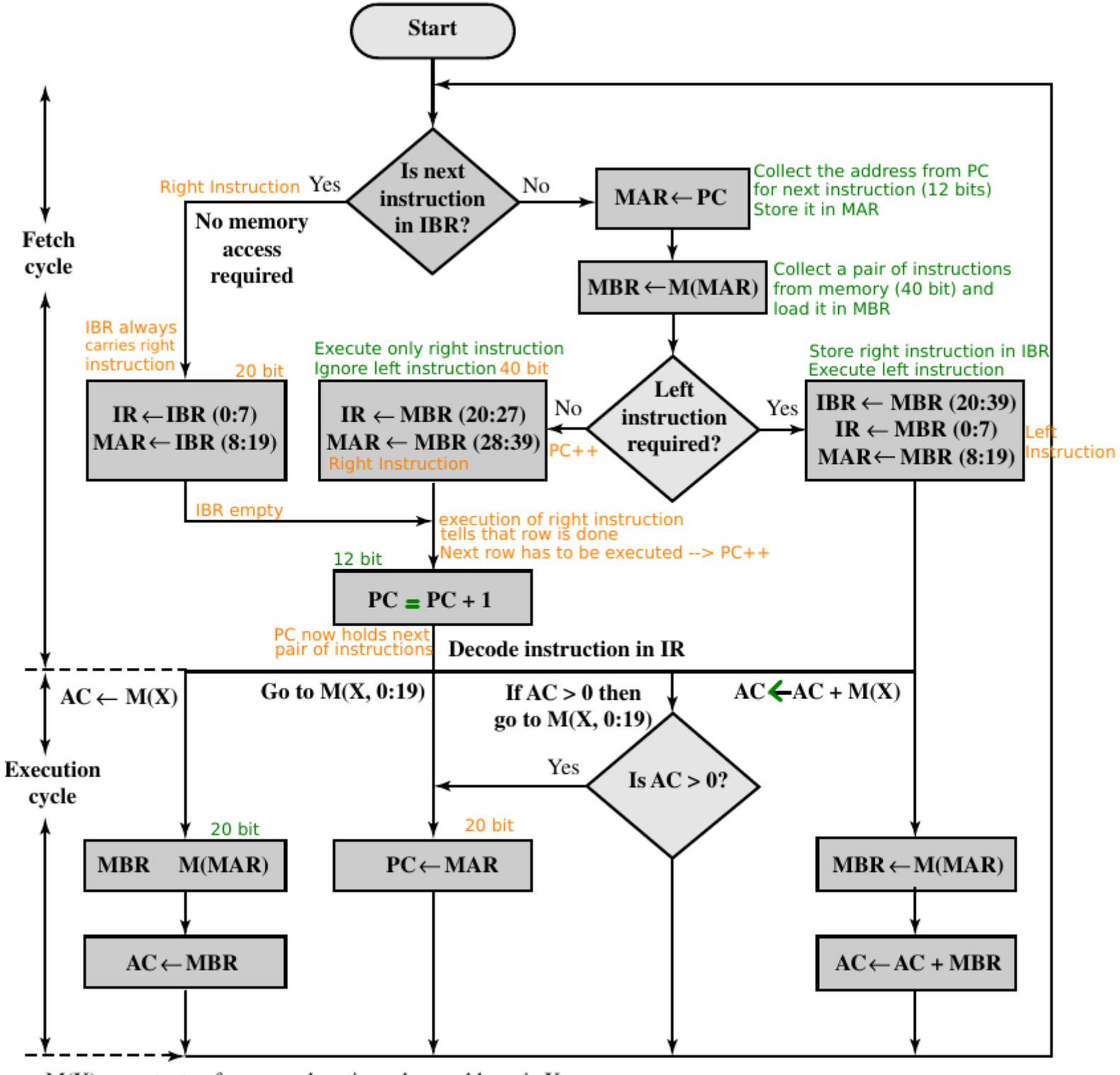

Arithmetic-logic unit (ALU)
AC
MQ
Arithmetic-logic circuits
40 bits
MBR
Input–output equipment
Instructions and data
Data bus
Memory Read
Memory Write (say result from ALU)
12 bits
IBR
PC
20 bits
Address bus
IR
MAR
8 bits
12 bits
control bus
Address bus
Control circuits
Control signals
Program Area
Main memory M
Data Area
Addresses
Program control unit



(a) Number word




Start
Is next instruction in IBR?
Yes
No
No memory access required
MAR ← PC
MBR ← M(MAR)
Left instruction required?
No
Yes
IR ← IBR (0:7)
MAR ← IBR (8:19)
IR ← MBR (20:27)
MAR ← MBR (28:39)
IBR ← MBR (20:39)
IR ← MBR (0:7)
MAR ← MBR (8:19)
PC PC + 1
Decode instruction in IR
Fetch cycle
Execution cycle
AC ← M(X)
Go to M(X, 0:19)
If AC > 0 then go to M(X, 0:19)
AC —AC + M(X)
Is AC > 0?
Yes
MBR M(MAR)
PC ← MAR
MBR ← M(MAR)
AC ← MBR
AC ← AC + MBR
M(X) = contents of memory location whose address is X
(i:j) = bits i through j



M(X) = contents of memory location whose address is X
(i:j) = bits i through j

- Van Neumann machine
  - Program (sequence of instructions) & data are stored in the same memory.
  - Advantages – (a) just-in-time compilation (b) self-modifying codes
  - Disadvantages – prone to (a) malaware and (b) software defects (c) data transfer and instruction fetches could not be performed at the same time (needed two clock cycles)

Harvard architecture

- Program (sequence of instructions) & data are stored in the physically separate storage area

- Advantages: (a) storage area & signal pathways (buses) are different & hence simultaneous access is possible (b) one instruction per cycle?
- Disadvantages: (a) embedding the data within instructions are often needed (ex. Self modifying code / ARM debugger break points etc), which is not possible if the memory is difference

A combination of modified Harvard and van Neumann machine is used in modern designs

- Split-cache version of modified Harvard architecture

- **Data transfer:** Move data between memory and ALU registers or between two ALU registers.
- **Unconditional branch:** Normally, the control unit executes instructions in sequence from memory. This sequence can be changed by a branch instruction, which facilitates repetitive operations.
- **Conditional branch:** The branch can be made dependent on a condition, thus allowing decision points.
- **Arithmetic:** Operations performed by the ALU.
- **Address modify:** Permits addresses to be computed in the ALU and then inserted into instructions stored in memory. This allows a program considerable addressing flexibility.

Instruction Type	Opcode	Symbolic Representation	Description
Data transfer	00001010	LOAD MQ	Transfer contents of register MQ to the accumulator AC
	00001001	LOAD MQ,M(X)	Transfer contents of memory location X to MQ
	00100001	STOR M(X)	Transfer contents of accumulator to memory location X
	00000001	LOAD M(X)	Transfer M(X) to the accumulator
	00000010	LOAD −M(X)	Transfer −M(X) to the accumulator
	00000011	LOAD |M(X)|	Transfer absolute value of M(X) to the accumulator
	00000100	LOAD −|M(X)|	Transfer −|M(X)| to the accumulator
Unconditional branch	00001101	JUMP M(X,0:19)	Take next instruction from left half of M(X)
	00001110	JUMP M(X,20:39)	Take next instruction from right half of M(X)
Conditional branch	00001111	JUMP+ M(X,0:19)	If number in the accumulator is nonnegative, take next instruction from left half of M(X)
	00010000	JUMP+ M(X,20:39)	If number in the accumulator is nonnegative, take next instruction from right half of M(X)
Arithmetic	00000101	ADD M(X)	Add M(X) to AC; put the result in AC
	00000111	ADD |M(X)|	Add |M(X)| to AC; put the result in AC
	00000110	SUB M(X)	Subtract M(X) from AC; put the result in AC
	00001000	SUB |M(X)|	Subtract |M(X)| from AC; put the remainder in AC
	00001011	MUL M(X)	Multiply M(X) by MQ; put most significant bits of result in AC, put least significant bits in MQ
	00001100	DIV M(X)	Divide AC by M(X); put the quotient in MQ and the remainder in AC
	00010100	LSH	Multiply accumulator by 2; i.e., shift left one bit position
	00010101	RSH	Divide accumulator by 2; i.e., shift right one position
Address modify	00010010	STOR M(X,8:19)	Replace left address field at M(X) by 12 rightmost bits of AC
	00010011	STOR M(X,28:39)	Replace right address field at M(X) by 12 rightmost bits of AC

Generation	Approximate Dates	Technology	Typical Speed (operations per second)
1	1946–1957	Vacuum tube	40,000
2	1958–1964	Transistor	200,000
3	1965–1971	Small and medium scale integration	1,000,000
4	1972–1977	Large scale integration	10,000,000
5	1978–1991	Very large scale integration	100,000,000
6	1991–	Ultra large scale integration	1,000,000,000

Model Number	First Delivery	CPU Technology	Memory Technology	Cycle Time (μs)	Memory Size (K)	Number of Opcodes	Number of Index Registers	Hardwired Floating-Point	I/O Overlap (Channels)	Instruction Fetch Overlap	Speed (relative to 701)
701	1952	Vacuum tubes	Electrostatic tubes	30	2–4	24	0	no	no	no	1
704	1955	Vacuum tubes	Core	12	4–32	80	3	yes	no	no	2.5
709	1958	Vacuum tubes	Core	12	32	140	3	yes	yes	no	4
7090	1960	Transistor	Core	2.18	32	169	3	yes	yes	no	25
7094 I	1962	Transistor	Core	2	32	185	7	yes (double precision)	yes	yes	30
7094 II	1964	Transistor	Core	1.4	32	185	7	yes (double precision)	yes	yes	50

Table 2.6 Evolution of Intel Microprocessors

(a) 1970s Processors

	4004	8008	8080	8086	8088
Introduced	1971	1972	1974	1978	1979
Clock speeds	108 kHz	108 kHz	2 MHz	5 MHz, 8 MHz, 10 MHz	5 MHz, 8 MHz
Bus width	4 bits	8 bits	8 bits	16 bits	8 bits
Number of transistors	2,300	3,500	6,000	29,000	29,000
Feature size (μm)	10		6	3	6
Addressable memory	640 Bytes	16 KB	64 KB	1 MB	1 MB

(b) 1980s Processors

	80286	386TM DX	386TM SX	486TM DX CPU
Introduced	1982	1985	1988	1989
Clock speeds	6 MHz–12.5 MHz	16 MHz–33 MHz	16 MHz–33 MHz	25 MHz–50 MHz
Bus width	16 bits	32 bits	16 bits	32 bits
Number of transistors	134,000	275,000	275,000	1.2 million
Feature size (μm)	1.5	1	1	0.8–1
Addressable memory	16 MB	4 GB	16 MB	4 GB
Virtual memory	1 GB	64 TB	64 TB	64 TB
Cache	—	—	—	8 kB

Table 2.6 Continued

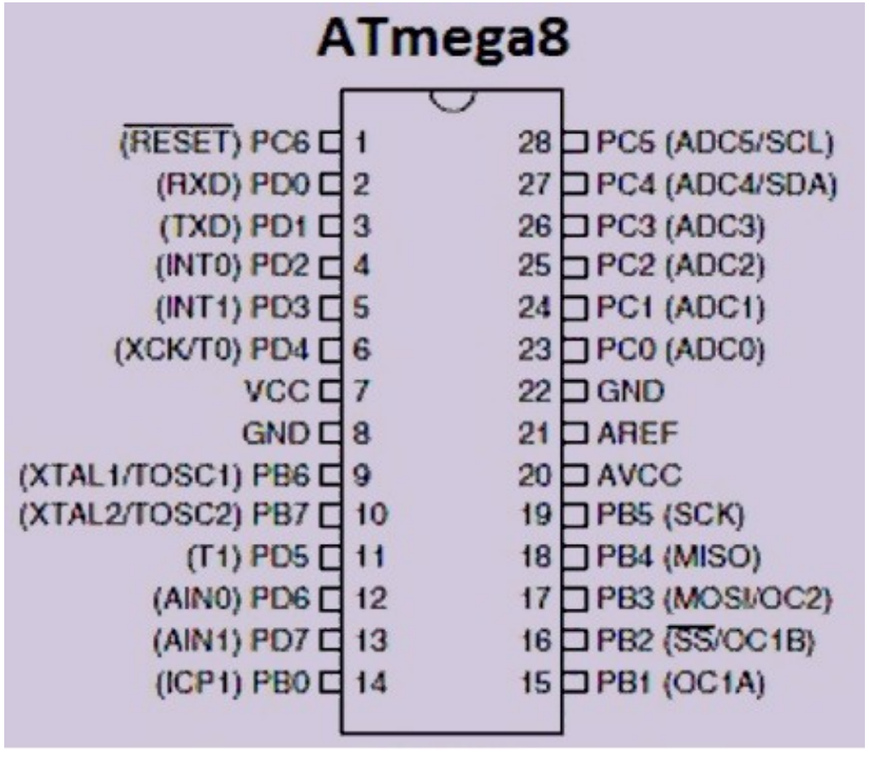
(c) 1990s Processors

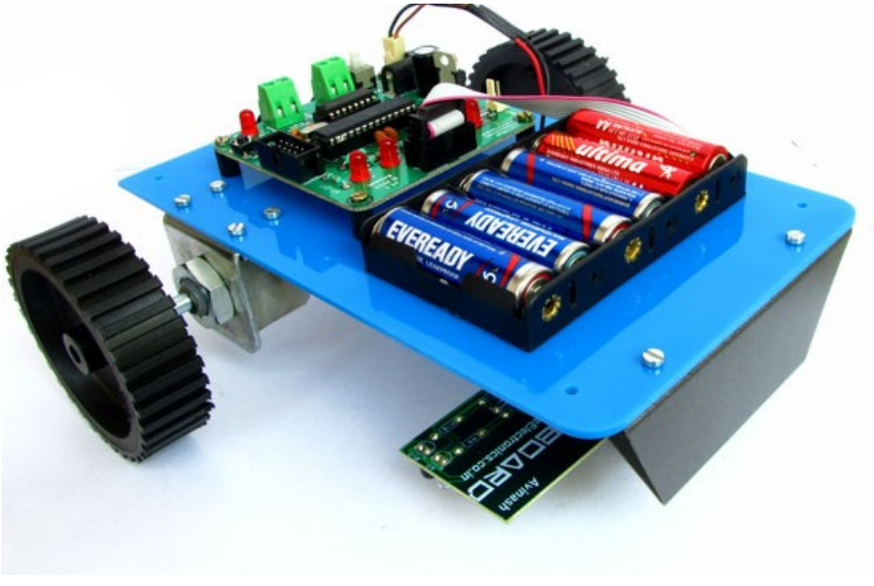
	486TM SX	Pentium	Pentium Pro	Pentium II
Introduced	1991	1993	1995	1997
Clock speeds	16 MHz–33 MHz	60 MHz–166 MHz,	150 MHz–200 MHz	200 MHz–300 MHz
Bus width	32 bits	32 bits	64 bits	64 bits
Number of transistors	1.185 million	3.1 million	5.5 million	7.5 million
Feature size (μm)	1	0.8	0.6	0.35
Addressable memory	4 GB	4 GB	64 GB	64 GB
Virtual memory	64 TB	64 TB	64 TB	64 TB
Cache	8 kB	8 kB	512 kB L1 and 1 MB L2	512 kB L2

(d) Recent Processors

	Pentium III	Pentium 4	Core 2 Duo	Core 2 Quad
Introduced	1999	2000	2006	2008
Clock speeds	450–660 MHz	1.3–1.8 GHz	1.06–1.2 GHz	3 GHz
Bus sidth	64 bits	64 bits	64 bits	64 bits
Number of transistors	9.5 million	42 million	167 million	820 million
Feature size (nm)	250	180	65	45
Addressable memory	64 GB	64 GB	64 GB	64 GB
Virtual memory	64 TB	64 TB	64 TB	64 TB
Cache	512 kB L2	256 kB L2	2 MB L2	6 MB L2

Atmel AVR Processors

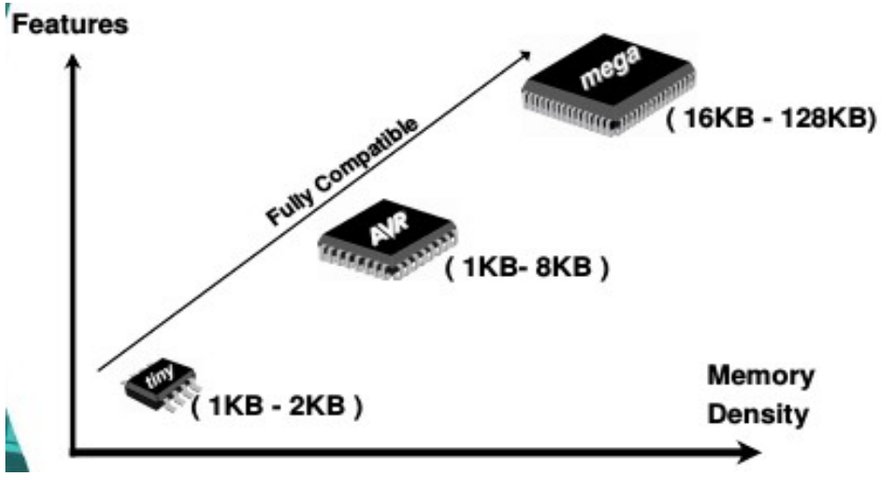




Advantages of Atmel AVR Processors

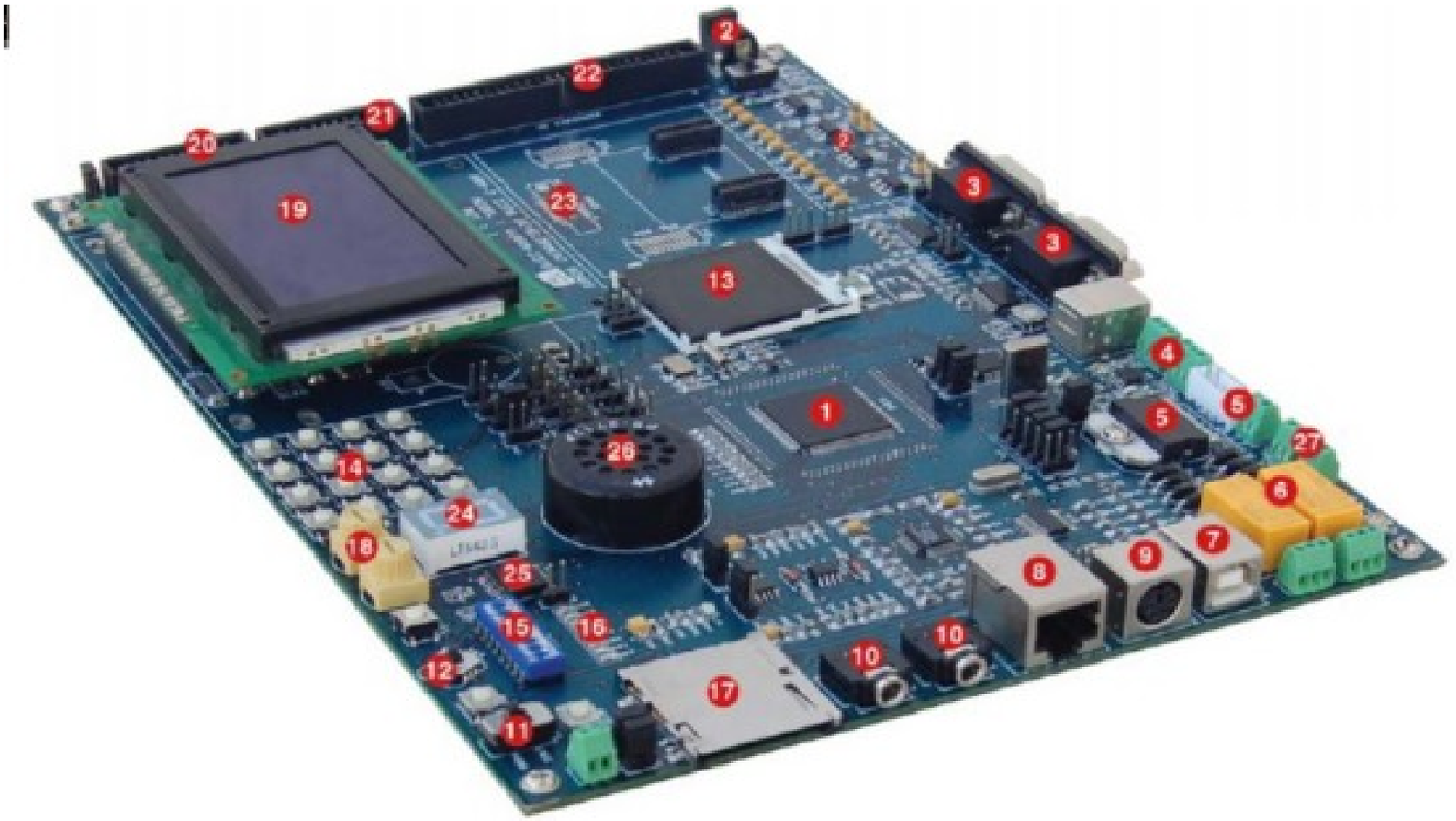
- High Performance 8-Bit MCU
- RISC Architecture
  - 32 Registers
  - 2-Address Instructions
  - Single Cycle Execution
- Low Power
- Large linear address spaces
- Efficient C Language Code Density
- On-chip in-system programmable memories

- Smart Battery
- Advanced Battery Charger
- Power Meter
- Temperature Logger
- Voltage Logger
- Tension Control
- Touch Screen Sensor
- Metering Applications
- UPS
- 3 Phase Motor Controller
- Industrial Control
- Power Management



Vi Microsystem’s ViARM LPC2378 Development Board

ViARM2378 ARM Development Board



In our lab ViARM2378 TFT LCD is not provided

1. NXP LPC2378 Micro controller (TQFP-144 Packaging).
2. Power supply section.
3. UART.
4. CAN Port.
5. Stepper Motor.
6. Relay.
7. USB 2.0 Device Conne
8. 10/100 Base T Ethernet Connector.
9. PS2- Keyboard connector.
10. Stereo Jack for USB Audio Device.
11. Prog/Exec Switch.
12. Joystick.
13. TFT LCD.
14. 4 x 4 Matrix Keypad.
15. 8 Way DIP switch.
16. LED.
17. SD Card Socket.
18. Analog input Trimmer.
19. 128 x 64 Pixels Graphics LCD.
20. Jtag Connector.
21. ADC, DAC and PWM Expansion slot.
22. 50Pin Expansion Header.
23. J-Trace.
24. Seven Segment Display.
25. Serial EEPROM.
26. Speaker.
27. Temperature Sensor

- Microprocessor Speed
  - Technology
    - Reduction of component size & lead length
    - Parallelism
    - Pipelining
  - -- Branch prediction
  - -- Data flow analysis
  - -- Speculative execution

T

Market	Embedded Device
Automotive	Ignition system Engine control Brake system
Consumer electronics	Digital and analog televisions Set-top boxes (DVDs, VCRs, Cable boxes) Personal digital assistants (PDAs) Kitchen appliances (refrigerators, toasters, microwave ovens) Automobiles Toys/games Telephones/cell phones/pagers Cameras Global positioning systems
Industrial control	Robotics and controls systems for manufacturing Sensors
Medical	Infusion pumps Dialysis machines Prosthetic devices Cardiac monitors
Office automation	Fax machine Photocopier Printers Monitors Scanners

Table 2.8 ARM Evolution

Family	Notable Features	Cache	Typical MIPS @ MHz
ARM1	32-bit RISC	None	
ARM2	Multiply and swap instructions; Integrated memory management unit, graphics and I/O processor	None	7 MIPS @ 12 MHz
ARM3	First use of processor cache	4 KB unified	12 MIPS @ 25 MHz
ARM6	First to support 32-bit addresses; floating-point unit	4 KB unified	28 MIPS @ 33 MHz
ARM7	Integrated SoC	8 KB unified	60 MIPS @ 60 MHz
ARM8	5-stage pipeline; static branch prediction	8 KB unified	84 MIPS @ 72 MHz
ARM9		16 KB/16 KB	300 MIPS @ 300 MHz
ARM9E	Enhanced DSP instructions	16 KB/16 KB	220 MIPS @ 200 MHz
ARM10E	6-stage pipeline	32 KB/32 KB	
ARM11	9-stage pipeline	Variable	740 MIPS @ 665 MHz
Cortex	13-stage superscalar pipeline	Variable	2000 MIPS @ 1 GHz
XScale	Applications processor; 7-stage pipeline	32 KB/32 KB L1 512 KB L2	1000 MIPS @ 1.25 GHz

Summary

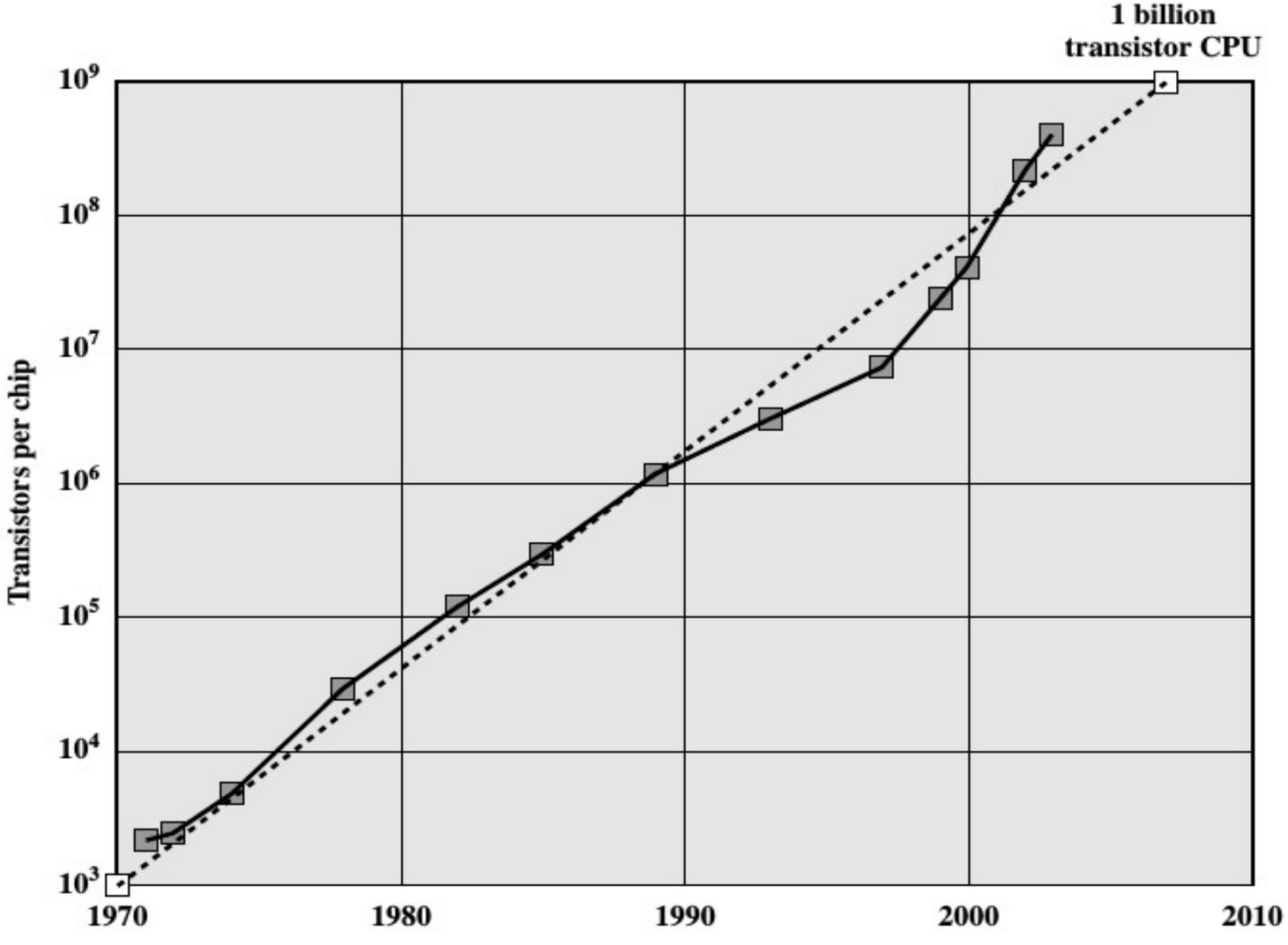
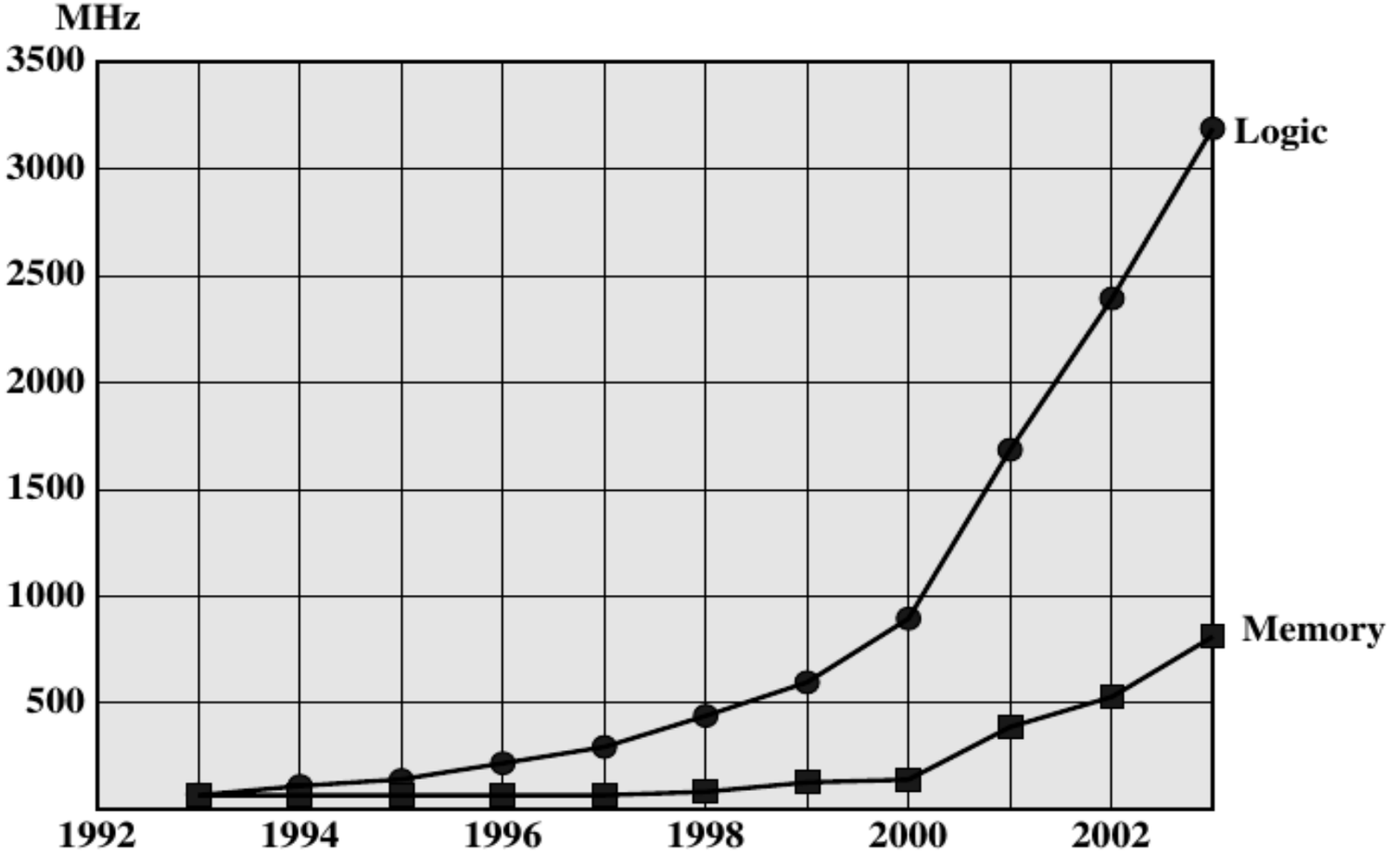
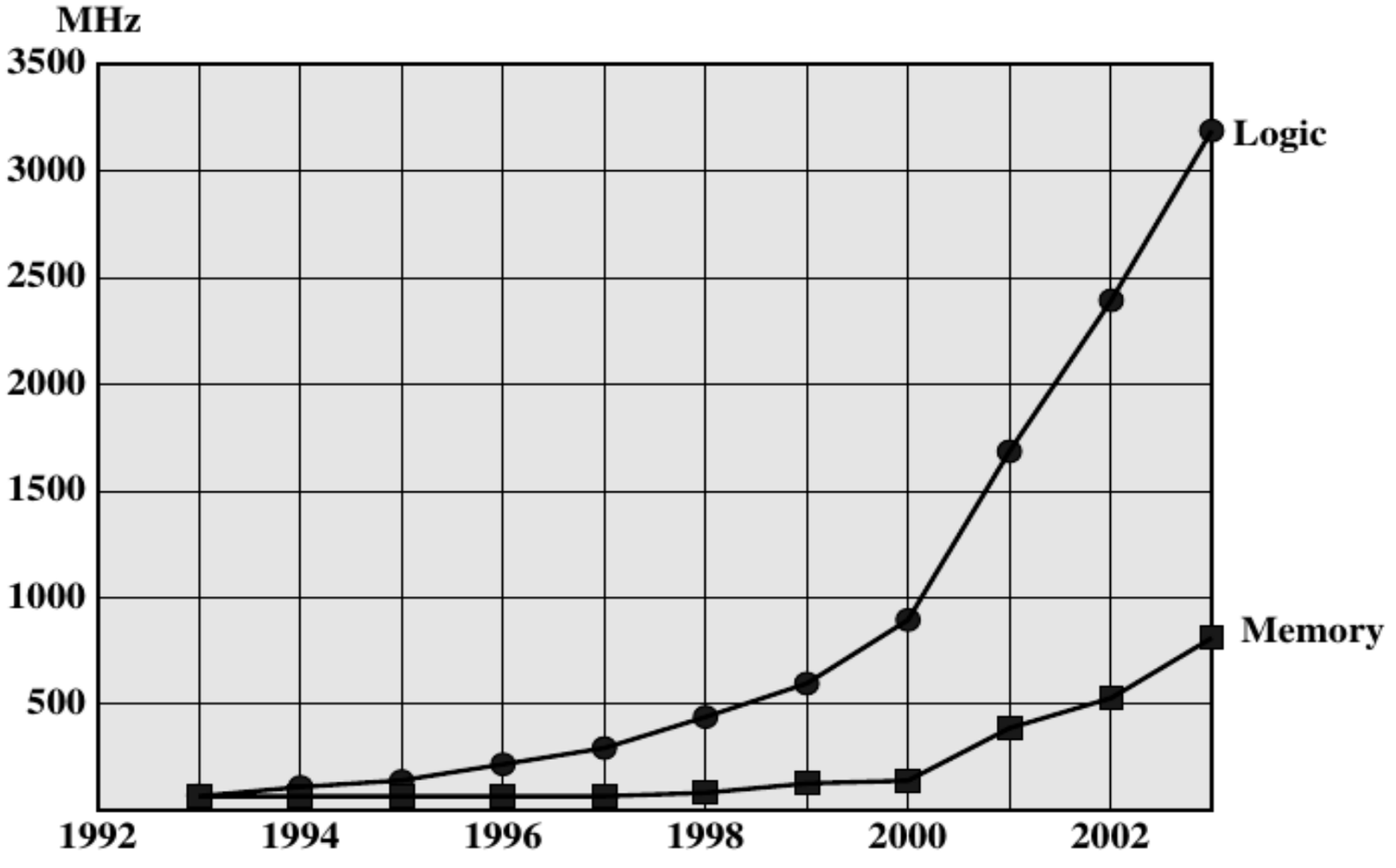
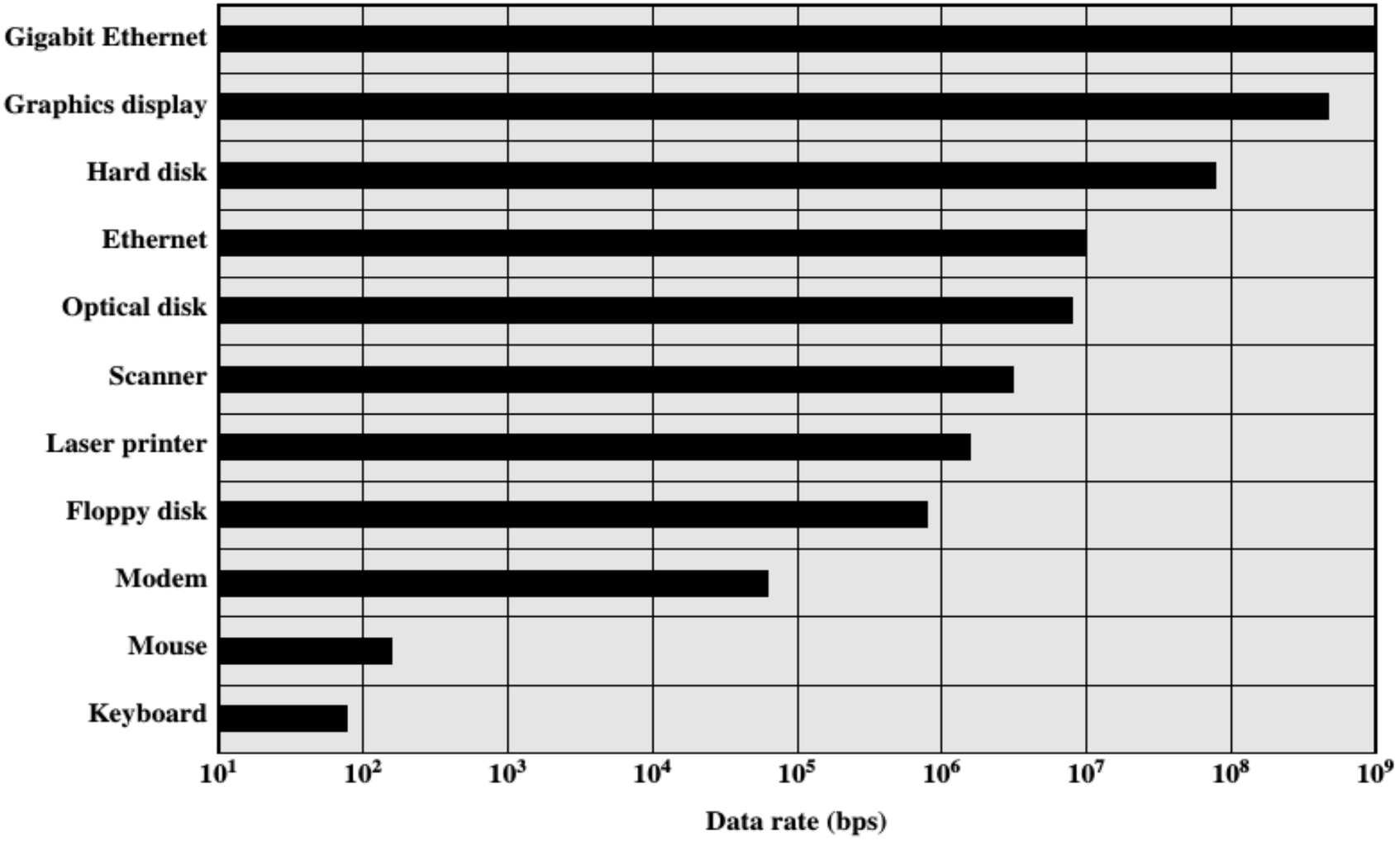


Figure 2.8 Growth in CPU Transistor Count [BOHR03]


MHz
3500
3000
2500
2000
1500
1000
500
1992
1994
1996
1998
2000
2002
Logic
Memory


MHz
3500
3000
2500
2000
1500
1000
500
1992
1994
1996
1998
2000
2002
Logic
Memory


Gigabit Ethernet
Graphics display
Hard disk
Ethernet
Optical disk
Scanner
Laser printer
Floppy disk
Modem
Mouse
Keyboard
10^1
10^2
10^3
10^4
10^5
10^6
10^7
10^8
10^9
Data rate (bps)