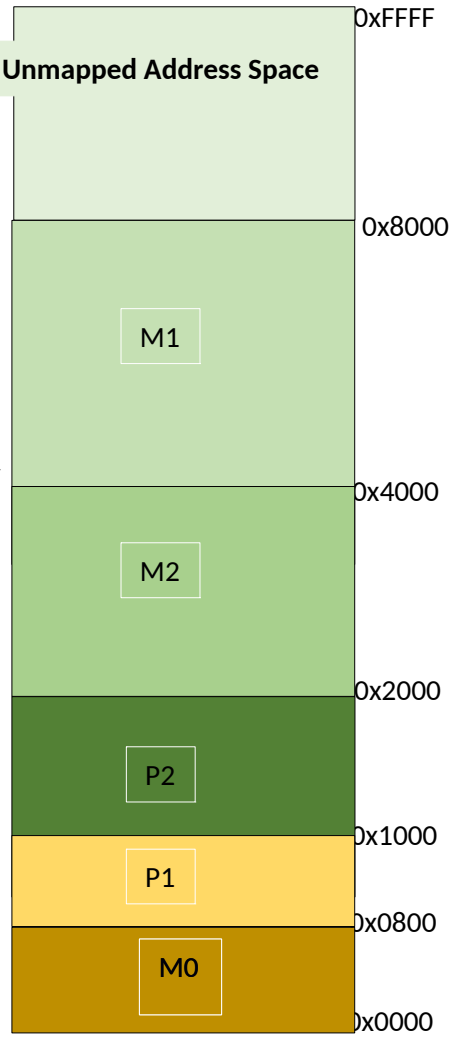
EE2016F19: Solutions to Tutorial 7

1. Design an IO/memory map for the processor which has 64KB address space and requires 2KB Internal Memory (M0), 16 KB EEPROM (M1) and 8KB RAM (M2). Additionally, attach a 2KB Keyboard Controller (P1) and a 4KB printer Controller (P2). First place M0, M1, M2 as well as P1 and P2 at suitable locations in memory space, with M0 starting at location 0000(H), such that all devices use the lower 32KB of IO/memory space and have regular mapping. Then obtain expression for chip select for each of the devices.

Ans:

For Regular Mapping:
M0 (2KB) start address must be a multiple of 0x0800.
M1 (16KB) start address must be a multiple of 0x4000.
M2 (8KB) start address must be a multiple of 0x2000.
P1 (2KB) start address must be a multiple of 0x0800.
P2 (4KB) start address must be a multiple of 0x1000.

First fix M0, then M1 & M2. Try to identify whether to fit in P1 in the empty space, then P2. See to that there are no gaps (unused space) – optimal use of address space.



Memory/ Peripheral	M0	P1	P2	M2	M1
Start Address	0000 0000 0000 0000	0000 1000 0000 0000	0001 0000 0000 0000	0010 0000 0000 0000	0100 0000 0000 0000
End Address	0000 0111 1111 1111	0000 1111 1111 1111	0001 1111 1111 1111	0011 1111 1111 1111	0111 1111 1111 1111

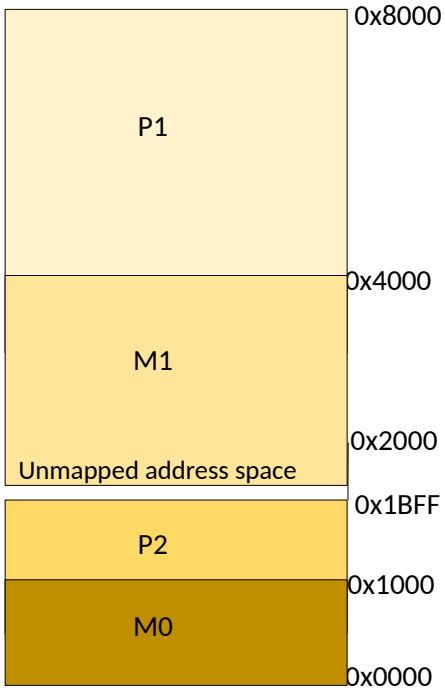
Let A15, A14, A13..... A0 represent the address lines.

Chip Select for M0 : $\overline{A15} \cdot \overline{A14} \cdot \overline{A13} \cdot \overline{A12} \cdot \overline{A11}$

Chip Select for P1 : $\overline{A15}$. $\overline{A14}$. $\overline{A13}$. $\overline{A12}$. A11
Chip Select for P2 : $\overline{A15}$. $\overline{A14}$. $\overline{A13}$. A12
Chip Select for M2 : $\overline{A15}$. A14 . A13
Chip Select for M1 : A15 . A14

2. Design an IO/memory map for the processor which has 32KB address space and requires 4KB Internal Memory (M0), 8KB external memory (M1), 16KB Network Controller (P1) and 3 KB Keyboard Controller (P2) . First place M0, M1 as well as P1 and P2 at suitable locations in memory space, with M0 starting at location 0000(H). Then obtain expression for chip select for each of the devices.
Ans:

For Regular Mapping:
M0 (4KB) start address must be a multiple of 0x1000.
M1 (8KB) start address must be a multiple of 0x2000.
P1 (16KB) start address must be a multiple of 0x4000.



Memory/ Peripheral	M0	P2	M1	P1
Start Address	0000 0000 0000 0000	0001 0000 0000 0000	0010 0000 0000 0000	0100 0000 0000 0000
End Address	0000 1111 1111 1111	0001 1011 1111 1111	0011 1111 1111 1111	0111 1111 1111 1111

Let A15, A14, A13..... A0 represent the address lines.

Chip Select for M0 : $\overline{A15}$. $\overline{A14}$. $\overline{A13}$. $\overline{A12}$

Chip Select for M1 : $\overline{A15}$. $\overline{A14}$. A13

Chip Select for P1 : $\overline{A15}$. A14

Chip Select for P2 : $\overline{A15}$. $\overline{A14}$. $\overline{A13}$. A12. [($\overline{A11}$. $\overline{A10}$) + ($\overline{A11}$. A10) + (A11 . $\overline{A10}$)]

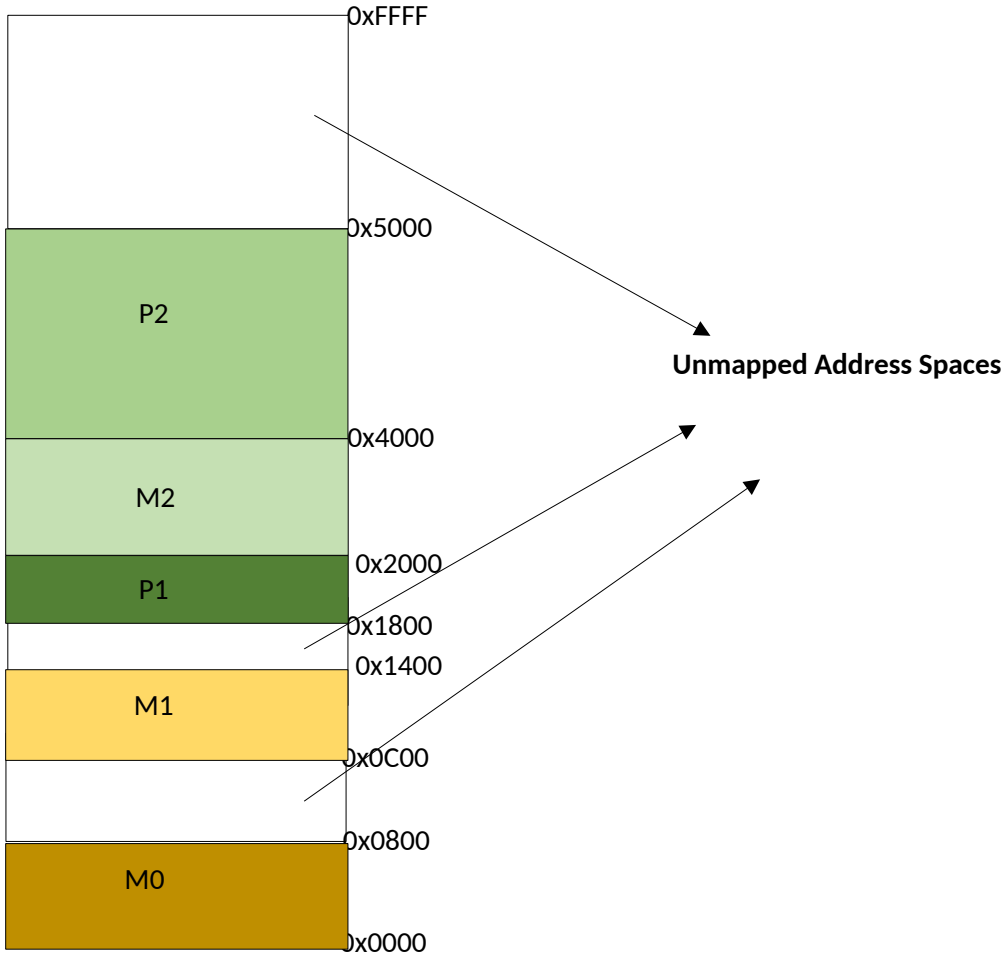
= $\overline{A15}$. $\overline{A14}$. $\overline{A13}$. A12. [$\overline{A11}$ + $\overline{A10}$]

3. Design an IO/memory map for the processor which has 64KB address space and requires 2KB Internal Memory (M0), 2 KB EEPROM (M1) and 8KB RAM (M2). Additionally, attach a 2KB Keyboard Controller (P1) and a 4KB printer Controller (P2). First place M0, M1, M2 as well as P1 and P2 at suitable locations in memory space, with M0 starting at location 0000(H) and M1 at location 0C00(H) .Then obtain expression for chip select for each of the devices.

Ans:

For Regular Mapping:

- M0 (2KB) start address must be a multiple of 0x0800.
- M1(2KB) start address must be a multiple of 0x0800.
- M2 (8KB) start address must be a multiple of 0x2000.
- P1 (2KB) start address must be a multiple of 0x0800.
- P2 (4KB) start address must be a multiple of 0x1000.



Peripheral		M1	P1	M2	P2
Start Address	0000 0000 0000 0000	0000 1100 0000 0000	0001 1000 0000 0000	0010 0000 0000 0000	0100 0000 0000 0000
End Address	0000 0111 1111 1111	0001 0011 1111 1111	0001 1111 1111 1111	0011 1111 1111 1111	0100 1111 1111 1111

Let A15, A14, A13..... A0 represent the address lines.

Chip Select for M0 : $\overline{A15} \cdot \overline{A14} \cdot \overline{A13} \cdot A12 \cdot \overline{A11}$

Chip Select for M1 : ~~A15~~ . ~~A14~~ . ~~A13~~(~~A12~~ . A11 . A10 + A12 . ~~A11~~ . ~~A10~~)

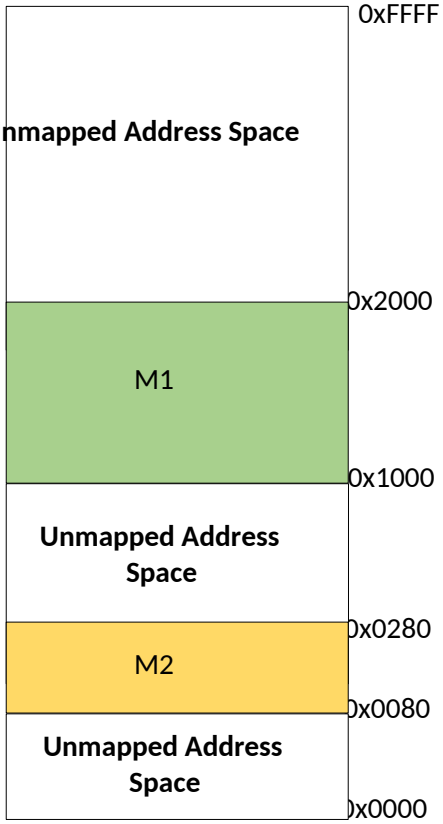
Chip Select for M2 : ~~A15~~ . ~~A14~~ . A13

Chip Select for P1 : ~~A15~~ . ~~A14~~ . ~~A13~~ . A12 . A11

Chip Select for P2 : ~~A15~~ . A14 . ~~A13~~ . ~~A12~~

4. Create a memory map for a processor with 16 address lines that need to connect to M1 – 4KB and M2 – 512 Bytes with M2 starting at location 0080 (H).
   Ans:

For Regular Mapping:
M1 start address must be a multiple of 0x1000



Memory/ Peripheral	M2	M1
Start Address	0000 0000 1000 0000	0001 0000 0000 0000
End Address	0000 0010 1000 0000	0001 1111 1111 1111

Let A15, A14, A13..... A0 represent the address lines.

Chip Select for M1 : $\overline{A15} \cdot \overline{A14} \cdot \overline{A13} \cdot A12$

Chip Select for M2 : $\overline{A15} \cdot \overline{A14} \cdot \overline{A13} \cdot \overline{A12} \cdot \overline{A11} \cdot \overline{A10}\ [\overline{A9}.\overline{A8}.A7 + \overline{A9}.A8.\overline{A7} + \overline{A9}.A8.A7 + A9.\overline{A8}.\overline{A7}]$

$= \overline{A15} \cdot \overline{A14} \cdot \overline{A13} \cdot \overline{A12} \cdot \overline{A11} \cdot \overline{A10}\ [\overline{A9}.\overline{A8}.A7 + \overline{A9}.A8 + A9.\overline{A8}.\overline{A7}\ ]$