ISE Tutorial

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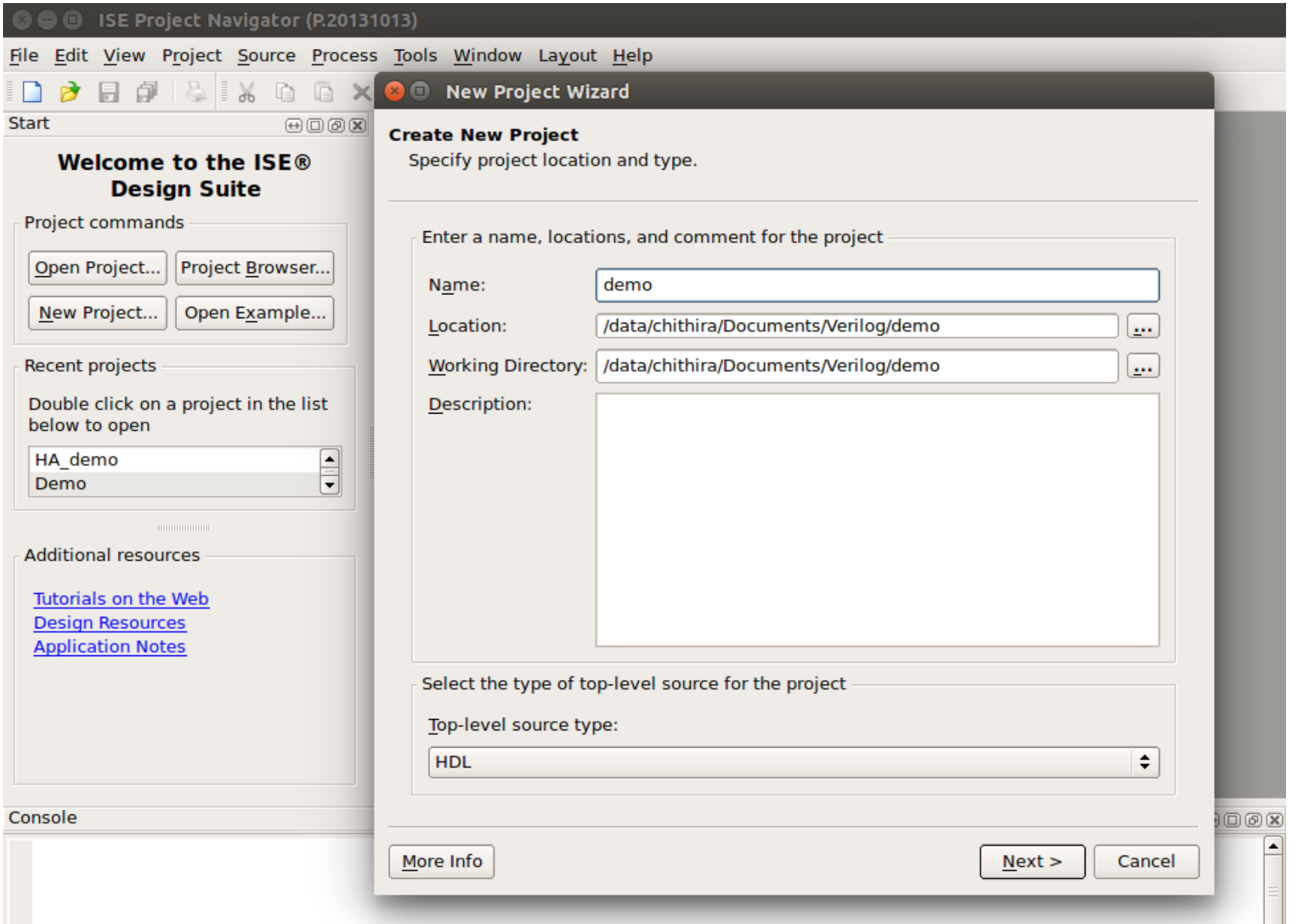
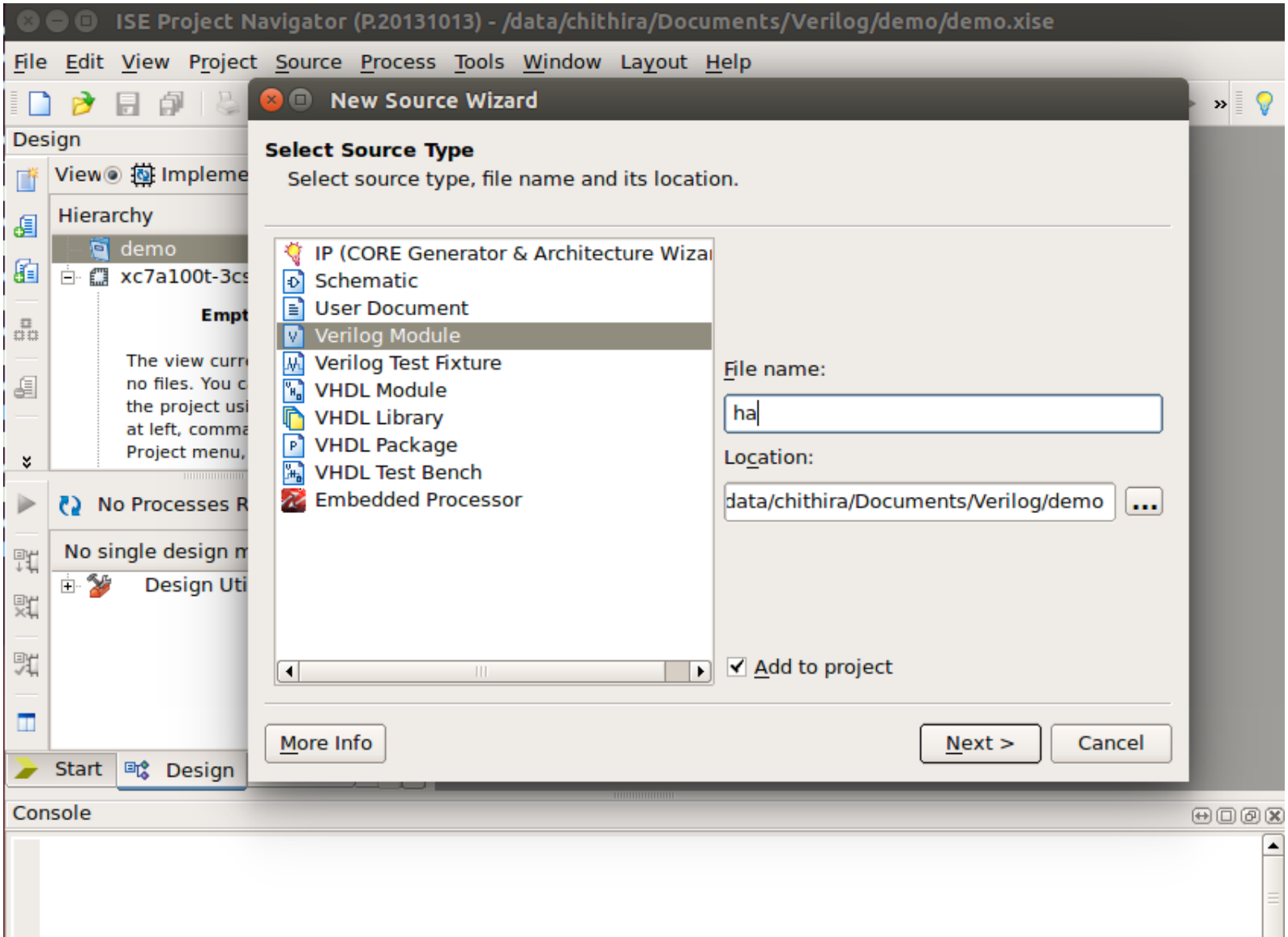
January 24, 2018

Creating a new project: File → Create New Project

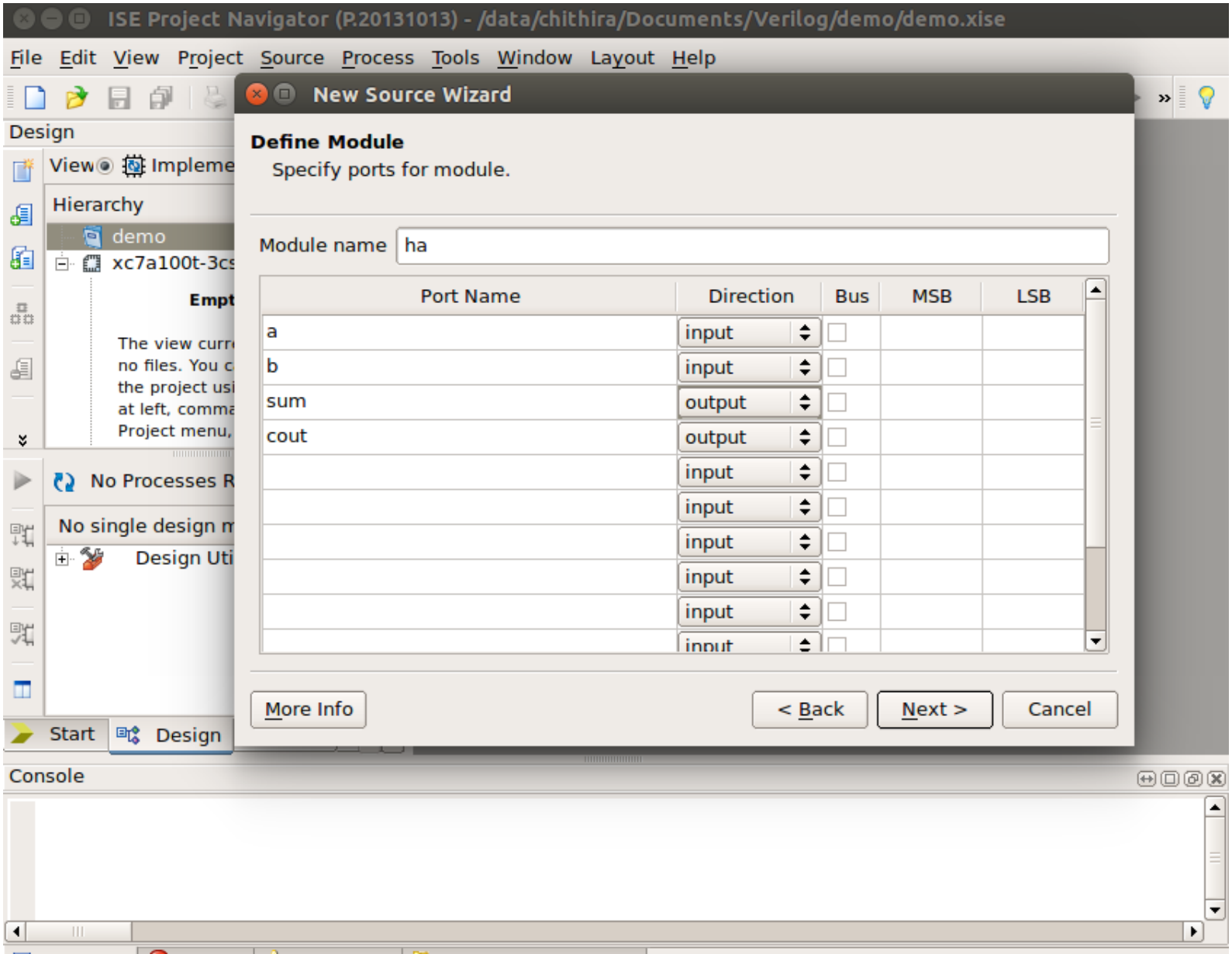
Enter project name and location and make sure that the top-level source type is 'HDL'. Click 'Next' and 'Finish'



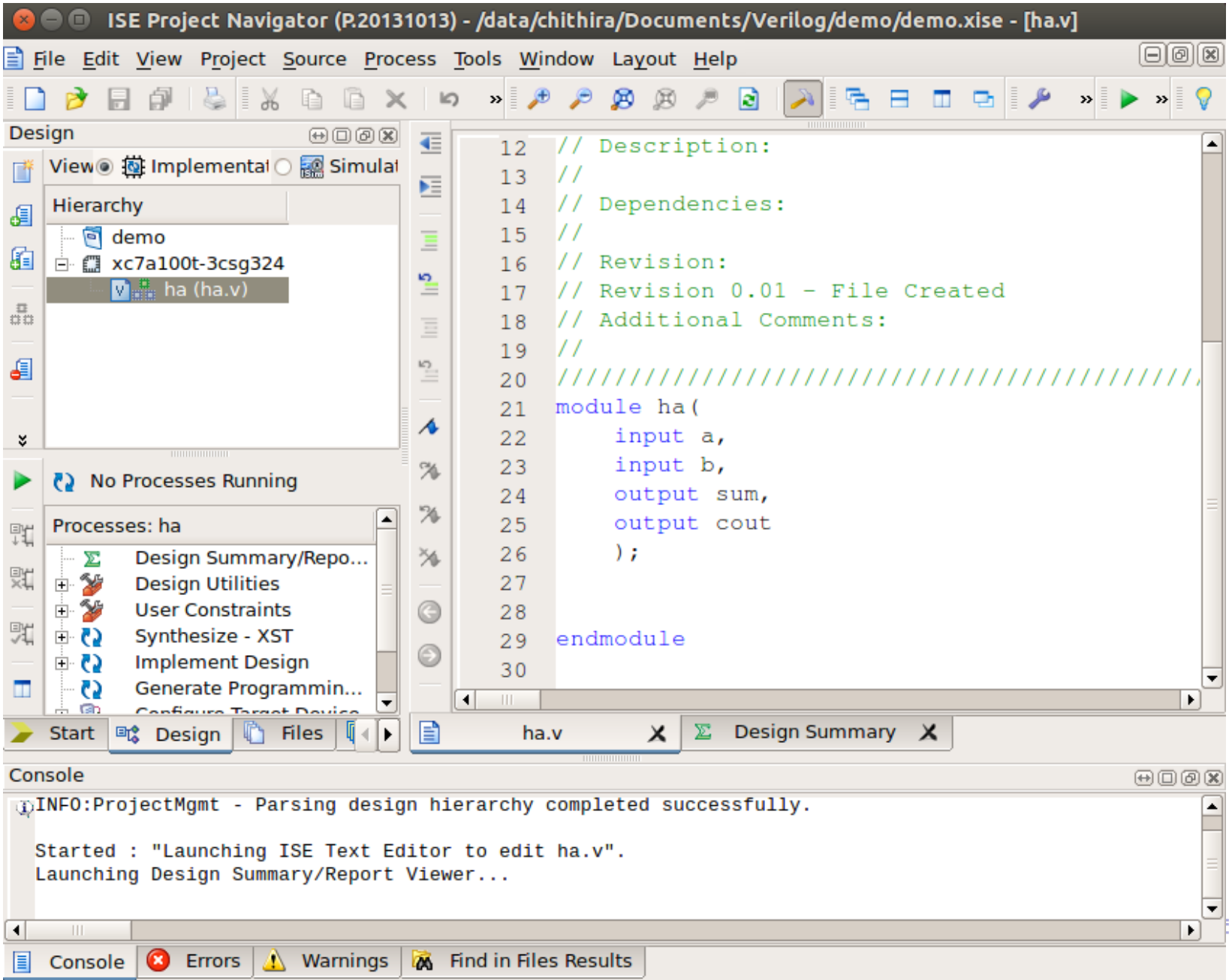
Creating verilog module: In 'Hierarchy' window, right click on the project name and select 'New source'
Select source type as 'Verilog Module' and enter file name. Make sure that 'Add to Project' box is ticked and click 'Next'.



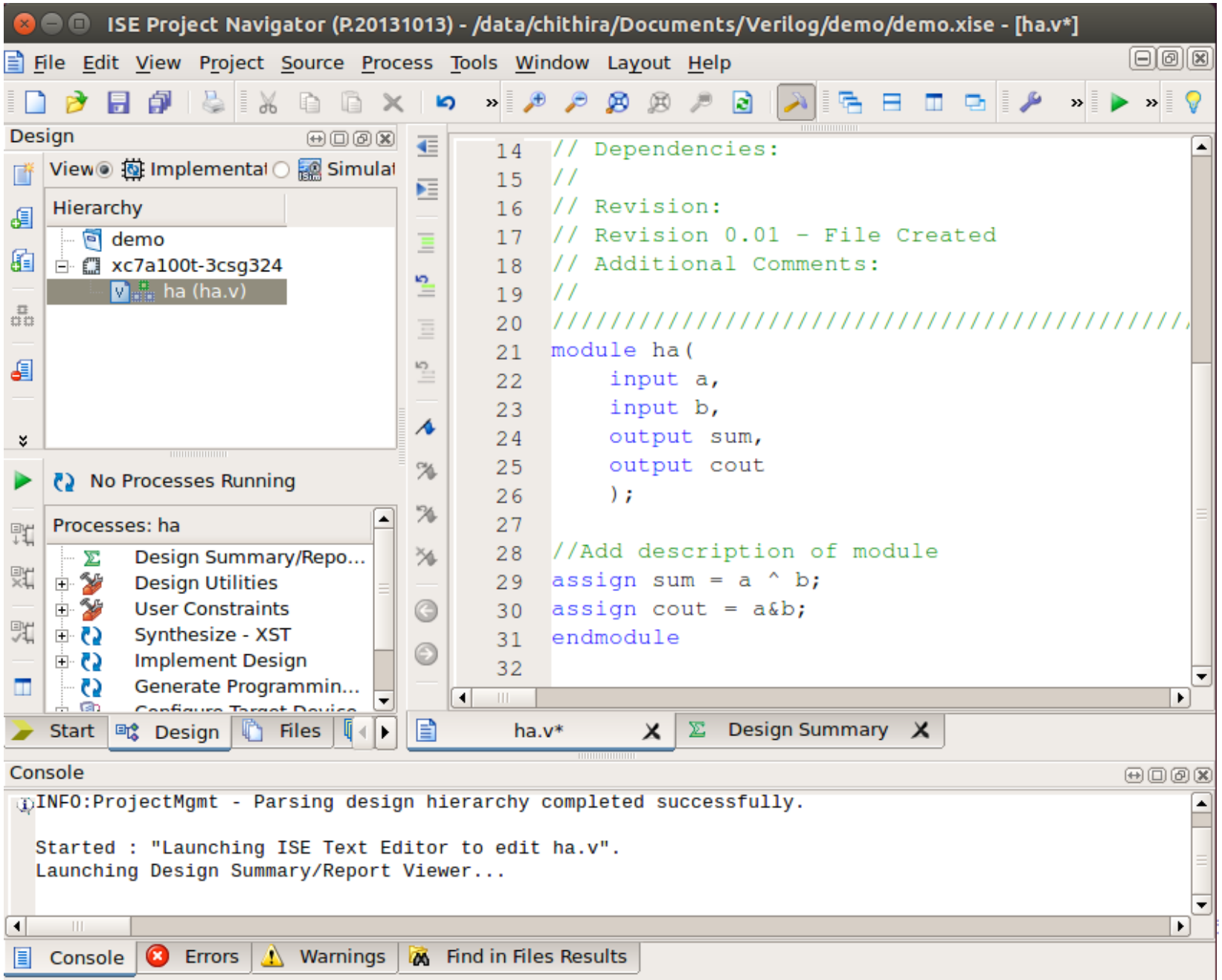
Defining port: Specify the port name and set the direction as input/output. Tick 'Bus' and specify 'MSB' in case the input/output port is a bus.



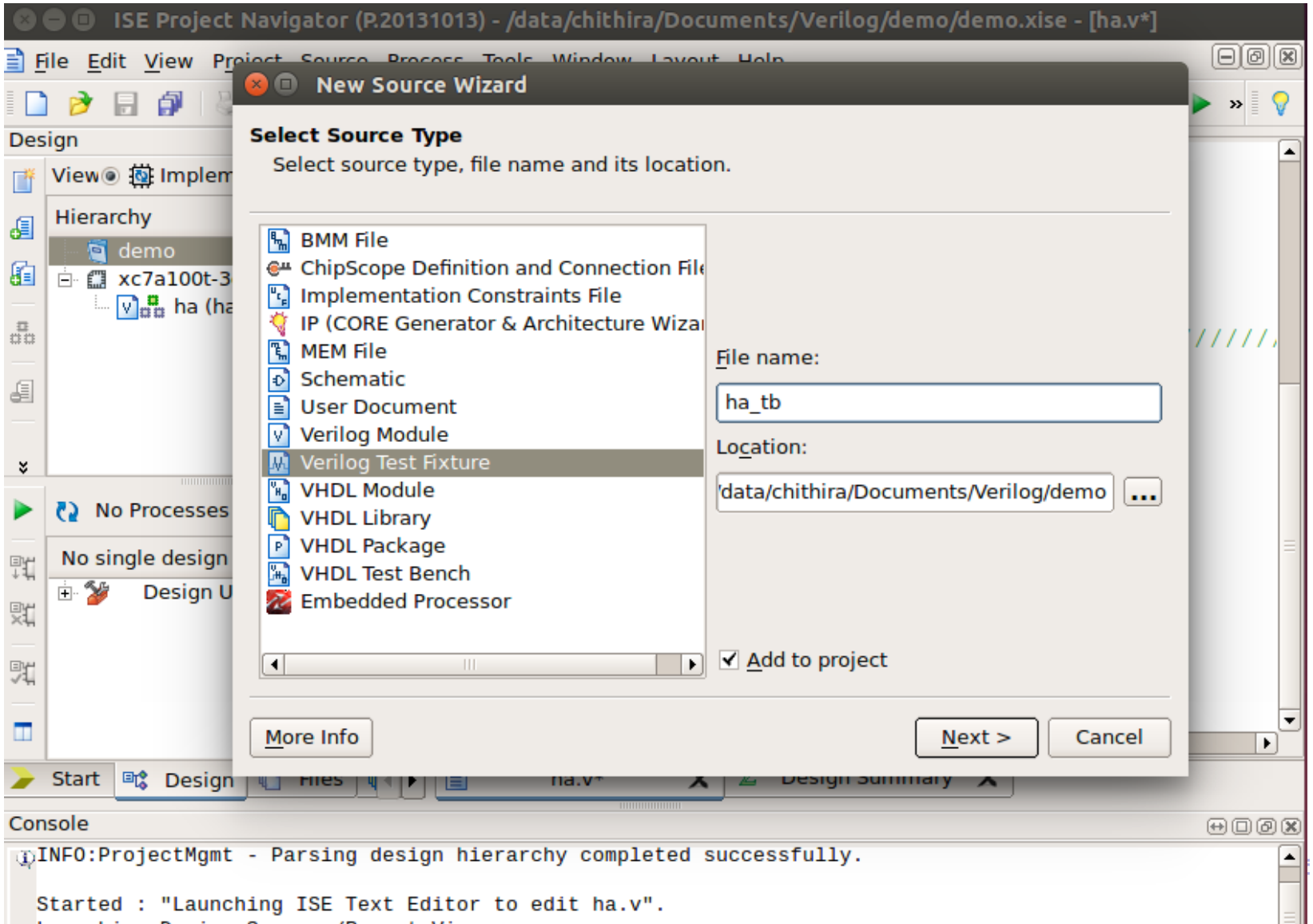
A file $< filename > .v$ is created with the module port declaration as shown in the figure.



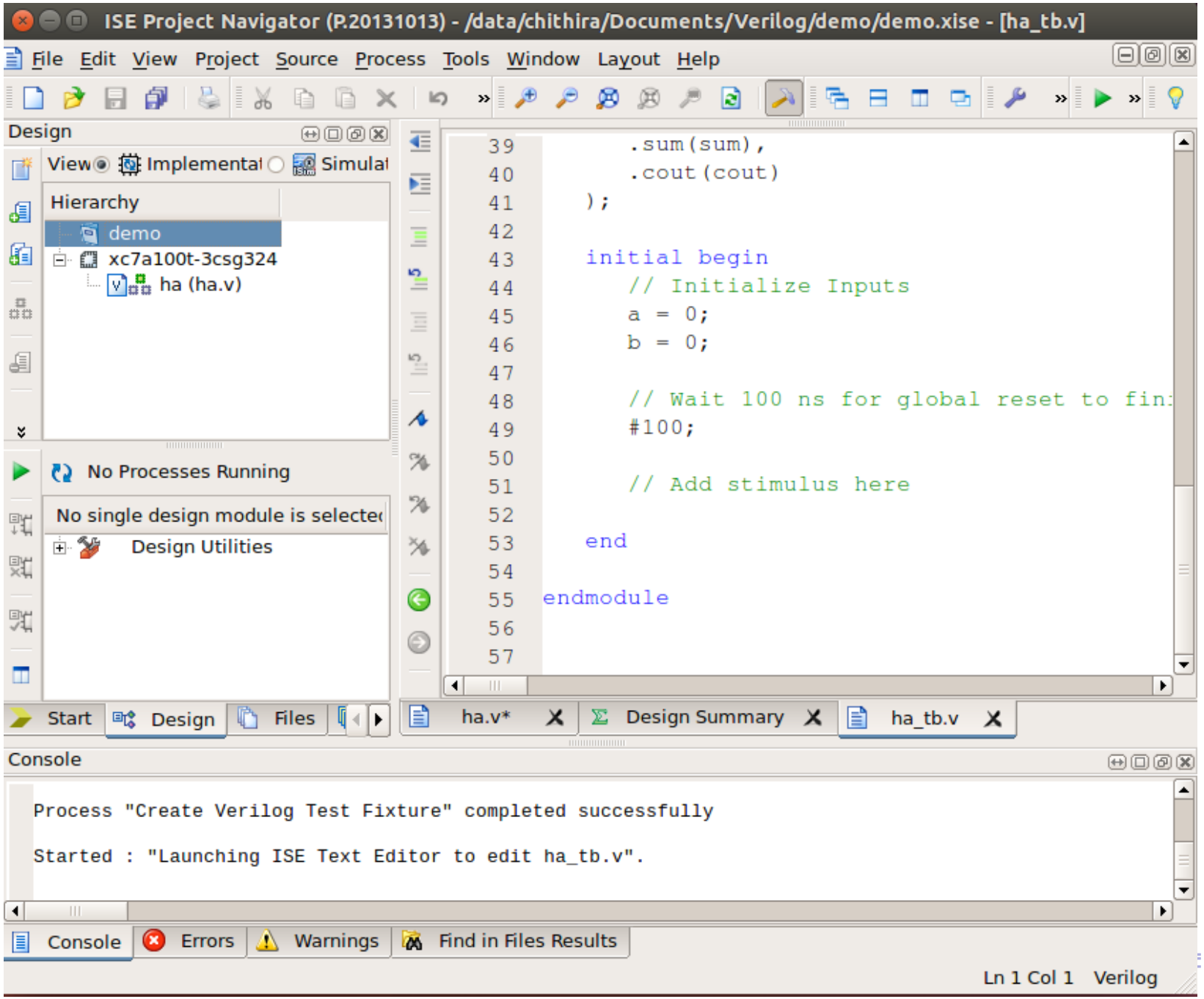
Add the description of the module between module port declaration and *endmodule*.



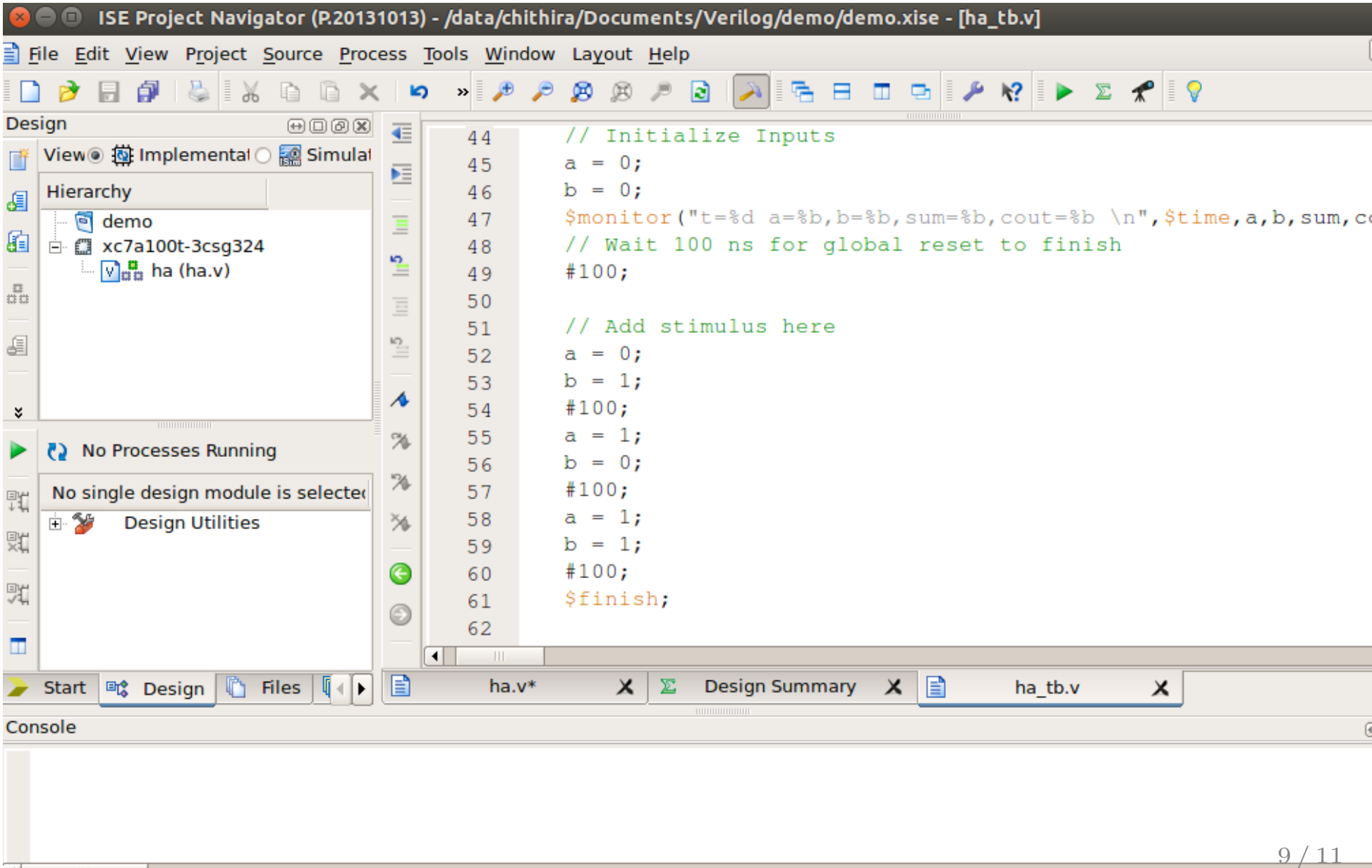
Creating test bench: In 'Hierarchy' window, right click on the project name and select 'New source'
Select source type as 'Verilog Test Fixture' and enter file name. Make sure that 'Add to Project' box is ticked and click 'Next'.



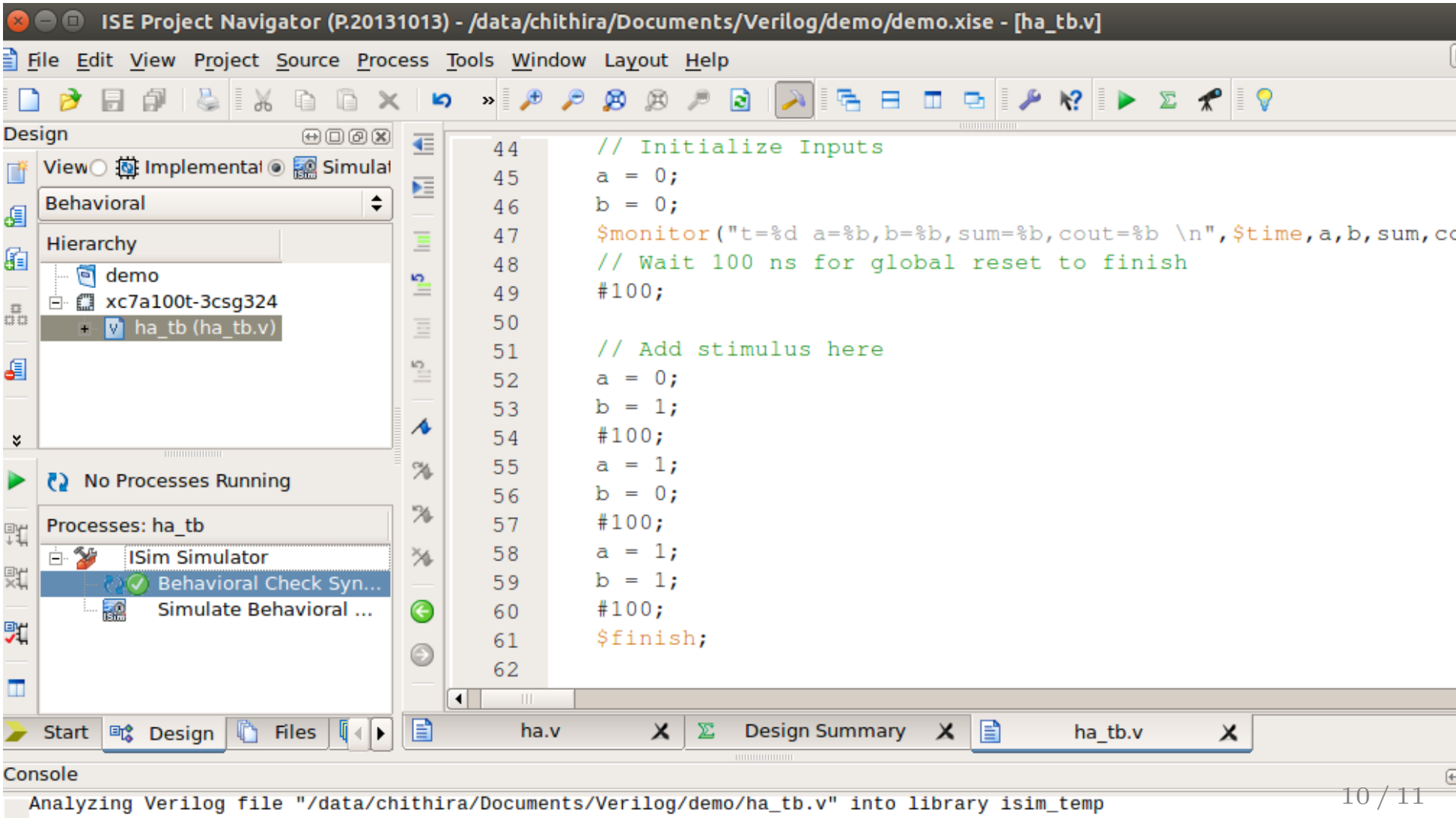
A test bench file is created as shown in the figure.



Add the input stimulus and *monitor* command for displaying the results.



Select ‘Simulation’ view and select the test bench in the ‘Hierarchy’ window. In the ‘Processes’ window, double click on ‘Behavioural Check Syntax’ to check for errors. The errors, if any, will be displayed in the console window.



Once the check syntax is completed successfully, double click on 'Simulate Behavioural Model' to run the logic simulation. The output of the *monitor* command will be displayed in the console window and the input/output waveforms in 'Default.wcfg' window.