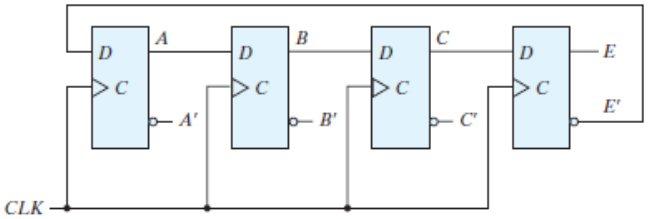
EE2001-Tutorial 8
Date: 22nd March 2018
Counters and Memory

1) (i) Design a counter with T flip-flops that goes through the following binary repeated sequence: 0, 1, 3, 7, 6, 4. Show that when binary states 010 and 101 are considered as don't care conditions, the counter may not operate properly. Find a way to correct the design.
(ii) It is necessary to generate six repeated timing signals T0 through T5. Design the circuit using
(a) flip-flops only; (b) a counter and a decoder.

2) (i) A digital system has a clock generator that produces pulses at a frequency of 80 MHz. Design a circuit that provides a clock with a cycle time of 50 ns.
(ii) Using JK flip-flops, (a) design a counter with the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6 and (b) draw the logic diagram of the counter.
(iii) Using D flip-flops, (a) design a counter with the following repeated binary sequence: 0, 1, 2, 4, 6 and (b) draw the logic diagram of the counter.
(iv) Using D flip-flops, (a) design a counter with the following repeated binary sequence: 0, 2, 4, 6, 8 and (b) draw the logic diagram of the counter.

3 (i) List the eight unused states in the given switch-tail ring counter. Determine the next state for each of these states and show that, if the counter finds itself in an invalid state, it does not return to a valid state. Modify the circuit so that the counter produces the same sequence of states and that the circuit reaches a valid state from any one of the unused states.



(ii) Show that a Johnson counter with n flip-flops produces a sequence of 2n states. List the 10 states produced with five flip-flops and the Boolean terms of each of the 10 AND gate outputs.

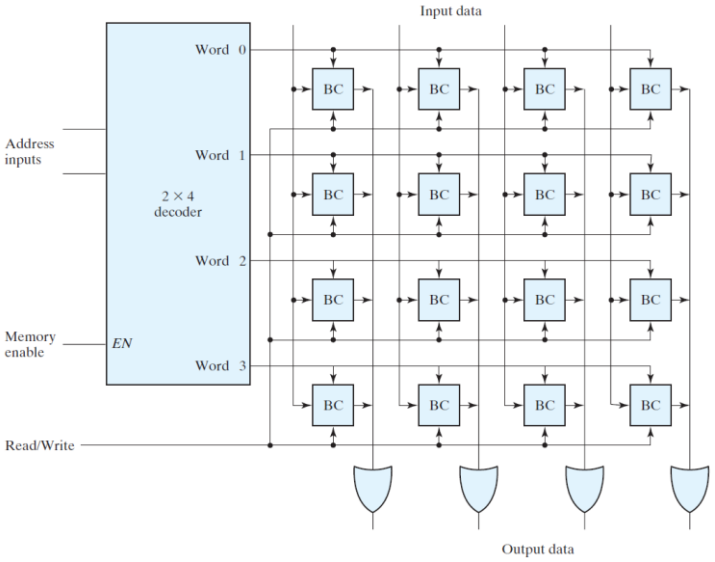
4) The memory units that follow are specified by the number of words times the number of bits per word. How many address lines and input–output data lines are needed in each of the following cases? Also for each case, give the number of bytes stored in the memories.
(a) 8K × 16;
(b) 2G × 8
(c) 16M × 32
(d) 256K × 64

5) Word number 563 in the memory shown here contains the binary equivalent of 1,212.
List the 10-bit address and the 16-bit memory content of the word.

Memory address		Memory content
Binary	Decimal	
0000000000	0	1011010101011101
0000000001	1	1010101110001001
0000000010	2	0000110101000110
⋮	⋮	⋮
1111111101	1021	1001110100010100
1111111110	1022	0000110100011110
1111111111	1023	1101111000100101

6) Show the memory cycle timing waveforms for the write and read operations. Assume a CPU clock of 150 MHz and a memory cycle time of 20 ns.

7) Enclose the given 4 × 4 RAM in a block diagram showing all inputs and outputs. Construct an 8 X 8 memory using four 4 × 4 RAM units.



8) A 16K X 4 memory uses coincident decoding by splitting the internal decoder into X -selection and Y -selection.
(a) What is the size of each decoder, and how many AND gates are required for decoding the address?
(b) Determine the X and Y selection lines that are enabled when the input address is the binary equivalent of 6,000.

9) (a) How many 32K × 8 RAM chips are needed to provide a memory capacity of 256K bytes?
(b) How many lines of the address must be used to access 256K bytes? How many of these lines are connected to the address inputs of all chips?
(c) How many lines must be decoded for the chip select inputs? Specify the size of the decoder.

10) A DRAM chip uses two-dimensional address multiplexing. It has 13 common address pins, with the row address having one bit more than the column address. What is the capacity of the memory?