EE2016 Microprocessors Theory and Lab

Tutorial 5 (4th week of Aug. 2019)

(You may refer AVR manuals & Mazidi)

1 Fill in the blanks

1. Pseudo instructions are also called as .....
2. The ROM size in the AVR chip which we use in our lab, is ..... Every member of the AVR family, regardless of the program ROM size, wakes up at the memory 0x..... when it is powered up.
3. The AVR instruction "LDI R20, 0x44" is a .....-byte instruction.
4. AVR complies to ..... (RISC / CISC) architecture
5. List those instructions out of the following instructions, which produce the opcode: (a) LDI R16, 0x25 (b) ADD R23, R19 (c) .ORG 0x500 (d) JMP HERE . Also which of them are directives?

2 Solve all the problems

1. State the content of R20, R21 IMMEDIATELY after each instruction and data memory location 0x120 after the following program:

LDI	R20,	5	;load R20 with 5
LDI	R21,	2	;load R21 with 2
ADD	R20,	R21	;Add R21 to R20
ADD	R20,	R21	add R20 to R21
STS	0x120,	R20	;store in location 0x120 the contents of R20

2. Write a simple program to toggle the I/O register of PORT B continuously forever.
3. Write a program to get data from the PINB and send it to the I/O register of PORT C continuously.
4. Show the status of the Z flag during the execution of the following program:

LDI	R20,	4	;R20=4
DEC	R20		;R20=R20-1
DEC	R20		;R20=R20-1
DEC	R20		;R20=R20-1
DEC	R20		;R20=R20-1