TASK 2 VHDL

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BGU
COMPUTER ENGEENIRING

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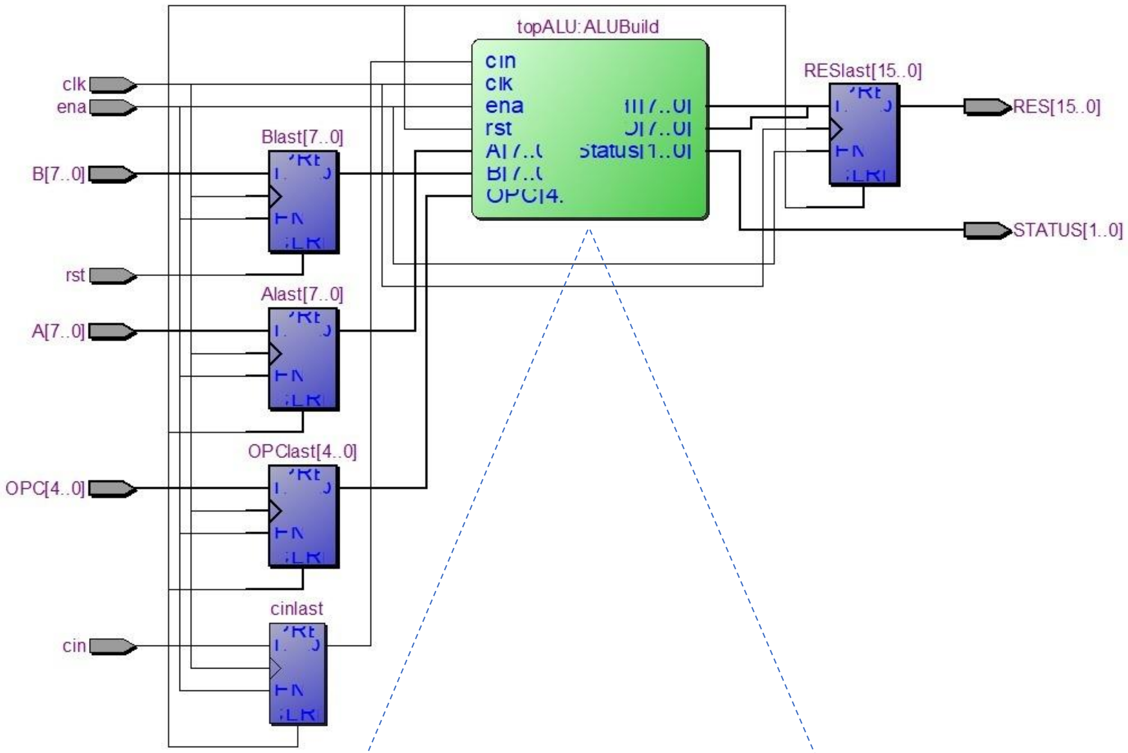
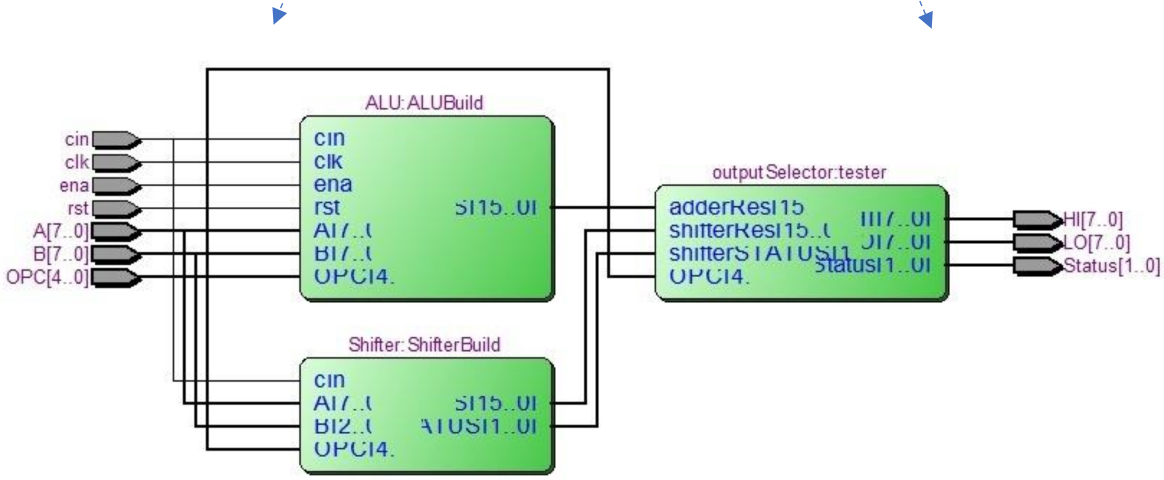
Conclutions: .... **Error! Bookmark not defined.**

Blocks diagram:

Top:

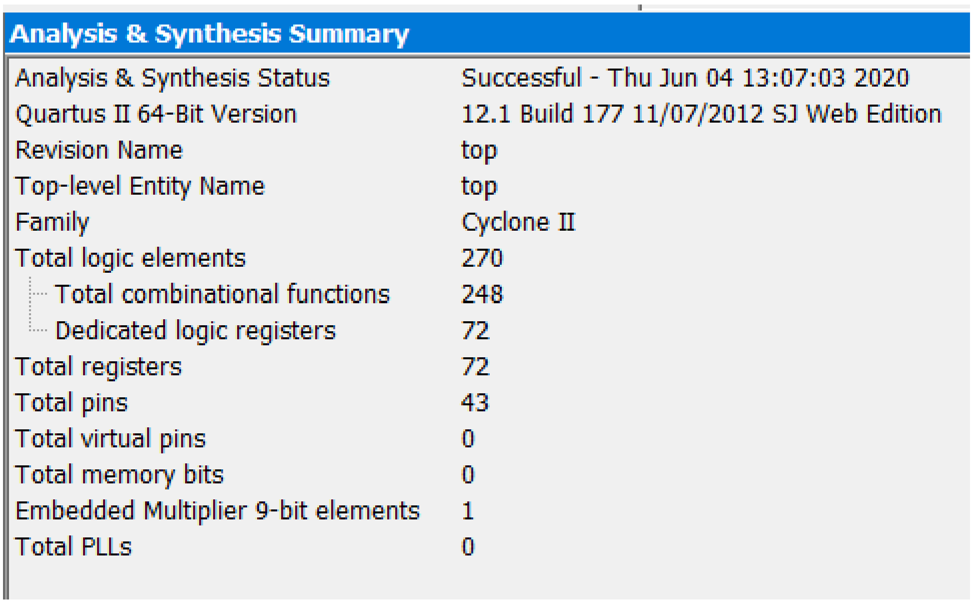


TopALU-subentity:



Logic usage:

Top:

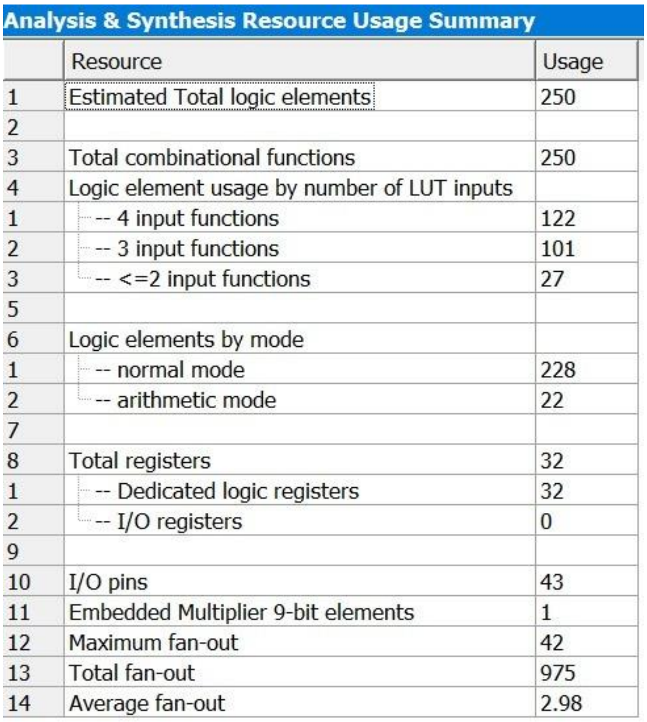


Analysis & Synthesis Summary

Analysis & Synthesis Status	Successful - Thu Jun 04 13:07:03 2020
Quartus II 64-Bit Version	12.1 Build 177 11/07/2012 SJ Web Edition
Revision Name	top
Top-level Entity Name	top
Family	Cyclone II
Total logic elements	270
Total combinational functions	248
Dedicated logic registers	72
Total registers	72
Total pins	43
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	1
Total PLLs	0

We can see that we used 1 Multiplier, 72 registered and total of 270 logic elements.

TopALU-subentity:



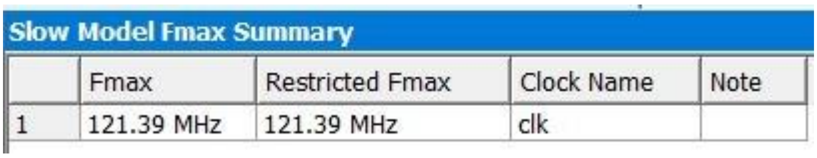
Analysis & Synthesis Resource Usage Summary

	Resource	Usage
1	Estimated Total logic elements	250
2		
3	Total combinational functions	250
4	Logic element usage by number of LUT inputs	
1	-- 4 input functions	122
2	-- 3 input functions	101
3	-- <=2 input functions	27
5		
6	Logic elements by mode	
1	-- normal mode	228
2	-- arithmetic mode	22
7		
8	Total registers	32
1	-- Dedicated logic registers	32
2	-- I/O registers	0
9		
10	I/O pins	43
11	Embedded Multiplier 9-bit elements	1
12	Maximum fan-out	42
13	Total fan-out	975
14	Average fan-out	2.98

We can see that we used 72-32= 40 registered just for the top level, for saving all the data.

Maximal operating clock:

we have found that the maximum frequency is 121.39Mhz

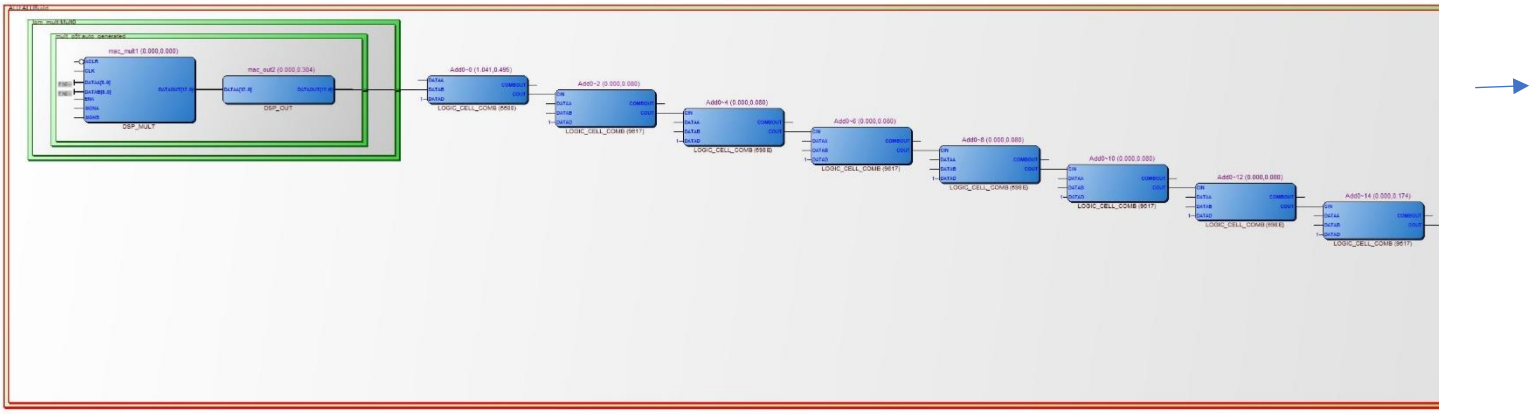


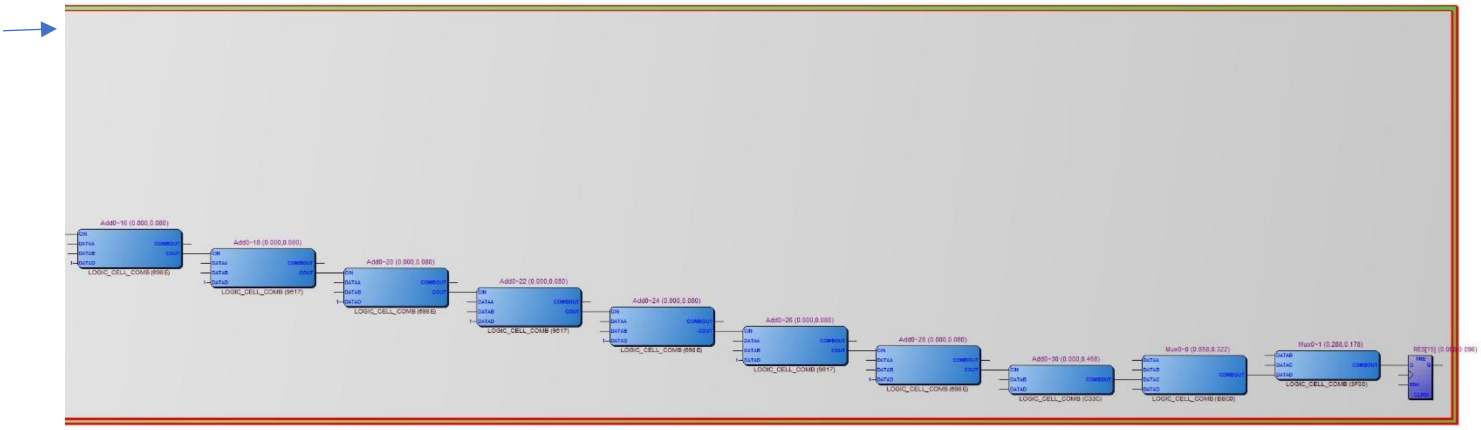
Slow Model Fmax Summary

	Fmax	Restricted Fmax	Clock Name	Note
1	121.39 MHz	121.39 MHz	clk	

So the Maximal operating clock is $\frac{1}{121.39Mhz} = 8.3ns$

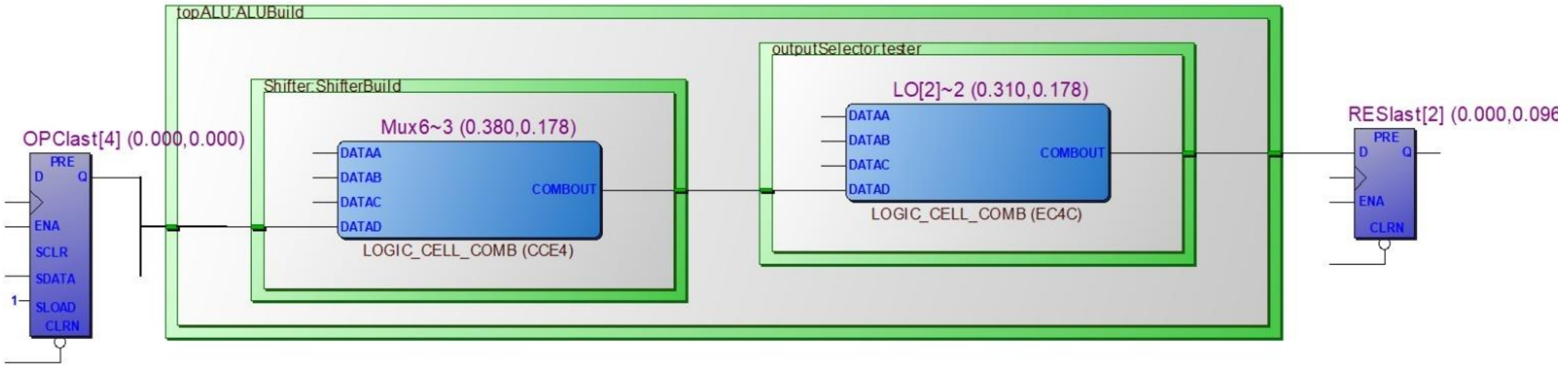
Longest path:

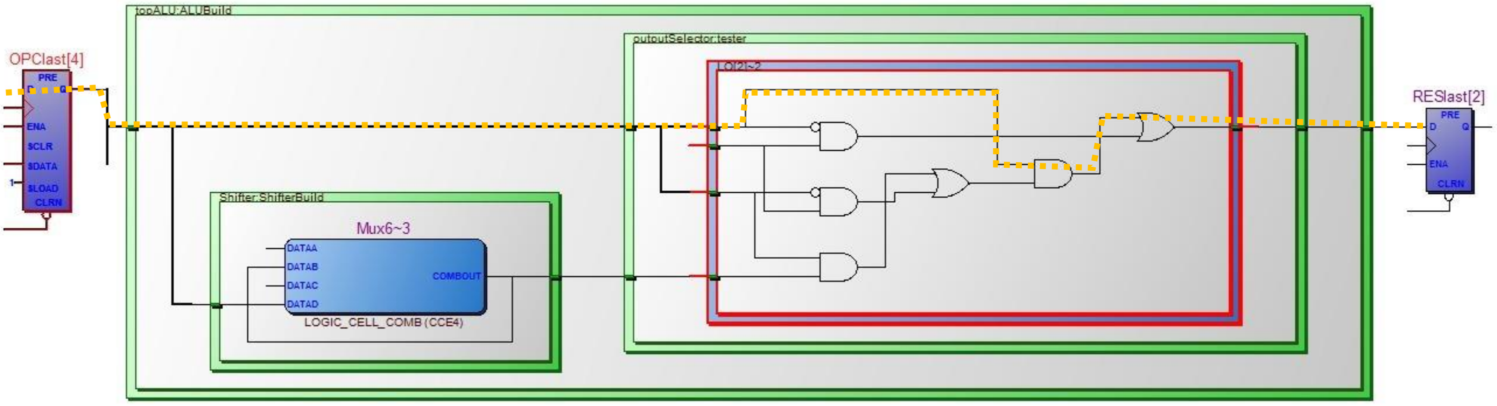




We can see that the longest path goes through the Multiplexer, it makes sense because its the most complex calculation we can do in this task.

Shortest Path:





We only use OPC[4] for the output selector.

We don’t use it for the Shifter or ALU entities.

so it makes sense it is the shortest path from start to finish.

Hardware Test Case:

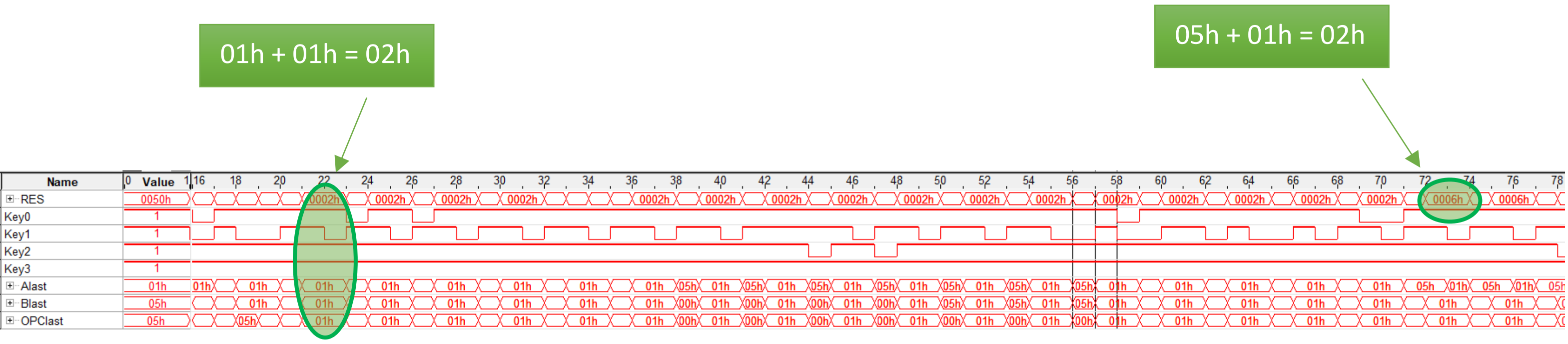
For the hardware test, we've disabled all the clk's from our code, we have changed the input from A,B and OPC to REGISTER, and KEY0-2 decided where the REGISTER goes (A B or OPC).

We've also added a process for the case where Key3 is pressed.

Single-Tap HardWare Test:

Add test:

we added 01h + 01h = 02h, and then we changed A to 05h so the result was 06h.

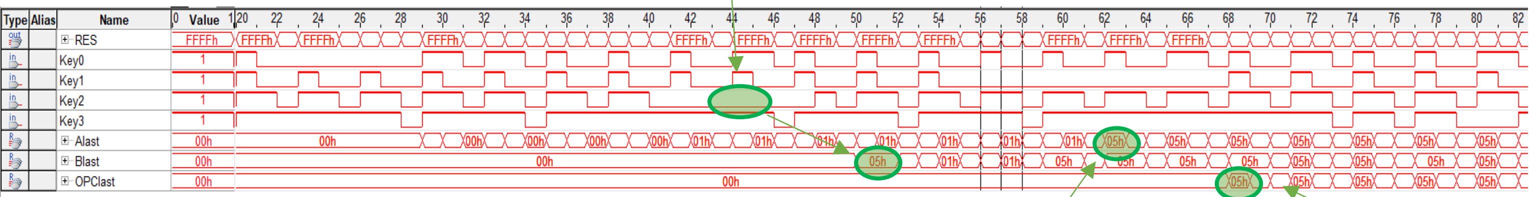


01h + 01h = 02h

05h + 01h = 02h

Mac test:

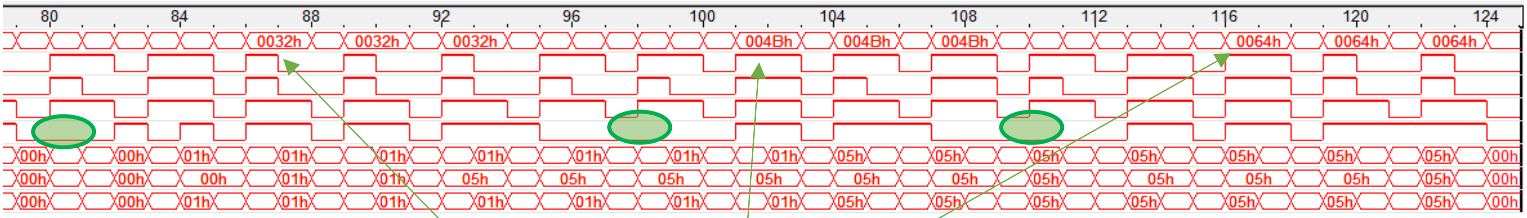
Button Key2 pushed -> B became 05(h)



A became 05(h)

OPC became 05(h)

Result became 16(h)

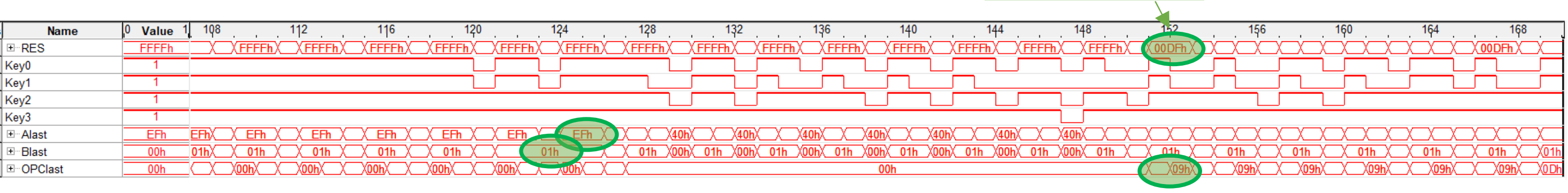


Then, every push of key3 added 16(h) to the Result

Shifter test:

we've put in A=EF(h) and in B=01(h) and the OPC= 01101, so we got in the result=DF(h), so we've got one rotation left trough carry as expected.

Result = DF(h)


Name
Value
RES
Key0
Key1
Key2
Key3
Alast
Blast
OPClast
00DFh