

# Operational Amplifiers

## 7.1 INTRODUCTION

The term 'Operational Amplifier' abbreviated as OPAMP, was originally the name of a circuit used for carrying out mathematical operations, such as summation and integration on input signals. An essential component for this purpose is a direct-coupled amplifier with high voltage gain. More recently the term 'OPAMP' has been given to linear IC which provides, apart from other characteristics, a high voltage gain (for a band of frequencies from dc upwards) and which, therefore, can be used to realize many functions besides mathematical operations. It is in this sense that OPAMP is also referred to as the basic analog integrated circuit.

The integrated operational amplifier has gained wide acceptance as a versatile, predictable and economic system building block. It offers all the advantages of monolithic ICs: small size, high reliability, reduced cost and temperature tracking.

The main objective of this chapter is to describe and analyze the properties of OPAMPS and their applications in practical circuits. For simplicity the applications of OPAMPS are broadly divided into linear applications and nonlinear applications. Finally the use of electronic analog computers has been discussed to show how we can use OPAMPS to simulate physical systems.

## 7.2 BASIC OPERATIONAL AMPLIFIER

### General Features of OPAMP

An OPAMP is a direct-coupled, high gain voltage amplifier designed to amplify signals over a wide frequency range (from dc upwards). Typically it has two input terminals and one output terminal and a gain of atleast  $10^5$ . Its circuit representation and symbol are shown in Figs. 7.1(a) and (b) respectively.

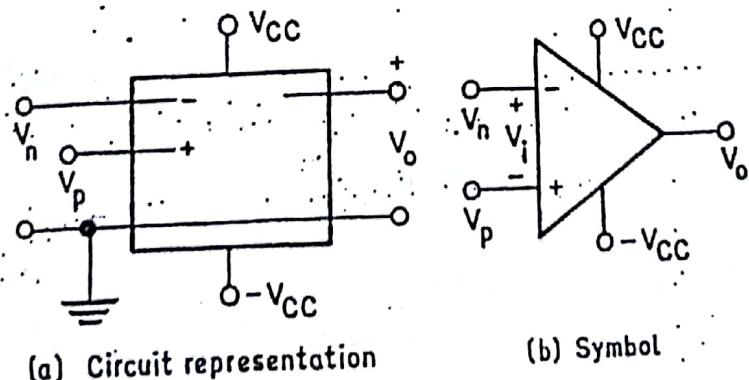


Fig. 7.1 OPAMP.

An OPAMP is basically a differential amplifier responding to the difference in voltages at the negative (inverting) and positive (noninverting) terminal. Thus

$$V_o = -A_v (V_n - V_p) = -A_v V_i; V_i = V_n - V_p$$

where

$A_v$  = voltage gain

$V_n$  = negative (inverting) terminal voltage

$V_p$  = positive (noninverting) terminal voltage

$V_o$  = output voltage.

If  $V_p = 0$ ,  $V_o = -A_v V_n$ . This means that the output is inverted ( $180^\circ$  out of phase) with respect to  $V_n$ ; so  $V_n$  is the inverting voltage. Similarly if  $V_n = 0$ ,  $V_o = A_v V_p$  which means that the output is in phase with input  $V_p$ ; so  $V_p$  is noninverting voltage.

An ideal OPAMP has following properties:

- (i) Infinite open-loop voltage gain,  $A_v$ ;
- (ii) infinite input resistance,  $R_i$ ;
- (iii) zero output resistance,  $R_o$ ;
- (iv) infinite bandwidth;
- (v) infinite CMRR (Common Mode Rejection Ratio).

In practice OPAMPs do not, of course, have ideal properties, but common types nevertheless impressive specifications as shown in Table 7.1.

Table 7.1 Characteristics of OPAMPS

Property	Ideal	Practical	(Typical*)
Open loop gain	Infinite	Very high	( $\approx 2 \times 10^5$ )
Open loop bandwidth	Infinite	Very high	Dominant pole (10 Hz)
CMRR	Infinite	High	( $\approx 90$ dB)
Input resistance	Infinite	High	( $\approx 2$ M)
Output resistance	Zero	Low	( $\approx 75$ $\Omega$ )

\*Typical values are specifications of IC OPAMP 741.

An equivalent circuit of the OPAMP with finite input and output resistances can be drawn as shown in Fig. 7.2.

As a consequence of OPAMP characteristics being very close to the ideal characteristics, following conditions prevail at input end of an OPAMP:

$R_i = \infty$ ; current into inverting and noninverting terminals is almost zero.

$A_v = \infty$ ; which means that for any finite  $V_o$ ,  $V_i = V_n - V_p = 0$ . Therefore the inverting and noninverting terminals have the same potential.

One practical limitation that cannot be ignored is that for linear operation, the output voltage cannot exceed  $\pm V_{CC}$ .

Normally OPAMP is used with a feedback network that determines the functions performed.

### Operational Amplifiers

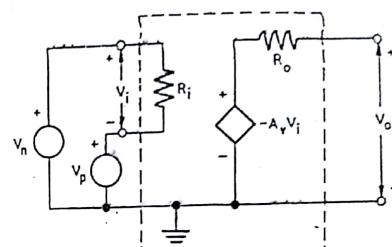


Fig. 7.2 Equivalent circuit of an OPAMP.

### Operational Amplifier Architecture

With the development of technology, design of commercial amplifiers has come close to the ideal (characterised earlier). To obtain these desired characteristics, several stages are employed in cascade. A majority of commercially available OPAMPS employ the four-stage structure displayed in Fig. 7.3.

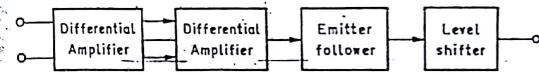


Fig. 7.3 Block diagram of 4-stage OPAMP.

The first stage is a differential amplifier with a double-ended output; this provides high input resistance, high gain for difference signals, and rejection of signals common to both terminals. The second stage is a single output differential amplifier that provides more gain and more discrimination. The third stage is an emitter follower, a buffer to provide low output resistance and isolation of the amplifier from the load. The last stage is a combination level shifter and drive stage. The level shifting corrects for any dc offset that have been introduced by the bias networks or by component imbalances. The driver is a power amplifier to provide large output current with a low output resistance.

Internal structure of each stage is somewhat complicated and it contains many transistors, resistors and diodes. But as OPAMPS are available in IC form, we shall not go into details of that and treat OPAMP as a black-box with the properties, as specified previously. However, the basic circuit and characteristics of a differential amplifier are discussed in Section 7.3.

### OPAMP Parameters

**Open-loop voltage gain ( $A_v$ ).** When the OPAMP is used without any feedback, the differential voltage gain is known as open-loop gain (voltage). With reference to Fig. 7.4 it is given as

$$A_v = -\frac{V_o}{(V_n - V_p)} \quad (7.2)$$

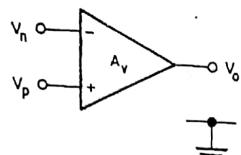


Fig. 7.4

Ideally  $A_v$  is infinite but practically for good OPAMPs, it is in the range of  $10^3$  to  $10^5$ . In the output voltage is limited to  $\pm V_{CC}$ , the supply voltage for such a high gain, the differential voltage should be very small, ideally zero.

**Input resistance ( $R_i$ ).** Input resistance is the open-loop incremental resistance looking into the input terminals and is typically  $2\text{ M}\Omega$ . Sometimes manufacturers quote the resistance between inputs and ground.

**Output resistance ( $R_o$ ).** The open-loop output resistance is usually between  $50\text{ }\Omega$  and  $500\text{ }\Omega$ , typical value for 741 being  $75\text{ }\Omega$ .

**Common mode rejection ratio (CMRR).** Ideally if two equal voltages are applied to the inputs of an OPAMP the output is zero, i.e. the signal which is common to both inputs should not contribute anything to the output voltage. Practically this is not the case as the output depends not only on the difference signal ( $V_p - V_n$ ) =  $V_d$  but also upon the average level  $V_c = (V_p + V_n)/2$ , called common mode signal. Thus

$$\begin{aligned} V_o &= A_d(V_p - V_n) + A_c \left( \frac{V_p + V_n}{2} \right) \\ &= A_d V_d + A_c V_c \\ &= A_d V_d \left( 1 + \frac{1}{\text{CMRR}} \cdot \frac{V_c}{V_d} \right) \end{aligned}$$

where

$A_d$  = difference mode gain

$A_c$  = common mode gain

$\text{CMRR} = |A_d/A_c|$ ; expressed in dB as  $20 \log |A_c/A_d|$

An OPAMP is designed with high CMRR (as high as 90 dB) so that

$$V_o = A_d V_d$$

which means that OPAMP with high CMRR rejects the common mode signal and the output voltage is for all practical purposes contributed only by the difference voltage signal  $V_d$ . Then with reference to Eq. (7.2)

$$A_v = A_d$$

**Example 7.1.** Determine the output voltage of an OPAMP for input voltages of  $V_1 = 120\text{ }\mu\text{V}$  ( $= V_p$ ) and  $V_2 = 80\text{ }\mu\text{V}$  ( $= V_n$ ). The OPAMP has a differential mode gain  $A_d = 10^3$  and CMRR is (i) 100 and (ii)  $10^5$ .

**Solution**

$$V_d = 120 - 80 = 40\text{ }\mu\text{V}$$

$$V_c = (120 + 80)/2 = 100\text{ }\mu\text{V}$$

Substituting values in Eq. (7.3)

$$V_o = A_d V_d \left( 1 + \frac{1}{100} \times \frac{100}{40} \right) = 1.025 A_d V_d$$

$$= 1.025 \times 1000 \times 40 \times 10^{-3} = 41\text{ mV}$$

The output is only 0.25% more than the output due to the difference signal of  $40\text{ }\mu\text{V}$ .

$$V_o = A_d V_d \left( 1 + \frac{1}{10^5} \times \frac{100}{40} \right) = A_d V_d$$

$$= 1000 \times 40 \times 10^{-3} = 40\text{ mV}$$

With this value of CMRR ( $10^5$ ) the effect of common mode signal can be totally ignored.

**Input offset voltage ( $V_{os}$ ).** When both inputs are tied to ground, i.e. both differential and common mode signals are zero, the output should be zero. In practice, however, mismatch in amplifier components results in measurable output voltage. Input offset voltage  $V_{os}$  is the differential input required to make the output zero and is typically  $1\text{ mV}$  (refer Fig. 7.5).

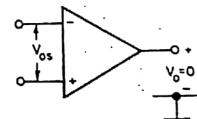


Fig. 7.5

With some OPAMPs, e.g. 741, two voltage offset terminals are provided and a potentiometer is connected between them. The slider of the potentiometer is connected to dc supply (negative) as shown in Fig. 7.6 and it is adjusted to a position on the potentiometer to give zero offset voltage.

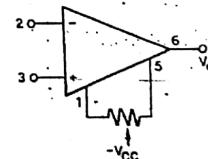


Fig. 7.6 Offset null on 741.

**Input bias current ( $I_B$ ).** Practical OPAMP exhibits unbalance due to mismatch of the transistors which results in unequal bias currents flowing through the input terminals of OPAMP. Input bias current is defined as the average of separate currents entering the two input terminals of a balanced amplifier and is given by

$$I_B = (I_{B1} + I_{B2})/2; \text{ when } V_0 = 0$$

The typical value for 741 is 80 nA.

**Input offset current ( $I_{IO}$ ).** It is defined as the difference between the two input currents at the two terminals of a balanced amplifier and is given by

$$I_{IO} = I_{B1} - I_{B2} \text{ when } V_0 = 0.$$

Typical value of  $I_{IO}$  for 741 is 20 nA.

**Output offset voltage.** It is the output voltage present when both the inputs are grounded.

**Power supply rejection ratio (PSRR).** PSRR is a measure of an OPAMP's ability to discriminate changes in power supply voltage. It is specified by the change in offset voltage for 1 V change in dc power supply. It is usually of 15  $\mu\text{V/V}$  in magnitude.

**Maximum differential input voltage.** This is the maximum value of differential input voltage which can be applied without damaging the OPAMP.

**Maximum common mode input voltage.** This is the maximum voltage to which the two inputs can be raised above ground potential before the OPAMP becomes nonlinear.

#### Frequency Response

Having an OPAMP with high open-loop voltage gain gives flexibility in that the amount of negative feedback can be chosen to bring down the gain to any required value. However, negative feedback may cause instability at high frequencies, because at high frequency the RC couplings produce phase-shift of output with respect to input. If this phase shift equals 180°, the feedback will be positive and undesired oscillations may occur.

To avoid this problem, some OPAMPS, such as 741 have internal RC networks which are designed to deliberately reduce gain at high frequency.

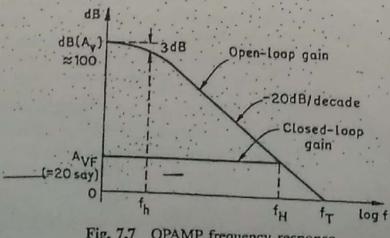


Fig. 7.7 OPAMP frequency response.

#### Operational Amplifiers

The open-loop frequency response (dB vs  $\log f$ ) of an OPAMP is plotted in Fig. 7.7. The open-loop gain  $A_v$  ( $= 10^5$  or 100 dB) remains constant up to a few hertz and drops by 3 dB ( $A_v/2$ ) at the half-power frequency (which is the bandwidth in a dc amplifier) and thereon drops at 20 dB/decade; typically  $f_h = 10$  Hz. The gain drops to 0 dB (unity) at a frequency of  $f_T$  (frequency of unity gain). It is easy to see that

$$\text{dB}(A_v)/20 = \log(f_h/f_T) \text{ or } f_T = A_v f_h \text{ (gain-bandwidth product).}$$

Thus  $f_T$  equals the gain-bandwidth product and is constant for an OPAMP. Its typical value is  $10^5 \times 10 = 1$  MHz. When OPAMP is used in feedback mode (refer Section 7.4, Fig. 7.16), the gain now reduces to  $A_{VF}$  while the half-power frequency (bandwidth) increases to  $f_H$  such that

$$A_v f_h = A_{VF} f_H.$$

In the feedback gain is 20 dB (10), the bandwidth increases to  $(10^5 \times 10)/10 = 10^5$  or 100 kHz.

#### Slew Rate

Because of the internal capacitances, an OPAMP cannot respond instantly to a change in input voltage. There is a limit to the rate at which capacitors will charge and so the rate of change of output voltage is also limited. The limitation is expressed in terms of slew rate which is defined as the maximum time rate of change of output voltage under large signal conditions. Thus

$$\text{Slew rate, } S = \left. \frac{dv_o}{dt} \right|_{\max}$$

Its unit is V/μs and typical value is 0.5 V/μs at  $A_{VF} = 1$  (gain with negative feedback; Eq. (7.15)). It is a measure of the ability of an OPAMP to handle large signals without distortions.

The effect of slew rate in response to an input voltage step is shown in Fig. 7.8.

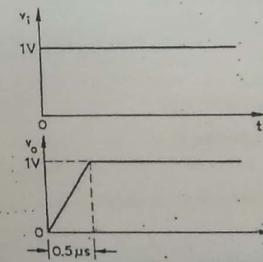


Fig. 7.8 Effect of slew rate.

$$v_o = V_m \sin \omega t$$

$$S = \left. \frac{dv_o}{dt} \right|_{\max}$$

$$= \omega V_m \cos \omega t_{\max}$$

$$= V_m \omega$$

$$S = 2\pi f V_m$$

Thus slew rate limit is a combination of maximum operating frequency and output voltage amplitude. If we attempt to make the output voltage change faster than the slew rate, it would result in distortion of the output wave form.

### 7.3 DIFFERENTIAL AMPLIFIER

The differential amplifier also known as the differential pair, long-tailed pair or emitter-coupled pair (source coupled for FET) is an important circuit because it is invariably used as the means of producing high voltage gain in IC OPAMP. In this context one of its virtues is that it is dc coupled—a necessity because large capacitors are not practicable in ICs and also, for many applications, dc coupling is a requirement.

Figure 7.9 shows the BJT version of a differential amplifier. It can be shown that for a small difference voltage  $V_d = V_1 - V_2$ , the circuit behaves as a linear amplifier. It will be assumed that source resistance  $R_s$  and base spreading resistance  $r_b$  are zero.  $R_E$  is the output resistance of the current-source bias network and current through  $R_E$  can be assumed negligible compared to  $I_C$ .

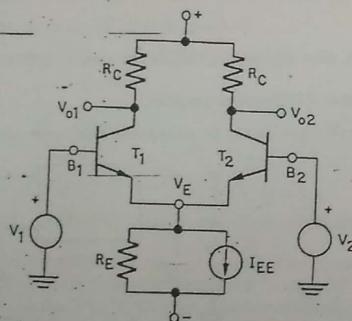


Fig. 7.9 The differential amplifier.

The circuit has two special modes of operation which are discussed below:

**Differential mode.** For  $V_1 = V_2$  and  $\beta \gg 1$ , the collector and emitter currents in each transistor stay equal. Further, because of symmetry of the circuit and negligible current in  $R_E$ ,  $I_C$  (in each collector)  $= I_{E1}/2$ .

Now let us apply an incremental signal  $\Delta V/2$  to  $B_1$  and simultaneously apply  $-\Delta V/2$  to  $B_2$  such that the differential voltage  $V_d = V_1 - V_2 = \Delta V$ . Assuming linearity we can say that  $I_{C1}$  increases by  $\Delta I_C$  and  $I_{C2}$  decreases by  $\Delta I_C$ . Consequently the current in  $R_E$  remains unchanged. Thus  $V_E$  remains

unchanged and so for such incremental changes ( $+\Delta V/2, -\Delta V/2$ ), we can assume each emitter to be grounded.

The situation just described is known as a differential mode because the input signals  $\Delta V/2$  applied to  $T_1$  and  $T_2$  are equal and opposite and a difference  $V_d$  exists. For the difference mode, the equivalent incremental circuit can be drawn as shown in Fig. 7.10(a).

**Common mode.** Now let us consider that both  $V_1$  and  $V_2$  increase by  $\Delta V/2$  and the difference  $V_d$  remains zero. Because of  $R_E$  both  $I_{C1}$  and  $I_{C2}$  will exhibit a small increase  $\Delta I_C$ . Changes in  $I_C$  appear at the emitter and the current in  $R_E$  increases by  $2\Delta I_C$ .

This situation, where equal voltages are applied to  $T_1$  and  $T_2$  is called the common mode. The incremental equivalent circuit is shown in Fig. 7.10(b). It is equivalent to a common emitter stage with an emitter resistance of  $2R_E$ .

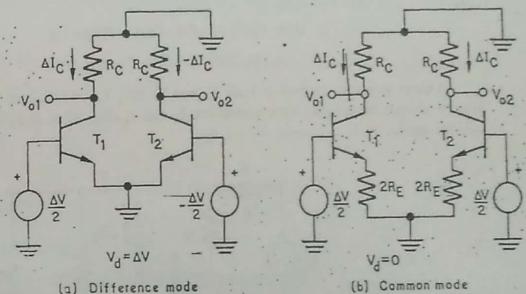


Fig. 7.10 Incremental circuits for differential amplifier operation.

It is evident from Figs. 7.10(a) and (b) that depending upon the input signal, the differential amplifier behaves as either a common emitter stage with emitter grounded (difference mode) or a common emitter stage with emitter resistance (common mode). Therefore, the gain of this amplifier is significantly higher for differential mode than for common mode. Usually, differential amplifiers are designed so that, for practical purposes, only difference signals are amplified.

#### Analysis of Differential Amplifier

As is evident from Figs. 7.10(a) and (b), the circuits for both common mode, difference mode and operations are identical on both sides. Hence only one side is to be analyzed.

**Difference mode gain ( $A_d$ ):** For difference mode with  $V_d/2$  applied to  $T_1$  and  $-V_d/2$  to  $T_2$ . Using half-circuit concept, the small-signal model of one side can be drawn as in Fig. 7.11.

The difference mode gain  $A_d$  is given as

$$A_d = V_{o1}/V_d = -\beta R_C/2r_n = -(g_m R_C/2) \quad (7.5)$$

As  $+V_d/2$  is applied at the base  $T_1$ ,  $V_{o1}$  is out-of-phase with it ( $A_d$  being negative), while the base of  $T_2$  is driven by  $-V_d/2$ , and so  $V_{o2}$  is in phase with  $V_d$ .

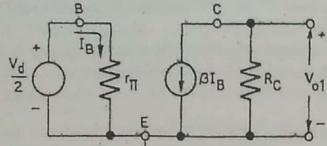


Fig. 7.11 Small signal model for difference mode.

**Common mode gain ( $A_c$ ).** When the signal  $V_c = 1/2 (\Delta V/2 + \Delta V/2) = \Delta V/2$  is applied to both transistors (common mode), we can draw the equivalent model as in Fig. 7.12. It easily follows that

$$A_c = V_{o1}/V_c = -\beta R_C/[2(1 + \beta)R_E + r_\pi] \\ = -R_C/2R_E, \text{ for } \beta \gg 1 \text{ and } r_\pi \ll 2R_E$$

As same signal is applied to both  $T_1$  and  $T_2$  both  $V_{o1}$  and  $V_{o2}$  are  $180^\circ$  out of phase with each other. Further comparing the gain expressions for  $A_d$  and  $A_c$  (Eqs. (7.5) and (7.6)), it is easily seen that a suitable choice of  $R_E$  can make  $A_c \ll A_d$ .

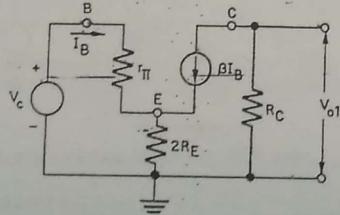


Fig. 7.12 Small-signal model for common mode.

**Common mode rejection ratio (CMRR).** The common mode rejection ratio is defined as

$$\text{CMRR} = A_d/A_c$$

Substituting values of  $A_d$  and  $A_c$  from Eqs. (7.5) and (7.6) we get

$$\text{CMRR} = \frac{-\beta_m R_C/2}{-R_C/2R_E} = \beta_m R_E$$

Thus large value of CMRR requires large  $R_E$ . Hence current sources with high output resistance are used in differential amplifiers.

#### FET Version of Differential Amplifier

MOSFETs or JFETs are also used for realizing differential amplifier for which the circuit is shown in Fig. 7.13.

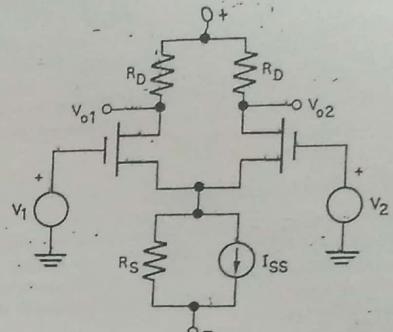


Fig. 7.13 FET version of differential amplifier.

Using similar analysis, as for BJT, CMRR can be found to be

$$\text{CMRR} = 1 + R_S(1 + \mu)/(r_d + R_D); \mu = g_m r_d \quad (7.8a)$$

$$= 1 + g_m R_S = g_m R_S; r_d \gg R_D \text{ and } \mu \gg 1 \quad (7.8b)$$

Active loads, often depletion MOSFETs, are used to realize  $R_D$  in Fig. 7.13.

#### Representation of Differential Amplifier

The differential amplifier can be represented as a linear amplifying block as shown in Fig. 7.14.

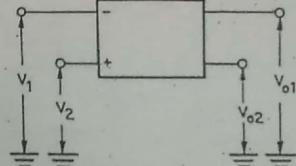


Fig. 7.14 Representation of a differential amplifier with inverting and noninverting inputs.

We can write

$$V_1 = V_d/2 + V_c \quad (7.9a)$$

$$V_2 = -V_d/2 + V_c \quad (7.9b)$$

$$V_d = V_1 - V_2 \quad (7.10a)$$

$$\frac{V_c}{V_e} = (V_1 + V_2)/2 \quad (7.10b)$$

We can thus write the output  $V_{o1}$  as

$$V_{o1} = A_d V_d + A_c V_c$$

For large value of CMRR ( $10^3 - 10^5$ )

$$= A_d \left( V_d + \frac{V_c}{CMRR} \right) \quad (7.1)$$

$$\begin{aligned} V_{o1} &= A_d V_d = A_d (V_1 - V_2) \\ &= A_d V_1 - A_d V_2 \end{aligned} \quad (7.1)$$

As per Eq. (7.12)  $V_1$  appears in  $V_{o1}$  in inverted form (as  $A_d$  has negative value (Eq. 7.5)) and appears in  $V_{o1}$  in noninverted form ( $-A_d$  is positive). This is indicated by -ve (inverting) and +ve (noninverting) terminals at the input of the differential amplifier.

Similarly,

$$\begin{aligned} V_{o2} &= -A_d V_d + A_c V_c \\ &= -A_d \left( V_d - \frac{V_c}{CMRR} \right) \\ &= -A_d V_d = -A_d V_1 + A_d V_2; \text{ for large CMRR} \end{aligned} \quad (7.1)$$

Notice that both the outputs are functions of  $V_d (= V_1 - V_2)$  only for large CMRR and are negative (or in phase opposition) of each other. If only one output is used, the differential amplifier can be represented as in Fig. 7.15.

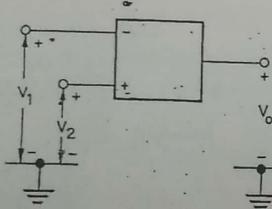


Fig. 7.15 Differential amplifier with single-ended output.

**Example 7.2.** In the differential amplifier of Fig. 7.9, transistors are biased at  $I_{CQ} = 100 \mu\text{A}$ ; each transistor has  $\beta = 2000$ . The amplifier is to be designed for  $A_d = 250$  and CMRR = 74 dB. Determine the value of  $R_C$  and  $R_E$ . What is the input resistance of the amplifier?

**Solution.** For each transistor

$$\begin{aligned} r_\pi &= \frac{25\beta}{I_C(\text{mA})}; \beta = 2000; I_{CQ} = 100 \mu\text{A} \\ &= \frac{25 \times 2000}{100} = 500 \text{ k}\Omega \end{aligned}$$

$$g_m = \beta/r_\pi = \frac{2000}{500} = 4 \text{ mS}$$

$$CMRR = A_d/A_c = 74 \text{ dB or } 5000$$

$$A_d = 250 \text{ (given)}$$

$$CMRR = g_m R_E; \text{ Eq. (7.7)}$$

$$5000 = 4 \times R_E \quad \text{or} \quad R_E = 1250 \text{ k}\Omega \text{ or } 1.25 \text{ M}\Omega$$

$$A_d = g_m R_C/2$$

$$250 = 4R_C/2 \quad \text{or} \quad R_C = 125 \text{ k}\Omega$$

$$R_{in} = 2r_\pi = 2 \times 500 = 1000 \text{ k}\Omega \text{ or } 1 \text{ M}\Omega$$

**Example 7.3.** Input to the differential amplifier of Example 7.2 comprises

$$v_1 = 15 \sin 100\pi t + 5 \sin 2\pi \times 10^3 t \text{ mV}$$

$$v_2 = 15 \sin 100\pi t - 5 \sin 2\pi \times 10^3 t \text{ mV}$$

The signal at 50 Hz is an interference signal and that at 1 kHz is to be processed.

Determine (i)  $v_{o1}(t)$  and (ii)  $v_{o2}(t)$ .

**Solution.**

$$v_d = v_1 - v_2$$

$$= 10 \sin 2\pi \times 10^3 t$$

$$v_c = (v_1 + v_2)/2 = 5 \sin 100\pi t$$

As calculated in Example 7.2

$$A_d = 250, A_c = 250/5000 = 0.05$$

$$v_{o1} = A_d v_d + A_c v_c$$

$$= 250 \times 10 \sin 2\pi \times 10^3 t + 0.05 \times 5 \sin 100\pi t$$

$$= 2500 \sin 2\pi \times 10^3 t + 0.25 \sin 100\pi t$$

Signal amplified      Interference attenuated

$$v_{o2} = -A_d v_d + A_c v_c$$

$$= -250 \sin 2\pi \times 10^3 t + 0.25 \sin 100\pi t$$

Signal amplified      Interference attenuated

**Example 7.4.** The circuit shown in Fig. 7.16 uses identical transistors with  $\beta = 200$ .

- (a) With  $v_1 = v_2 = 0$ , determine  $I_{CQ}$  and  $I_{BQ}$ . Choose a suitable value of  $V_{CEQ}$ .
- (b) With the input conditions in part (a) and bias currents as calculated, find  $v_{o1}$  and  $v_{o2}$  and emitter voltage.
- (c) Evaluate  $A_d$ ,  $A_c$  and CMRR.
- (d) Determine input resistances to differential and common mode signals ( $R_{id}$  and  $R_{ic}$ ).

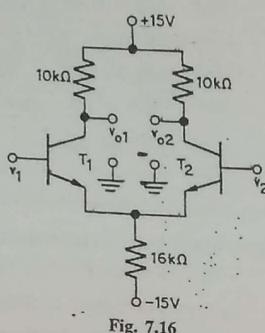


Fig. 7.16

**Solution.** (a) For any one collector-emitter loop

$$15 - 10I_C - V_{CE} - 2 \times 16I_C + 15 = 0$$

Choose  $V_{CEQ} = 12$  V  
It gives

$$I_{CQ} = 0.428 \text{ mA}$$

$$I_{BQ} = 0.428/200 = 2.14 \mu\text{A}$$

$$r_\pi = (25 \times 200)/0.428 = 11.7 \text{ k}\Omega$$

$$g_m = \beta/r_\pi = 200/11.7 = 17 \text{ mS}$$

$$v_{o1} = 15 - 0.428 \times 10 = +10.72 \text{ V}$$

$$v_{o2} = v_{o1} = +10.72 \text{ V}$$

$$R_C = 10 \text{ k}\Omega, R_E = 16 \text{ k}\Omega$$

$$A_d = g_m R_C / 2 \\ = 17 \times 10/2 = 85$$

$$A_c = R_C / 2R_E \\ = 10/(2 \times 16) = 0.313$$

$$\text{CMRR} = A_d / A_c = 271$$

(b)

(c)

(d) With reference to Fig. 7.11

$$R_{id} = 2r_\pi = 2 \times 11.7 = 23.4 \text{ k}\Omega$$

( $r_\pi$  is contributed in series from each side)

With reference to Fig. 7.12

$$R_{ic} = r_\pi + 2(\beta + 1) R_E \\ = (11.7 + 2 \times 201 \times 16) \text{ k}\Omega = 6.44 \text{ M}\Omega$$

7.1 BASIC OPERATIONAL AMPLIFIER CIRCUITInverting Amplifier

Consider the OPAMP connected in the circuit of Fig. 7.16 described below.

- Input signal  $V_1$  is applied to the inverting terminal through series resistance  $R_1$ .
- Output ( $V_o$ ) is feedback to the inverting terminal through the feedback resistance  $R_F$ .
- The noninverting terminal of OPAMP is grounded.

The circuit is easily analyzed on the assumptions that for the OPAMP  $A_v = \infty$ ,  $R_f = \infty$  and  $R_o = \infty$ . These imply  $V_i$  (differential voltage) is almost 0 and OPAMP does not draw any current so that current through  $R_1$  is the same as the current through  $R_F$ .  $V_i = 0$  also means that the inverting terminal is a virtual ground. It then follows that

$$I = V_i/R_1 = -V_o/R_F \quad (7.15)$$

$$V_o/V_i = -(R_F/R_1) = A_{VF}$$

IT IS INVERTED!

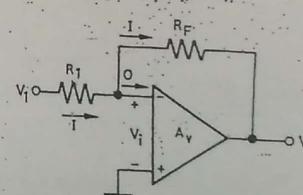


Fig. 7.17 Inverting OPAMP circuit.

Thus this circuit acts as an inverting amplifier with closed loop voltage gain  $A_{VF}$ , which has negative value indicating phase inversion of the output signal (w.r.t. the input signal). As the value of  $A_{VF}$  depends entirely upon the externally connected resistors, it can be made as accurate as desired by selecting external resistors of appropriate accuracy. Recall that in fabrication of ICs, resistor ratios can be controlled with much greater precision than values of individual resistors.

Practical Inverting OPAMP Circuit

The equivalent circuit for an inverting stage using a practical OPAMP is shown in Fig. 7.18. Here

For steady state ac operation the result of Eq. (7.15) generalizes to its phasor form

$$\bar{A}_{VF} = \bar{V}_o / \bar{V}_i = -\bar{Z}_F / \bar{Z}_1$$

where  $\bar{Z}_1$  = input impedance and  $\bar{Z}_F$  = feedback impedance.

input resistance  $R_i = \infty$  but output resistance  $R_o$  and gain  $A_v$  are finite. Nodal analysis of this circuit gives

$$A_{VF} = \frac{V_o}{V_i} = \frac{-A_v R_F + R_o}{R_i (1 + A_v) + R_F + R_o}$$

We see that the output is negative w.r.t. input, i.e. it is inverted.

For  $R_o \rightarrow 0$  and  $A_v \rightarrow \infty$ ,  $A_{VF}$  reduces to the value given in Eq. (7.15) wherein OPAMP is regarded as ideal.

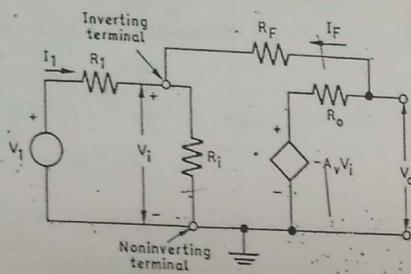


Fig. 7.18 Circuit equivalent of inverting amplifier (practical).

**Example 7.5.** For the inverting OPAMP circuit of Fig. 7.19

$$R_i = 1 \text{ M}\Omega, R_o = 0, A_{\infty} = 2.5 \times 10^5, R_1 = 10 \text{ k}\Omega, R_F = 1 \text{ M}\Omega$$

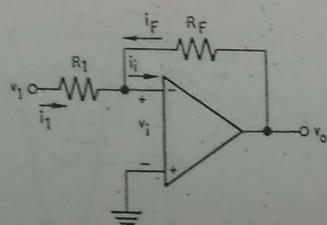


Fig. 7.19

If  $V_o = -5 \text{ V}$ , calculate  $v_i$ ,  $i_o$ ,  $i_1$  and  $i_F$ . Do these values justify the assumption that the OPAMP is ideal?

**Solution.**

$$v_o/v_i = -(R_F/R_1); \text{ Eq. (7.15)}$$

or

$$\begin{aligned} v_i &= -v_o (R_1/R_F) \\ &= 5 \times (10/10^3) = 0.05 \text{ V or } 50 \text{ mV} \\ v_i &= 5/(2.5 \times 10^5) = 0.02 \text{ mV} \end{aligned}$$

$$v_i \ll v_i$$

$$\begin{aligned} i_1 &= (v_1 - v_i)/R_1 \\ &= (5 \times 10^3 - 0.02)/10 = 500 \mu\text{A} = -i_F \\ i_i &= v_i/R_i \\ &= 0.02/1000 = 0.00002 \mu\text{A} \end{aligned}$$

$$i_i \ll i_1$$

As the OPAMP satisfies conditions (i) and (ii) above, it can be regarded as ideal.

**Example 7.6.** For the circuit shown in Fig. 7.20, calculate  $V_o$ . The OPAMP is ideal.

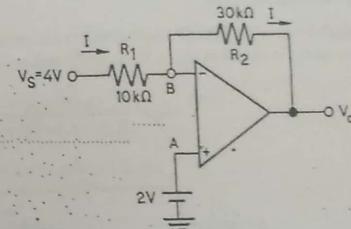


Fig. 7.20

**Solution.** Here

$$\begin{aligned} V_B &= V_A = 2 \text{ V} \\ I &= (V_S - V_B)/R_1 = (4 - 2)/10 \text{ k}\Omega = 0.2 \text{ mA} \\ V_o &= -IR_F + V_B = -0.2 \times 30 + 2 = -4 \text{ V} \end{aligned}$$

Had the result of such a calculation exceeded the supply voltage, then  $V_o$  would be limited to the supply voltage.

#### Noninverting Amplifier

The OPAMP is used as a noninverting amplifier stage as in the circuit shown in Fig. 7.21. Assuming ideal conditions,

$$\begin{aligned} V(\text{at A}) &= V_1 \text{ as } V_1 = 0 \\ \frac{V_1}{R_1} + \frac{(V_T - V_o)}{R_F} &= 0 \end{aligned}$$

$$V_o/V_1 = 1 + (R_F/R_1)$$

We see that output is of same sign as input, i.e. it is not inverted.

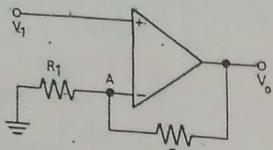


Fig. 7.21 Noninverting amplifier.

The desired amplifier gain can be achieved by selecting the proper values of  $R_F$  and  $R_1$ . The noninverting amplifier configuration provides high input impedance because the path to ground for the input is through the high input impedance inverting terminal.

#### Practical Noninverting Stage

The practical noninverting OPAMP stage is analyzed in an identical manner as is the inverting stage. Equivalent circuit is shown in Fig. 7.22. It easily follows from nodal analysis that

$$A_{VF} = \frac{A_v (R_1 + R_F)}{R_1 (1 + A_v) + R_F + R_o}$$

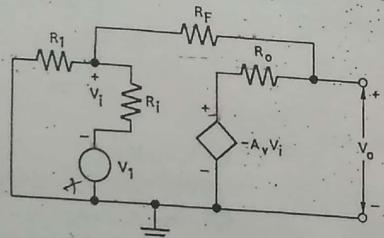


Fig. 7.22 Circuit model—noninverting amplifier (practical).

It can be verified that for  $A_v = \infty$

$$A_{VF} = 1 + (R_F/R_1)$$

**Example 7.7.** For the circuit shown in Fig. 7.23 sketch the wave forms of  $v_s$  and  $v_o$ .  
Solution.

$$v_s = 2 \sin \omega t$$

Assuming ideal OPAMP

$$\bar{v}_B/R_S = (v_o - v_B)/R_F$$

or

$$v_o = (1 + R_F/R_S)v_B$$

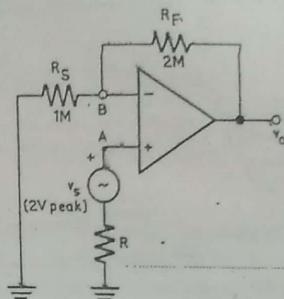


Fig. 7.23

$$v_B = v_A = v_s$$

$$v_o = (1 + R_F/R_S)v_s$$

$$= (1 + 2/1) \times 2 \sin \omega t = 6 \sin \omega t$$

The wave forms of  $v_s$  and  $v_o$  are shown in Fig. 7.24.

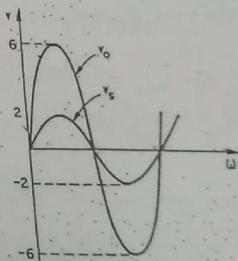


Fig. 7.24

Can you think the use of resistance  $R$ ? What will happen if  $R_F$  is made  $10 \text{ M}\Omega$ ?

#### 7.5. APPLICATIONS OF OPAMPS

While the ideal OPAMP is a linear device in that the output is directly proportional to the input for all values of input voltage, the practical OPAMPS have characteristic as shown in Fig. 7.25.

As the transfer characteristic shows, the practical OPAMP acts as a linear device over a certain range of the input and as a nonlinear (saturating) device otherwise. The applications of OPAMP can be accordingly classified as linear and nonlinear applications.

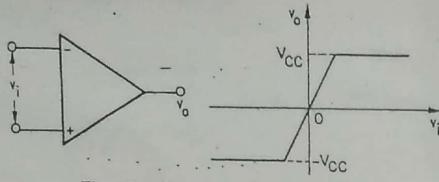


Fig. 7.25 OPAMP transfer characteristic.

## 7.6. LINEAR APPLICATIONS OF OPAMPS

## Adder or Summing Amplifier

Figure 7.26 gives the circuit of the OPAMP used as an adder. Since the inverting terminal of OPAMP acts as a virtual ground

$$\text{or } i_1 + i_2 + i_3 = i_F$$

$$\text{or } v_1/R_1 + v_2/R_2 + v_3/R_3 = -v_o/R_F$$

$$\text{If } R_F = R_1 = R_2 = R_3 \text{ then } v_o = -(v_1 + v_2 + v_3)$$

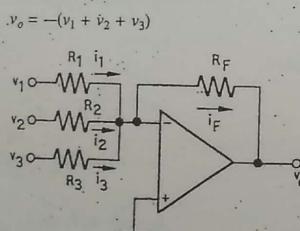


Fig. 7.26 OPAMP adder circuit.

Thus the circuit acts as an inverting adder.

If

$$\text{then } R_1 = R_2 = R_3 = 3R_F$$

$$\begin{aligned} v_o &= -1/3(v_1 + v_2 + v_3) \\ &= \text{average of three inputs} \end{aligned}$$

## Subtractor

The OPAMP can be used as a subtractor with the circuit as shown in Fig. 7.27.

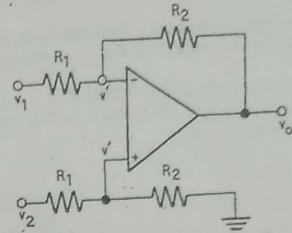


Fig. 7.27 OPAMP subtractor circuit.

Assuming ideal OPAMP, we can write

$$(v_1 - v')/R_1 = (v' - v_o)/R_2 \quad (i)$$

and

$$(v_2 - v')/R_1 = v'/R_2 \quad (ii)$$

Eliminating  $v'$  in Eqs. (i) and (ii), we get

$$\begin{aligned} v_o &= (R_2/R_1)(v_2 - v_1) \\ &= (v_2 - v_1) \text{ for } R_2 = R_1 \end{aligned} \quad (7.21)$$

Thus the circuit acts as a unity gain subtractor.

## Voltage Follower

This simple configuration shown in Fig. 7.28 is called voltage follower wherein the output is fed back to the inverting terminal of the OPAMP with input applied at the noninverting terminal. It is in fact a noninverting amplifier of Fig. 7.21 with  $R_F = 0$  and  $R_1$  as open circuit. As per Eq. (7.17).

$$\begin{aligned} v_o/v_i &= 1 + R_F/R_1 \\ &= 1 + 0 = 1 \end{aligned}$$

Thus the output follows the input.

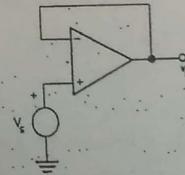


Fig. 7.28 Voltage follower.

If we analyze the circuit by using nonideal model, we find that if the OPAMP has open-loop gain of  $A$ , input impedance  $R_i$  and output impedance of  $R_o$ , then in the voltage follower configuration input impedance becomes  $AR_i$  and the output impedance becomes  $R_o/A$  (Reader should verify this), i.e. the input impedance is increased and output impedance is reduced considerably.

This circuit is used in isolating a high impedance source from a low impedance load. Isolating circuit is called a *buffer* and this particular type of buffer is called *unity gain buffer*. Example 7.8. In the circuit of Fig. 7.29(a)  $R_s = 1 \text{ k}\Omega$  and  $R_L = 10 \text{ k}\Omega$  for the OPAMP.  $A = 10^5$ ,  $R_i = 100 \text{ k}\Omega$  and  $R_o = 100 \Omega$ . For  $v_o = 10 \text{ V}$ . Calculate (i)  $v_s$  (ii)  $v_o/v_s$  and (iii) input output resistance of the circuit.

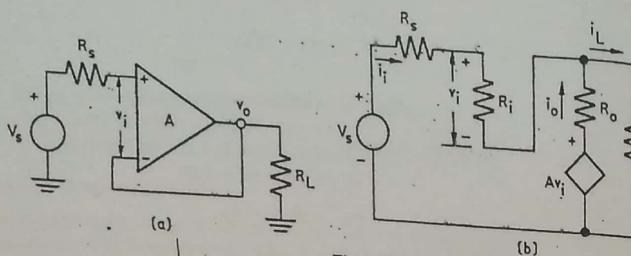


Fig. 7.29

**Solution.** The equivalent circuit is shown in Fig. 7.29(b). For

$$v_o = 10 \text{ V}$$

$$i_L = v_o/R_L = (10/10) = 1 \text{ mA}$$

As  $i_i$  is very small

$$i_o \approx i_L$$

Hence

$$\begin{aligned} Av_i &= v_o + i_o R_o = v_o + i_L R_o \\ &= 10 + 10^{-3} \times 10^2 = 10.1 \text{ V} \end{aligned}$$

Therefore

$$v_i = (Av_i)/A = 10.1 \times 10^{-5} \text{ V}$$

Hence

$$i_i = v_i/R_i = 1.01 \times 10^{-10} \text{ A}$$

Then

$$\begin{aligned} v_s &= v_o + i_i(R_s + R_i) \\ &= 10.00001 \text{ V} \end{aligned}$$

$$A_{VF} = v_o/v_s$$

$$= 10/10.00001 = 0.999999$$

Thus it is a voltage follower with unity gain. Also our assumption of ideal OPAMP is justified. Input resistance:

$$\begin{aligned} R_{IF} &\equiv v_s/i_i \\ &= 10/(1.01 \times 10^{-10}) \\ &= 10^{11} \Omega = AR_i; \text{ very high} \end{aligned}$$

Output resistance:  
Open circuiting load

Substituting  $v_i$  from Eq. (ii) in Eq. (i)

$$i_i = \frac{v_s}{R_s + (1 + A)R_i + R_o} \quad (\text{iv})$$

$$i_o = -i_i \quad (\text{v})$$

$$v_{oc} = Av_i + R_o i_i$$

$$= \frac{(R_o + AR_i)v_s}{R_s + (1 + A)R_i + R_o} \quad (\text{vi})$$

$$AR_i \gg R_o \quad (\text{vii})$$

$$(1 + AR_i) \approx AR_i \gg (R_s + R_o)$$

Therefore

$$v_{oc} \approx v_s$$

Short circuiting output

$$i_{sc} = \frac{v_s}{R_s + R_i} + \frac{Av_i}{R_o} \quad (\text{viii})$$

But

$$v_i = v_s; \text{ as } R_s i_i \text{ is negligible}$$

Then

$$\begin{aligned} i_{sc} &\approx \frac{v_s}{R_o} \text{ as } A \gg 1 \\ R_{oF} &= v_{oc}/i_{sc} \\ &= R_o/A \quad (\text{ix}) \end{aligned}$$

Substituting values

$$R_{oF} = 100/10^5 = 10^{-3} \Omega; \text{ extremely low} \quad (\text{x})$$

**Current to Voltage Converter (Transresistance Amplifier)**

Figure 7.30 shows the circuit for a current to voltage converter.

The input current  $I_i$  is applied directly to the inverting input of the OPAMP. Therefore  $I_F = I_i$  and  $V_o = -I_i R_F$ .

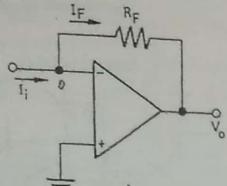


Fig. 7.30 Current to voltage converter.

One of the disadvantages of this configuration is that the input bias current gets added to the output current. Hence

$$V_o = -(I_B + I_i) R_F$$

Therefore, care should be taken to keep  $I_B$  as small as possible.

Often a capacitor is used in parallel with  $R_F$  to reduce noise at high frequencies.

#### Voltage to Current Converter (Transconductance Amplifier)

For driving relays, analog meters, etc. a voltage to current converter is commonly used. The circuit is shown in Fig. 7.31.

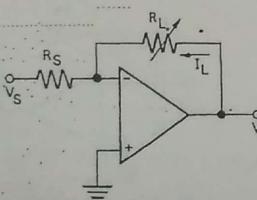


Fig. 7.31 Voltage to current converter.

Using the concept of virtual ground,

$$V_s/R_S = -V_o/R_L = -I_L$$

$$\text{or } I_L = -V_s/R_S$$

As is clear from the above equation, the output current is independent of the load resistance  $R_L$  and the circuit works as a constant current source if  $V_s = \text{constant}$ .

It may be observed here that the circuit of voltage to current converter of Fig. 7.31 is the same as that of the inverting amplifier (Fig. 7.17).

If the load is not of 'floating' type, i.e. if one end of it is grounded, a different circuit configuration as shown in Fig. 7.32(a) is used. A robust constant current source for grounded load can be arranged by using an external transistor also as shown in Fig. 7.32(b).

For the circuit of Fig. 7.32(b) voltage at noninverting terminal is

$$V_1 = V_s \left( \frac{R_2}{R_1 + R_2} \right)$$

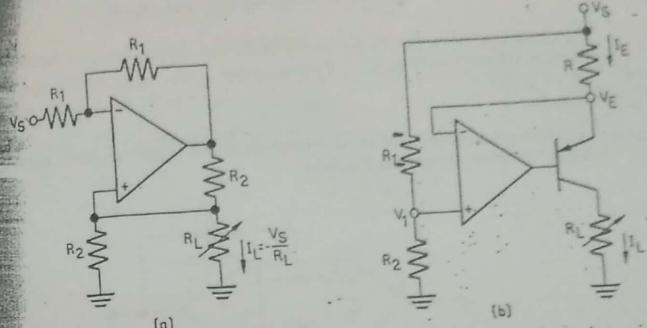


Fig. 7.32 Voltage to current converter for grounded load.

Voltage at inverting terminal is nearly  $V_E$ . Due to feedback these two input voltages become equal so that  $V_1 = V_E$ . A current  $I_E$  is set up in the emitter, which is given by

$$I_E = (V_S - V_E)/R = (V_S - V_1)/R$$

$$= (V_S/R) (R_1/(R_1 + R_2))$$

$$I_L = I_C = I_E; \text{ independent of } R_L$$

Now if, due to any reason,  $V_E$  goes below  $V_1$ , then output voltage of OPAMP (positive) increases. Both these effects cause the forward bias on the emitter base junction to be reduced, this in turn reduces the emitter current  $I_E$  and so in effect  $V_E$  is increased and comes back to  $V_1$ . Thus a constant current is maintained through load  $R_L$ . Here a low output current OPAMP is used to drive the transistor which in turn drives the high current load. Polarity may be reversed by using *n-p-n* transistor.

#### Constant Voltage Source

The circuit of Fig. 7.33 gives a setup that yields a constant voltage at the output which is independent of the load  $R_L$ . It can easily be shown that

$$V_o = -(R_F/R_S)V_s$$

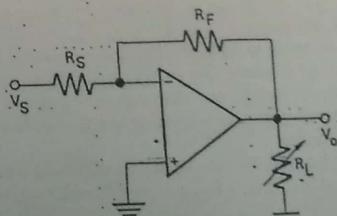


Fig. 7.33 Constant voltage source.

The circuit has low output impedance and hence can act as a voltage reference source, if  $v_1$  is a reference voltage such as a cell or a Zener device.

*✓ Integrator*

Integrators are used in a variety of measurement and signal processing applications. The OPAMP integrator is drawn in Fig. 7.34.

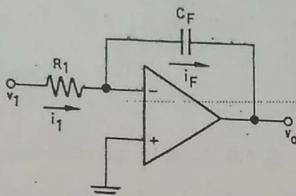


Fig. 7.34 OPAMP as an integrator.

Because there is a virtual ground at the input,

$$\begin{aligned} v_o &= -\frac{1}{C_F R_1} \int v_1 dt \\ i_1 &= v_1 / R_1 = i_F \\ i_F &= \frac{dv_o}{dt} \\ v_o &= -(1/C_F) \int i_F dt \\ &= -(1/C_F R_1) \int v_1 dt \end{aligned} \quad (7.21)$$

So the output is a scaled version of the integral of the input voltage.

Two sources of error are inherently present in an OPAMP integrator. These are:

1. A very small dc off-set voltage present at the OPAMP input.
2. Input bias current which flows through the feedback capacitor.

*[These two effects integrate over time and produce continually rising output till the OPAMP saturates. This limits the time period over which the circuit can be used as an integrator before its operation must be recycled. Recycling would limit the error amplitude to acceptable value.]*

*[The effect of bias current can be minimized by increasing  $C_F$  and simultaneously decreasing  $R_1$  for a specified time constant  $C_F R_1$ .]*

The practical set up of an OPAMP integrator is shown in Fig. 7.35. With switch  $S_a$  in position 1, the input is zero. At the same time switch  $S_b$  is also in position 1, which charges the feedback capacitor to voltage  $V_0$ , thereby providing an initial condition. With both switches  $S_a$  and  $S_b$  in position 2, the circuit goes into integrating mode with the initial condition as established in position 1 of the switches.

Inclusion of  $R_2$  between the noninverting terminal and ground reduces the component of bias current flowing towards  $C$ . This effect is minimized when  $R_2 = R_1$  (input resistance).

*Differentiator*

If we interchange the role of  $R$  and  $C$  in the integrator of Fig. 7.34, as in Fig. 7.36, we get

### Operational Amplifiers

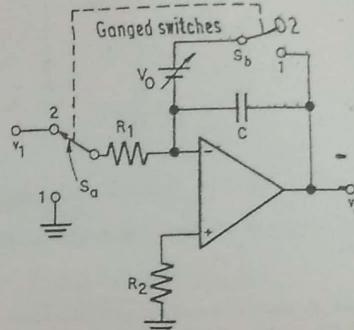


Fig. 7.35

A differentiator. Here the output voltage is proportional to the time rate of change of input voltage.

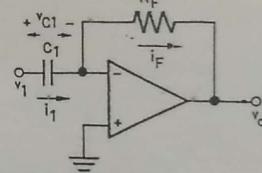


Fig. 7.36 OPAMP differentiator.

From Fig. 7.36

$$i_1 = C_1 \frac{dv_{Cl}}{dt}$$

Assuming ideal operation ( $v_{Cl} = v_1$ )

$$-v_o/R_F = C_1 \frac{dv_1}{dt}$$

$$v_o = -(R_F C_1) \frac{dv_1}{dt} \quad (7.23)$$

If the input to the differentiator is  $v_1 = \sin \omega t$ , the output is  $v_o = -R_F C_1 \omega \cos \omega t$ . It means that the output voltage increases linearly with signal frequency. This leads to amplification of the high frequency noise component which greatly enhances signal distortion. For this reason differentiation is avoided in electronic circuits.

At low frequency the property of the differentiator that the output voltage amplitude increases linearly with frequency leads to the use of differentiator as frequency-to-voltage signal converter.

**Example 7.9.** For Fig. 7.37 sketch  $v_o$  for 50 ms after switch  $S$  is opened.

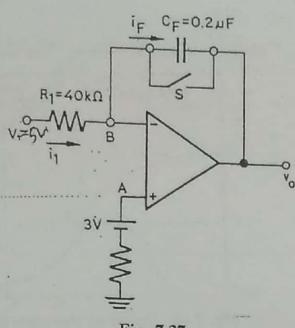


Fig. 7.37

**Solution.** (a) When switch  $S$  closed

$$v_o = V_B = V_A$$

$$= +3 \text{ V}$$

(b) When  $S$  is opened,

$$v_o = -(1/C_F) \int_0^t i_1 dt + 3$$

$$i_1 = (5 - 3)/40 \text{ k}\Omega = 0.5 \times 10^{-4} \text{ A}$$

Substituting values in Eq. (i), we get

$$\begin{aligned} v_o &= -(10^6/0.2) \int_0^t 0.5 \times 10^{-4} dt + 3 \\ &= -250t + 3 \end{aligned}$$

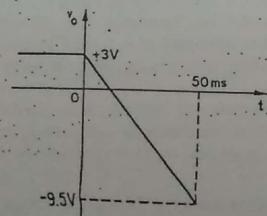


Fig. 7.38

$$v_o(50 \text{ ms}) = -250 \times 50 \times 10^{-3} + 3 = -9.5 \text{ V} \quad (\text{iv})$$

As per Eq. (ii) the output voltage is a negative going linear ramp beginning at +3 V reaching a value of -9.5 V at  $t = 50 \text{ ms}$  as plotted in Fig. 7.38

**Example 7.10.** For the OPAMP circuit of Fig. 7.39 find the output voltage as a function of time.

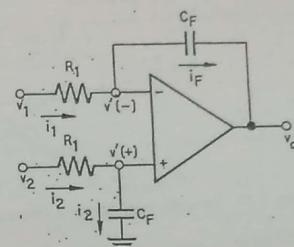


Fig. 7.39

**Solution.** According to OPAMP characteristic

$$v'(-) = v'(+) = v'$$

$$i_1 = (v_1 - v')/R_1 \quad (\text{i})$$

$$(v_o - v') = -(1/C_F) \int i_1 dt \quad (\text{ii})$$

$$i_2 = (v_2 - v')/R_1 \quad (\text{iii})$$

$$v' = (1/C_F) \int i_2 dt \quad (\text{iv})$$

Substituting Eq. (i) in Eq. (ii) and Eq. (iii) in Eq. (iv), we get

$$v_o - v' = -(1/R_1 C_F) \int (v_1 - v') dt \quad (\text{v})$$

$$v' = (1/R_1 C_F) \int (v_2 - v') dt \quad (\text{vi})$$

Adding Eqs (v) and (vi) we have

$$v_o = (1/R_1 C_F) \int (v_2 - v_1) dt \quad (\text{vii})$$

Hence the circuit acts as a differential integrator.

#### OPAMP Circuits with Frequency Sensitive Elements

When the input and feedback circuit elements are frequency sensitive, these can be written in impedance form in the frequency domain. The corresponding OPAMP circuit diagram is drawn in

Fig. 7.40. By analogy with Fig. 7.17 it immediately follows that

$$\frac{\bar{V}_o(j\omega)}{\bar{V}_i(j\omega)} = -\frac{\bar{Z}_F(j\omega)}{\bar{Z}_1(j\omega)}$$

when  $\bar{V}_o(j\omega)$  and  $\bar{V}_i(j\omega)$  are indeed the phasors

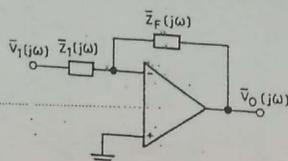


Fig. 7.40 Inverting amplifier with frequency sensitive elements.

### 7.7 OPAMP FILTERS

#### Low-pass Filter

The OPAMP integrator of Fig. 7.34 is easily modified to a low-pass filter by adding a resistor  $R_1$  in series with the feedback capacitor  $C_1$ .

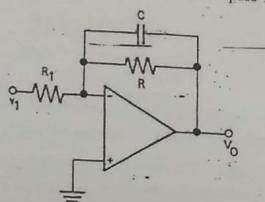


Fig. 7.41 A simple low-pass filter.

parallel to the feedback capacitor. The modified circuit is presented in Fig. 7.41. For this case

$$\bar{Z}_F(j\omega) = \frac{1}{j\omega C} \parallel R = \frac{R}{1 + jCR\omega}$$

$$\bar{Z}_1(j\omega) = R_1$$

$$\frac{\bar{V}_o(j\omega)}{\bar{V}_i(j\omega)} = \frac{R/R_1}{1 + jCR\omega} = \tau = CR$$

$$\text{Critical frequency, } \omega_c = 1/\tau = 1/CR$$

The frequency response ( $\text{dB} - \log f$  and  $\phi - \log f$  plots) are presented in Fig. 7.42.

<sup>1</sup>Negative sign is not included as it is easily removed by a unit gain OPAMP circuit in tandem.

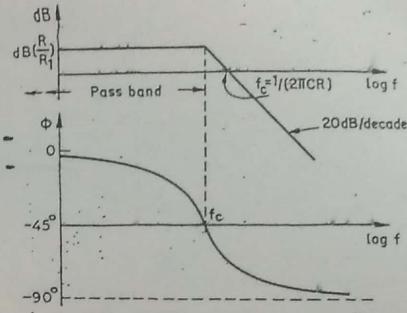


Fig. 7.42 Frequency response—low-pass filter.

#### High-pass Filter

Consider the differentiation circuit of Fig. 7.36 modified to include  $R_1$  in series with capacitor  $C_1$ . It can easily be established that

$$\frac{\bar{V}_o(j\omega)}{\bar{V}_i(j\omega)} = \frac{jC_1 R_F \omega}{1 + jC_1 R_F \omega}; \tau = 1/C_1 R_F \quad (7.26)$$

$$\text{Critical frequency, } \omega_c = 1/\tau = 1/C_1 R_F$$

The frequency response corresponding to Eq. (7.26) is plotted in Fig. 7.43 from which it is easily seen that the circuit acts as a high-pass filter and so will pick-up any high frequency noise as already stated for the differentiator. It may also be observed from Eq. (7.26) and Fig. 7.43 that the modified circuit acts as an approximate differentiator at  $\omega \ll \omega_c$ .

OPAMP filter circuits with better performance compared to the above simple circuit will now be taken up.

The integrator and differentiator circuits described earlier are examples of simple filters, although usually a practical low- or high-pass filter is required to provide constant gain in the pass region. Filter circuits that are constructed using OPAMPs are called active filters. These are superior to passive filters constituted of  $R$ ,  $L$  and  $C$  in several respects. Active filters have the great advantage of not needing  $L$ -component, which is bulky and expensive particularly for linear operation.

Typical active low-pass and high-pass filter circuits are shown in Figs. 7.44(a) and (b) respectively. These filters are essentially noninverting amplifiers with input frequency-sensitive circuits. The gain ( $A$ ) in the pass region is determined by  $R_1$  and  $R_2$ , the cut-off frequency ( $f_c$ ) by  $C$  and  $R$ .

Consider the low-pass filter, Fig. 7.44(a). The voltage  $\bar{V}_p$  at the noninverting input is related to the circuit input  $\bar{V}_i$  by potential divider relationship.

<sup>1</sup>Negative sign is not included as it is easily removed by a unit gain OPAMP circuit in tandem.

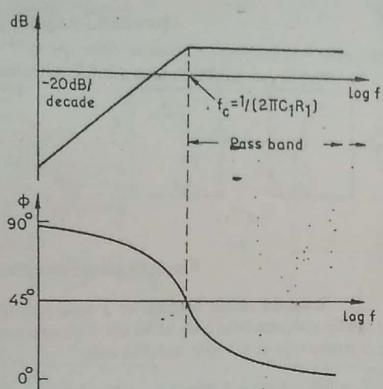


Fig. 7.43 Differentiator as high-pass filter.

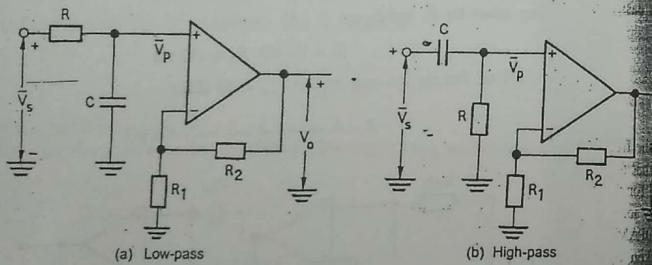


Fig. 7.44 Active filters.

Hence

$$\frac{\bar{V}_o}{\bar{V}_s} = \left( \frac{1/j\omega C}{R + 1/j\omega C} \right) \bar{V}_s = \frac{\bar{V}_s}{1 + j\omega\tau}; \tau = RC$$

From Eq. (7.17)

$$\frac{\bar{V}_o}{\bar{V}_s} = 1 + \frac{R_2}{R_1} = A$$

Then

$$\frac{\bar{V}_o}{\bar{V}_s} = \frac{A}{1 + j\omega\tau}; f_c \text{ (cut-off frequency)} = 1/2\pi\tau$$

The frequency response of this filter is shown in Fig. 7.45(a); the phase versus frequency characteristic is omitted for clarity.

Analysis of high-pass filter of Fig. 7.44(b) gives

$$\frac{\bar{V}_o}{\bar{V}_s} = \frac{A}{1 + 1/j\omega\tau}; f_c = 1/2\pi\tau; \tau = RC \quad (7.27)$$

The variation in gain magnitude with frequency for this case is shown in Fig. 7.45(b).

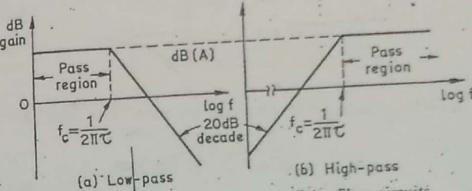


Fig. 7.45 Frequency-response of the filter circuits.

**Example 7.11.** Find the step response of low-pass and high-pass filters of Figs. 7.44(a) and (b). Also sketch both the responses.

**Solution.** For this purpose we shall use the Laplace transform technique.  
For unit step input (Fig. 7.46(a))

$$v_s(t) = u(t) \rightarrow V_s(s) = 1/s$$

(a) Low-pass filter: In s-domain

$$\frac{V_o(s)}{V_s(s)} = \frac{1}{1 + s\tau}; s = j\omega$$

$$V_o(s) = \frac{\alpha}{s(s + \alpha)}; \alpha = 1/\tau$$

Partial fractioning

$$V_o(s) = \frac{1}{s} - \frac{1}{s + \alpha}$$

Taking inverse Laplace transform, we have

$$v_o(t) = (1 - e^{-t/\tau}) u(t)$$

This response is sketched in Fig. 7.46(b).

(b) High-pass filter: In s-domain

$$\frac{V_o(s)}{V_s(s)} = \frac{1}{1 + 1/s\tau} = \frac{s}{s + \alpha}; \alpha = 1/\tau$$

$$v_o(s) = \frac{1}{(s + \alpha)}$$

$$v_o(t) = e^{-\alpha t} u(t)$$

This response is sketched in Fig. 7.46(c).

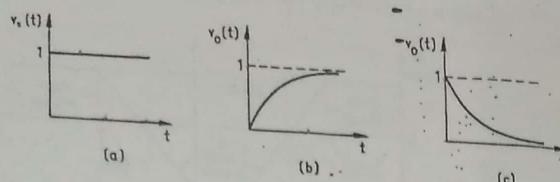


Fig. 7.46

#### Band-reject Filter

When it is required to suppress a specified frequency band from a system's output a summing amplifier can be used in conjunction with low- and high-pass filters as in Fig. 7.47(a).

At frequencies below  $f_{c1}$  the summing amplifier input signal supplied by the low-pass filter is reduced; similarly when  $f > f_{c2}$  the low-pass filter output is reduced. Between  $f_{c1}$  and  $f_{c2}$ , filter outputs are attenuated; this range usually covers a particularly troublesome frequency band suppressed. The rejection band is indicated in dB-log  $f$  plot of Fig. 7.47(b).

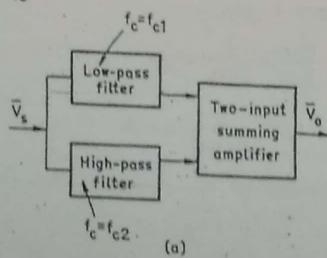


Fig. 7.47 Band-reject filter.

#### Band-pass Filter

By forming a cascade of low- and high-pass filters as in Fig. 7.48(a) a specified frequency band is amplified (passed) as shown in Fig. 7.48(b).

The filter positions can be reversed, i.e. high-pass followed by low-pass; outside the pass-band ( $f_{c2} - f_{c1}$ ) the gain falls off due to loss of amplification by one or other of the filters.

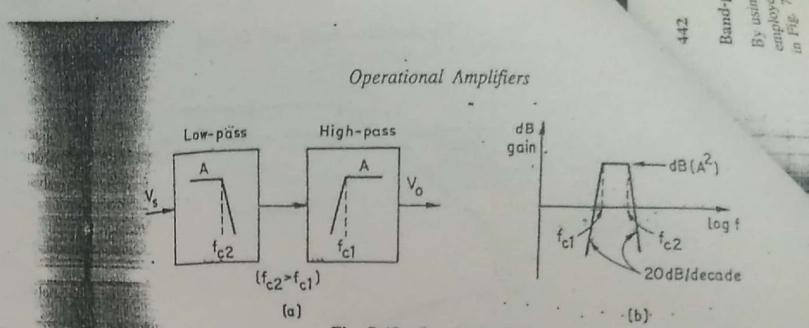


Fig. 7.48 Band-pass filter.

**Example 7.12.** Draw the circuit diagram of a band-pass filter, specified bandwidth is 30 kHz, centred at 18 kHz with pass-band gain of 40 dB. Calculate suitable component values. Estimate the open-loop gain at frequencies of 0.3 kHz and 132 kHz.

**Solution:**  $f_{c1} = (18 - 30/2) = 3 kHz,  $f_{c2} = (18 + 30/2) = 33 kHz. Each section has a pass region gain of 20 dB, i.e.$$

$$A = 10 = 1 + R_2/R_1$$

satisfactory values for  $R_1$  and  $R_2$  are

$$R_1 = 20 \text{ k}\Omega, R_2 = 180 \text{ k}\Omega$$

choose  $C = 1 \text{ nF}$ . For the low-pass section ( $f_{c2} = 33 \text{ kHz}$ ):

$$R = \frac{1}{2\pi \times 33 \text{ kHz} \times 1.2 \text{ nF}} = 4 \text{ k}\Omega$$

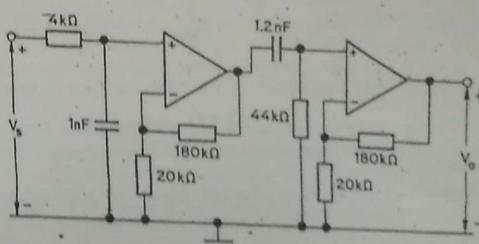


Fig. 7.49 Circuit diagram for the band-pass filter in Example 7.12.

for the high-pass section ( $f_{c1} = 3 \text{ kHz}$ ):

$$R = \frac{1}{2\pi \times 3 \text{ kHz} \times 1.2 \text{ nF}} = 44 \text{ k}\Omega$$

Its complete circuit is drawn in Fig. 7.49.

At 0.3 kHz (one decade below  $f_{c1}$ ) the gain is 20 dB. At 132 kHz (two octaves above  $f_{c2}$ ) the gain is 28 dB (20 dB/decade corresponds to 6 dB/octave).

## Band-pass Filter Using Single OPAMP

By using multiple feedbacks it is possible to devise a band-pass filter with a single OPAMP. A circuit employed is shown in Fig. 7.50(a). It has the frequency response of a tuned amplifier shown in Fig. 7.50(b).

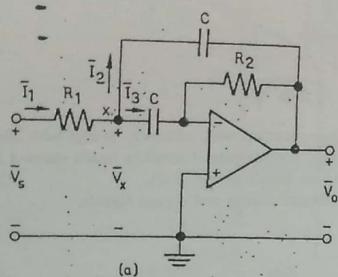
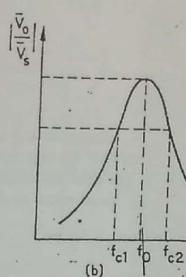


Fig. 7.50

The  $Q$  factor (selectivity) of a band-pass filter is defined as

$$Q = \frac{f_0}{f_{c2} - f_{c1}}$$

where  $f_0$  = centre frequency,  $(f_{c2} - f_{c1})$  = bandwidth.

Applying Kirchhoff's law to the filter circuit of Fig. 7.50(a), we can write

$$\bar{I}_1 = \frac{\bar{V}_s - \bar{V}_x}{R_1}$$

$$\bar{I}_2 = (\bar{V}_x - \bar{V}_o) j\omega C$$

 $\bar{I}_3 = j\omega C \bar{V}_x$ ; OPAMP input ports are at ground potential.

At node x

$$\bar{I}_1 = \bar{I}_2 + \bar{I}_3$$

Substituting values, we get

$$\frac{\bar{V}_s - \bar{V}_x}{R_1} = (\bar{V}_x - \bar{V}_o) j\omega C + j\omega C \bar{V}_x$$

As per Eq. (7.23)

$$v_o = -(CR_2)(dv_x/dt)$$

Taking Laplace transform

$$V_o(s) = -(CR_2)(sV_x(s))$$

$$V_x(s) = -\frac{V_o(s)}{s(CR_2)}$$

$$\bar{V}_x = -\frac{\bar{V}_o}{j\omega CR_2}$$

Substituting for  $\bar{V}_x$  in previous equation and reorganizing the system network function as

$$\frac{\bar{V}_o}{\bar{V}_s} = \frac{-0.5(R_2/R_1)}{1 + j[(\omega CR_2)/2 - 1/(2\omega CR_1)]} \quad (7.29)$$

The gain has a maximum value when the imaginary term vanishes, i.e. when

$$\frac{\omega CR_2}{2} = \frac{1}{2\omega CR_1}$$

It then follows that

$$f(f_0) = \frac{1}{2\pi C\sqrt{(R_1 R_2)}}$$

At this frequency

$$\left| \frac{\bar{V}_o}{\bar{V}_s} \right| = \frac{0.5R_2}{R_1}$$

The two cut-off frequencies occur when this imaginary term equals  $\pm 1$ . It easily follows that

$$(f_{c2} - f_{c1}) = \frac{1}{2\pi CR_1} \quad (7.30)$$

Hence

$$Q = \frac{f_0}{(f_{c2} - f_{c1})} = \sqrt{(R_2/R_1)} \quad (7.31)$$

## 7.5 NONLINEAR APPLICATIONS OF OPAMPS

## Comparator

Comparator is one of the several important nonlinear application of OPAMPs. The Fig. 7.51(a) shows an OPAMP noninverting comparator.

The circuit compares two voltages. One is a fixed reference voltage  $V_R$  and the other is a time varying analog voltage  $v_i$ . When the input  $v_i$  is slightly greater than  $V_R$ , the effective small positive voltage at the noninverting input gets amplified by the amplifier and the gain is the large open-loop gain. Consequently, the output of the OPAMP saturates at  $+V$ , the supply voltage. Similarly, when the input is slightly less than  $V_R$ , the OPAMP saturates at  $-V$ . Thus the level of the OPAMP circuit output voltage switches between  $\pm V$ , the sign indicating whether the input is higher or lower than the reference voltage.

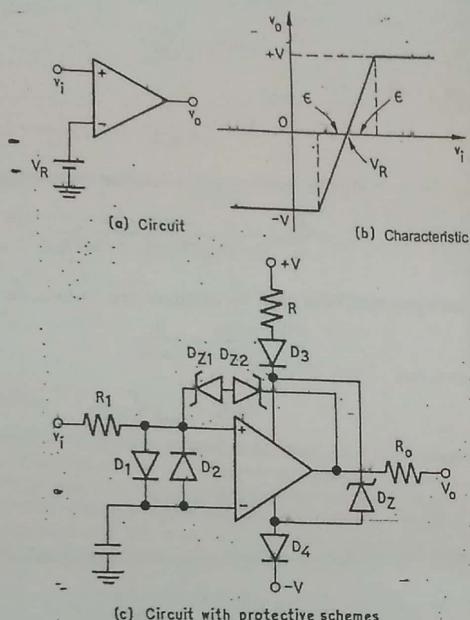


Fig. 7.51 OPAMP comparator.

The input-output characteristic of the comparator of Fig. 7.51(a) is sketched in Fig. 7.51(b). The change-over region around  $V_R$  is  $\epsilon$  on either side where

$$\epsilon = V/A; V = \text{saturation value}, A = \text{OPAMP gain}$$

As  $A$  is extremely high ( $10^5$  or more),  $\epsilon$  is in  $\mu\text{V}$  (see Example 7.14) and can be ignored for practical purposes. If  $V_R = 0$ , i.e. the inverting terminal is grounded, the comparator becomes a zero-crossing comparator. Also by interchanging the terminals of OPAMP to which  $v_i$  and  $V_R$  are connected, the comparator becomes an inverting one.

The OPAMP comparator with all the protections is given in Fig. 7.51(c). For protecting OPAMP against the excessive input voltage, diodes  $D_1$  and  $D_2$  are used across the input. Similarly for limiting the output swing, zener diodes  $D_{Z1}$  and  $D_{Z2}$  are used in feedback path. The resistor  $R_1$  limits the current through input protection diodes. To protect the OPAMP from damage due to wrong polarity of the dc supply, diodes  $D_3$  and  $D_4$  are used as shown. For the output short-circuit protection, a series output resistor  $R_o$  is used. For protection from excessive dc supply zener diode  $D_Z$  with a  $V_Z$  equal to 2 V is used.

**Example 7.13.** For Fig. 7.52 sketch the output waveform  $v_o$ , if  $v_i = 5 \sin \omega t$ .

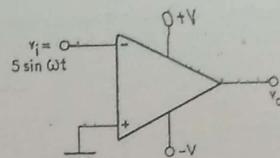


Fig. 7.52

**Solution.** The circuit acts as an inverting comparator with reference voltage zero. The output state of the OPAMP changes whenever the input crosses zero. Circuit is hence called a zero detector circuit. The input and output wave forms are drawn in Fig. 7.53.

This circuit works as an interface between analog and digital signals.

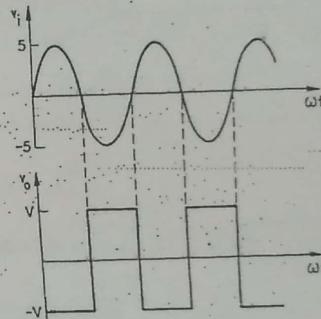


Fig. 7.53

**Example 7.14.** In the comparator of Fig. 7.51(a)  $V_R = 2 \text{ V}$ .

- OPAMP supply voltage is  $\pm 15 \text{ V}$ . What value of  $v_i$  will cause the output voltage to change from positive to negative. Given:  $A = 10^5$  for the OPAMP.
- Sketch the input/output wave forms when  $v_i = 8 \sin \omega t \text{ V}$ .

**Solution.** (a) The change-over region around  $V_R$  is

$$\epsilon(\text{on each side}) = 15/10^5 = 15 \mu\text{V} \text{ (of input)}$$

Total change in input for switching from positive to negative or vice versa is  $2\epsilon$ .

$$v_i^+ \text{ at the edge of positive change-over} = 2 + 0.00015 = 2.00015 \text{ V}$$

$$v_i^- \text{ at the edge of negative change-over} = 2 - 0.00015 = 1.99985 \text{ V}$$

For  $v_i < v_i^-$ , the comparator will switch over to  $-15 \text{ V}$  and to  $+15 \text{ V}$  at  $v_i > v_i^+$ .

As said before  $\epsilon$ -region can be ignored without loss of accuracy

- The input-output wave forms are sketched in Fig. 7.54 wherein  $\theta = \sin^{-1}(2/8) = 14.5^\circ$

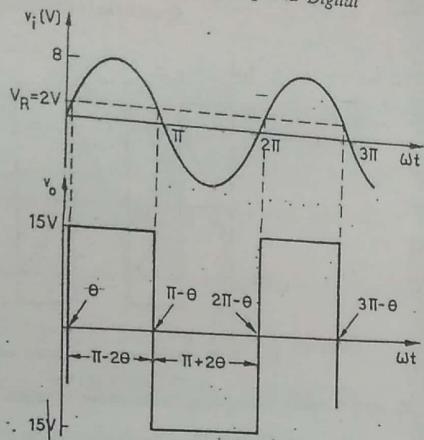


Fig. 7.54

Comparison with Fig. 7.53 reveals that  $V_R$  causes the positive rectangular parts of the output voltage waves to be shorter in width than negative parts as indicated in Fig. 7.54.

#### Window Comparator (Sense Amplifier)

By combining a noninverting and an inverting comparator, both having different reference voltages, we can realize a window comparator shown in Fig. 7.55. The output  $v_o$  of the comparator goes to zero (zero) when  $v_i$  is between  $V_{\text{Low}}$  and  $V_{\text{High}}$  (reader should verify this).

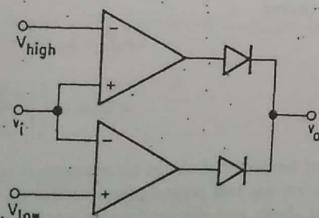


Fig. 7.55 Window comparator (sense amplifier).

#### Logarithmic Amplifier

A logarithmic amplifier has an output voltage which is proportional to the logarithm of the input.

$$v_o \propto \log v_i$$

The linear OPAMP can be combined with a nonlinear element such as a diode or a transistor to achieve this. The output gets greatly compressed. Therefore, the response of a meter across output will be like that of a decibel meter. Though a diode can be used for realizing a log amplifier

the grounded base transistor (BJT) is used because its exponential relation between current and voltage extends over a much wider voltage range. A typical circuit is shown in Fig. 7.56.

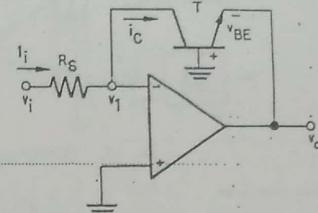


Fig. 7.56 Logarithmic amplifier.

Since the base of the transistor is grounded and  $v_i = 0$  (+ terminal of OPAMP is grounded), therefore  $v_{CB} = 0$ . Collector current is given as

$$i_C = \beta i_B \quad (i)$$

$$i_C = \beta I_s \exp(ev_{BE}/kT) \quad (ii)$$

for a forward biased emitter-base pn-junction. We can write Eq. (ii) as

$$i_C = I_0 \exp(ev_{BE}/kT); I_0 = \beta I_s$$

$$v_{BE} = (kT/e) \ln(i_C/I_0)$$

Since the transistor emitter is connected to the output of the OPAMP,

$$v_o = v_{EB} = -v_{BE} = -(kT/e) \ln(i_C/I_0) \\ = -(kT/e) \ln(v_i/I_0 R_S) \text{ as } i_C = v_i/R_S$$

Thus  $v_o$  is proportional to  $\log v_i$ .

One disadvantage of this configuration is that output depends on temperature ( $T$ ) and reverse saturation current ( $I_s = I_0/\beta$ ). These effects can be reduced by suitable compensating circuits which will not be discussed here.

Antilog amplifier can be made by interchanging positions of  $R_S$  and the transistor in Fig. 7.56.

**Example 7.15.** Design a multiplier using log and antilog amplifiers.

**Solution.** We can sum the logarithms of the two inputs  $x$  and  $y$  and using antilog circuit, obtain the product as indicated by the following relationship.

$$\log x + \log y = \log xy$$

$$\text{Antilog}(\log xy) = xy$$

A multiplier based on this approach is shown in Fig. 7.57.

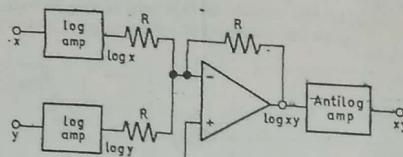


Fig. 7.57 OPAMP multiplier.

**Square Wave Generator**

A simple square wave generator can be constructed using an OPAMP and a pair of back-to-back connected zener diodes as shown in Fig. 7.58.

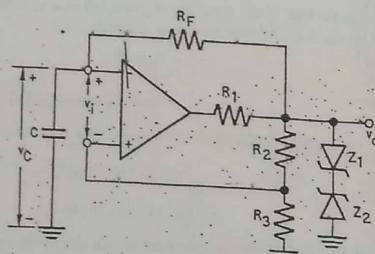


Fig. 7.58 Square wave generator.

As the output  $v_o$  of the circuit is connected to the ground by two zener diodes it is therefore limited to either  $+V_Z$  or  $-V_Z$  assuming that both zener diodes have identical breakdown voltage. The capacitor  $C$  is charged through the resistor  $R_F$  from the output voltage  $v_o$  and a fraction  $\beta = R_2/(R_2 + R_3)$  of the output voltage is feedback to the noninverting terminal of the OPAMP. The differential input voltage is given by

$$v_i = v_C - \beta v_o$$

- When  $v_i$  is +ve the output will be  $-V_Z$  and when  $v_i$  is -ve, the output will be  $+V_Z$ . If we consider an instant when  $v_C < \beta v_o$ , then the capacitor will start charging exponentially towards  $V_Z$  ( $= V_Z$ ) through  $R_F$ , while the output will remain constant at  $V_Z$ . When  $v_C$  exceeds  $\beta v_o$  by a fraction of volts,  $v_i$  becomes -ve and output becomes  $-V_Z$ . Since the voltage across the capacitor does not change suddenly, it discharges exponentially to  $-V_Z$ . The output and capacitor voltage waveforms are shown in Fig. 7.59.

If we assume at  $t = 0$ ,  $v_C = -\beta V_Z$ , then the expression for the capacitor voltage for the first cycle will be given by

$$v_C(t) = V_Z [1 - (1 + \beta) \exp(-t/R_F C)]$$

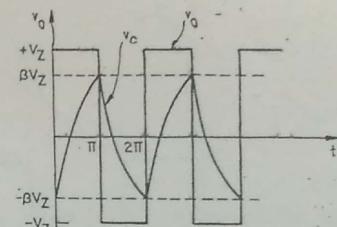


Fig. 7.59 Waveforms in square wave generator.

$$T_1 = T_2, v_C(t) = +\beta V_Z. \text{ Substituting in the above equation}$$

$$+\beta V_Z = V_Z [1 - (1 + \beta) \exp(-T_1/R_F C)]$$

which gives

$$T_1 = R_F C \ln \left( \frac{1 + \beta}{1 - \beta} \right)$$

The discharging time  $T_2$  is similarly given by

$$T_2 = R_F C \ln \left( \frac{1 + \beta}{1 - \beta} \right)$$

Thus the time period

$$T = T_1 + T_2 ; T_1 = T_2 = T/2$$

$$= 2R_F C \ln \left( \frac{1 + \beta}{1 - \beta} \right)$$

With the help of the above circuit we get symmetrical square waveform. If unsymmetrical waveform is desired then we use two zener diodes such that  $V_{Z1} \neq V_{Z2}$ .

The circuit above provides good square wave in audio frequency range. Maximum frequency at which circuit can operate is limited by the slew rate of the OPAMP.

**Triangular Wave Generator**

Triangular wave can be generated by integrating the square wave.

In the OPAMP circuit of Fig. 7.60 the output of the comparator switches between +ve and -ve saturation voltages depending upon the input. The matched zener diode pair clamps the output to either  $+V_Z$  or  $-V_Z$ . Let us assume that at  $t = 0$ ,  $v_2 = +V_Z$ . Then the current through the integrator is given by

$$I = V_Z / (R_3 + R_4) ; v_2 = V_Z \quad (i)$$