Zakhary Kaplan

Altera · Kingston, ON

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Education

Bachelor of Applied Science | University of Toronto *Sep 2018 – Jun 2023*

- Studied *Computer Engineering* at the Faculty of Applied Science & Engineering.
- Achieved *Dean's List Scholar* for all semesters; conferred *High Honours* upon graduation.

Work

FPGA Architect | Altera (formerly Intel) *Jul 2023* – Present

- Working on Altera's next-generation FPGA's architectures.

Teaching Assistant | University of Toronto *Aug 2022 – May 2023*

- Hired as an undergraduate teaching assistant for C++ project-based lab component of ECE244 (Programming Fundamentals), and for Verilog processor design and ARM assembly labs for ECE243 (Computer Organization).

Computer Architect | Qualcomm *May 2021 – Aug 2022*

- Created transaction level model for cache architecture for use in several IPs within the Snapdragon's digital signal processor (DSP).
- Diagrammed architectures and prepared internal presentations justifying designs.
- Lead exploration of high-level synthesis (HLS) workflows within architecture team.

Software Developer | Geomechanica Inc. *May 2020 – Aug 2020*

- Developed and tested features for Irazu, a geomechanical simulation software.
- Duties included implementation of CAD editor tools, visualization of simulation outputs, project file management, and licensing. Worked using Qt in C++.

Researcher | University of Toronto *May 2020 – Aug 2020*

- Explored use of machine learning (ML) to extract topics from tweets via natural language processing with TensorFlow on BERT and XLNet models.
- Researched improvements to distributed ML using federated learning (FL) on PyTorch. Developed framework for conducting experiments. Coauthor of paper presented at IEEE INFOCOM discussing findings of FL project.

Projects

Nintendo Game Boy Emulator | Rust *2022* – Present

- Implemented a complete hardware emulator of the DMG-01 Nintendo Game Boy, including a cycle accurate SM83 (Z80-derivative) CPU model.

Neovim Plugin | Lua *2022 – 2023*

- Created and currently maintaining an open source Neovim plugin for managing trailing whitespace. Featured in *This Week In Neovim* newsletter.

KAP-16 Instruction Set Architecture | Specification *2021 – 2022*

- Designed a 16-bit instruction set architecture (ISA) for a custom CPU. Used Huffman codings when deciding encodings to innovatively improve instruction density.

Mapper | C++, GTK *2020*

- Solved NP-complete graph problems (travelling salesman variant) using advanced meta-heuristic and simulated annealing iterative improvement algorithms.

16-bit CPU | Verilog, DE1-SoC *2020*

- Implemented an 16-bit toy CPU in Verilog with clearly defined control and data paths. Compiled and tested on DE1-SoC FPGA development board.

Publications

- **Optimizing Federated Learning on Non-IID Data with Reinforcement Learning** *IEEE INFOCOM 2020*
  Hao Wang, Zakhary Kaplan, Di Niu, Baochun Li.

Relevant Courses

ECE241: **Digital Systems** A+

Digital logic circuit design with substantial hands-on laboratory work using Verilog on FPGA boards.

ECE243: **Computer Organization** A+

CPU design in Verilog and ARM instruction set architecture. Focus on memory, caches, and scheduling IO with interrupts.

ECE345: **Algorithms & Data Structures** A+

Trees, graphs, amortized analysis, hashing, dynamic programming, greedy, NPC.

APS360: **Artificial Intelligence Fundamentals** A+

Optimizing neural networks, autoencoders, RNNs, NLP, GANs.

ECE334: **Digital Electronics** A+

Digital design techniques for integrated circuits, CMOS logic design, Elmore delays.

ECE344: **Operating Systems** A+

Concurrency, deadlock, CPU scheduling, memory management, file systems.

ECE244: **Programming Fundamentals** A+

Object-oriented programming in C++.