tel: 416-602-2925
mail: me@zakhary.dev
web: zakhary.dev
git: git.zakhary.dev

Zakhary Kaplan

Technical Skills

Assembly | C | C++ | Rust | Python | Lua | MATLAB | Arduino | Unix | Vim | ARM | FPGA | Quartus II | Verilog | HLS | Emulation | Transaction Level Modelling | Caches | Algorithms | VSLI | ML | PyTorch | TensorFlow

Relevant Courses

Digital Systems | A+
- Digital logic circuit design with substantial hands-on laboratory work using Verilog on FPGA boards.

Digital Electronics | A+
- Digital design techniques for integrated circuits, CMOS logic design, Elmore delays.

Computer Organization | A+
- CPU design in Verilog and ARM instruction set architecture. Focus on memory, caches, and scheduling IO with interrupts.

Operating Systems | A+
- Concurrency, deadlock, CPU scheduling, memory management, file systems.

Algo. & Data Structures | A+
- Trees, graphs, amortized analysis, hashing, dynamic programming, greedy, NPC.

Programming Fund. | A+
- Object-oriented programming in C++.

AI Fundamentals | A+
- Optimizing neural networks, autoencoders, RNNs, NLP, GANs.

Education

Bachelor of Applied Science in progress | University of Toronto *2018–Present*
- Studying **Computer Engineering** in the Faculty of Applied Science & Engineering.
- **3.94 Grade Point Average** cumulative over all semesters to date.
- **Dean's List Scholar** for all semesters to date.

Experience

Teaching Assistant | University of Toronto *September–December 2022*
- Hired as an undergraduate teaching assistant for C++ project-based lab component of ECE244 (Programming Fundamentals). Will invigilate and grade written exams.

Computer Architect | Qualcomm *May 2021–August 2022*
- Created transaction level model for cache architecture for use in several IPs within the Snapdragon's digital signal processor (DSP).
- Diagrammed architectures and prepared internal presentations justifying designs.
- Lead exploration of high-level synthesis (HLS) workflows within architecture team.

Software Developer | Geomechanica Inc. *May–August 2020*
- Developed and tested features for Irazu, a geomechanical simulation software.
- Duties included implementation of CAD editor tools, visualization of simulation outputs, project file management, and licensing. Worked using Qt in C++.

Researcher | iQua Research Group *May–August 2019*
- Explored use of machine learning (ML) to extract topics from tweets via natural language processing with TensorFlow on BERT and XLNet models.
- Researched improvements to distributed ML using federated learning (FL) on PyTorch. Developed framework for conducting experiments: github.com/iQua/flsim.

Projects

Nintendo Game Boy Emulator | Rust *2022*
- Implemented a complete hardware emulator of the DMG-01 Nintendo Game Boy handheld console, including a cycle accurate SM83 (Z80-derivative) CPU model.

Neovim Plugin | Lua *2022*
- Created and currently maintaining an open source Neovim plugin for managing trailing whitespace. Featured in *This Week In Neovim* newsletter.

KAP-16 Instruction Set Architecture *2021*
- Designed a 16-bit instruction set architecture (ISA) for a custom CPU. Used Huffman codings innovatively as improvement to instruction density: git.zakhary.dev/kap-16.

16-bit CPU | Verilog, DE1-SoC *2019*
- Implemented an 16-bit toy CPU in Verilog with clearly defined control and data paths. Compiled and tested on DE1-SoC FPGA development board.

Mapper | C++, GTK *2019*
- Solved NP-complete graph problems (travelling salesman variant) using advanced meta-heuristic and simulated annealing iterative improvement algorithms.

Publications

- **Optimizing Federated Learning on Non-IID Data with Reinforcement Learning**
  Hao Wang, Zakhary Kaplan, Di Niu, Baochun Li. *IEEE INFOCOM 2020*.