Zakhary Kaplan

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Education

BASc in Computer Engineering | University of Toronto *Sep 2018 – Jun 2023*

- Obtained 3.89/4.0 GPA. Course average 88%.
- Conferred *High Honours* upon graduation; *Dean's List Scholar* for all semesters.
- Completed certificates in *Artificial Intelligence* and *Engineering Business*.

Work

FPGA Architect | Altera *(formerly Intel)* *Jul 2023* – Present

- Designed workflow and toolkit for analyzing fabric routing delays in SPICE using raw netlist data at transistor level.
- Modelled FPGA fabric clock-tree self-balancing delay blocks; workflow tracks nightly regressions in RTL.
- Explored feasibility of proposed changes to routing fabric informed by modelling performance impact.

Teaching Assistant | University of Toronto *Aug 2022 – May 2023*

- ECE243 *Computer Organization*: ARM v7 assembly for Cortex A9, Verilog soft-core CPUs, embedded programming.
- ECE244 *Programming Fundamentals*: C++ language, object-oriented programming, data structures, and complexity.

Computer Architect | Qualcomm *May 2021 – Aug 2022*

- Created transaction level model for cache prefetcher used by IPs within Snapdragon's digital signal processor (DSP).
- Worked on architecture specification for multi-level cache system informed by data-driven simulation results.
- Lead exploration of high-level synthesis (HLS) workflows within architecture team.

Software Developer | Geomechanica Inc. *May 2020 – Aug 2020*

- Developed and tested geomechanical simulation features in C++/Qt, including: CAD editor, rendering, and licences.

ML/AI Researcher | University of Toronto *May 2019 – Aug 2019*

- Applied ML to extract topics from tweets using NLP sentiment analysis with TensorFlow on BERT and XLNet.
- Researched distributed ML via federated learning in PyTorch; coauthored IEEE INFOCOM paper on findings.

Publications

- **Optimizing Federated Learning on Non-IID Data with Reinforcement Learning** *IEEE INFOCOM 2020*
  Hao Wang, Zakhary Kaplan, Di Niu, Baochun Li.

Projects

- **Game Boy Emulator**: Hardware emulator of the DMG-01 Game Boy, including a cycle accurate SM83 (Z80-derivative) CPU model. Includes native (macOS/Linux/Windows), iOS, and web frontends. Contains over 30kloc.
- **Dynamic DNS Client**: Daemon for periodically querying and updating DNS server records.
- **Dotfiles**: Workspace configuration with portable installer script; supports `git`, `nvim`, `tmux`, `zsh`, and more.
- **16-bit ISA**: Designed 16-bit ISA for theoretical CPU; used Huffman coding to improve instruction density.
- **16-bit CPU**: Verilog implementation with distinct control/data paths; compiled for DE1-SoC FPGA board.
- **Mapper**: NP-complete graph problem solver (travelling salesman) using meta-heuristics and simulated annealing.

Relevant Courses

- **Software**: Algorithms & Data Structures (A+), Operating Systems (A+), Compilers (A+), Networks (A-), Security (A+).
- **Hardware**: Digital Systems (A+), Computer Organization (A+), Computer Architecture (A-), Digital Electronics (A+).
- **Engineering**: Machine Learning (A), Signals & Systems (A), Control Theory (A-).
- **Mathematics**: Linear Algebra (A+), Complex Analysis (A+), Multivariate Calculus (A), Probability (A).