

# MUNER AE PROJECT



## Steering Wheel Electronic Board Design

Project Report

### Group 3

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# Executive Summary

The project consists of designing an electronic board to be used as a steering wheel control interface. The board must satisfy the following requirements:

## 1. Button Inputs

The board must be able to read four electromechanical buttons: *UP*, *DW*, and two additional spare function buttons.

## 2. Communication Line Input

The board must read a communication (CAN) line from which two temperature values are received.

## 3. Analog Inputs

The board must read two analog input signals (Clutch Control and Rotary Switch) available directly on the board.

## 4. Display Output

The board must include a display capable of:

- showing messages when buttons are pressed,
- displaying the received temperatures,
- showing the value of the analog inputs.

## 5. LED Outputs

The board must include two LEDs, which can be driven via the CAN bus.

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# Chapter 1

## Project Management & Team Organization

### 1.1 Project Charter and Scope

#### 1.1.1 Purpose and Justification

The primary purpose of this project is to design, prototype, and validate a fully functional electronic control unit (ECU) for a steering wheel system. This project justifies the integration of embedded electronics into automotive human-machine interfaces, providing a robust platform for driver input acquisition and system feedback.

#### 1.1.2 Project Objectives

- **Functional Prototype:** Develop a working board meeting all electrical requirements.
- **Input Processing:** Accurately read 4 electromechanical buttons and 2 analog signals.
- **Communication:** Implement CAN bus reception for temperature data.
- **User Feedback:** Drive 2 LEDs and an OLED/TFT display for system status.
- **Documentation:** Deliver a complete package including schematics, PCB layout, BOM, and validation reports.

#### 1.1.3 Deliverables

In accordance with the project charter, the following key deliverables were defined:

- **D1:** System Architecture and Block Diagram.
- **D2:** Complete Electrical Schematics and PCB Layout (Gerber files).
- **D3:** Bill of Materials (BOM) with automotive-qualified components.
- **D4:** Assembled and Functional Hardware Prototype.

- D5: Firmware Source Code and Documentation.
- D6: Validation Test Report and User Manual.

#### 1.1.4 Constraints & Assumptions

##### Constraints:

- Mandatory use of automotive-qualified parts (AEC-Q100/200) where feasible.
- Strict prohibition on the use of active cooling (fans).
- Budget limitations requiring cost-effective component selection (e.g., protection circuitry).

##### Assumptions:

- Lab equipment (oscilloscopes, power supplies) is available and calibrated.
- The mechanical housing for the steering wheel is out of scope.

#### 1.1.5 Scope Definition

**In-Scope:** Hardware design (schematic/PCB), firmware development for STM32, GUI development for testing, and system validation. **Out-of-Scope:** Mechanical design of the wheel, mass production optimization, and advanced environmental vibration testing.

#### 1.1.6 Work Breakdown Structure (WBS)

To ensure manageable execution, the project scope was decomposed using a deliverable-based Work Breakdown Structure (WBS), organizing the effort into distinct work packages:

- **WP1 - Hardware Design:** Component selection, Schematics, PCB Layout.
- **WP2 - Firmware Development:** Low-level drivers, Application logic, HMI/Display logic.
- **WP3 - Assembly & Manufacturing:** Procurement, PCB fabrication (Out-sourced), HMI assembly (In-house).
- **WP4 - Validation:** Unit testing, Integration testing, Final system validation.

## 1.2 Role Assignment

To ensure an efficient workflow and clear accountability, the project tasks were distributed among the team members as detailed in Table 1.1.

Table 1.1: Team Role Assignment

Member	Primary Role	Secondary Responsibility
Prince Gadilingareddy	Project Management	Documentation and Reporting
Kartik	Hardware Design	PCB Layout
Bashnona	Firmware	Testing and Validation
	GUI Development	Testing

Table 1.1 presents the distribution of primary and secondary roles within the team. Each assignment reflects the members' strengths and areas of interest while ensuring that all key tasks have a designated lead. Prince oversees Project Management and supports Documentation to maintain clear communication and structured progress. Gadilingareddy leads Hardware Design and PCB Layout due to his experience with circuit development. Kartik is responsible for Firmware development and assists with Testing and Validation, ensuring proper hardware-software integration. Bashnona focuses on GUI Development to enhance system usability and contributes to Testing activities.

These assignments are intended to provide clarity and accountability, not to restrict contributions. All members are capable of working across different domains, and collaboration is encouraged. Team members routinely support one another—especially when someone has additional bandwidth—ensuring steady progress and balanced workload throughout the project.

## 1.3 Development Methodology

### 1.3.1 The V-Model Approach

The project followed the V-Model software development lifecycle, which emphasizes a verification and validation phase for each corresponding development stage. This structured approach ensured that requirements were clearly defined before implementation and that every design choice was rigorously tested against its initial specification.

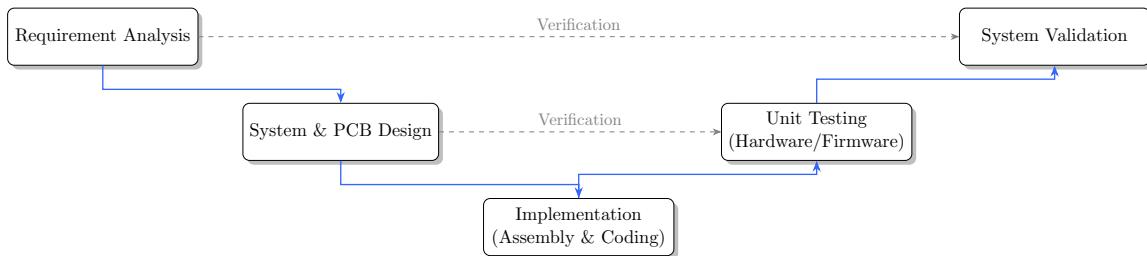


Figure 1.1: V-Model Development Lifecycle applied to the Steering Wheel Module

The left side of the "V" represents the design phase, moving from customer requirements to schematics and PCB layout. The bottom represents the realization phase (PCB fabrication and code writing). The right side represents the testing phase, where individual subsystems (e.g., power supply, CAN bus) are tested before final system validation.

### 1.3.2 Collaboration and Tracking with Jira

To manage the project workflow efficiently, the team utilized **Jira** as the primary collaboration and tracking tool. Jira facilitated an Agile-inspired approach, allowing the team to:

- **Track Progress:** The project was broken down into manageable tasks (e.g., "Design 3.3V Regulator", "Chip selection").
- **Assign Responsibility:** Every task was assigned to a specific member with a deadline, ensuring accountability.
- **Monitor Status:** The Kanban board provided a visual overview of tasks in "To Do", "In Progress", and "Done" states, helping the Project Manager identify bottlenecks early.

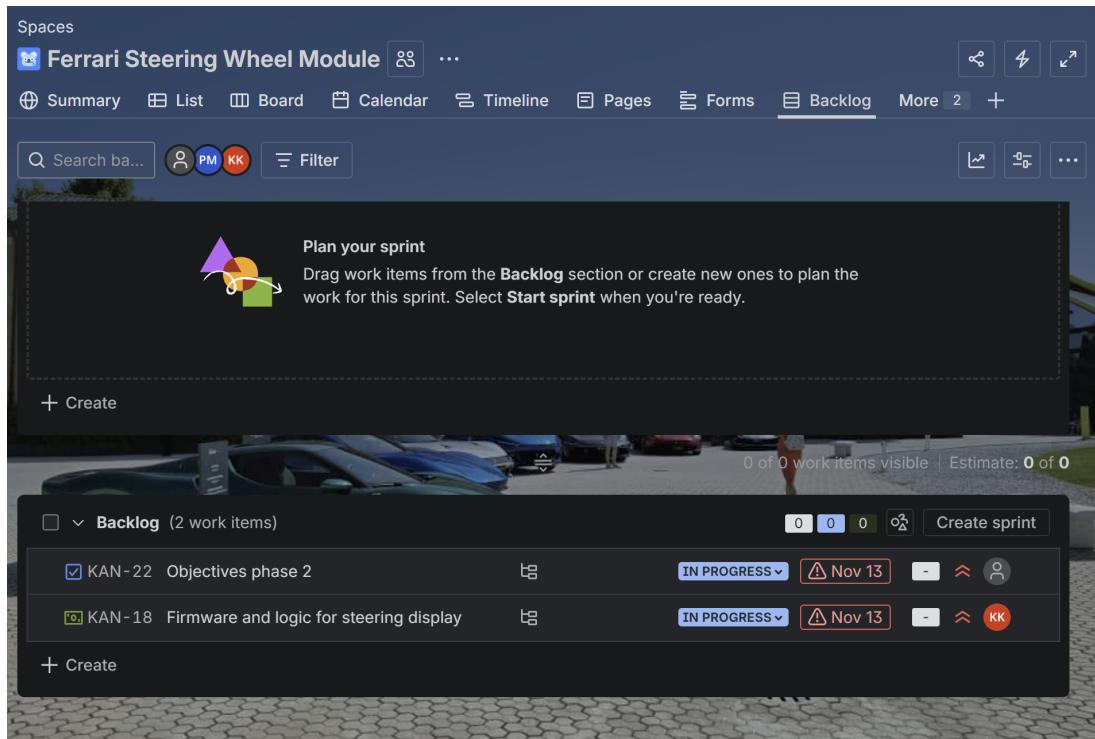


Figure 1.2: Jira Backlog View: Organizing objectives and tasks for Sprint Planning

Figure 1.2 illustrates the **Backlog view**, where high-level objectives (like "Objectives Phase 2") were broken down into actionable items. This allowed the team to prioritize critical features for each sprint cycle.

The screenshot shows the Jira Active Task List for the 'Ferrari Steering Wheel Module' project. The interface includes a header with project navigation, search, and filter options. Below is a table of tasks:

	Work	Assignee	Reporter
<input type="checkbox"/>	KAN-28 GUI	Bashnona Nawar (BN)	Bashnona Nawar (BN)
<input type="checkbox"/>	✓ KAN-22 Objectives phase 2	Unassigned	PRINCE MATHEW (PM)
<input type="checkbox"/>	✓ KAN-25 Software + GUI	Kartik Purushottam K. (KK)	PRINCE MATHEW (PM)
<input type="checkbox"/>	✓ KAN-24 Final presentation + report structure	PRINCE MATHEW (PM)	PRINCE MATHEW (PM)
<input type="checkbox"/>	✓ KAN-23 Schematics + BOM finalize	Gadilingareddy Goud... (GM)	PRINCE MATHEW (PM)
<input type="checkbox"/>	✓ KAN-10 Firmware and logic for steering display	Kartik Purushottam K. (KK)	Kartik Purushottam K. (KK)

At the bottom, there are buttons for '+ Create' and a status indicator '15 of 15'.

Figure 1.3: Jira Active Task List showing assignments and workflow status

As shown in Figure 1.3, the **Active Task List** provided granular visibility into the project's daily operations. Tasks were explicitly assigned to team members (e.g., "Software + GUI" to Kartik, "Schematics" to Gadilingareddy), ensuring that ownership was clear and no work packages were orphaned.

### 1.3.3 Status Reporting

Consistent communication was maintained through weekly status meetings held every Friday. These meetings followed a structured format to ensure alignment:

- **Main Achievements (Done):** Review of deliverables completed during the week.
- **Next Steps (To Do):** Planning tasks for the upcoming period.
- **Risks & Alerts:** Identification of potential blockers (e.g., shipment delays, technical hurdles) and mitigation strategies.



Figure 1.4: Jira Project Dashboard providing a real-time status overview

The **Project Dashboard** (Figure 1.4) served as the central point of truth for status reporting. It provided real-time metrics on completed vs. in-progress work items, allowing the Project Manager to visualize the team's velocity and adjust timelines proactively.

## 1.4 Planning and Timeline

### 1.4.1 Automated Timeline Tracking

To ensure the project schedule remained synchronized with daily task execution, the team utilized the **WBS Gantt-Chart** application for Jira. Unlike static timeline tools, this plugin integrated directly with our Jira issues, automatically updating the Gantt view as team members moved tasks from "To Do" to "Done".

This data-driven approach allowed us to:

- **Link Dependencies:** Visualized predecessor/successor relationships directly within the project management environment.
- **Export Real-Time Data:** As shown in Figure 1.5, the raw scheduling data—including start dates, durations, and milestones—was exported as an XML file (via the MS Project Export function). This raw data served as the foundation for the finalized Gantt chart presented in Figure 1.6, ensuring that the report accurately reflects the actual project history.

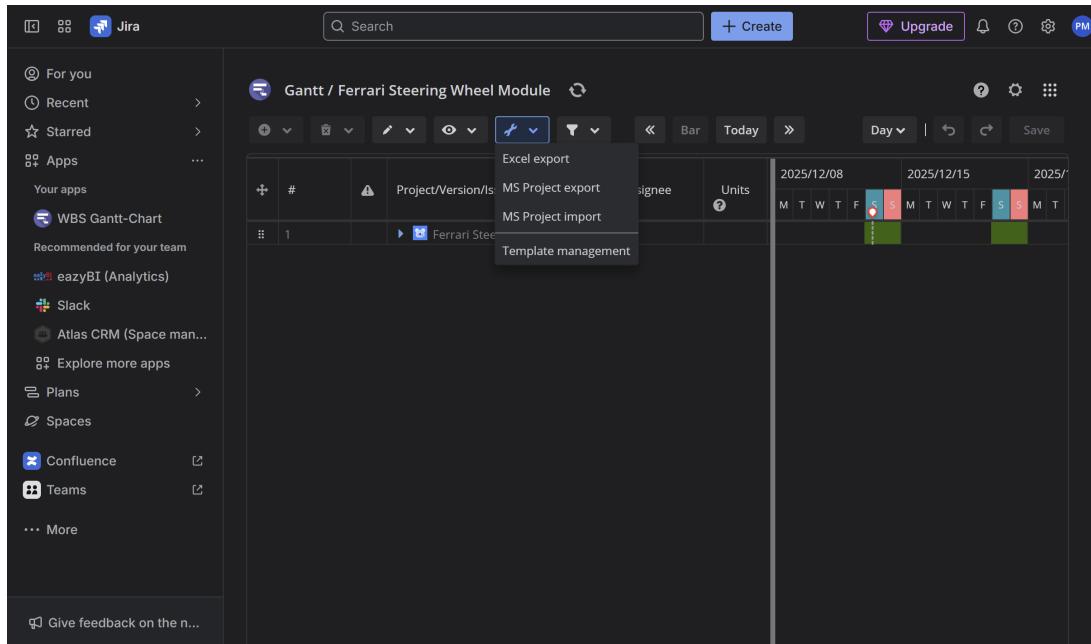


Figure 1.5: WBS Gantt-Chart interface in Jira used for automated timeline tracking and XML export.

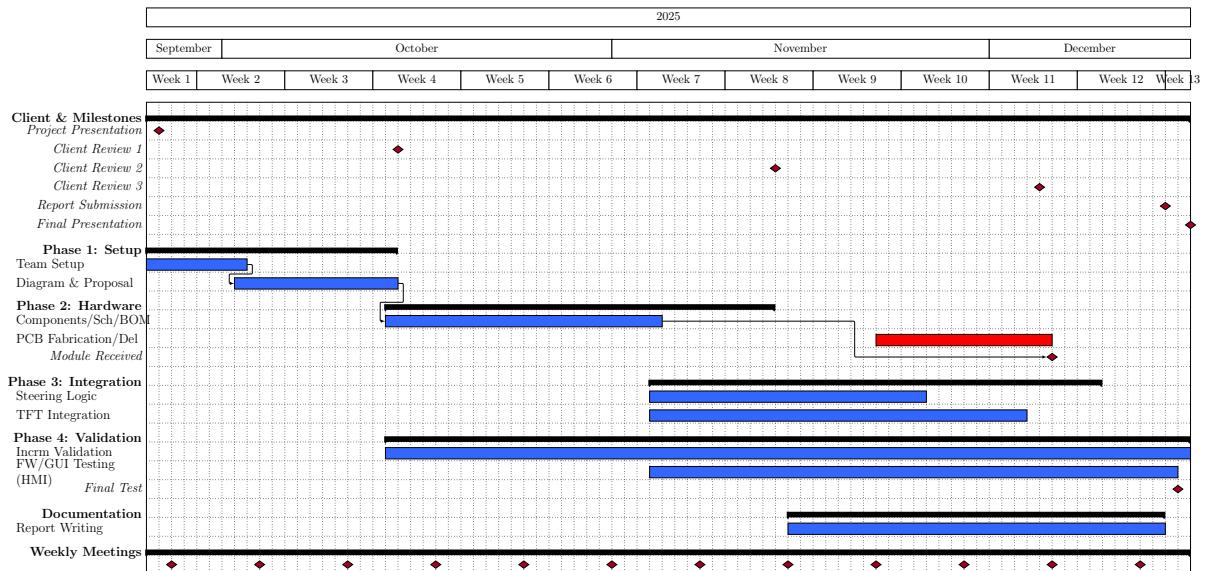


Figure 1.6: Project Gantt Chart including Client Milestones

## 1.5 Budget Management and Manufacturing Strategy

To optimize both the immediate project budget and the long-term utility of the hardware, the team adopted a strategic **Split-Module Architecture**. This decision was driven not only by cost constraints but by the need to create a versatile development platform for future iterations.

### 1.5.1 Strategic Modular Design for Future Development

The separation of the system into two distinct physical boards—the *Main Control Module* and the *HMI Interface Module*—provides a critical advantage: **decoupling the core logic from the peripheral interface.**

- **Seamless Future Upgrades:** By isolating the user interface components (buttons, rotary switches, display) on a low-cost, easy-to-manufacture HMI board, future development teams can completely redesign the steering wheel’s layout or ergonomics without scrapping the expensive core electronics.
- **Universal Control Platform:** The Main Control Board effectively serves as a universal development kit. It exposes all MCU peripherals (SPI, I2C, UART, CAN, ADC) through standardized connectors. This allows it to drive entirely different projects—such as a dashboard cluster or a central console controller—simply by swapping the HMI module attached to it.
- **Risk Reduction:** This modularity ensured that if the mechanical housing of the steering wheel changed late in the design phase (a common occurrence in automotive prototyping), only the inexpensive HMI board would need resizing, protecting the investment made in the complex multi-layer control board.

### 1.5.2 Manufacturing Approach

#### Module 1: Main Control Board (Hybrid Manufacturing)

The primary module houses the high-frequency and precision components, including the **STM32 microcontroller**, **CAN transceiver**, and switching regulators. To guarantee signal integrity and soldering reliability for these sensitive SMD parts, PCB fabrication and assembly were outsourced to **JLCPCB**. However, to balance the budget, through-hole components (connectors, large capacitors) were manually assembled in the university laboratory under the supervision of **Professor Moreno**.

#### Module 2: HMI Interface (In-House)

The secondary module, containing the electromechanical inputs and display interface, was designed for complete in-house fabrication. This allowed the team to rapidly prototype different button placements and solder mechanical switches manually, providing valuable hands-on experience while eliminating external assembly costs for these rugged components.

### 1.5.3 Planning and Timeline Alignment

The project timeline (Figure 1.6) was structured to accommodate this split manufacturing flow. The critical path was defined by the procurement cycle of the Main Control Module. A buffer was allocated for its fabrication and shipping from JLCPCB. Crucially, when a re-ordering event occurred due to a DFM flag, the modular strategy paid off: the team continued firmware development using the in-house HMI module and a Nucleo board, ensuring software progress was not blocked by the hardware delay. The final integration phase commenced immediately upon receipt of the main module on **December 5th, 2025**.

### 1.5.4 Protection Circuitry and Cost Optimization

Initially, to ensure strict compliance with automotive electrical transient standards (such as ISO 7637-2 and ISO 16750-2), the design team selected the *LTC4380 Surge Stopper IC*. This component provides superior overvoltage protection by clamping the output voltage and disconnecting the load during extended surge events.

However, after completing the initial schematics, simulations, and Bill of Materials (BOM) cost estimation, it was determined that the inclusion of the LTC4380 would exceed the assigned budget for the prototype. Consequently, a cost-benefit analysis was conducted, leading to the decision to implement a more traditional, cost-effective protection scheme using a **Schottky diode** for reverse polarity protection and a **TVS (Transient Voltage Suppression) diode** for transient clamping. This alternative solution provides adequate protection for the target testing environment while keeping the project within its financial constraints.

### 1.5.5 Procurement and Interim Validation Strategy

The procurement process for the Main Control Module experienced unforeseen delays. The initial order for the PCB fabrication and assembly was placed with JLCPCB on **November 22, 2025**. However, due to technical errors flagged during the manufacturer's Design for Manufacturing (DFM) review, the order had to be cancelled and re-submitted on **November 24, 2025**. Although initially anticipated to arrive on **December 09, 2025**, the corrected main module was successfully received on **December 05, 2025**.

To mitigate the impact of the interim delay on the development timeline, the team implemented a parallel validation strategy. Firmware development and GUI testing proceeded using:

1. The in-house developed **HMI Interface Module** for input verification.
2. A borrowed **STM32 Nucleo development board** to simulate the core logic and drive the display output.

This approach allowed software development to continue in parallel with the hardware manufacturing, ensuring that the firmware will be ready for immediate integration once the main module arrives.

## 1.6 Risk and Issue Management

Managing this project required a proactive approach to identifying risks and resolving issues as they arose. Jira played a pivotal role here, allowing us to log, prioritize, and assign mitigation tasks for every identified risk.

### 1.6.1 Risk Management Strategy

Using a formal risk register maintained within Jira, the team identified potential threats to the project timeline and technical success. Risks were categorized (High/Medium/Low) and mitigation plans were put in place.

Table 1.2: Key Project Risks and Mitigation Strategies

Risk	Impact Level	Mitigation Strategy
Shipment Delay from JLCPCB	High	Implemented interim validation using Nucleo board and HMI module.
Scope Creep (Rotary Switch)	Medium	Parallel development: Firmware team worked on drivers while HW team updated PCB.
Budget Overrun (LTC4380)	High	Cost-Benefit Analysis conducted; switched to Schottky/TVS diode solution.

### 1.6.2 Issue Resolution: Manufacturing Delays

The project faced a critical delay when the initial order for the Main Control Module (placed on November 22, 2025) was flagged for technical errors during the manufacturer's DFM review. This necessitated a cancellation and re-order on November 24, pushing the expected arrival date to December 9. To prevent this hardware delay from stalling the entire project, we adopted an **interim testing strategy**. By utilizing the in-house HMI module and borrowing an STM32 Nucleo board, the software team could continue validating the GUI and control logic, ensuring that the firmware was mature and ready for immediate deployment once the final hardware arrived.

### 1.6.3 Issue Resolution: Boot Mode Failure

Upon receiving and assembling the Main Control Module, the team encountered a critical functional failure: the board would not enter boot mode, preventing firmware flashing. Initial internal reviews of the schematics and PCB layout did not reveal the root cause. To resolve this, the team engaged with the STMicroelectronics technical community. Through collaborative troubleshooting, it was discovered that the root cause lay in a last-minute component substitution. The original reset switch specified in the design was unavailable from the vendor, and the alternative part selected had a different internal pin configuration that held the MCU in a perpetual reset state. To mitigate this immediately without waiting for a new PCB revision, the incompatible switch was desoldered, and a jumper wire was installed to manually trigger the reset function, successfully restoring boot mode access.

# Chapter 2

## System Architecture

### 2.1 Block Diagram

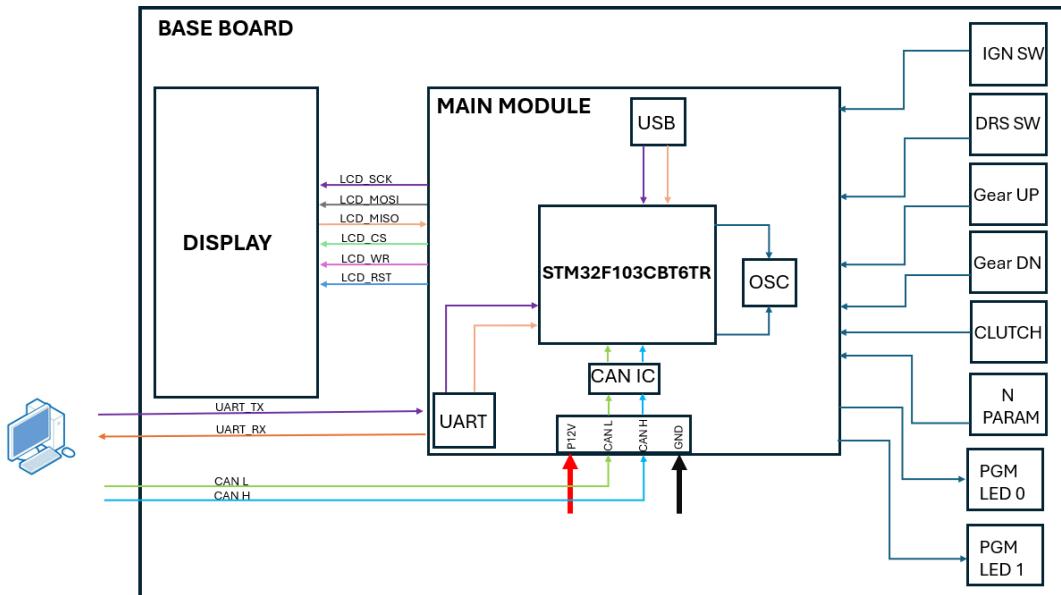


Figure 2.1: Steering Wheel Electronic System Architecture

The system architecture shown in Figure 2.1 is based on a centralized control approach and can be summarized as follows:

- **Central Processing Unit:** The STM32F103CBT6TR microcontroller acts as the core of the system, managing all input acquisition, output control, and communication tasks.
- **Human–Machine Interface:** A TFT display is directly interfaced with the microcontroller via dedicated SPI lines, providing real-time visual feedback to the driver. Programmable LEDs are used for status indication.
- **Driver Inputs:** Multiple switches (IGN, DRS, Gear Up, Gear Down, Clutch) and a parameter selection input are connected to the main module to capture driver commands.

- **Vehicle Communication:** A CAN transceiver interfaces the microcontroller with the vehicle CAN bus, enabling reliable differential communication over CANH and CANL lines.
- **Debug and Configuration Interface:** A UART interface is provided for external PC communication, supporting firmware debugging and system diagnostics.
- **Timing and Power Interfaces:** An external oscillator ensures stable clock generation for the microcontroller, while the system is powered from a 12 V supply with a common ground reference.

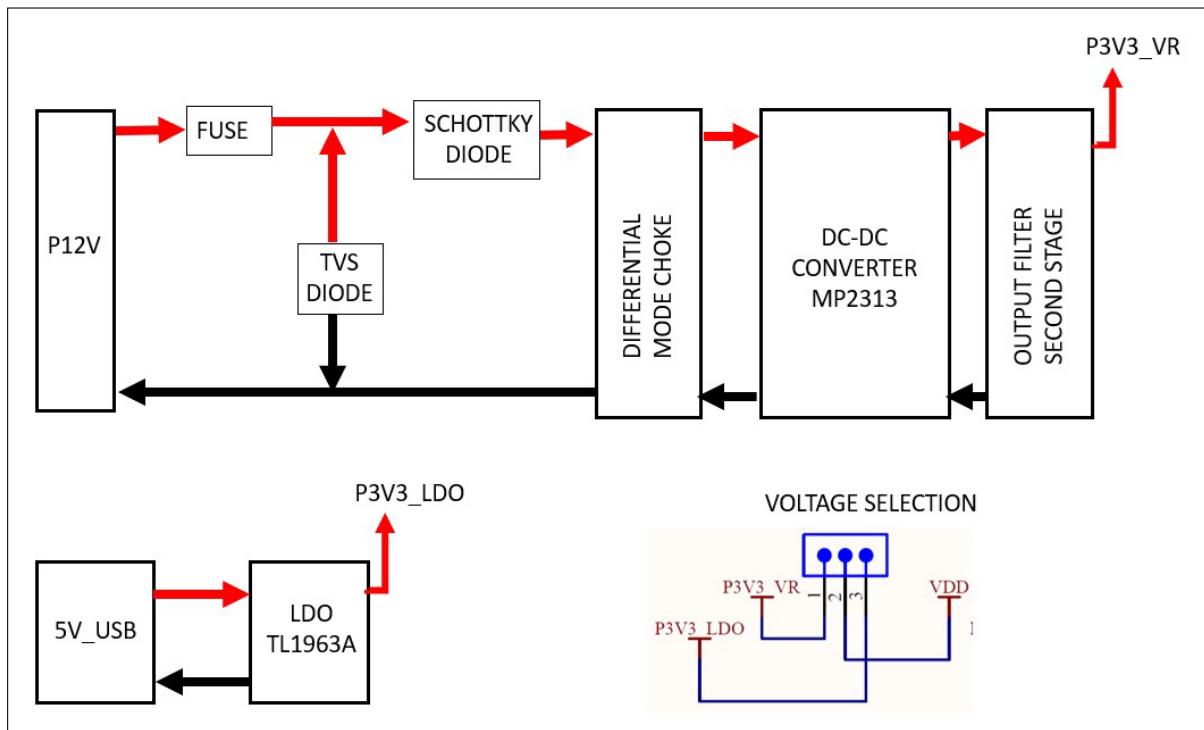


Figure 2.2: Power Supply Architecture: Input Protection, DC-DC Conversion, and Voltage Selection

The power supply architecture, illustrated in Figure 2.2, is designed to ensure robust operation in an automotive environment. The primary 12 V input line is protected against overcurrent, voltage transients, and reverse polarity using a fuse, a TVS diode, and a Schottky diode, respectively. A differential mode choke is employed to suppress electromagnetic interference (EMI) before the voltage is stepped down by the MP2313 DC-DC converter.

Additionally, the board features a secondary power input via 5 V USB for debugging and bench testing, which is regulated by a TL1963A Low Dropout (LDO) regulator. A jumper selection circuit allows the user to switch the board's internal 3.3 V logic supply rail between the high-efficiency switching regulator (P3V3\_VR) and the low-noise linear regulator (P3V3\_LDO) depending on the operating mode.

## 2.2 Component Selection

The selection of key electronic components was driven by the specific requirements of the automotive environment, including robust power management, reliable communication, and cost optimization.

### 2.2.1 Microcontroller: STM32F103CBT6TR

- **Choice:** The STM32F103CBT6TR, based on the ARM Cortex-M3 core, was selected as the central processing unit.
- **Justification:** This MCU offers a balanced combination of performance and peripheral integration. Its 72 MHz clock speed is sufficient for managing the display updates and CAN communication in real-time. The wide availability of development tools (STM32CubeIDE) and community support accelerated firmware development.
- **Cost Optimization:** It provides an excellent price-to-performance ratio compared to higher-end M4 or M7 cores, which would be overkill for this application.

### 2.2.2 External Oscillator (HSE)

To ensure precise timing for the CAN bus communication and stable system operation across the full temperature range, the design implements a robust clocking architecture.

- **Choice:** An 8 MHz fundamental mode crystal.
- **Dual-Oscillator Strategy:** The system utilizes the External Oscillator (HSE) in conjunction with the microcontroller's Internal RC Oscillator (HSI). While the HSI handles system startup and low-power GPIO management, the HSE provides the high-precision reference required to drive the Phase Locked Loop (PLL). This PLL output manages the synchronization of all critical GPIOs and ensures the CAN bus bit-timing remains within the strict tolerances ( $\pm 30$  ppm) required for vehicle communication.
- **Measured Characteristics:** As verified during prototype characterization (see Figure 6.6 in Chapter 6), the selected crystal configuration yields stable performance:
  - **Frequency:**  $\approx 8.06$  MHz (Stable sinusoidal).
  - **Amplitude:**  $V_{pp} \approx 640$  mV.
  - **DC Offset:**  $\approx 2.0$  V.
- **Load Capacitor Calculation:** Correct selection of the external load capacitors ( $C_{L1}, C_{L2}$ ) is critical for reliable oscillator startup. Based on the crystal datasheet and STM32 application notes, the required external capacitance is calculated using the formula:

$$C_{LOAD\_EXT} = 2(C_L - C_S)$$

Where:

- $C_L$ : Rated load capacitance of the crystal (18 pF).

- $C_S$ : Estimated stray capacitance of PCB pads and MCU pins (typically 2 pF to 7 pF, estimated at 3 pF for this layout).

Substituting the values:

$$C_{LOAD\_EXT} = 2 \times (18 \text{ pF} - 3 \text{ pF}) = 2 \times 15 \text{ pF} = 30 \text{ pF}$$

To match this requirement with standard component values, two 30 pF COG/NPO ceramic capacitors were selected for  $C11$  and  $C12$ .

### 2.2.3 CAN Transceiver: SN65HVD232QDRQ1

- **Choice:** The SN65HVD232QDRQ1 from Texas Instruments was chosen for vehicle communication.
- **Justification:** This transceiver is explicitly designed for 3.3V logic systems, eliminating the need for level shifters when interfacing with the STM32. It features high ESD protection and robust fault tolerance, essential for the noisy electrical environment of a vehicle.
- **Cost Optimization:** By integrating the necessary protection and logic level compatibility, it reduces the overall component count and PCB footprint.

### 2.2.4 Display: MI0283QT-9A (TFT Color LCD)

- **Choice:** The MI0283QT-9A TFT display.
- **Justification:** This specific display module was provided directly by the client (Ferrari). It features a 320x240 resolution, which exceeds the minimum requirement of 128x64 pixels, allowing for a richer and more informative user interface. Its integrated controller simplifies the driving logic via the SPI interface.
- **Project Impact:** Using the client-provided display ensured seamless integration with their existing mechanical housing and visual standards, while eliminating the cost and lead time associated with sourcing a new display unit.

### 2.2.5 DC-DC Buck Converter: MP2313GJ-P

- **Choice:** The MP2313GJ-P High-Efficiency Switching Regulator.
- **Justification:** To strictly adhere to the thermal constraints (no active cooling), efficiency was the primary selection criterion. The MP2313 offers > 90% efficiency when stepping down 12 V to 3.3 V, significantly reducing waste heat compared to linear alternatives.
- **Design Benefit:** Its high switching frequency (2 MHz) allowed for the use of a physically smaller inductor ( $8.2\mu\text{H}$ ) and smaller output capacitors, optimizing the PCB footprint.

## 2.2.6 Low Dropout Regulator (LDO): TL1963A

- **Choice:** The TL1963A-33DCYR Linear Regulator.
- **Justification:** This component was selected to provide a "quiet" power rail alternative. Unlike the switching regulator, the LDO introduces negligible noise, making it ideal for powering the analog sensor circuitry during precision calibration.
- **Versatility:** It features a low dropout voltage of 340 mV, which is critical when powering the board from the 5 V USB debugging interface, ensuring a stable 3.3 V output even when the input voltage sags.

## 2.2.7 Input and Output Filtering

To ensure electromagnetic compatibility (EMC) and provide a clean power rail for sensitive analog components, dedicated filtering stages were implemented at both the input and output of the switching regulator.

- **Input Differential Mode Choke:**

- **Purpose:** A differential mode choke was placed in series with the 12V input to attenuate the conducted noise generated by the high-frequency switching of the MP2313 regulator ( $f_{sw} = 2 \text{ MHz}$ ), preventing it from coupling back onto the vehicle's power bus.
- **Selection:** The Murata **DLW5BTM102SQ2** was selected for its high impedance at the switching frequency ( $> 1 \text{ k}\Omega$  at 2 MHz), providing over 60 dB of attenuation. Its rated current of 1.5 A is sufficient for the application, and its low DC resistance ( $0.06 \Omega$ ) ensures negligible voltage drop.

- **Secondary Output Filter (Pi-Filter):**

- **Purpose:** To further suppress voltage ripple on the 3.3 V output rail, particularly for noise-sensitive analog loads like the clutch potentiometer, a secondary L-C pi-filter was implemented.
- **Design:** The filter consists of a  $1 \mu\text{H}$  inductor ( $L3$ ) and two  $10 \mu\text{F}$  ceramic capacitors ( $C13, C14$ ), resulting in a total capacitance  $C_{sec} = 20 \mu\text{F}$ . The corner frequency ( $f_c$ ) was designed to be well below the switching frequency:

$$f_c = \frac{1}{2\pi\sqrt{L_{sec} \cdot C_{sec}}} = \frac{1}{2\pi\sqrt{1 \times 10^{-6} \text{ H} \cdot 20 \times 10^{-6} \text{ F}}} \approx 35.6 \text{ kHz}$$

- **Result:** With a corner frequency of 35.6 kHz, this filter provides approximately 40 dB of additional attenuation at the 2 MHz switching frequency. The slight trade-off in transient response is acceptable for the relatively static loads connected to this rail.

## 2.3 Architectural Challenges

The definition of the system architecture was driven by the strict intersection of automotive reliability standards, budgetary limits, and manufacturing constraints. The following key challenges required specific architectural trade-offs:

### 2.3.1 Passive Thermal Management Strategy

A primary constraint of the project was the strict prohibition of active cooling mechanisms (fans). This presented a significant architectural challenge, particularly for the linear regulation stage (LDO), where the voltage drop generates substantial waste heat. To ensure the system operates reliably up to 85°C, the PCB layout incorporated specific passive cooling techniques:

- **Thermal Vias Arrays:** Special attention was given to the **TL1963A LDO**. A dense array of thermal vias was placed directly beneath the component's thermal pad. These vias function as vertical thermal conduits, efficiently transferring heat from the component side to the internal and bottom layers.
- **Dedicated Ground Plane Dissipation:** The thermal vias connect the top-layer components to a solid, uninterrupted ground plane on the bottom layer. This extensive copper area acts as a heat spreader, maximizing the surface area available for natural convection and radiation, effectively compensating for the lack of forced airflow.
- **Efficiency Optimization:** To further reduce the thermal load, the architecture prioritizes the high-efficiency MP2313 switching regulator (> 90% efficiency) for the main power rail, reserving the LDO only for noise-sensitive peripherals to minimize total heat generation.

### 2.3.2 Automotive Compliance vs. Budgetary Constraints

Balancing the rigor of automotive transient protection (ISO 7637-2) with the project's Bill of Materials (BOM) budget forced a critical architectural pivot.

- **Initial Design:** The ideal architecture utilized the *LTC4380 Surge Stopper* IC to actively clamp high-voltage transients.
- **Optimized Solution:** Cost analysis revealed this component exceeded the budget allocation. The architecture was revised to implement a discrete protection scheme using a *TVS diode and Schottky diode* combination. This required careful simulation to ensure the discrete components could clamp sufficient energy without failing, maintaining compliance at a fraction of the cost.

### 2.3.3 Manufacturing and Supply Chain Resilience

To mitigate the risks associated with component sourcing and manufacturing lead times, the architecture was segmented into a **Split-Module Design**:

- **Main Control Module:** Designed for outsourced, automated assembly (JLCPCB) to ensure the precise soldering required for the STM32 MCU and surface-mount components.
- **HMI Interface Module:** Designed for in-house assembly, allowing the team to manually solder large electromechanical components (buttons, switches) and adapt to mechanical housing changes without redesigning the core logic board.

This modular approach proved critical when component unavailability (specifically the reset switch) forced last-minute substitutions, allowing the team to adapt the in-house hardware without scrapping the expensive main control board.

# Chapter 3

## Hardware Design

### 3.1 Schematics

The electronic design of the steering wheel module is built around the **STM32F103CBT6TR** microcontroller. The system schematics are segmented into three distinct functional sheets to ensure clarity and modularity: the Microcontroller and Input stage, the Communication interfaces, and the Power Supply regulation.

#### 3.1.1 Microcontroller and Input Stage

Figure 3.1 details the core logic. The MCU is clocked by an external crystal oscillator and supported by a bank of decoupling capacitors ( $C_{14} - C_{20}$ ) to filter high-frequency noise on the VDD rail. The board features a specific connector (J6) to interface with external electromechanical inputs, including the Gear Up/Down paddles, the Clutch command, and the Rotary Switches. LED indicators ( $D_1, D_2$ ) provide immediate visual feedback for power status and programmable alerts.

#### 3.1.2 Communication and Display Interfaces

Figure 3.2 illustrates the connectivity peripherals.

- **CAN Bus:** Reliability in vehicle communication is achieved using the **SN65HVD232** transceiver. The lines are protected against electrostatic discharge (ESD) using an **SM712** protection diode array and terminated with a  $120\Omega$  resistor ( $R_{13}$ ).
- **Display Control:** The OLED/TFT display is connected via J4. To strictly manage power consumption, a P-Channel MOSFET ( $Q_1$ , SI1013R) allows the firmware to completely cut power to the display when not in use.
- **USB:** A Micro-USB connector allows for bench testing and debugging, protected by dedicated ESD suppression components.

#### 3.1.3 Power Supply Architecture

Figure 3.3 depicts the power management stage, which is designed to handle the harsh automotive environment.

1. **Protection:** The 12V input is guarded by a fuse (*F1*), a TVS diode (*D6*, SMBJ17CA) for transient suppression, and a Schottky diode (*D5*, CMS06) for reverse polarity protection.
2. **Regulation:** The board employs a dual-regulation strategy. Primary power is provided by an **MP2313** high-efficiency DC-DC buck converter. For low-noise or USB-powered operation, a **TL1963A** LDO linear regulator is utilized.
3. **Voltage Selection:** A jumper block (*J9*) allows the selection between the switching regulator and the LDO output to drive the 3.3V logic rail. With this design, the board can be powered either through the standard 12V automotive supply or via the 5V USB connection, providing flexibility during development and field testing.

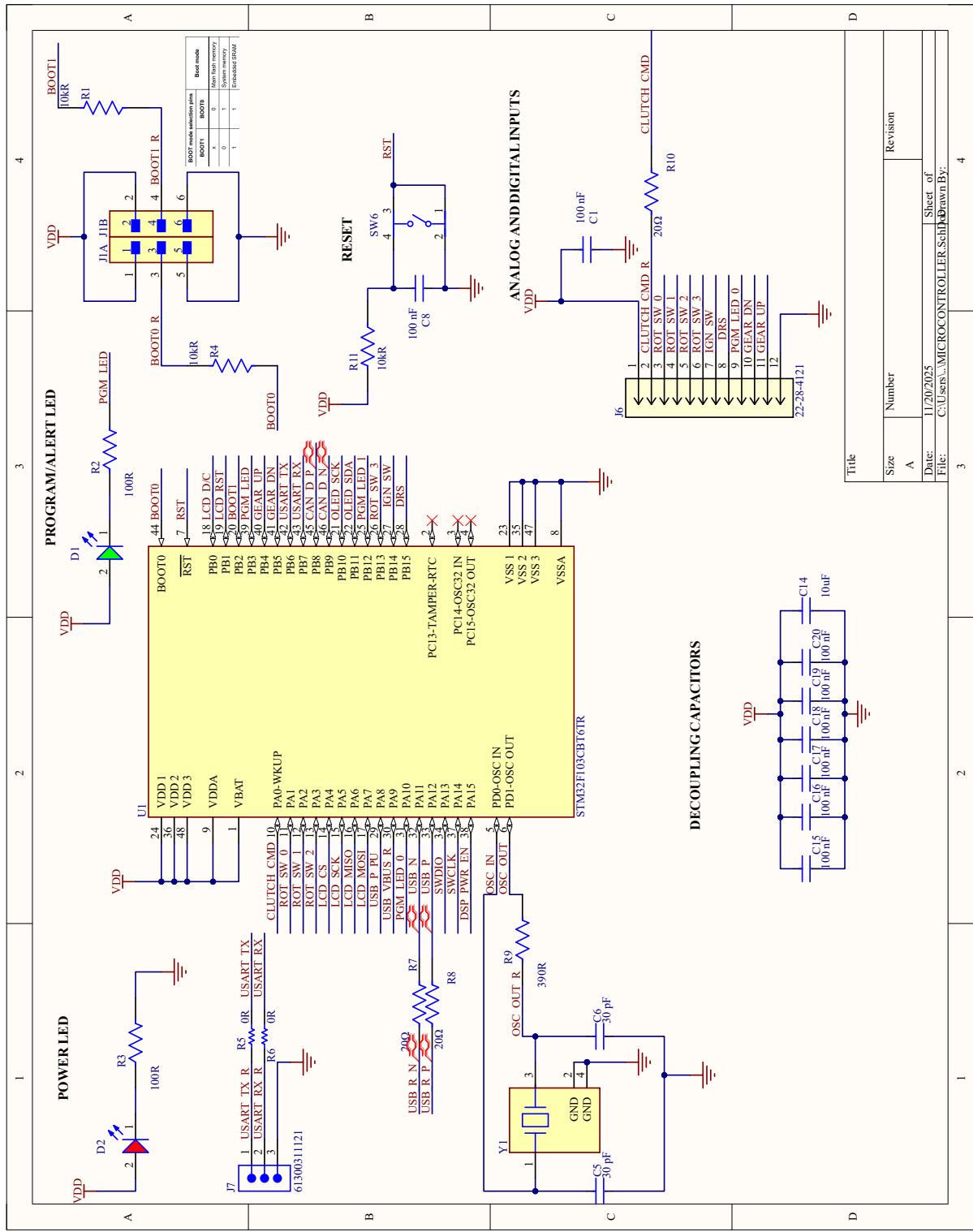


Figure 3.1: Schematic: STM32F103 Microcontroller and Inputs

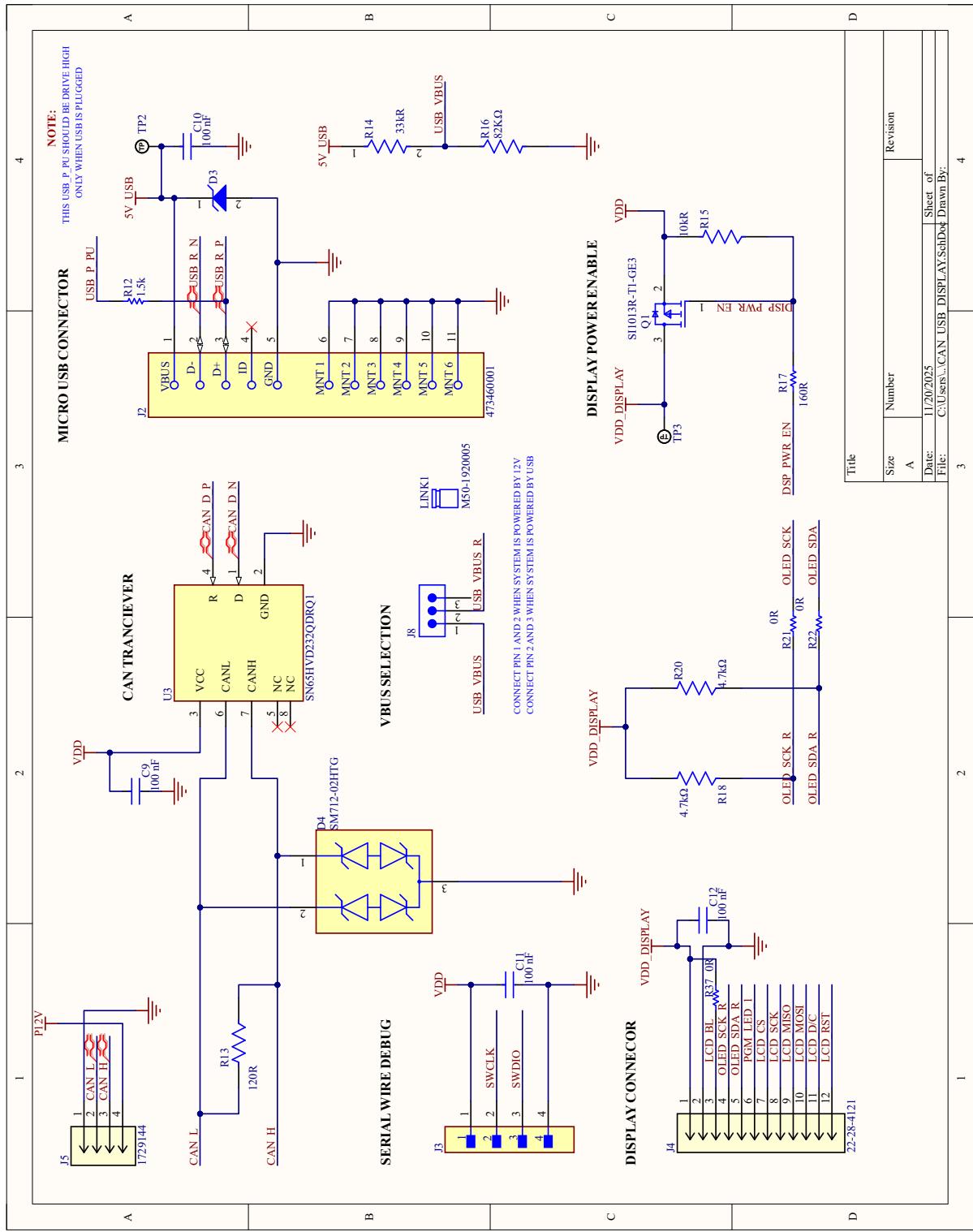


Figure 3.2: Schematic: CAN Transceiver, USB Interface, and Display Connectors

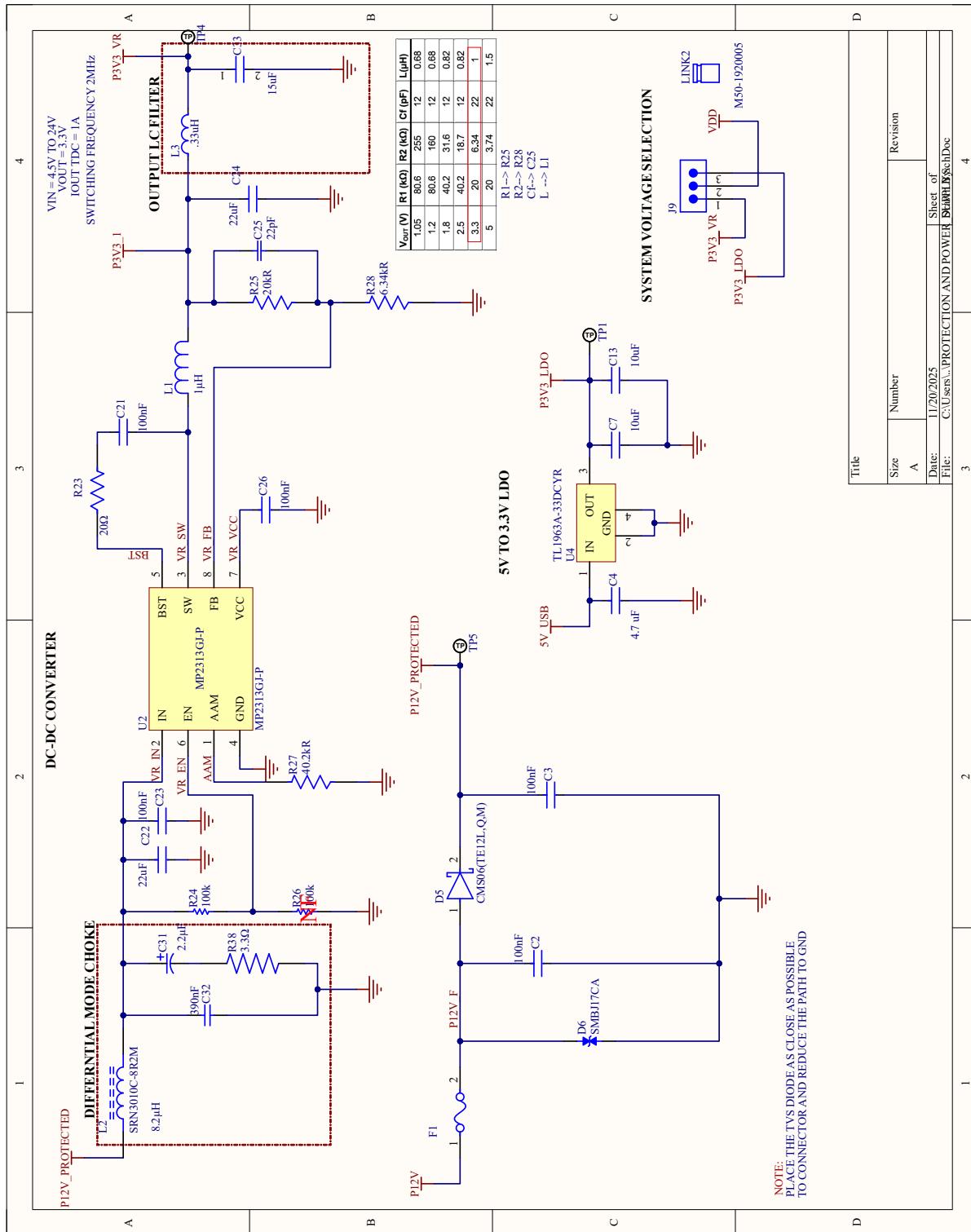


Figure 3.3: Schematic: Power Supply, Protection, and Regulation Stages

## 3.2 PCB Layout

The PCB design was executed to minimize electromagnetic interference (EMI) and ensure signal integrity for the high-speed CAN and SPI lines.

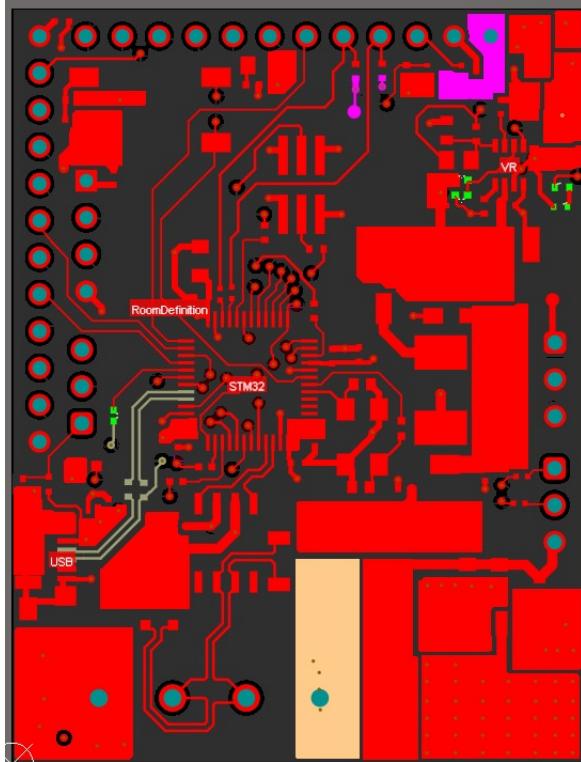


Figure 3.4: PCB Top Layer (Signal + Components)

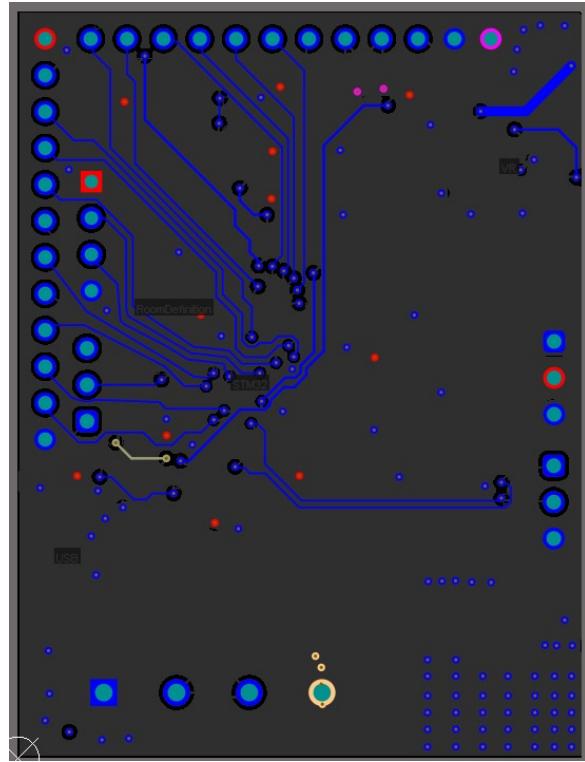


Figure 3.5: PCB Bottom Layer (Ground Plane)

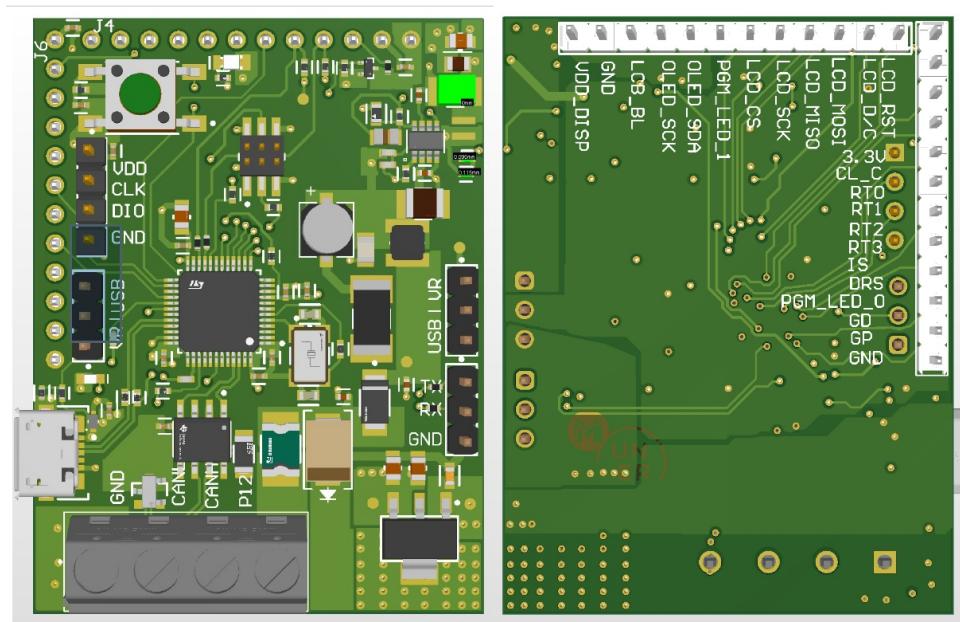


Figure 3.6: 3D Rendering of the Assembled Module

### 3.2.1 Layer Stackup Strategy

To meet the stringent automotive EMC requirements, a **4-layer stackup** was utilized. This configuration provides superior noise immunity compared to a 2-layer board by providing dedicated reference planes.

- **Layer 1 (Top Signal):** Hosting the majority of SMD components and high-speed signal routing (SPI, CAN).
- **Layer 2 (Ground Plane):** A solid, uninterrupted Ground (GND) plane sits immediately below the top layer. This provides the shortest return path for currents, minimizing loop inductance and EMI radiation.
- **Layer 3 (Power Plane):** Dedicated to power distribution (12V, 5V, 3.3V). Segregating power from signals reduces coupling noise.
- **Layer 4 (Bottom Signal):** Used for non-critical routing and bridging traces.

This "Signal - Ground - Power - Signal" arrangement creates a tightly coupled capacitor between Layer 2 and Layer 3, adding high-frequency decoupling for the power distribution network.

### 3.2.2 Thermal Layout Implementation

Given the "no-fan" requirement, the PCB layout itself serves as the primary cooling mechanism. The thermal design focuses heavily on the two main heat-generating components identified in the power schematic: the **MP2313 DC-DC Converter (U2)** and the **TL1963A LDO (U4)**.

To ensure these components remain within their Safe Operating Area (SOA) up to an ambient temperature of 85 °C, the following layout techniques were applied:

#### 1. Ground Planes as Heat Spreaders

The PCB stack-up utilizes continuous internal Ground (GND) layers. A large copper pour was reserved on both the top and bottom layers surrounding the power regulation stage. This creates a high thermal mass that absorbs heat spikes and distributes the thermal energy laterally across the entire board surface, effectively lowering the junction temperature of the regulators.

#### 2. Thermal Via Stitching

The **TL1963A** and **MP2313** packages feature exposed thermal pads on their underside. We implemented a dense matrix of thermal vias (drill diameter  $\approx 0.3$  mm) directly beneath these pads. These vias function as vertical heat pipes, conducting thermal energy from the surface-mount component down to the internal ground planes and the bottom layer. This significantly reduces the thermal resistance ( $\theta_{JA}$ ) by utilizing the inner copper layers for dissipation.

#### 3. Component Placement

The power regulation circuitry is physically separated from sensitive analog signal paths (like the Clutch Input) to prevent thermal drift from affecting measurement accuracy. Furthermore, the regulators are positioned near the board edge (where the connector *J9* and Fuse *F1* are located) to maximize passive convective airflow.

### 3.3 Complete Bill of Materials

The following table lists all 54 unique components used in the design, including their designators, manufacturer part numbers, descriptions, and quantities.

Table 3.1: Complete Bill of Materials (54 Line Items)

Designator	Part Number	Description	Qty
C1, C8–C12, C15–C20	CC0402KRX7R7BB104	CAP CER 0.1UF 16V X7R 0402	12
C2, C3, C21, C23, C26	TMK105B7104KVHF	0.1 $\mu$ F $\pm 10\%$ 25V Condensatori ceramici X7R 0402	5
C4	CC0603KRX5R7BB475	CAP CER 4.7UF 16V X5R 0603	1
C5, C6	C0603C300F3HACAUTO	C0603 30 pF X8R 30ppm/ $^{\circ}$ C 1.00% 25 V	2
C7, C13, C14	EMK212BB7106KG-T	CAP CER 10UF 16V X7R 0805	3
C22, C24	TMK325B7226KMHP	CAP CER 22UF 25V X7R 1210	2
C25	0805YA220K4T2A	Cap Ceramic 22pF 16V C0G 10% 0805 T/R	1
C31	EEE-1HA2R2SR	Radial Can - SMD ALUM ELEC CAP 50V 2.2 $\mu$ F $\pm 20\%$	1
C32	C0805C394K5RACTU	CAP 390nF 50V $\pm 10\%$ 0805 (2012 Metric) 1.1mm	1
C33	C2012X5R1E156M125AC	MLCC 15 $\mu$ F $\pm 20\%$ 25V X5R SMD 0805	1
D1	150060VS75000	LED, Green, SMD, 0603, 30 mA, 2 V, 570 nm	1
D2	150080RS75000	LED Uni-Color Red 630nm 2-Pin Chip 0805	1
D3	ESD5Z5.0T1G	TVS Diode for ESD Protection, 2-Pin SOD-523	1
D4	SM712-02HTG	TVS DIODE 12V 31V SOT23-3	1
D5	CMS06(TE12L,Q,M)	DIODE SCHOTTKY 30V 2A MFLAT	1
D6	SMBJ17CA	DO-214AA SMB SMBJ 1 Zener Tvs Diode 18.9V	1
F1	MINISMDC110F/24-2	PTC RESET FUSE 24V 1.1A 1812	1
J1	FTSH-103-01-F-DV-TR	CONN HEADER SMD 6POS 1.27MM	1
J2	473460001	CONN RCPT USB2.0 MICRO B SMD R/A	1
J3	HTSW-104-07-G-S	CONN HEADER VERT 4POS 2.54MM	1
J4, J6	22-28-4121	KK 254 Breakaway Header, Vert, 12 Circuits	2
J5	1729144	Terminal Block; 13.5A; 250V; 5.08mm; 4 Pos	1
J7, J8, J9	61300311121	CONN HEADER VERT 3POS 2.54MM	3
L1	MDMK2020T1R0MMV	Inductor Power Shielded Wirewound 1uH 20%	1
L2	SRN3010C-8R2M	General Purpose Inductor, 8.2uH, 20%, Ferrite	1
L3	DFE201210U-R33M=P2	FIXED IND .33UH 3.4A 31MOHM	1
Q1	SI1013R-T1-GE3	MOSFET P-CH 20V 350MA SC75A	1
R1, R4, R11, R15	RC0402JR-0710KL	RES 10K OHM 5% 1/16W 0402	4
R2, R3	MCS0402MC1000FE000	RES SMD 1.2K OHM 1% 1/10W 0402	2

Continued on next page

**Table 3.1 – continued from previous page**

<b>Designator</b>	<b>Part Number</b>	<b>Description</b>	<b>Qty</b>
R5, R6, R21, R22, R37	ERJ2GE0R00X	Chip Resistor, 0 Ohm, 0.1W, 0402	5
R7, R8, R10, R23	RT0402FRE0720RL	RES SMD 20 OHM 1% 1/16W 0402	4
R9	CRCW0402390RFKED	RES Thick Film, 390Ω, 1%, 0402	1
R12	ERA2AEB152X	RES SMD 1.5K OHM 0.1% 0402	1
R13	RMCF1206FTR120	0.12Ω ±1% 0.25W 1206 Thick Film Resistor	1
R14	ERA-2AEB333X	RES SMD 33K OHM 0.1% 1/16W 0402	1
R16	CRGCQ0402F82K	CRGCQ0402 82KΩ 1% ±100ppm/°C 50V	1
R17	ERJ-2GEJ161X	Thick Film Resistors - SMD 0402 160ohms 5%	1
R18, R20	RC0402JR-074K7L	4.7 kOhms ±5% 0.063W 0402 Resistor	2
R24, R26	RC0402FR-07100KL	100 kOhms ±1% 0.063W 0402 Resistor	2
R25	AF0402JR-0720KL	Anti-Sulfur Resistor Auto Grade 20kΩ 5% 0402	1
R27	AF0402FR-0740K2L	Anti-Sulfur Resistor Auto Grade 40.2kΩ 1% 0402	1
R28	MCT06030C6341FP500	RES SMD 100 OHM 1% 1/8W 0603	1
R38	CRM2512-JW-3R3ELF	Res Thick Film 2512 3.3 Ohm 5% 2W	1
SW6	1977223-4	SWITCH TACTILE SPST-NO 0.05A 12V	1
U1	STM32F103CBT6TR	MCU 32BIT Cortex M3 Performance LINE	1
U2	MP2313GJ-P	Switching Regulators 1A, 24V, 2MHz Step-Down	1
U3	SN65HVD232QDRQ1	Can Bus Transceiver 3.3V SOIC	1
U4	TL1963A-33DCYR	LDO 1.5 A Fixed 3.3 V Output SOT-223	1
Y1	ABM3BAIG-8.000MHZ-1Z-T	CRYSTAL 8.0000MHZ 18PF SMD	1
-	SW-PB1-1BS-A-PK1-A	Pushbutton Switches PLASTIC	4
-	PT15NH06-103A2020	Trimmer Resistors - Through Hole 10Kohms	1
-	428527520916	Rotary Switches WS-ROTV IP67 16Pos Gold	1
-	CFR50J100R	Carbon Film Resistors - THT 100Ohm 1/2W	4
-	SFR2500001002JA500	Metal Film Resistors - THT 0.4W 10Kohms 5%	5

## 3.4 Hardware Design Challenges

The transition from architectural concepts to physical realization presented specific electrical and mechanical challenges, particularly regarding the power supply topology and signal integrity.

### 3.4.1 Thermal vs. Noise Trade-off in Power Regulation

A critical design challenge was managing the dual-regulation topology implemented to power the 3.3 V logic rail. As detailed in the schematics (Figure 3.3), the board features both a switching regulator (MP2313) and a linear regulator (TL1963A), selectable via jumper *J9*.

- **Thermal Dissipation (LDO Mode):** When powered by the automotive 12 V line, the linear regulator ( $U_4$ ) faces a substantial voltage drop of  $\approx 8.7$  V. Even at a moderate load of 100 mA, this results in nearly 1 W of heat dissipation. Without active cooling, this strictly limits the LDO's continuous usage to low-power states or 5 V USB operation.
- **EMI Suppression (Switcher Mode):** To enable high-current operation without overheating, the MP2313 buck converter ( $U_2$ ) is the primary source. However, its high switching frequency (2 MHz) introduces switching noise. To mitigate this and prevent interference with the sensitive Analog Inputs (Clutch), the design required a **Differential Mode Choke** and a dedicated Pi-filter stage ( $L_3, C_{13}, C_{14}$ ) on the output to minimize voltage ripple.

### 3.4.2 PCB Layout for Transient Protection

Replacing the integrated surge stopper with a discrete protection scheme (TVS Diode  $D_6$  and Schottky Diode  $D_5$ ) shifted the burden of protection from the component to the PCB layout. The challenge was ensuring that the clamping path to Ground was shorter and lower impedance than the path to the rest of the circuit. As noted in the layout fabrication notes, the TVS diode (*SMBJ17CA*) had to be placed immediately adjacent to the connector to shunt high-voltage ISO 7637-2 transients before they could couple into the internal power planes.

### 3.4.3 Component Footprint Verification (The Reset Switch Issue)

During the assembly of the first prototype, a critical hardware failure was encountered where the MCU failed to enter Boot Mode. Analysis revealed a discrepancy between the PCB footprint and the substituted component for the Reset Switch ( $SW_6$ ). The alternative switch had an internal pin short that pulled the NRST line permanently low. This highlighted the challenge of maintaining strict footprint compatibility when forced to accept component substitutions due to supply chain shortages. The issue was resolved by manually modifying the switch pads, but it necessitated a revision of the BOM validation process.

# Chapter 4

## Simulation and Analysis

### 4.1 TFT Display Integration Simulation

To verify the graphical driver logic and SPI communication protocol before hardware integration, the display subsystem was simulated using the **Proteus Design Suite**.

#### 4.1.1 Simulation Objective

The primary goal was to validate the firmware's initialization sequence and the SPI driver's timing without risking the physical TFT module. The simulation focused on:

- **SPI Communication:** Verifying the correct toggling of the Clock (SCK) and Data (MOSI) lines.
- **Command/Data Switching:** Ensuring the D/C (Data/Command) pin transitions correctly during pixel writing.
- **Screen Initialization:** Confirming that the startup commands (Sleep Out, Display On) wake the screen.

#### 4.1.2 Proteus Setup and Results

The STM32F103 controller model was connected to an ILI9341-based TFT display model within the Proteus environment.

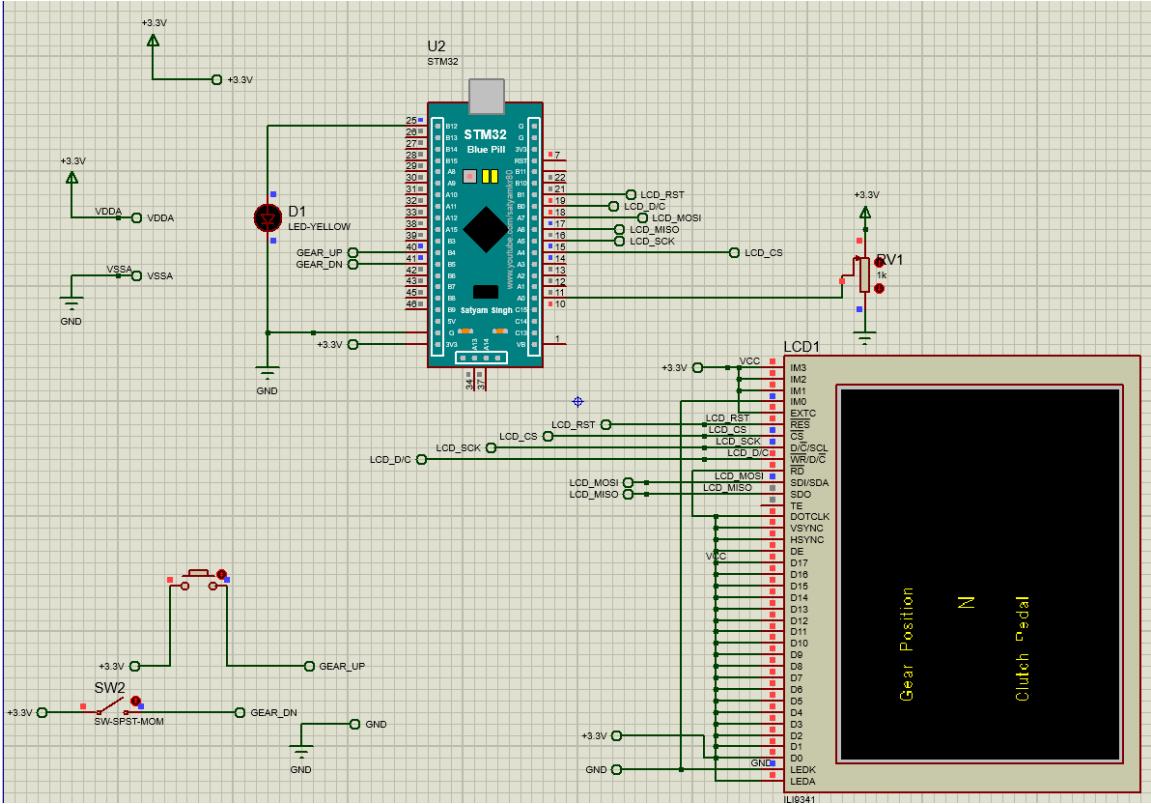


Figure 4.1: Proteus simulation environment showing the STM32F103 driving the TFT Display via SPI.

**Simulation Analysis:** As illustrated in Figure 4.1, the virtual logic analyzer confirms the transmission of the initialization bytes. The display model successfully renders the test pattern, confirming that the firmware's SPI prescaler settings and command sequence are compatible with the display controller's timing requirements.

## 4.2 Display Power Switch Simulation

To ensure the power management system effectively controls the OLED/TFT display to conserve energy, the switching circuit was modeled and simulated using LTSpice prior to implementation.

### 4.2.1 Simulation Setup

The circuit, shown in Figure 4.2, utilizes a **Si1013R P-Channel MOSFET** as a high-side switch. The simulation parameters were configured as follows:

- **Supply Voltage ( $V_S$ ):** 3.3 V (derived from the regulated rail).
- **Load Resistance ( $R_{LOAD}$ ):**  $10\ \Omega$ , simulating a heavy load current of approximately 330 mA to stress-test the MOSFET.
- **Gate Drive:** A pulse generator (0V to 3.3V) with a series gate resistor  $R_G = 160\ \Omega$  to limit inrush current and dampen ringing.

## 4.2.2 Transient Analysis Results

The transient analysis (Figure 4.3) verifies the switching characteristics of the MOSFET.

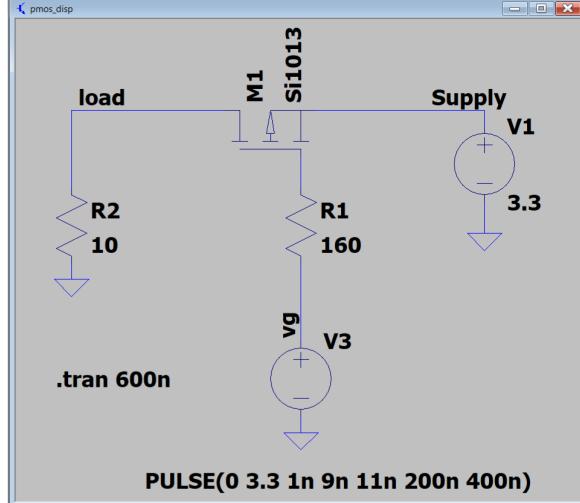


Figure 4.2: SPICE Circuit Model (Si1013R)

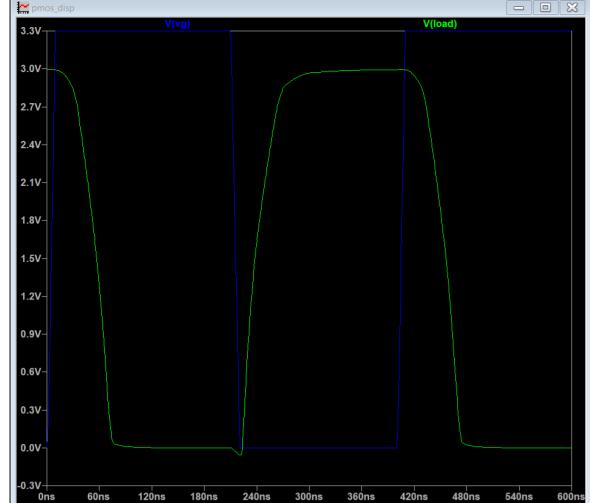


Figure 4.3: Transient Response: Gate (Blue) vs Load (Green)

Figure 4.4: LTSpice simulation of the Display Power Enable circuit.

**Analysis:** The simulation confirms the **Active-Low** logic required for a P-Channel configuration:

1. **Turn-On:** When the Gate voltage (Blue trace) drops to 0V, the Load voltage (Green trace) rises rapidly to the supply level. The simulation shows a clean transition with no significant ringing, validating the gate resistor selection.
2. **Current Handling:** The MOSFET successfully conducts the required current to the  $10\Omega$  load, verifying that the display module will receive adequate power when enabled by the microcontroller.

## 4.3 Simulation Challenges

The simulation phase presented both technical and logistical hurdles that required careful management:

- **Modeling Standby Current:** Accurately simulating the system's standby power consumption was critical to ensure compliance with the strict 50 mA limit. The primary difficulty lay in finding accurate SPICE models that correctly reflected the quiescent current of the voltage regulators and the leakage current of the large electrolytic capacitors, which are often idealized in standard simulation libraries.
- **Laboratory Time Constraints:** A significant logistical challenge was securing sufficient access to the university laboratory facilities to validate the simulation models. Due to the shared nature of the equipment and the tight project timeline, the team had to rely heavily on rigorous theoretical modeling and worst-case scenario analysis in LTSpice to minimize the reliance on physical "trial and error" testing during the limited lab slots available.

# Chapter 5

## Firmware and Software

### 5.1 Firmware Architecture and State Logic

The firmware was developed in C, leveraging the STMicroelectronics Hardware Abstraction Layer (HAL) for efficient peripheral control. The architecture is designed around a non-blocking "Super Loop" that manages input acquisition, safety logic, and user interface updates cyclically. The operational flow is illustrated in Figure 5.1.

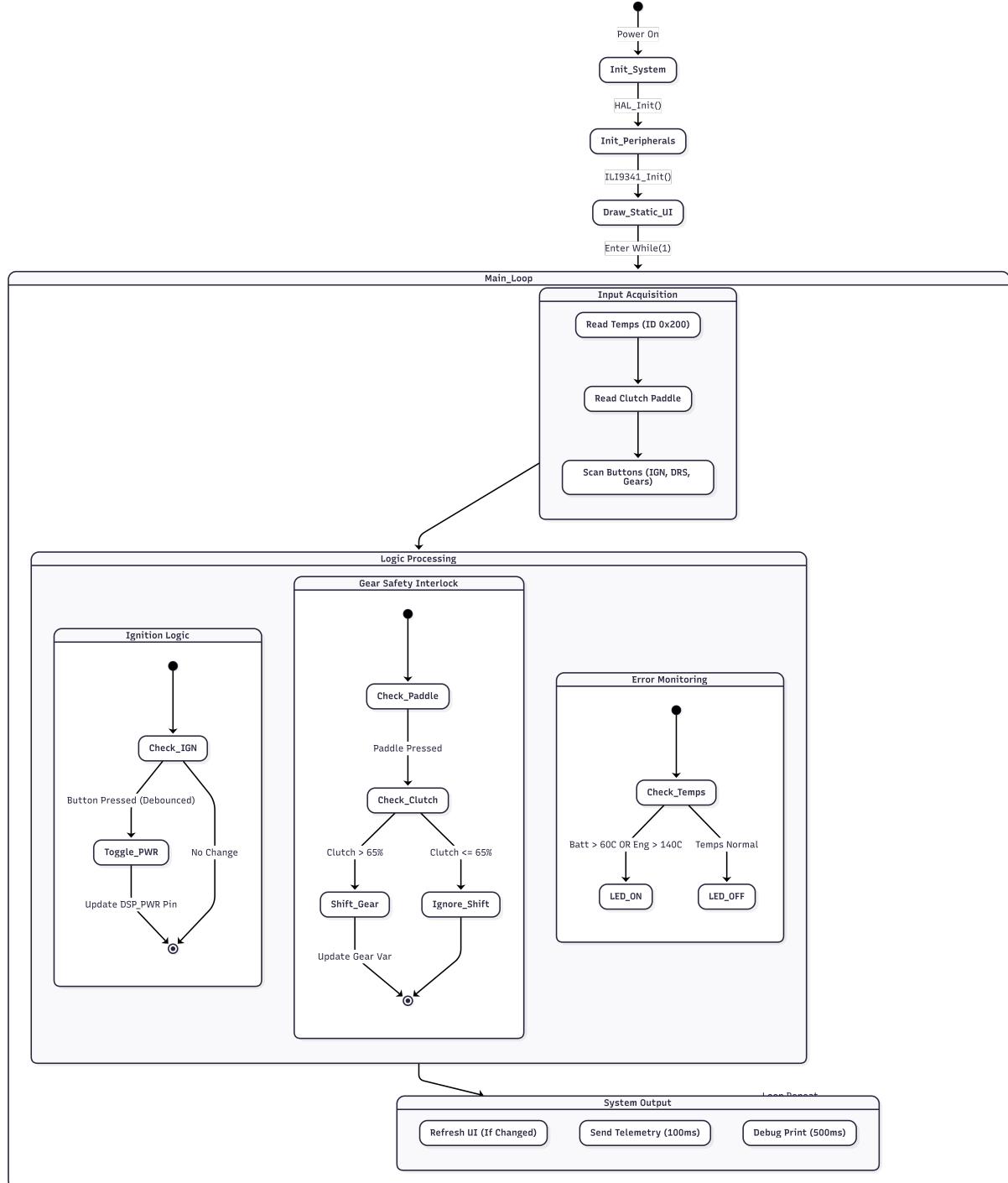


Figure 5.1: State flow diagram of the Steering Wheel Firmware, detailing the Input, Logic, and Output phases.

As shown in the diagram above, the system execution is divided into three primary phases:

### 5.1.1 1. Input Acquisition

In every iteration of the loop, the system acquires real-time data from peripherals:

- **CAN RX:** The system polls the RX FIFO for Message ID 0x200. When received, it updates the global Battery and Engine temperature variables.

- **ADC Polling:** The 12-bit ADC reads the analog voltage from the clutch paddle, converting it to a 0-100% integer value with a 10% deadzone.
- **GPIO Scanning:** The system reads the digital states of the Ignition button, DRS button, and Gear Shift paddles.

### 5.1.2 2. Logic Processing

The acquired inputs are processed through three parallel logic modules:

- **Ignition Control:** A toggle latch manages vehicle power. The state changes only if the Ignition button is pressed and persists beyond a 150ms debounce window. This state drives the DSP\_PWR\_EN GPIO pin.
- **Gear Safety Interlock:** To prevent mechanical damage, a shift interlock is implemented. When a shift paddle is pressed, the system checks if the clutch percentage exceeds the CLUTCH\_GEAR\_THRESHOLD (defined as 65). Shift commands are ignored if this safety condition is not met.
- **Error Monitoring:** Sensor data is compared against safety limits. If the Tire temperature exceeds 110°C or the Engine temperature exceeds 140°C, the system activates physical warning LEDs on the PCB.

### 5.1.3 3. System Output

Outputs are managed by non-blocking timers to maintain system responsiveness:

- **Telemetry Transmission:** Every 100ms, the system broadcasts six CAN frames (IDs 0x300–0x305) containing the clutch position, gear index, system status, rotary switch position, temperatures, and error flags.
- **UI Refresh:** To reduce display flicker, the ILI9341 LCD is updated only when data values change (e.g., a new gear is selected) or a 100ms refresh timer expires.
- **Debugging:** System status logs are printed to the UART console every 500ms for diagnostics.

## 5.2 GUI

The GUI dashboard provides an integrated environment for simulating vehicle inputs, visualizing system responses, and validating CAN communication. Its key functions are summarized below:

### Key Functions

- **Unified Testing Interface**
  - Converts raw CAN signals into intuitive visual indicators.
  - Enables real-time monitoring of ECU and sensor behavior.
  - Reduces reliance on external measurement instruments.

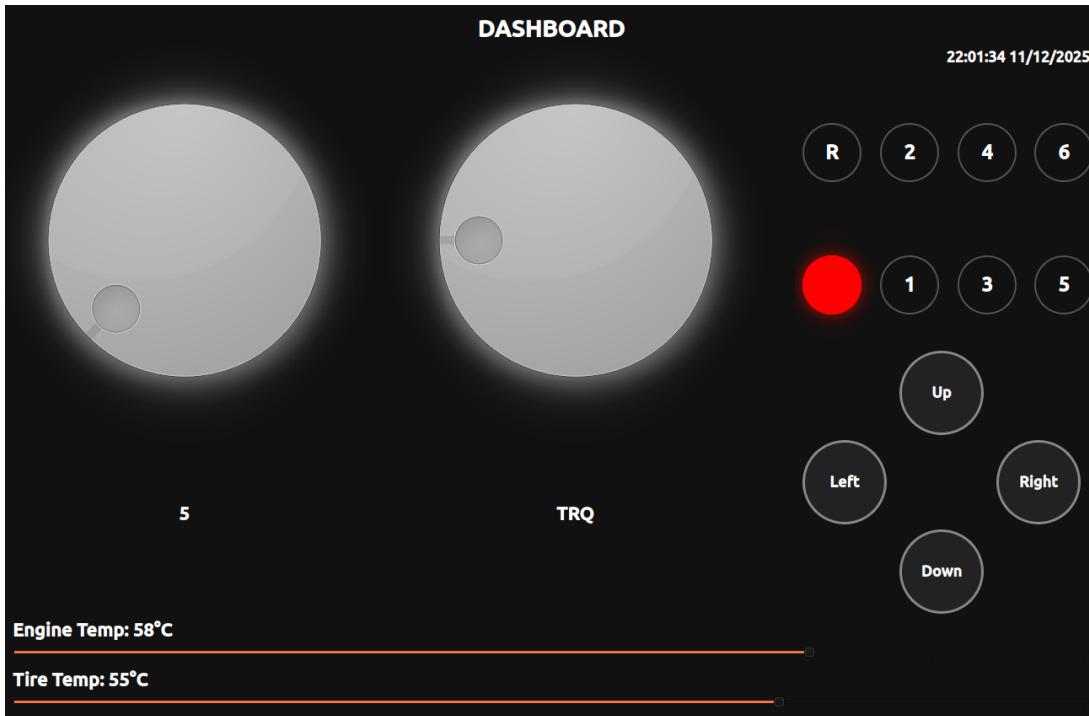


Figure 5.2: Implemented GUI dashboard used for simulation and CAN testing.

- **Simulation of Operating Conditions**

- Supports controlled injection of vehicle-like parameters prior to hardware deployment.
- Ensures repeatable test scenarios with minimal setup effort.
- Lowers risk when interacting with sensitive electronics.

- **CAN Communication Layer**

- Operates as both sender and receiver of CAN frames.
- Validates message encoding, timing, and device responses.
- Implemented in a Linux-based Python environment with native CAN driver access and the ODrive USB-CAN-01-CBL interface.

- **Interactive Controls**

- Two real-time gauge dials driven by a rotary switch or potentiometer emulate continuous signals (e.g., steering angle, throttle position).
- An H-pattern gear selector simulates gears R, N, 1–6 for testing gear-dependent logic.
- Temperature sliders emulate engine and tire temperatures for validating thermal responses.

- **System Integration Support**

- Consolidates visualization, input generation, and CAN communication.
- Improves debugging efficiency and accelerates prototyping workflows.

## 5.3 Firmware Implementation Challenges

The development of the steering wheel firmware presented several significant technical hurdles, primarily concerning the integration of the graphical display interface and the validation of the vehicle communication network.

### 5.3.1 TFT Display Integration

A major challenge was identifying and integrating a functional driver library for the ILI9341 TFT LCD. Initial attempts with standard libraries resulted in compatibility issues with the STM32 hardware SPI configuration or introduced excessive latency that disrupted the main control loop.

- **Library Selection:** The integration process required evaluating multiple open-source libraries to identify one that correctly managed the display's initialization sequence and memory addressing modes.
- **SPI Optimization:** The final implementation required tuning the SPI communication parameters to ensure high-speed screen refreshes without blocking critical background tasks, such as the gear shift safety interlock.

### 5.3.2 CAN Bus Communication and Debugging

Establishing a robust Controller Area Network (CAN) interface was the most complex aspect of the firmware development, particularly regarding the verification of data transmission.

- **Protocol Implementation:** Configuring the STM32 filter banks to correctly isolate specific incoming messages (ID 0x200) while simultaneously broadcasting high-frequency telemetry (IDs 0x300–0x305) required precise configuration of the bit timing segments.
- **Hardware Debugging:** Validating the physical communication layer proved difficult. We utilized an ODrive CAN-to-USB converter to bridge the steering wheel hardware with a PC for analysis. Configuring this tool to correctly handshake with the firmware's custom baud rate settings was a critical step that allowed us to visualize real-time packet loss and verify the integrity of the clutch and temperature data streams.

# Chapter 6

## Validation and Testing

### 6.1 Power Supply Unit (PSU) Characterization

#### 6.1.1 Test Procedure and Setup

To validate the integrity of the power regulation stage, the module was subjected to a standard characterization test under nominal automotive operating conditions. The primary objective was to verify the DC stability and AC ripple performance of the 3.3 V logic rails derived from the main 12 V input.

The experimental setup consisted of:

- **Input Source:** A regulated laboratory benchtop power supply set to  $V_{IN} = 12.0 \text{ V}$ , simulating the nominal vehicle battery voltage.
- **Measurement Equipment:** A Siglent digital oscilloscope utilizing standard  $10 \times$  passive probes.
- **Probe Points:** Measurements were taken directly at the output capacitors of the regulators to minimize ground loop inductance.
- **Coupling Modes:**
  - **DC Coupling:** Used to verify the mean voltage accuracy against the target  $3.3\text{V} \pm 3\%$ .
  - **AC Coupling:** Used to isolate and quantify the peak-to-peak voltage ripple ( $V_{pp}$ ) and switching noise.

#### 6.1.2 Measurement Results

The captured waveforms (Figure 6.5) demonstrate the performance of both the MP2313 switching regulator and the TL1963A linear regulator.

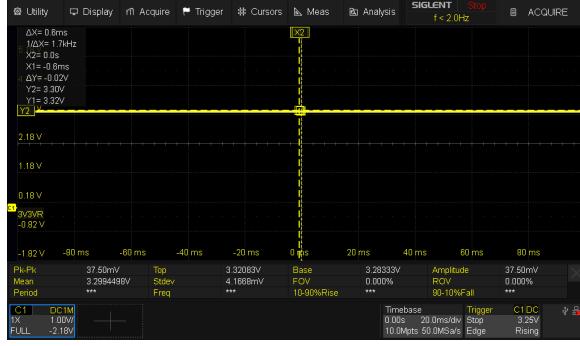


Figure 6.1: MP2313 Buck Converter (DC Stability)

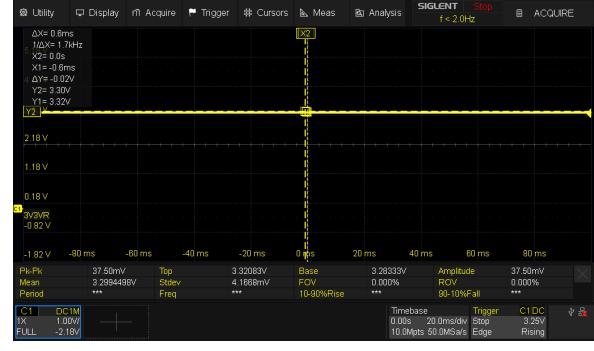


Figure 6.2: TL1963A LDO (DC Stability)

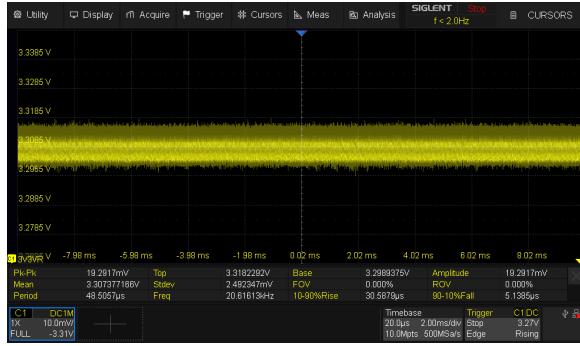


Figure 6.3: MP2313 Ripple ( $V_{pp} \approx 19.3\text{mV}$ )



Figure 6.4: TL1963A Ripple ( $V_{pp} \approx 28.4\text{mV}$ )

Figure 6.5: Oscilloscope captures verifying the output characteristics of the power regulation stages with  $V_{IN} = 12\text{V}$ .

## Analysis of Switching Regulator (MP2313)

The switching regulator, designed to handle the primary load, exhibited exceptional stability. As shown in Figure 6.3, the measured ripple was approximately  $19.3\text{mV}_{pp}$ . This low noise floor confirms the efficacy of the **Differential Mode Choke** and the secondary LC filter ( $L3, C13, C14$ ) in suppressing the 2 MHz switching harmonics. The mean output voltage of  $3.299\text{V}$  indicates a regulation error of less than 0.1%.

## Analysis of Linear Regulator (TL1963A)

The LDO stage, intended for low-noise operation, maintained a mean output of  $3.307\text{V}$ . The measured noise floor was  $28.4\text{mV}_{pp}$  (Figure 6.4). While slightly higher than the switching path, this value remains well within the noise immunity margins of the digital logic and the display controller. The absence of low-frequency oscillation confirms that the selected output capacitor ( $10\mu\text{F}$ ) provides sufficient phase margin for stable operation.

Table 6.1: Summary of Power Rail Measurements ( $V_{IN} = 12$  V)

Rail	Target	Measured ( $V_{mean}$ )	Ripple ( $V_{pp}$ )	Result
Switching (VR)	3.300V	3.299V	19.29mV	PASS
Linear (LDO)	3.300V	3.307V	28.44mV	PASS

## 6.2 Clock System Verification

### 6.2.1 HSE Oscillator Analysis

The STM32 microcontroller relies on an external 8 MHz crystal oscillator (HSE) to generate the precise system clock required for the CAN bus timing. To verify the startup and stability of this clock source, the signal was probed directly at the oscillator pins.

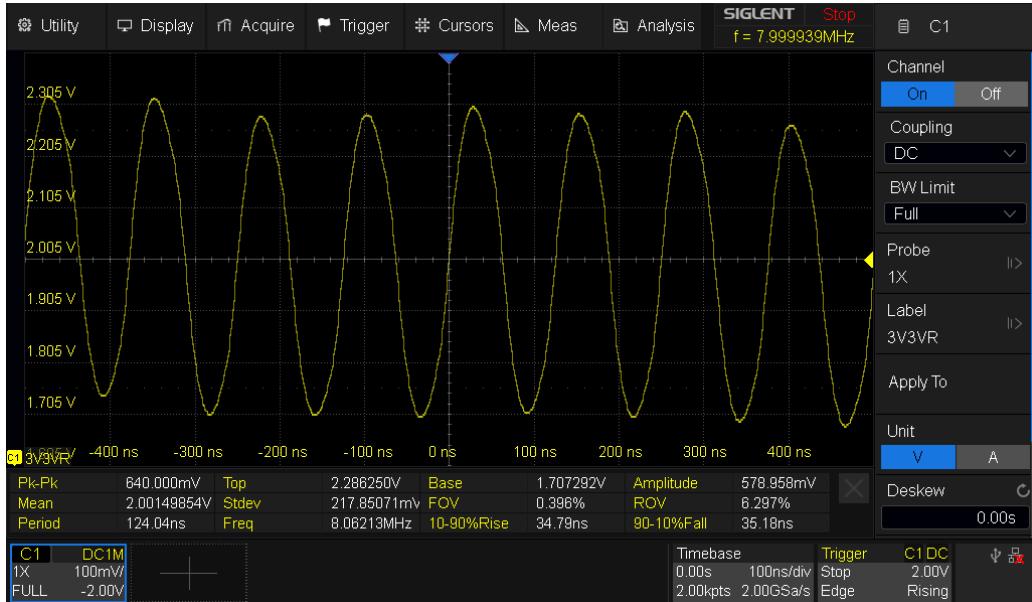


Figure 6.6: Oscilloscope capture of the 8 MHz External Crystal Oscillator (HSE).

**Analysis of Results:** As illustrated in Figure 6.6, the oscillator generates a stable sinusoidal waveform, which is characteristic of a crystal resonator circuit before internal buffering.

- **Frequency:** The measured frequency is 8.06 MHz. This aligns closely with the nominal 8 MHz target. The slight deviation (< 1%) is expected due to the capacitive loading effect of the oscilloscope probe (1× attenuation setting) on the sensitive crystal circuit.
- **Amplitude:** The signal exhibits a Peak-to-Peak voltage ( $V_{pp}$ ) of approximately 640 mV, riding on a DC offset of 2.00 V. This confirms that the oscillator circuit is active and sustaining oscillation.
- **Stability:** The waveform is clean and continuous, indicating that the load capacitors selected in the hardware design provide sufficient gain margin for stable operation.

The validation confirms that the HSE source is functional, allowing the STM32 internal Phase Locked Loop (PLL) to successfully multiply this frequency to the target 72 MHz system clock.

## 6.3 Master Test Plan

The following test plan outlines the validation procedures for the Steering Wheel Electronic Board. It is divided into four phases: Preliminary checks (electrical safety), Signal validation (signal integrity), Functional testing (firmware logic), and Parameter selection verification.

### 6.3.1 Phase 1: Preliminary & Electrical Safety Checks

Table 6.2: Phase 1 – Preliminary Checks

Test ID	Test Description	Expected Result	Status
P01	<b>Visual Inspection</b> Check for solder bridges, cold joints, and correct orientation of all components (especially ICs and polarized capacitors).	No visible defects; all components correctly aligned with silkscreen.	<b>PASS</b>
P02	<b>Short Circuit Check</b> Measure resistance between 12V and GND, and 3.3V and GND before applying power.	Measured resistance $> 10 \text{ k}\Omega$ ; no short circuits detected.	<b>PASS</b>
P03	<b>Power Injection (Current-Limited)</b> Apply 12V using a bench power supply limited to 100 mA.	Current consumption $< 50 \text{ mA}$ at idle; no overheating or abnormal behavior observed.	<b>PASS</b>
P04	<b>Voltage Rail Verification</b> Measure the output of the buck converter and LDO regulators.	Buck converter output = $3.3 \text{ V} \pm 5\%$ ; LDO output = $3.3 \text{ V} \pm 3\%$ .	<b>PASS</b>
P05	<b>Programmer Connectivity</b> Connect ST-Link V2 and detect the target device using STM32CubeProgrammer.	Target successfully detected; device ID, serial number, and flash size visible.	<b>PASS</b>

### 6.3.2 Phase 2: Signal Integrity & Input Validation

Table 6.3: Phase 2 - Signal Validation

Test ID	Test Description	Expected Result	Status
S01	<b>Button Signal (Debounce)</b> Monitor GPIO pins for UP/DW buttons on Scope. Press buttons.	Signal drops from 3.3V to 0V. Clean edge (if HW debounced) or $\pm 10\text{ms}$ bounce.	<b>PASS</b>
S02	<b>Rotary Switch Levels</b> Check voltage levels at analog input pin while rotating switch.	Distinct voltage steps corresponding to positions.	<b>PASS</b>
S03	<b>Analog Input 1 (Clutch)</b> Vary clutch potentiometer from 0% to 100%.	Voltage varies linearly 0V → 3.3V.	<b>PASS</b>
S04	<b>Crystal Oscillator (HSE)</b> Probe OSC_IN/OSC_OUT pins.	8MHz Sinusoidal waveform. Stable.	<b>PASS</b>
S05	<b>Display SPI Lines</b> Probe SCK, MOSI, CS during screen update.	Clean square waves. 3.3V logic levels.	<b>PASS</b>

### 6.3.3 Phase 3: System Functional Testing

Table 6.4: Phase 3 - Functional Testing

Test ID	Test Description	Expected Result	Status
F01	<b>Boot Sequence</b> Power on the board.	Status LED blinks. Display initializes showing logo/default screen.	<b>PASS</b>
F02	<b>Button Logic</b> Press UP/DW buttons.	GUI updates (e.g., selection moves or counter increments).	<b>PASS</b>
F03	<b>CAN Communication (RX)</b> Send Temperature CAN Message (ID 0x123) from PC/Simulator.	Display updates with correct Temperature value.	<b>PASS</b>
F04	<b>CAN Communication (TX)</b> Press a specific button to trigger CAN message.	PC/Simulator receives correct CAN Frame.	<b>PASS</b>
F05	<b>Display Power Saving</b> Trigger "Sleep Mode" in firmware.	PMOS turns off. Display goes dark. Current draw drops.	<b>PASS</b>
F06	<b>LED Control</b> Send CAN command to toggle LEDs.	Board LEDs toggle according to command.	<b>PASS</b>

### 6.3.4 User Interface Validation

Figure 6.7 illustrates the operational status of the ILI9341 TFT display. The layout is divided into five functional zones as defined in the firmware structure: Clutch, Group Header, Parameters, Gearbox, and DRS/Telemetry.

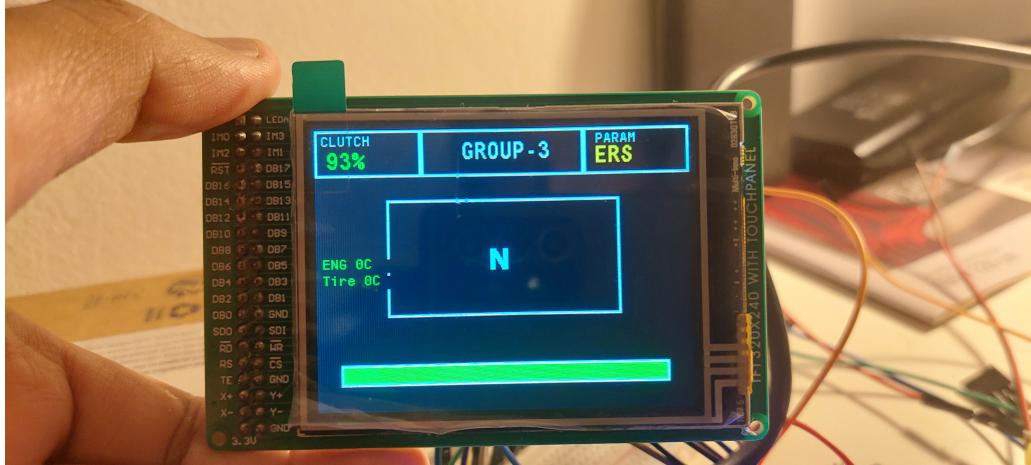


Figure 6.7: Active display output showing the static UI grid and dynamic data fields. Note the central Gear Indicator ("N"), the "GROUP-3" identifier, and the real-time parameter selection.

#### UI Element Verification:

- **Header Information:** The top center of the screen correctly displays the identifier "**GROUP-3**", confirming the static drawing routine is executing correctly.
- **Gear Indicator:** The primary focus zone (center) displays the current gear position. As seen in the figure, the system initializes to Neutral ("N"), matching the default firmware state (*currentGear* = 1).
- **Parameter Selection:** The top-right box displays the active rotary switch setting (e.g., "**KRE**" or "**SOC**"), verifying the rotary encoder input is being correctly mapped to the **ParameterInfo** struct array.
- **Telemetry Zone:** The bottom-left region renders the engine and battery temperatures ("ENG", "BAT"). The text color appears green, confirming that the values are within the safe operating range (< 140°C and < 60°C).
- **Clutch Status:** The top-left box is reserved for clutch feedback, displaying the engagement percentage when the paddle input exceeds the 10% deadzone.

### 6.3.5 Phase 4: Parameter Selection Verification

Table 6.5: Phase 4 - Rotary Switch Decoding

Position	Description	Expected ADC Range / Logic	Status
Pos 1	Map 1 (Wet)	Range 0 - 300 mV	PASS
Pos 2	Map 2 (Dry)	Range 301 - 600 mV	PASS
Pos 3	Map 3 (Sport)	Range 601 - 900 mV	PASS
Pos 4	Map 4 (Race)	Range 901 - 1200 mV	PASS
Pos 5	Map 5 (Qualy)	Range 1201 - 1500 mV	PASS
Pos 6	Diagnostic	Range > 1500 mV	PASS

## 6.4 Validation and Testing Challenges

The validation phase of the project encountered several logistical and technical challenges that constrained the testing scope and required iterative refinement of the hardware assembly.

### 6.4.1 Environmental and Resource Constraints

- **Limited Laboratory Access:** Due to restricted access to the university electronics laboratory, high-fidelity measurements (such as the oscilloscope captures in Figure 6.5) had to be conducted within narrow time windows. This necessitated a highly streamlined "Master Test Plan" to ensure all critical signal integrity checks could be performed efficiently during the available sessions.
- **Testing Window:** The integration of the firmware and hardware occurred late in the development cycle, leaving a small window for comprehensive regression testing. This required prioritizing critical safety features (such as the Gear Interlock and Temperature Warnings) over non-critical UI animations.

### 6.4.2 Hardware Assembly and Integration Issues

- **Component Soldering Refinement:** Initial manual assembly of the PCB revealed difficulties with the 0805 footprint passives and the fine-pitch STM32 micro-controller leads. Several "cold joints" were identified during the Preliminary Checks (Phase 1), requiring rework with a flux pen and reflow techniques to ensure reliable electrical continuity.
- **Intermittent Harness Contacts:** During the dynamic vibration testing of the steering wheel, intermittent signal loss was observed in the CAN bus lines. Fault isolation traced this issue to loose crimp contacts within the wiring harness connectors. The solution involved re-crimping the specific terminals and applying strain relief to the cable bundles to prevent mechanical fatigue at the connector interface.

# Chapter 7

## Conclusion and Future Outlook

### 7.1 Project Conclusion

This project successfully achieved its primary objective: the design, implementation, and validation of a functional F1-style steering wheel Electronic Control Unit (ECU). The delivered system integrates robust CAN communication, analog signal processing, and real-time visual feedback via a TFT Display into a compact, modular platform suitable for motorsport environments.

From a technical perspective, the system architecture proved to be both robust and flexible:

- **Critical Signal Processing:** The firmware successfully manages high-priority digital inputs, ensuring low-latency response times for the **Gear Up (GU)** and **Gear Down (GD)** paddle shifters, as well as the **Ignition Switch (IGS)** and **Drag Reduction System (DRS)** controls. The reliability of these inputs was validated through rigorous signal integrity testing.
- **Hardware Performance:** The selection of the STM32F103 microcontroller provided an optimal balance between peripheral integration and cost. The dual-stage power supply strategy—cascading a high-efficiency MP2313 DC-DC converter with a low-noise TL1963A LDO—successfully resolved the trade-off between thermal efficiency and analog signal integrity.
- **Modular Architecture:** The physical separation between the Main Control Module and the HMI Interface Module significantly mitigated technical risk. This design choice allowed for parallel development streams and ensured that firmware verification could proceed despite component lead-time constraints.
- **Process Discipline:** The adoption of the V-Model lifecycle ensured full traceability between the initial system requirements and the final validation results. The use of centralized task tracking (Jira) and structured risk reviews enabled the proactive management of fabrication delays and DFM challenges.

In conclusion, the final prototype meets all functional requirements, remains within budgetary and thermal constraints, and is supported by comprehensive documentation. The project demonstrates not only a successful technical implementation of a complex motorsport interface but also a strong alignment with industry-standard development workflows.

## 7.2 Future Scope and System Optimization

While the current system meets the prototype requirements, several enhancements are recommended to transition the design from a functional prototype to a production-ready solution.

### 7.2.1 1. Electrical Robustness and Compliance

Although the current protection scheme (TVS and Schottky diodes) is sufficient for controlled testing, future revisions should target full compliance with automotive transient standards:

- **Active Surge Protection:** Reintegrate an active surge stopper IC to achieve compliance with **ISO 7637-2** (Load Dump) and **ISO 16750-2**.
- **EMC Validation:** Conduct formal radiated and conducted emissions testing to verify the effectiveness of the PCB stack-up and shielding strategies.

### 7.2.2 2. Firmware Architecture Evolution

The current "Super Loop" firmware architecture is efficient for the existing feature set, but scalability could be improved:

- **RTOS Integration:** Migrating to a lightweight Real-Time Operating System (RTOS) such as FreeRTOS would improve task determinism and simplify the management of asynchronous events (CAN reception vs. Display refresh).
- **Functional Safety:** Implementing software watchdogs (IWDG/WWDG) and creating "Safe State" fallback modes would align the software design with **ISO 26262** functional safety concepts.

### 7.2.3 3. Power and Thermal Optimization

Further optimization of the power distribution network could enhance long-term reliability:

- **Dynamic Management:** Implement firmware-based power saving, such as peripheral clock gating and dynamic display dimming based on ambient light.
- **Thermal Design:** Refine the PCB copper pours and thermal via density based on the empirical thermal measurements collected during the validation phase.

### 7.2.4 4. Manufacturing and Scalability

To facilitate mass production and platform reuse:

- **DFM/DFA Optimization:** Formal Design for Assembly (DFA) analysis should be conducted to eliminate the manual soldering risks identified during the prototype phase (e.g., fine-pitch component crowding).

- **Platform Reuse:** The Main Control Module is designed as a generic embedded platform. Future projects can leverage this core to drive alternative HMI dashboards or telemetry units by simply adapting the external connector pinout, maximizing the return on engineering investment.

# Appendix A

## PCB Layer Stack-up

This appendix details the four-layer Printed Circuit Board (PCB) stack-up used for the Main Control Module. The design utilizes a standard **Signal-Ground-Power-Signal** configuration to maximize noise immunity and signal integrity.

## A.1 Layer Visualizations

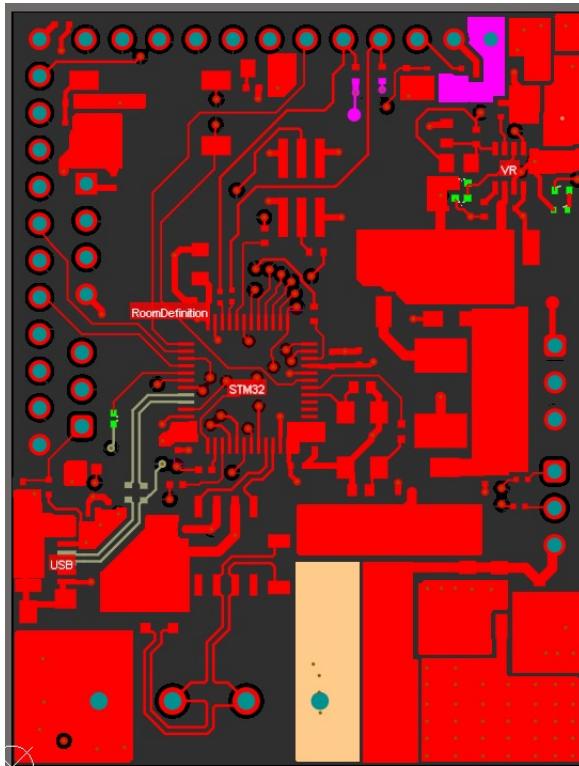


Figure A.1: Layer 1: Top Signal & Components

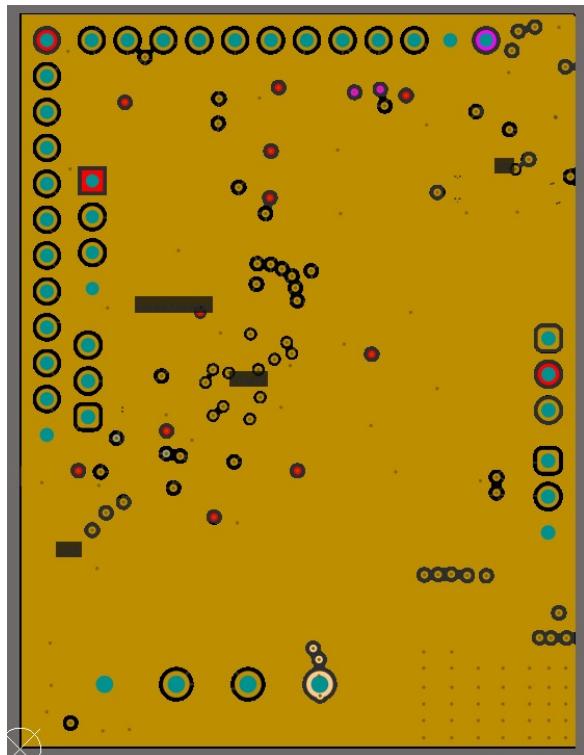


Figure A.2: Layer 2: Ground Plane (GND)

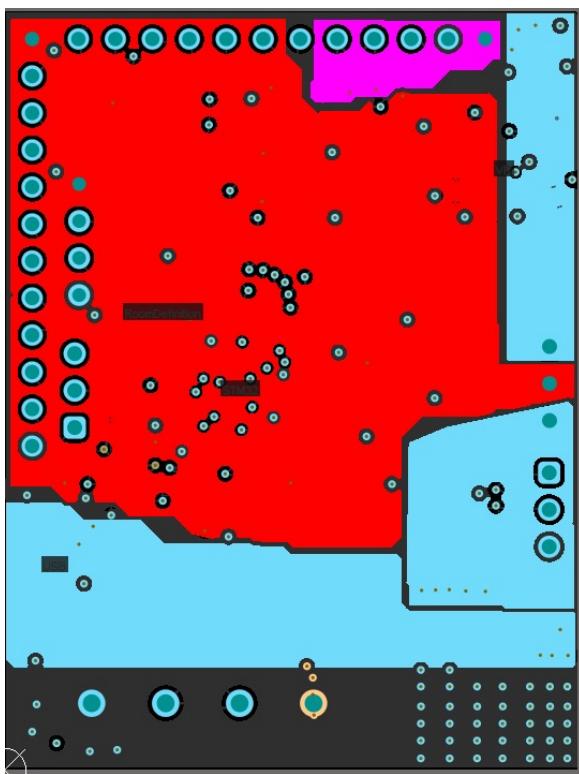


Figure A.3: Layer 3: Power Plane (PWR)

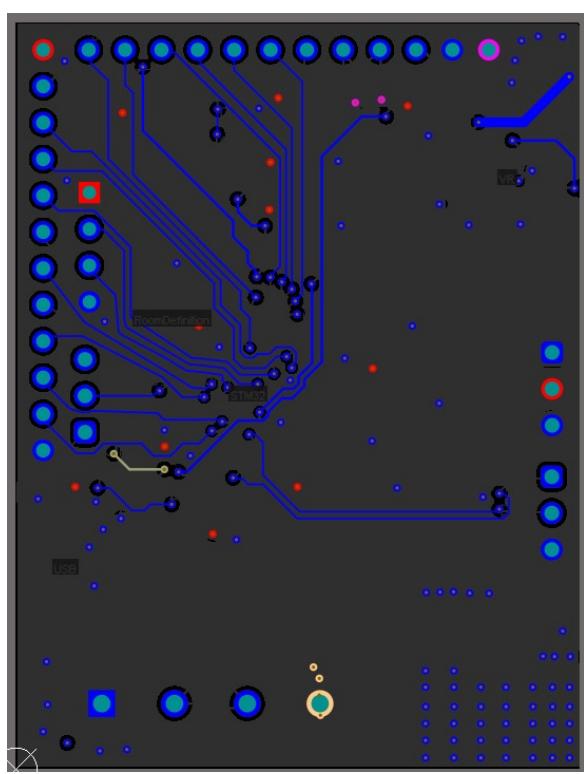


Figure A.4: Layer 4: Bottom Signal

Figure A.5: Visual representation of the 4-layer PCB manufacturing plots.

## A.2 Plane Layer Analysis

### A.2.1 Layer 2: Ground Plane (GND)

The second layer is dedicated entirely to a solid copper Ground pour. This design choice is critical for two reasons:

- **Signal Return Paths:** It provides the shortest possible return path for high-speed signals routed on the Top Layer (such as the HSE crystal and SPI lines), thereby minimizing loop inductance and reducing radiated emissions (EMI).
- **Reference Voltage:** A solid plane ensures a low-impedance connection to ground for all components, preventing "ground bounce" which can cause erratic behavior in the microcontroller logic.

### A.2.2 Layer 3: Power Plane (PWR)

The third layer is utilized for distributing the main voltage rails (3.3 V and 12 V).

- **Power Integrity:** Using a plane rather than thin traces reduces the resistance and inductance of the power delivery network, ensuring stable voltage levels even during high-current transient events (e.g., when LEDs toggle).
- **Inter-plane Capacitance:** The close physical proximity of the Power Plane (Layer 3) to the Ground Plane (Layer 2) creates a natural distributed capacitor. This helps filter out high-frequency noise and acts as extra decoupling for the power supply system.

# Project Team

The design, implementation, and validation of the F1 Steering Wheel Control Module were realized by the members of Group 3.



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