		μ-instr address	μ-instr datapath	SC-cmds	Signals	Next Address	MP ROM	
							signals	@+SC-cmds
	Fetch	0x10	AB←MU←PC	CAR++	MU=0,ABw	-	0x6400 0000	0x000
		0x11	IR←ALU←Mux ←RAM[AB],PC++	CAR++	Mux=0,ALU=9,IRw, PC++	-	0x3200 0009	0x000
		0x12	- (goto Address Mode)	AM-MAP	-	-	0x2000 0000	0x200
Addressing Mode	Implied (opc:---- 10-0)	0x14	- (goto OpCode Map)	OP-MAP	-	-	0x2000 0000	0x300
	Immediate (opc:1—00 0-0 or ---0 10-1)	0x15	AB←MU←PC,PC++	OP-MAP	MU=0,ABw,PC++	-	0x3400 0000	0x300
	zero page (opc:---0 01--)	0x16	AB←MU←PC,PC++	CAR++	MU=0,ABw,PC++	-	0x3400 0000	0x000
		0x17	MU←ALU←Mux ←RAM[AB]	CAR++	Mux=0,ALU=9,MU=4	-	0x2000 0209	0x000
		0x18	AB←MU	OP-MAP	MU=3,ABw	-	0x2400 0180	0x300
	zero page,X (opc:---1 01--)	0x19	AB←MU←PC,PC++ TMP←ALU←Acc	CAR++	MU=0,ABw,PC++ ALU=6,TMPw	-	0x3420 0006	0x000
		0x1A	Acc←ALU←Mux ←RAM[AB]	CAR++	Mux=0,ALU=9,Accw	-	0x2004 0009	0x000
		0x1B	MU←ALU←Mux←X	CAR++	Mux=5,ALU=4,MU=4	-	0x2000 0254	0x000
		0x1C	AB←MU Acc←ALU←Mux←TMP	OP-MAP	MU=3,ABw Mux=7,ALU=9,Accw	-	0x2404 01F9	0x300
	zero page,Y (opc:10-1 011-)	0x1D	AB←MU←PC,PC++ TMP←ALU←Acc	CAR++	MU=0,ABw,PC++ ALU=6,TMPw	-	0x3420 0006	0x000
		0x1E	Acc←ALU←Mux ←RAM[AB]	CAR++	Mux=0,ALU=9,Accw	-	0x2004 0009	0x000
		0x1F	MU←ALU←Mux←Y	CAR++	Mux=6,ALU=4,MU=4	-	0x2000 0264	0x000
		0x20	AB←MU Acc←ALU←Mux←TMP	OP-MAP	MU=3,ABw Mux=7,ALU=9,Accw	-	0x2404 01F9	0x300
	relative (opc:---1 00-0)	0x21	AB←MU←PC,PC++ TMP←ALU←Acc	CAR++	MU=0,ABw,PC++ ALU=6,TMPw	-	0x3420 0006	0x000
		0x22	Acc←ALU←Mux ←-PC-lo	CAR++	Mux=2,ALU=9,Accw	-	0x2004 0029	0x000
		0x23	PC-lo←ALU←Mux ←RAM[AB],brch	CAR++	Mux=0,ALU=4,brch	-	0x2000 0804	0x000
		0x24	Acc←ALU←Mux←TMP	Next-Address	Mux=7,ALU=9,Accw	0x10	0x2004 0079	0x110
	absolute (opc:---0 11--)	0x25	AB←MU←PC,PC++	CAR++	MU=0,ABw,PC++	-	0x3400 0000	0x000
		0x26	MU←ALU←Mux ←RAM[AB],PC++	CAR++	Mux=0,ALU=9,MU=4 PC++	-	0x2000 0209	0x000
		0x27	AB←MU←PC,PC++	CAR++	MU=0,ABw,PC++	-	0x3400 0000	0x000
		0x28	MU←ALU←Mux ←RAM[AB]	CAR++	Mux=0,ALU=9,MU=5	-	0x2000 0289	0x000
		0x29	AB←MU	OP-MAP	MU=3,ABw	-	0x2400 0180	0x300

Addressing Mode	absolute,X (opc:---1 11--)	0x2A	AB←MU←PC,PC++ TMP←ALU←Acc	CAR++	MU=0,ABw,PC++ ALU=6,TMPw	-	0x3420 0006	0x000
		0x2B	Acc←ALU←Mux ←RAM[AB]	CAR++	Mux=0,ALU=9,Accw	-	0x2004 0009	0x000
		0x2C	MU←ALU←Mux←X	CAR++	Mux=5,ALU=4,MU=7	-	0x2000 03D4	0x000
		0x2D	AB←MU←PC,PC++ Acc←ALU←Mux←TMP	CAR++	MU=0,ABw,PC++ Mux=7,ALU=9,Accw	-	0x3404 0079	0x000
		0x2E	MU←ALU←Mux ←RAM[AB]	CAR++	Mux=0,ALU=9,MU=5	-	0x2000 0289	0x000
		0x2F	MU(@hi++) if carry	CAR++	MU=6	-	0x2000 0300	0x000
		0x30	AB←MU	OP-MAP	MU=3,ABw	-	0x2400 0180	0x300
	absolute,Y (opc:---1 10-1 or 10-1 111-)	0x31	AB←MU←PC,PC++ TMP←ALU←Acc	CAR++	MU=0,ABw,PC++ ALU=6,TMPw	-	0x3420 0006	0x000
		0x32	Acc←ALU←Mux ←RAM[AB]	CAR++	Mux=0,ALU=9,Accw	-	0x2004 0009	0x000
		0x33	MU←ALU←Mux←Y	CAR++	Mux=6,ALU=4,MU=7	-	0x2000 03E4	0x000
		0x34	AB←MU←PC,PC++ Acc←ALU←Mux←TMP	CAR++	MU=0,ABw,PC++ Mux=7,ALU=9,Accw	-	0x3404 0079	0x000
		0x35	MU←ALU←Mux ←RAM[AB]	CAR++	Mux=0,ALU=9,MU=5	-	0x2000 0289	0x000
		0x36	MU(@hi++) if carry	CAR++	MU=6	-	0x2000 0300	0x000
		0x37	AB←MU	OP-MAP	MU=3,ABw	-	0x2400 0180	0x300
	X,indirect (opc:---0 00-1)	0x38	AB←MU←PC,PC++ TMP←ALU←Acc	CAR++	MU=0,ABw,PC++ ALU=6,TMPw	-	0x3420 0006	0x000
		0x39	Acc←ALU←Mux ←RAM[AB]	CAR++	Mux=0,ALU=9,Accw	-	0x2004 0009	0x000
		0x3A	MU←ALU←Mux←X	CAR++	Mux=5,ALU=4,MU=4	-	0x2000 0254	0x000
		0x3B	AB←MU Acc←ALU←Mux←TMP	CAR++	MU=3,ABw Mux=7,ALU=9,Accw	-	0x2404 01F9	0x000
		0x3C	MU←ALU←Mux ←RAM[AB]	CAR++	Mux=0,ALU=9,MU=4	-	0x2000 0209	0x000
		0x3D	AB-lo++	CAR++	MU=2	-	0x2000 0100	0x000
		0x3E	MU←ALU←Mux ←RAM[AB]	CAR++	Mux=0,ALU=9,MU=5	-	0x2000 0289	0x000
		0x3F	AB←MU	OP-MAP	MU=3,ABw	-	0x2400 0180	0x300
	indirect,Y (opc:---1 00-1)	0x40	AB←MU←PC,PC++ TMP←ALU←Acc	CAR++	MU=0,ABw,PC++ ALU=6,TMPw	-	0x3420 0006	0x000
		0x41	MU←ALU←Mux ←RAM[AB]	CAR++	Mux=0,ALU=9,MU=4	-	0x2000 0209	0x000
		0x42	AB←MU	CAR++	MU=3,ABw	-	0x2400 0180	0x000
		0x43	Acc←ALU←Mux ←RAM[AB]	CAR++	Mux=0,ALU=9,Accw	-	0x2004 0009	0x000
		0x44	MU←ALU←Mux←Y	CAR++	Mux=6,ALU=4,MU=7	-	0x2000 03E4	0x000
		0x45	Acc←ALU←Mux←TMP AB-lo++	CAR++	Mux=7,ALU=9,Accw MU=2	-	0x2004 0179	0x000
		0x46	MU←ALU←Mux ←RAM[AB]	CAR++	Mux=0,ALU=9,MU=5	-	0x2000 0289	0x000
		0x47	MU(@hi++) if carry	CAR++	MU=6	-	0x2000 0300	0x000
		0x48	AB←MU	OP-MAP	MU=3,ABw	-	0x2400 0180	0x300

Instruction OpCode								
	ORA	0x50	Acc←ALU←Mux ←RAM[AB],P(NZ)	Next-Address	Mux=0,ALU=E,Accw CF=1	0x10	0x2004 100E	0x110
	AND	0x51	Acc←ALU←Mux ←RAM[AB],P(NZ)	Next-Address	Mux=0,ALU=1,Accw CF=1	0x10	0x2004 1001	0x110
	EOR	0x52	Acc←ALU←Mux ←RAM[AB],P(NZ)	Next-Address	Mux=0,ALU=0,Accw CF=1	0x10	0x2004 1000	0x110
	ADC	0x53	Acc←ALU←Mux ←RAM[AB],P(NZ)	Next-Address	Mux=0,ALU=5,Accw CF=3	0x10	0x2004 3005	0x110
	STA	0x54	OUT←ALU←Acc	CAR++	ALU=6,OUTw	-	0x2800 0006	0x000
		0x55	RAM[AB]←OUT	Next-Address	R/W_=0	0x10	0x0000 0000	0x110
	LDA	0x56	Acc←ALU←Mux ←RAM[AB],P(NZ)	Next-Address	Mux=0,ALU=9,Accw CF=1	0x10	0x2004 1009	0x110
	CMP	0x57	ALU←Mux←RAM[AB] P(NZC)	Next-Address	Mux=0,ALU=F CF=2	0x10	0x2000 200F	0x110
	SBC	0x58	Acc←ALU←Mux ←RAM[AB],P(NZ)	Next-Address	Mux=0,ALU=7,Accw CF=3	0x10	0x2004 3007	0x110
	ASL Mem	0x59	OUT←ALU←Mux ←RAM[AB],P(NZC)	CAR++	Mux=0,ALU=C,OUTw CF=2	-	0x2800 200C	0x000
		0x5A	RAM[AB]←OUT	Next-Address	R/W_=0	0x10	0x0000 0000	0x110
	ASL Acc	0x5B	TMP←ALU←Acc	CAR++	ALU=6,TMPw	-	0x2020 0006	0x000
		0x5C	Acc←ALU←Mux ←TMP,P(NZC)	Next-Address	Mux=7,ALU=C,Accw CF=2	0x10	0x2004 207C	0x110
	ROL Mem	0x5D	OUT←ALU←Mux ←RAM[AB],P(NZC)	CAR++	Mux=0,ALU=D,OUTw CF=2	-	0x2800 200D	0x000
		0x5E	RAM[AB]←OUT	Next-Address	R/W_=0	0x10	0x0000 0000	0x110
	ROL Acc	0x5F	TMP←ALU←Acc	CAR++	ALU=6,TMPw	-	0x2020 0006	0x000
		0x60	Acc←ALU←Mux ←TMP,P(NZC)	Next-Address	Mux=7,ALU=D,Accw CF=2	0x10	0x2004 207D	0x110
	LSR Mem	0x61	OUT←ALU←Mux ←RAM[AB],P(NZC)	CAR++	Mux=0,ALU=3,OUTw CF=2	-	0x2800 2003	0x000
		0x62	RAM[AB]←OUT	Next-Address	R/W_=0	0x10	0x0000 0000	0x110
	LSR Acc	0x63	TMP←ALU←Acc	CAR++	ALU=6,TMPw	-	0x2020 0006	0x000
		0x64	Acc←ALU←Mux ←TMP,P(NZC)	Next-Address	Mux=7,ALU=3,Accw CF=2	0x10	0x2004 2073	0x110
	ROR Mem	0x65	OUT←ALU←Mux ←RAM[AB],P(NZC)	CAR++	Mux=0,ALU=B,OUTw CF=2	-	0x2800 200B	0x000
		0x66	RAM[AB]←OUT	Next-Address	R/W_=0	0x10	0x0000 0000	0x110
	ROR Acc	0x67	TMP←ALU←Acc	CAR++	ALU=6,TMPw	-	0x2020 0006	0x000
		0x68	Acc←ALU←Mux ←TMP,P(NZC)	Next-Address	Mux=7,ALU=B,Accw CF=2	0x10	0x2004 207B	0x110
	STX	0x69	OUT←ALU←Mux←X	CAR++	Mux=5,ALU=9,OUTw	-	0x2800 0059	0x000
		0x6A	RAM[AB]←OUT	Next-Address	R/W_=0	0x10	0x0000 0000	0x110
	TXA	0x6B	Acc←ALU←Mux←X P(NZ)	Next-Address	Mux=5,ALU=9,Accw CF=1	0x10	0x2004 1059	0x110
	TXS	0x6C	SP←ALU←Mux←X	Next-Address	Mux=5,ALU=9,SPw	0x10	0x2040 0059	0x110
	LDX	0x6D	X←ALU←Mux ←RAM[AB],P(NZ)	Next-Address	Mux=0,ALU=9,Xw CF=1	0x10	0x2008 1009	0x110
	TAX	0x6E	X←ALU←Acc P(NZ)	Next-Address	ALU=6,Xw CF=1	0x10	0x2008 1006	0x110
	TSX	0x6F	X←ALU←Mux←SP P(NZ)	Next-Address	Mux=3,ALU=9,Xw CF=1	0x10	0x2008 1039	0x110

Instruction OpCode								
	DEC	0x70	OUT←ALU←Mux ←RAM[AB],P(NZ)	CAR++	Mux=0,ALU=A,OUTw CF=1	-	0x2800 100A	0x000
		0x71	RAM[AB]←OUT	Next-Address	R/W_=0	0x10	0x0000 0000	0x110
	DEX	0x72	X←ALU←Mux←X P(NZ)	Next-Address	Mux=5,ALU=A,Xw CF=1	0x10	0x2008 105A	0x110
	INC	0x73	OUT←ALU←Mux ←RAM[AB],P(NZ)	CAR++	Mux=0,ALU=8,OUTw CF=1	-	0x2800 1008	0x000
		0x74	RAM[AB]←OUT	Next-Address	R/W_=0	0x10	0x0000 0000	0x110
	NOP	0x75	-	Next-Address	-	0x10	0x2000 0000	0x110
	CPX	0x76	TMP←ALU←Acc	CAR++	ALU=6,TMPw	-	0x2020 0006	0x000
		0x77	Acc←ALU←Mux←X	CAR++	Mux=5,ALU=9,Accw	-	0x2004 0059	0x000
		0x78	ALU←Mux←RAM[AB] P(NZC)	CAR++	Mux=0,ALU=F CF=2	-	0x2000 200F	0x000
		0x79	Acc←ALU←Mux←TMP	Next-Address	Mux=7,ALU=9,Accw	0x10	0x2004 0079	0x110
	INX	0x7A	X←ALU←Mux←X P(NZ)	Next-Address	Mux=5,ALU=8,Xw CF=1	0x10	0x2008 1058	0x110
	SED	0x7B	P(D←1)	Next-Address	CF=4,F=3	0x10	0x2001 C000	0x110
	CPY	0x7C	TMP←ALU←Acc	CAR++	ALU=6,TMPw	-	0x2020 0006	0x000
		0x7D	Acc←ALU←Mux←Y	CAR++	Mux=6,ALU=9,Accw	-	0x2004 0069	0x000
		0x7E	ALU←Mux←RAM[AB] P(NZC)	CAR++	Mux=0,ALU=F CF=2	-	0x2000 200F	0x000
		0x7F	Acc←ALU←Mux←TMP	Next-Address	Mux=7,ALU=9,Accw	0x10	0x2004 0079	0x110
	INY	0x80	Y←ALU←Mux←Y P(NZ)	Next-Address	Mux=6,ALU=8,Yw CF=1	0x10	0x2010 1068	0x110
	CLD	0x81	P(D←0)	Next-Address	CF=5,F=3	0x10	0x2001 D000	0x110
	LDY	0x82	Y←ALU←Mux ←RAM[AB],P(NZ)	Next-Address	Mux=0,ALU=9,Yw CF=1	0x10	0x2010 1009	0x110
	TAY	0x83	Y←ALU←Acc P(NZ)	Next-Address	ALU=6,Yw CF=1	0x10	0x2010 1006	0x110
	CLV	0x84	P(V←0)	Next-Address	CF=5,F=6	0x10	0x2003 5000	0x110
	STY	0x85	OUT←ALU←Mux←Y	CAR++	Mux=6,ALU=9,OUTw	-	0x2800 0069	0x000
		0x86	RAM[AB]←OUT	Next-Address	R/W_=0	0x10	0x0000 0000	0x110
	DEY	0x87	Y←ALU←Mux←Y P(NZ)	Next-Address	Mux=6,ALU=A,Yw CF=1	0x10	0x2010 106A	0x110
	TYA	0x88	Acc←ALU←Mux←Y	Next-Address	Mux=6,ALU=9,Accw CF=1	0x10	0x2004 1069	0x110
	PLA	0x89	SP←ALU←Mux←SP	CAR++	Mux=3,ALU=8,SPw	-	0x2040 0038	0x000
		0x8A	AB←MU	CAR++	MU=1,ABw	-	0x2400 0080	0x000
		0x8B	Acc←ALU←Mux ←RAM[AB],P(NZ)	Next-Address	Mux=0,ALU=9,Accw CF=1	0x10	0x2004 1009	0x110
	JMP (indirect)	0x8C	PC-lo←ALU←Mux ←RAM[AB]	CAR++	Mux=0,ALU=9,PC-lw	-	0x2080 0009	0x000
		0x8D	AB-lo++	CAR++	MU=2	-	0x2000 0100	0x000
		0x8E	PC-hi←ALU←Mux ←RAM[AB]	Next-Address	Mux=0,ALU=9,PC-hw	0x10	0x2100 0009	0x110

Instruction OpCode								
	JMP (absolute)	0x8F	AB←MU←PC,PC++	CAR++	MU=0,ABw,PC++	-	0x3400 0000	0x000
		0x90	TMP←ALU←Mux ←RAM[AB]	CAR++	Mux=0,ALU=9,TMPw	-	0x2020 0009	0x000
		0x91	AB←MU←PC	CAR++	MU=0,ABw	-	0x2400 0000	0x000
		0x92	PC-lo←ALU←Mux ←TMP	CAR++	Mux=7,ALU=9,PC-lw	-	0x2080 0079	0x000
		0x93	PC-hi←ALU←Mux ←RAM[AB]	Next-Address	Mux=0,ALU=9,PC-hw	0x10	0x2100 0009	0x110
	CLI	0x94	P(I←0)	Next-Address	CF=5,F=2	0x10	0x2001 5000	0x110
	SEI	0x95	P(I←1)	Next-Address	CF=4,F=2	0x10	0x2001 4000	0x110
	CLC	0x96	P(C←0)	Next-Address	CF=5,F=0	0x10	0x2000 5000	0x110
	SEC	0x97	P(C←1)	Next-Address	CF=4,F=0	0x10	0x2000 4000	0x110
	PLP	0x98	SP←ALU←Mux←SP	CAR++	Mux=3,ALU=8,SPw	-	0x2040 0038	0x000
		0x99	AB←MU	CAR++	MU=1,ABw	-	0x2400 0080	0x000
		0x9A	P←ALU←Mux ←RAM[AB],P(all flags)	Next-Address	Mux=0,ALU=9,CF=7	0x10	0x2000 7009	0x110
	PHA	0x9B	AB←MU OUT←ALU←Acc	CAR++	MU=1,ABw ALU=6,OUTw	-	0x2C00 0086	0x000
		0x9C	SP←ALU←Mux←SP RAM[AB]←OUT	Next-Address	Mux=3,ALU=A,SPw R/W_=0	0x10	0x0040 003A	0x110
	PHP	0x9D	AB←MU OUT←ALU←Mux←P	CAR++	MU=1,ABw Mux=4,ALU=9,OUTw	-	0x2C00 00C9	0x000
		0x9E	SP←ALU←Mux←SP RAM[AB]←OUT	Next-Address	Mux=3,ALU=A,SPw R/W_=0	0x10	0x0040 003A	0x110
	BIT	0x9F	ALU←Mux←RAM[AB] P(NZ)	CAR++	Mux=0,ALU=1 CF=1	-	0x2000 1001	0x000
		0xA0	ALU←Mux←RAM[AB] P(N←M7,V←M6)	Next-Address	ALU=9 CF=6	0x10	0x2000 6009	0x110
	JSR	0xA1	AB←MU←PC,PC++	CAR++	MU=0,ABw,PC++	-	0x3400 0000	0x000
		0xA2	TMP←ALU←Mux ←RAM[AB]	CAR++	Mux=0,ALU=9,TMPw	-	0x2020 0009	0x000
		0xA3	AB←MU OUT←ALU←Mux←PC-hi	CAR++	MU=1,ABw Mux=1,ALU=9,OUTw	-	0x2C00 0099	0x000
		0xA4	SP←ALU←Mux←SP RAM[AB]←OUT	CAR++	Mux=3,ALU=A,SPw R/W_=0	-	0x0040 003A	0x000
		0xA5	AB←MU OUT←ALU←Mux←PC-lo	CAR++	MU=1,ABw Mux=2,ALU=9,OUTw	-	0x2C00 00A9	0x000
		0xA6	SP←ALU←Mux←SP RAM[AB]←OUT	CAR++	Mux=3,ALU=A,SPw R/W_=0	-	0x0040 003A	0x000
		0xA7	AB←MU←PC	CAR++	MU=0,ABw	-	0x2400 0000	0x000
		0xA8	PC-lo←ALU←Mux ←TMP	CAR++	Mux=7,ALU=9,PC-lw	-	0x2080 0079	0x000
		0xA9	PC-hi←ALU←Mux ←RAM[AB]	Next-Address	Mux=0,ALU=9,PC-hw	0x10	0x2100 0009	0x110
	RTS	0xAA	SP←ALU←Mux←SP	CAR++	Mux=3,ALU=8,SPw	-	0x2040 0038	0x000
		0xAB	AB←MU	CAR++	MU=1,ABw	-	0x2400 0080	0x000
		0xAC	PC-lo←ALU←Mux ←RAM[AB]	CAR++	Mux=0,ALU=9,PC-lw	-	0x2080 0009	0x000
		0xAD	SP←ALU←Mux←SP	CAR++	Mux=3,ALU=8,SPw	-	0x2040 0038	0x000
		0xAE	AB←MU	CAR++	MU=1,ABw	-	0x2400 0080	0x000
		0xAF	PC-hi←ALU←Mux ←RAM[AB]	CAR++	Mux=0,ALU=9,PC-hw	-	0x2100 0009	0x000
		0xB0	PC++	Next-Address	PC++	0x10	0x3000 0000	0x110

Instruction OpCode	RTI	0xB1	SP←ALU←Mux←SP	CAR++	Mux=3,ALU=8,SPw	-	0x2040 0038	0x000
		0xB2	AB←MU	CAR++	MU=1,ABw	-	0x2400 0080	0x000
		0xB3	P←ALU←Mux ←RAM[AB],P(all flags)	CAR++	Mux=0,ALU=9,CF=7	-	0x2000 7009	0x000
		0xB4	SP←ALU←Mux←SP	CAR++	Mux=3,ALU=8,SPw	-	0x2040 0038	0x000
		0xB5	AB←MU	CAR++	MU=1,ABw	-	0x2400 0080	0x000
		0xB6	PC-lo←ALU←Mux ←RAM[AB]	CAR++	Mux=0,ALU=9,PC-lw	-	0x2080 0009	0x000
		0xB7	SP←ALU←Mux←SP	CAR++	Mux=3,ALU=8,SPw	-	0x2040 0038	0x000
		0xB8	AB←MU	CAR++	MU=1,ABw	-	0x2400 0080	0x000
		0xB9	PC-hi←ALU←Mux ←RAM[AB]	Next-Address	Mux=0,ALU=9,PC-hw	0x10	0x2100 0009	0x110
	BRK	0x00	AB←MU,brk OUT←ALU←Mux←PC-hi	CAR++	MU=1,ABw,brk Mux=1,ALU=9,OUTw	-	0x2C00 0499	0x000
		0x01	SP←ALU←Mux←SP RAM[AB]←OUT	CAR++	Mux=3,ALU=A,SPw R/W_=0	-	0x0040 003A	0x000
		0x02	AB←MU OUT←ALU←Mux←PC-lo	CAR++	MU=1,ABw Mux=2,ALU=9,OUTw	-	0x2C00 00A9	0x000
		0x03	SP←ALU←Mux←SP RAM[AB]←OUT	CAR++	Mux=3,ALU=A,SPw R/W_=0	-	0x0040 003A	0x000
		0x04	AB←MU OUT←ALU←Mux←P	CAR++	MU=1,ABw Mux=4,ALU=9,OUTw	-	0x2C00 00C9	0x000
		0x05	SP←ALU←Mux←SP RAM[AB]←OUT	CAR++	Mux=3,ALU=A,SPw R/W_=0	-	0x0040 003A	0x000
		0x06	MU←Interrupt	CAR++	MU=4	-	0x2000 0200	0x000
		0x07	MU←Interrupt	CAR++	MU=5	-	0x2000 0280	0x000
		0x08	AB←MU,brk	CAR++	MU=3,ABw,brk	-	0x2400 0580	0x000
		0x09	PC-lo←ALU←Mux ←RAM[AB],brk	CAR++	Mux=0,ALU=9,PC-lw brk	-	0x2080 0409	0x000
		0x0A	MU←Interrupt	CAR++	MU=4	-	0x2000 0200	0x000
		0x0B	MU←Interrupt	CAR++	MU=5	-	0x2000 0280	0x000
		0x0C	AB←MU P(I←1)	CAR++	MU=3,ABw CF=4,F=2	-	0x2401 4180	0x000
		0x0D	PC-hi←ALU←Mux ←RAM[AB]	Next-Address	Mux=0,ALU=9,PC-hw	0x10	0x2100 0009	0x110
		0x0E	PC++	Next-Address	PC++	0x00	0x3000 0000	0x100

Notes :

- SYNC signal is active only in the first cycle of the Fetch sequence.
- R/W signal is active while reading from the memory and low on writing, it is almost all the time active.