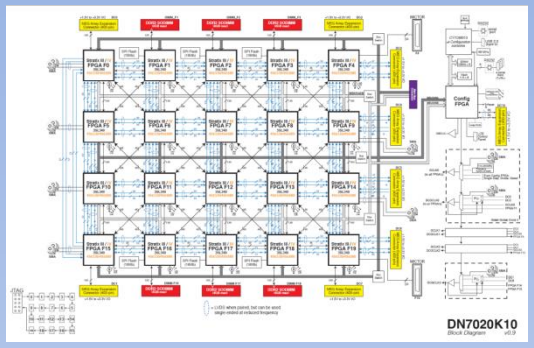
# VHDL programmering för inbyggda system

## **Välkommen**




- Debugging Tools – SignalTap II Embedded Logic Analyze
- What is a glitch?
- Timing mode accuracy
- How Does it Work?
- SignalTap II Design Flow
- Dokumentation: http://www.altera.com/literature/hb/qts/qts_qii53009.pdf

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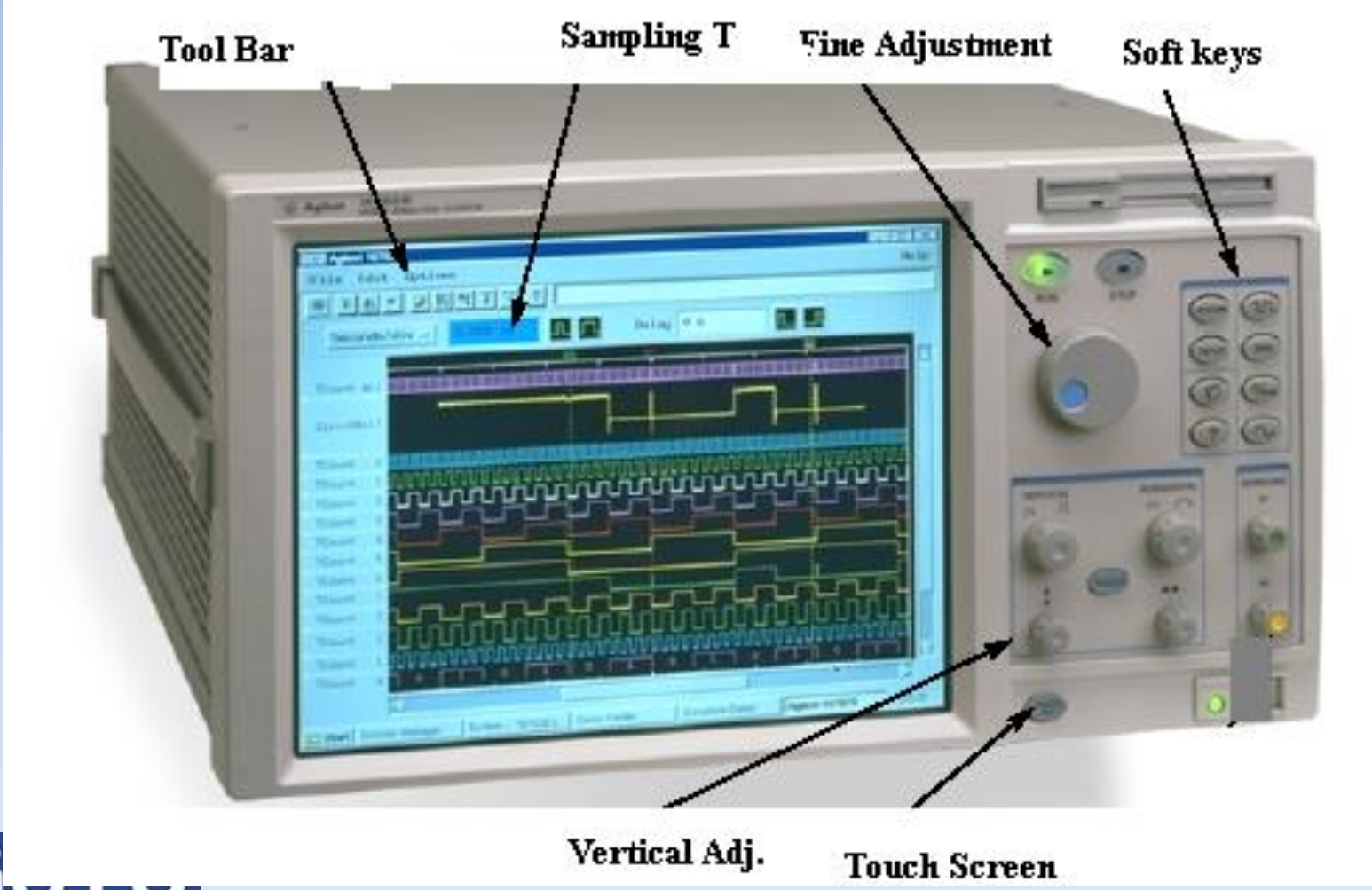
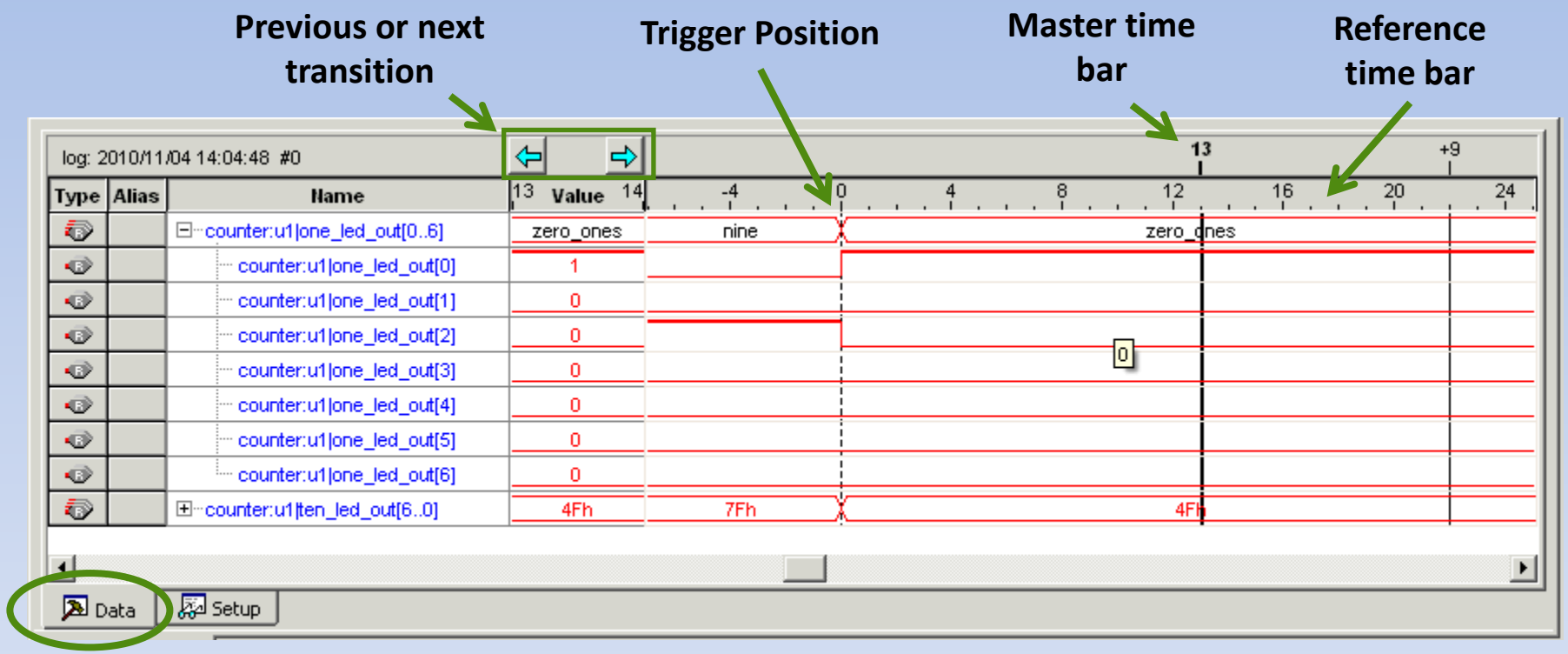
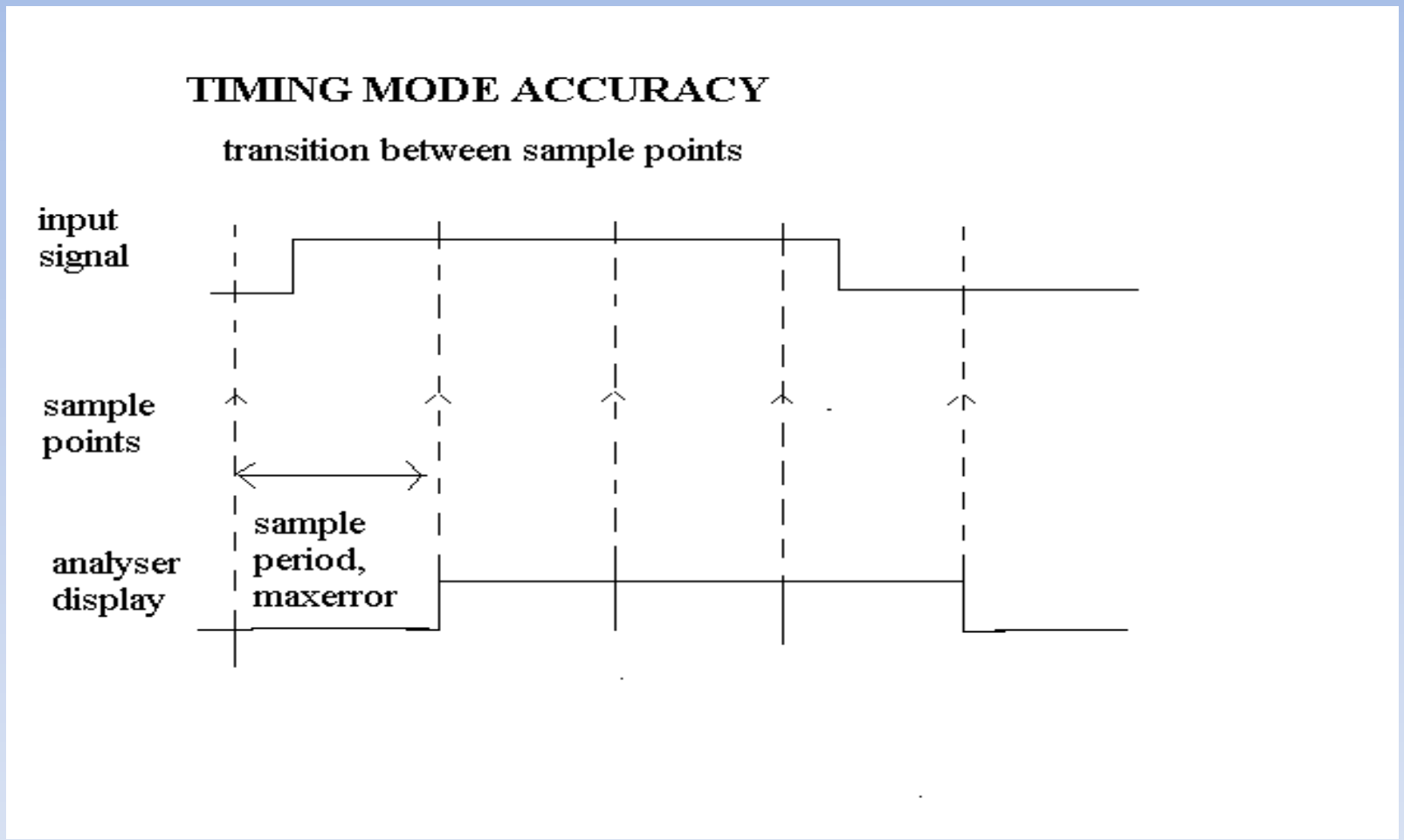
# Logik Analysator



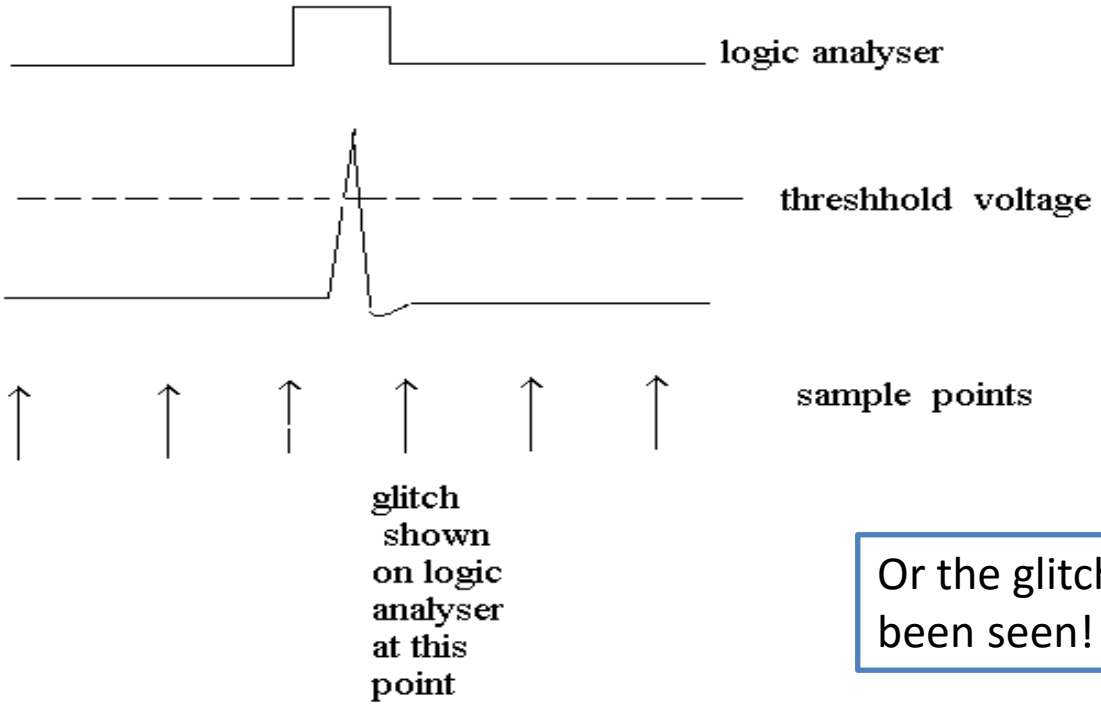
# SignalTap II Embedded Logic Analyzer



# Timing mode accuracy



# What is a glitch?




Or the glitch will not been seen!

# SignalTap II ELA Agenda

- **SignalTap II ELA overview & features**
- Using SignalTap II ELA interface
- ELA = Embedded Logic Analyzer

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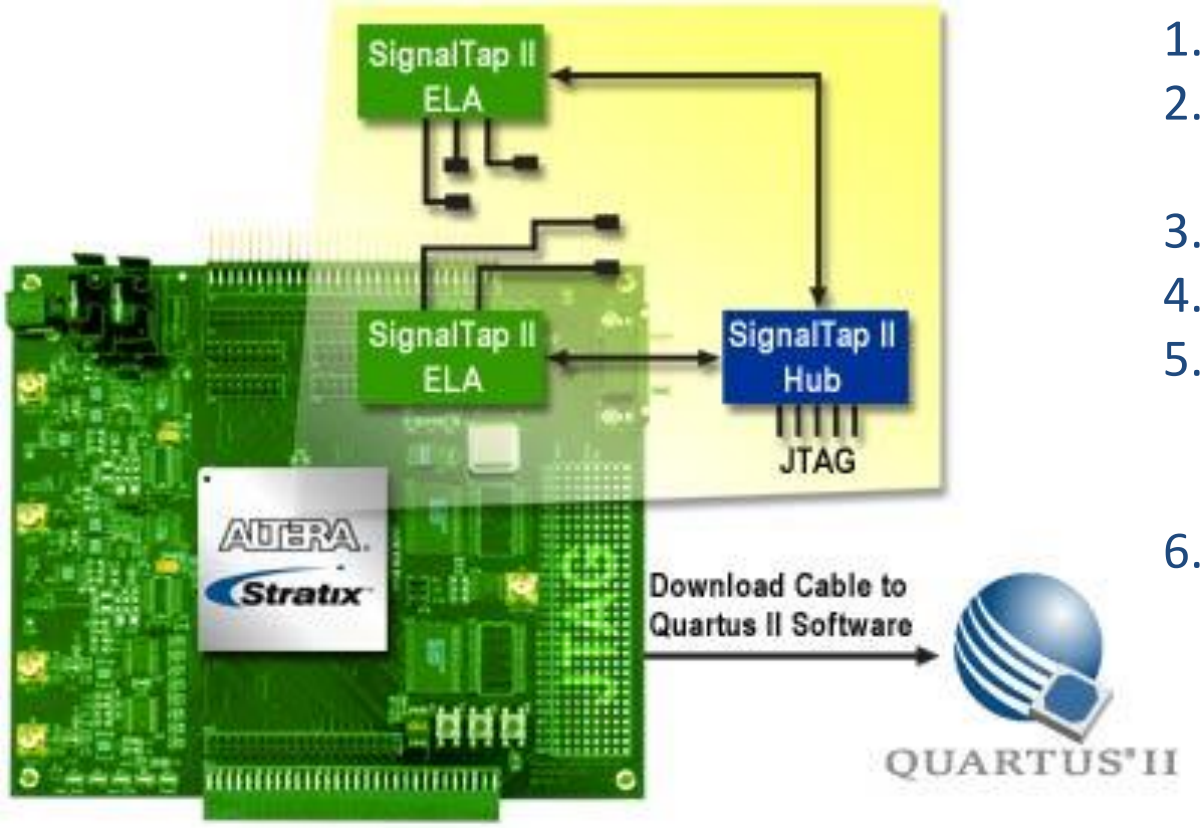
# How Does it Work?




1. Configure ELA
2. Download ELA into FPGA along with design
3. Start running ELA
4. Defined trigger event(s)
5. Samples and stores internal signal states in device memory
6. Captured samples transferred to Quartus II software through JTAG

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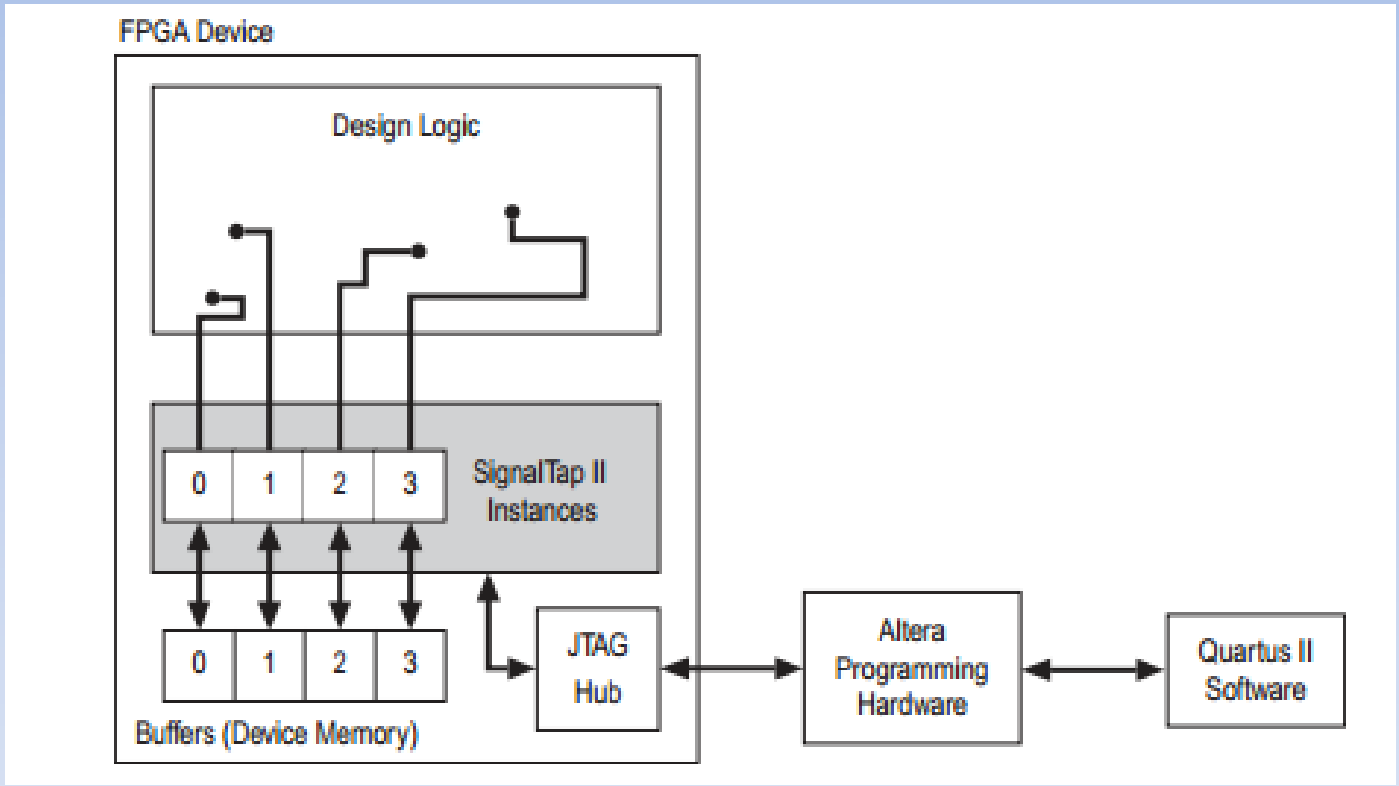
# How Does it Work?



# ELA Resource Utilization

- Logic elements
  - Number of channels
  - Trigger levels
- Memory block count
  - Number of channels
  - Sample depth
  - Selectable trade-off between depth & number of channels
  - 128K sample depth with 1024 channels not practical – 32,768 M4K blocks
- Estimated resource usage displayed and update during SignalTap II configuration

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# SignalTap II Agenda

- SignalTap II ELA overview & features
- **Using SignalTap II ELA interface**

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# Using STP File

1. Create .STP file
   - Assign sample clock
   - Specify sample depth
   - Assign signals to STP file
   - Specify triggering conditions and flow
   - Specify storage qualifier(s) (optional)
   - Setup JTAG
2. Save .STP file & compile with design
3. Program device
4. Acquire data

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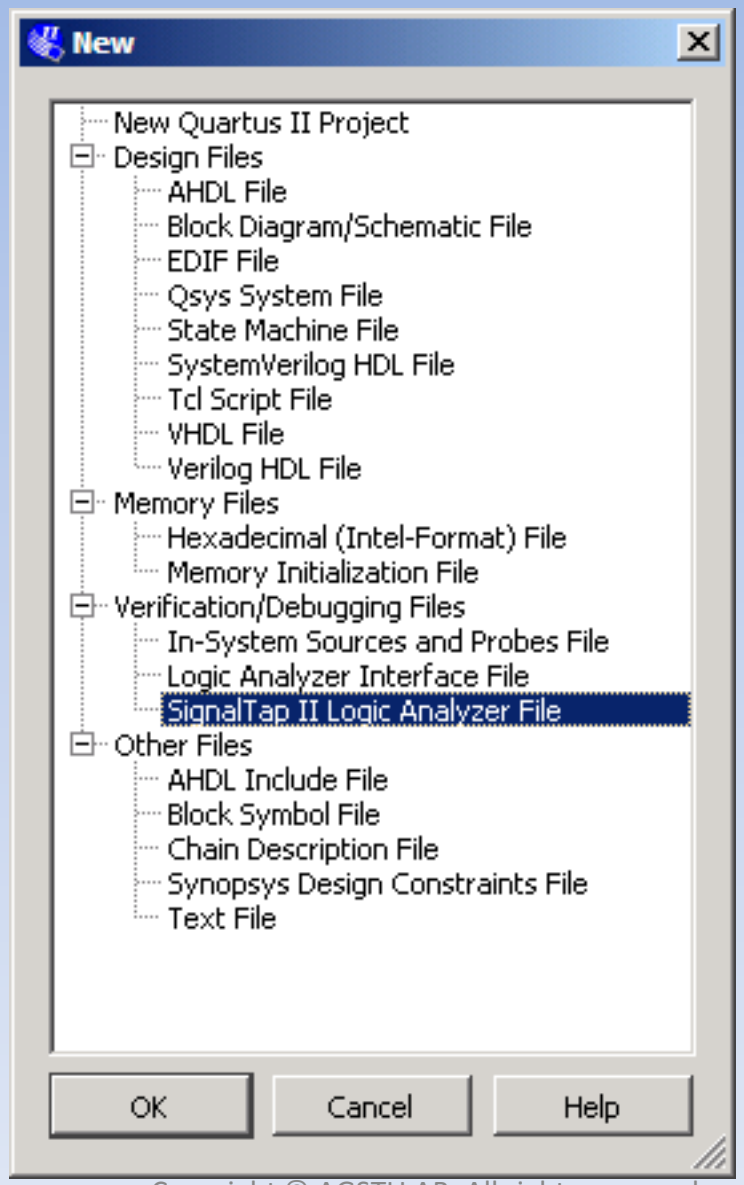
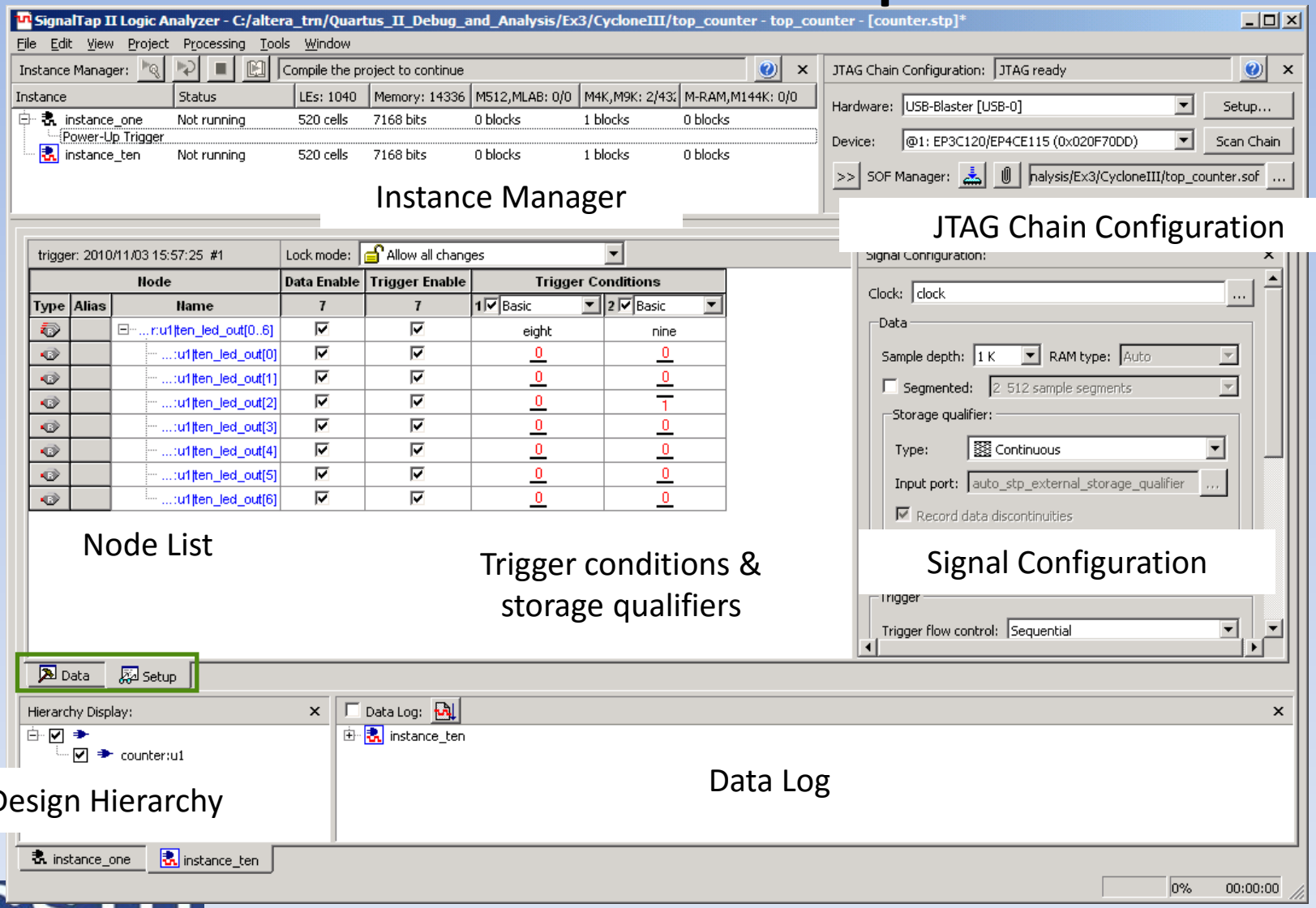
# 1) Create a New .STP File

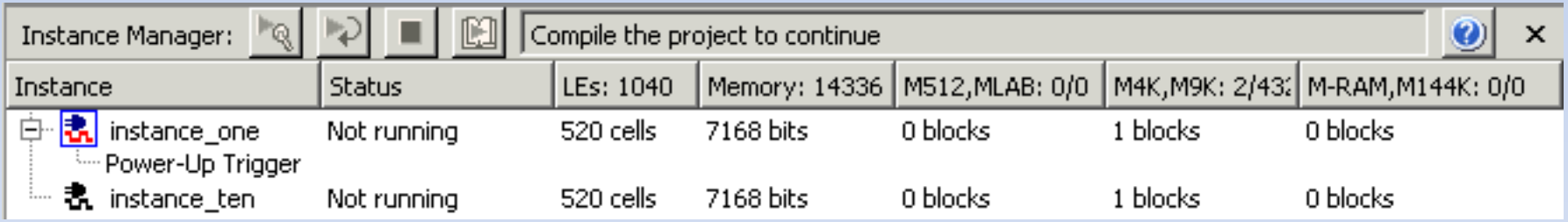


# Main .STP File Components



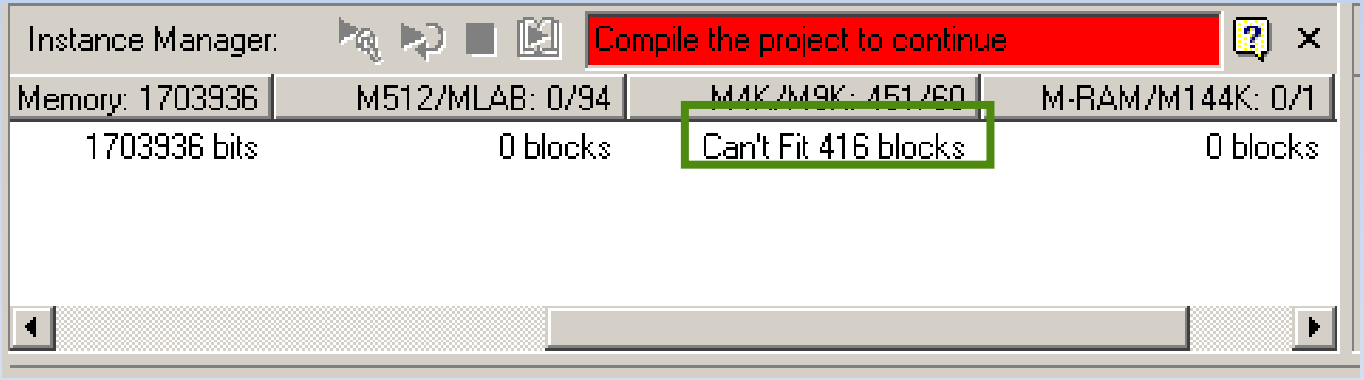
# Instance Manager

- Create new instances (right-click)
- Displays the current status of each instance
- Run and control instances



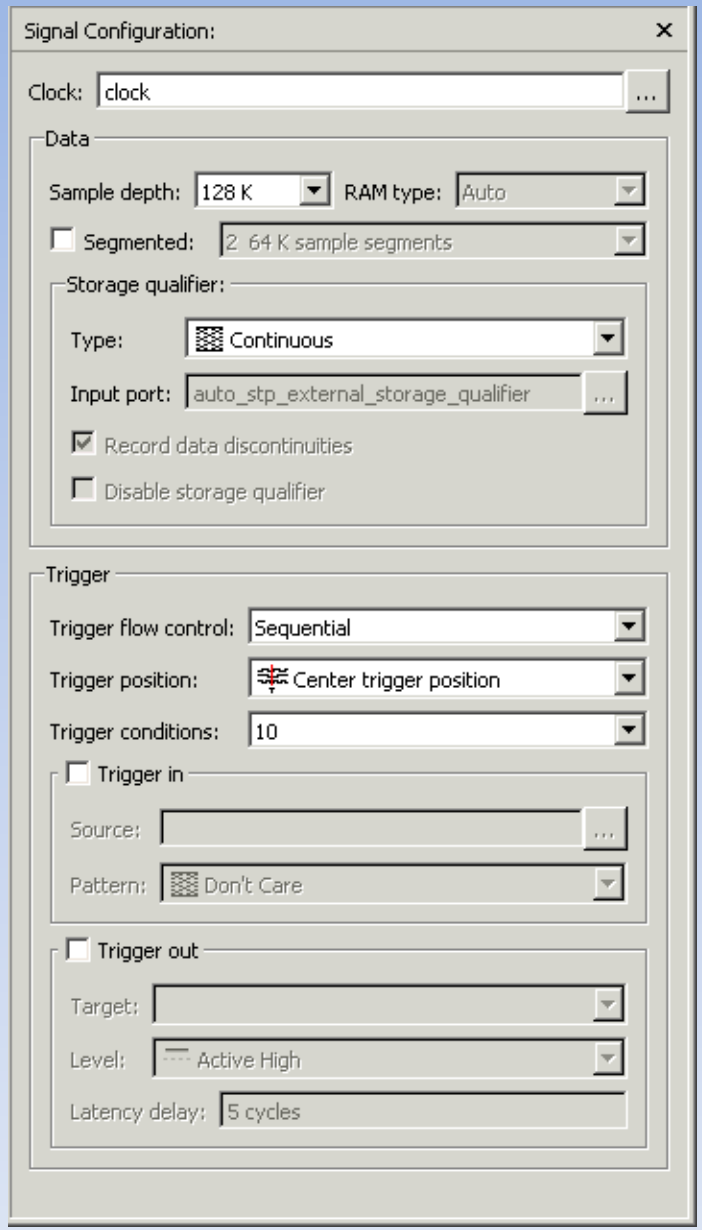
# Fitting Prediction

- Predict whether current configuration can fit before lengthy compilation



# Signal Configuration

- Manages data capture & signal configuration
  - Sample clock
  - Sample depth
  - Buffer type
  - Storage qualification
  - Trigger flow
  - Trigger position
  - Trigger-in & trigger-out
- Settings similar to external test equipment

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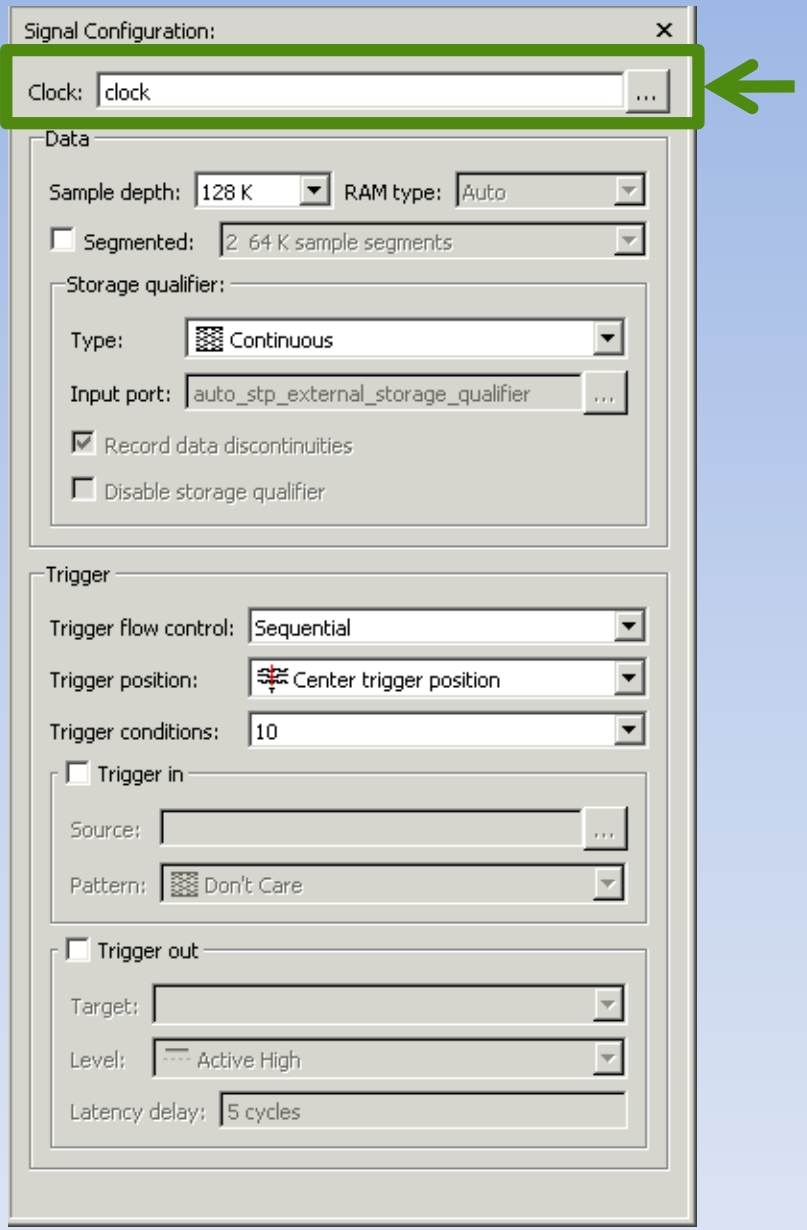
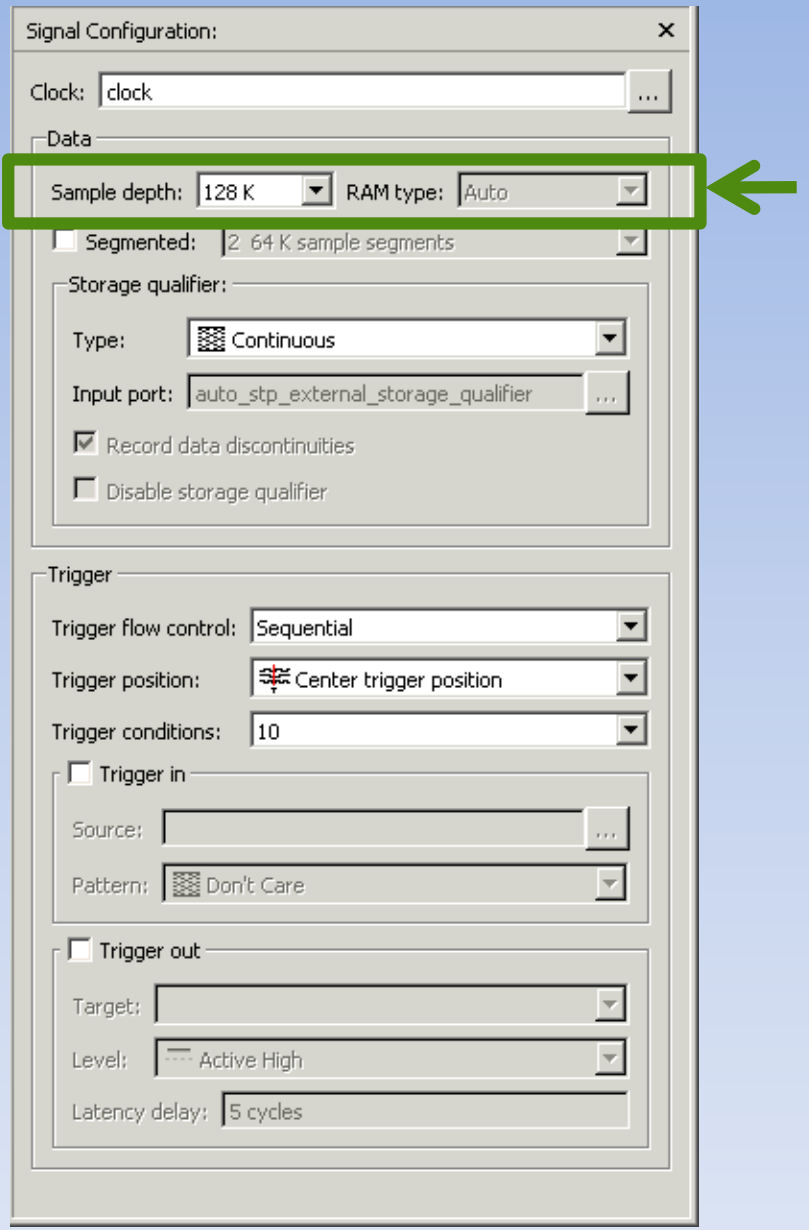
# Sample Clock



# Sample Depth

- Sample depth
  - 0 to 128K sample depth
- Select RAM type for supported FPGAs
  - Defaults to Auto on unsupported device families

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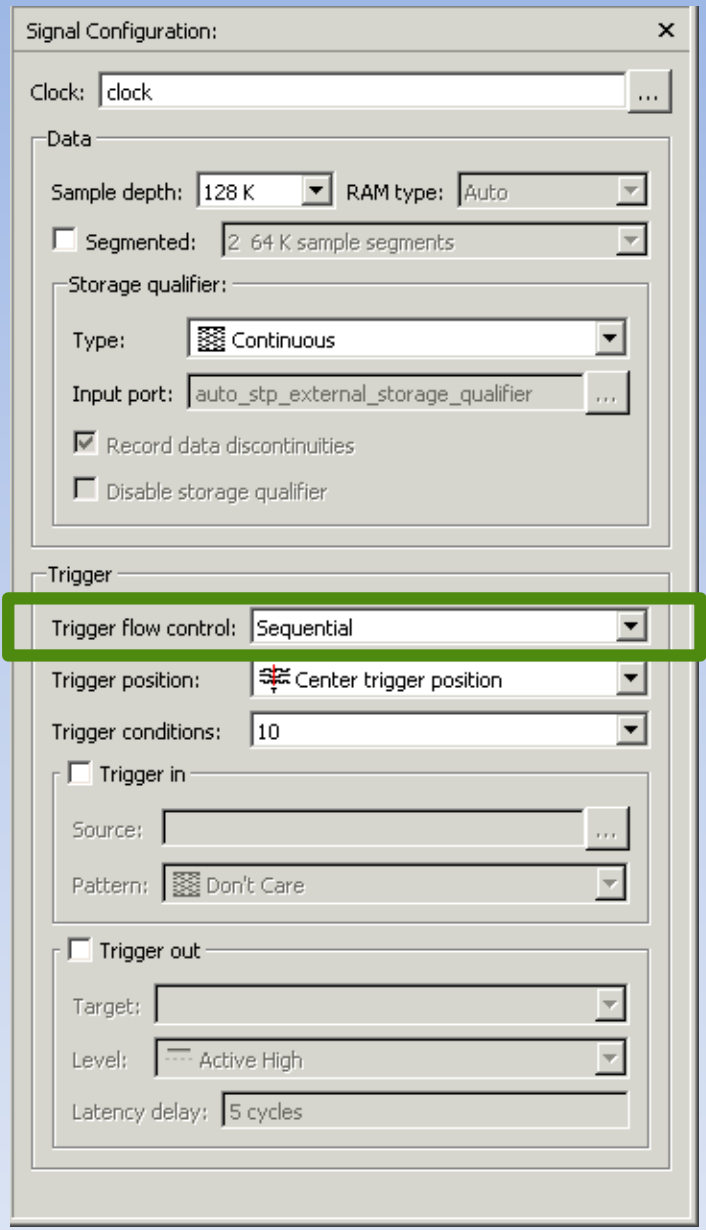
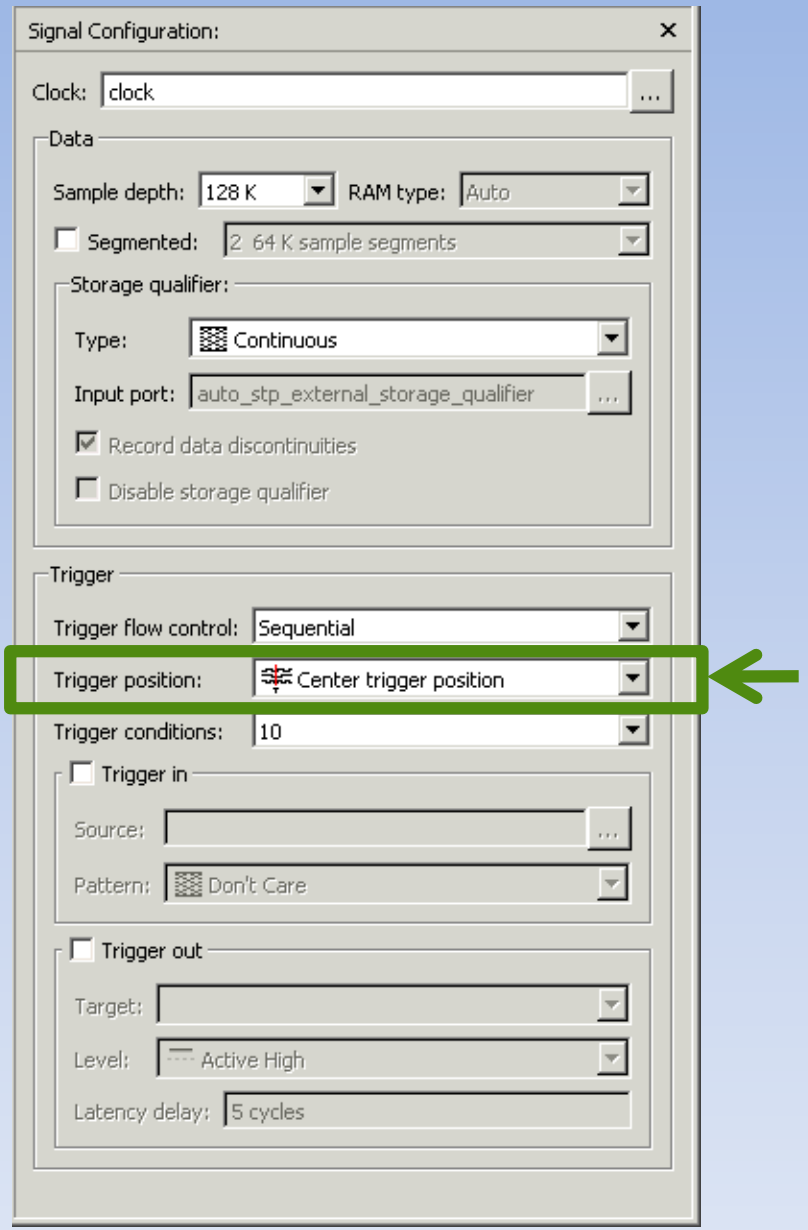
# Trigger Flow Control

- Sequential
  - Trigger conditions evaluated in numerical order
  - Trigger in (condition “0”) followed by conditions 1, 2, 3, etc.
  - Buffer or 1st buffer segment filled on final condition
  - Subsequent segments filled only when final condition reoccurs



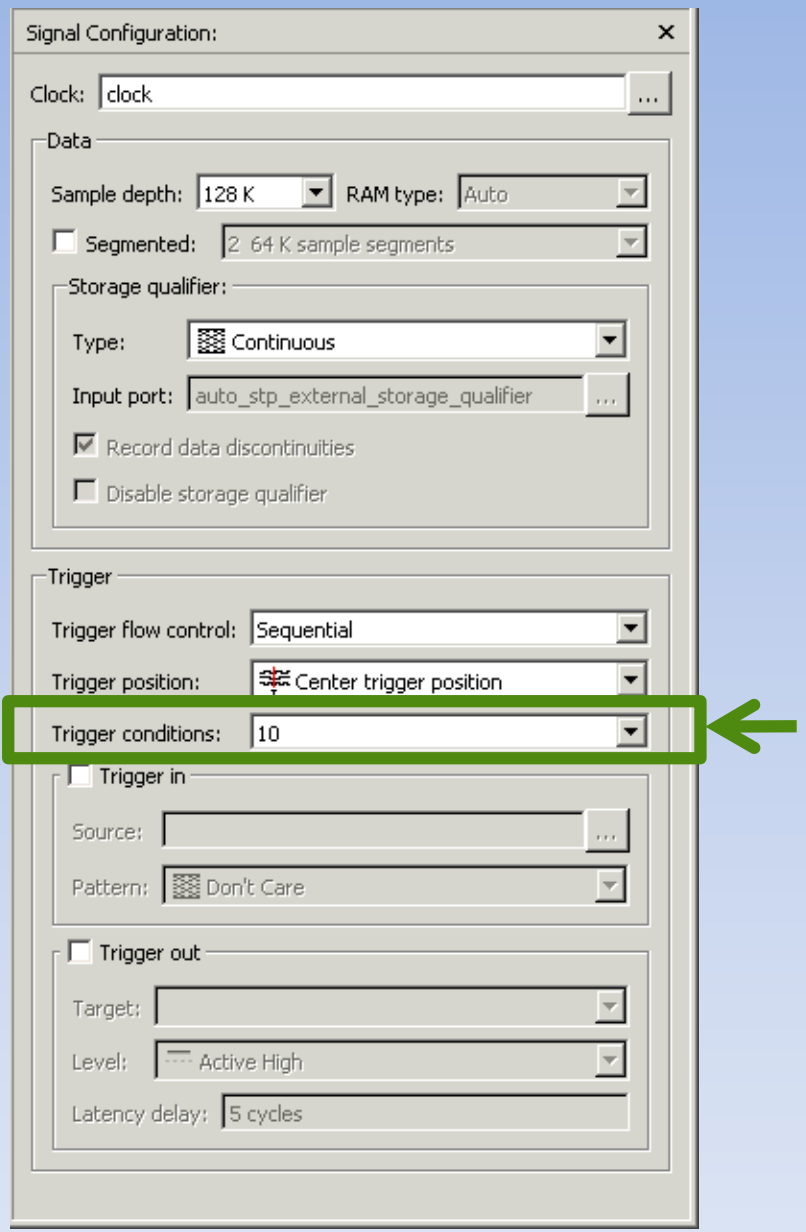
# Trigger Position

- Location in buffer (or buffer segment) where trigger sample located
- Three default positions
  - Pre (12% before trigger, 88% after)
  - Center (50% before, 50% after)
  - Post (88% before, 12% after)



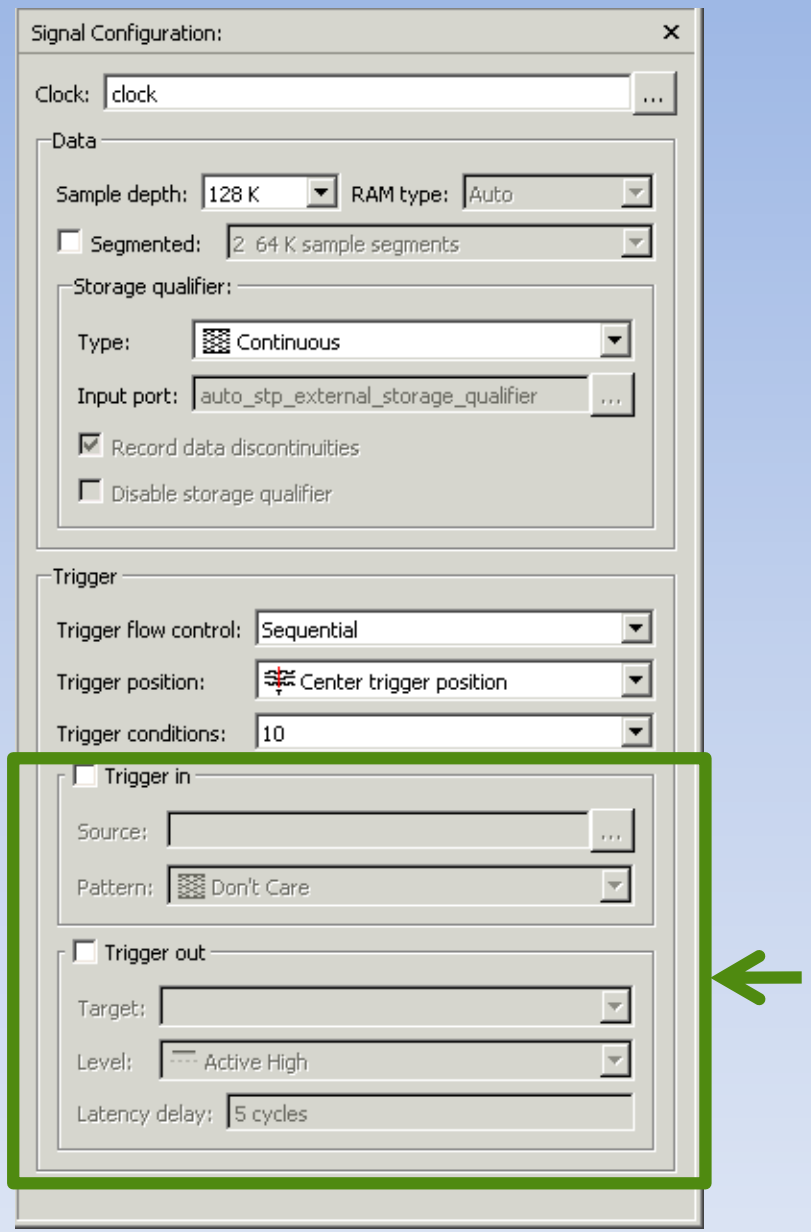
# Trigger Conditions

- Create up to 10 trigger conditions for each SignalTap II instance
- Conditions appear as separate columns in node list
- Order and analysis of conditions depends on flow control setting

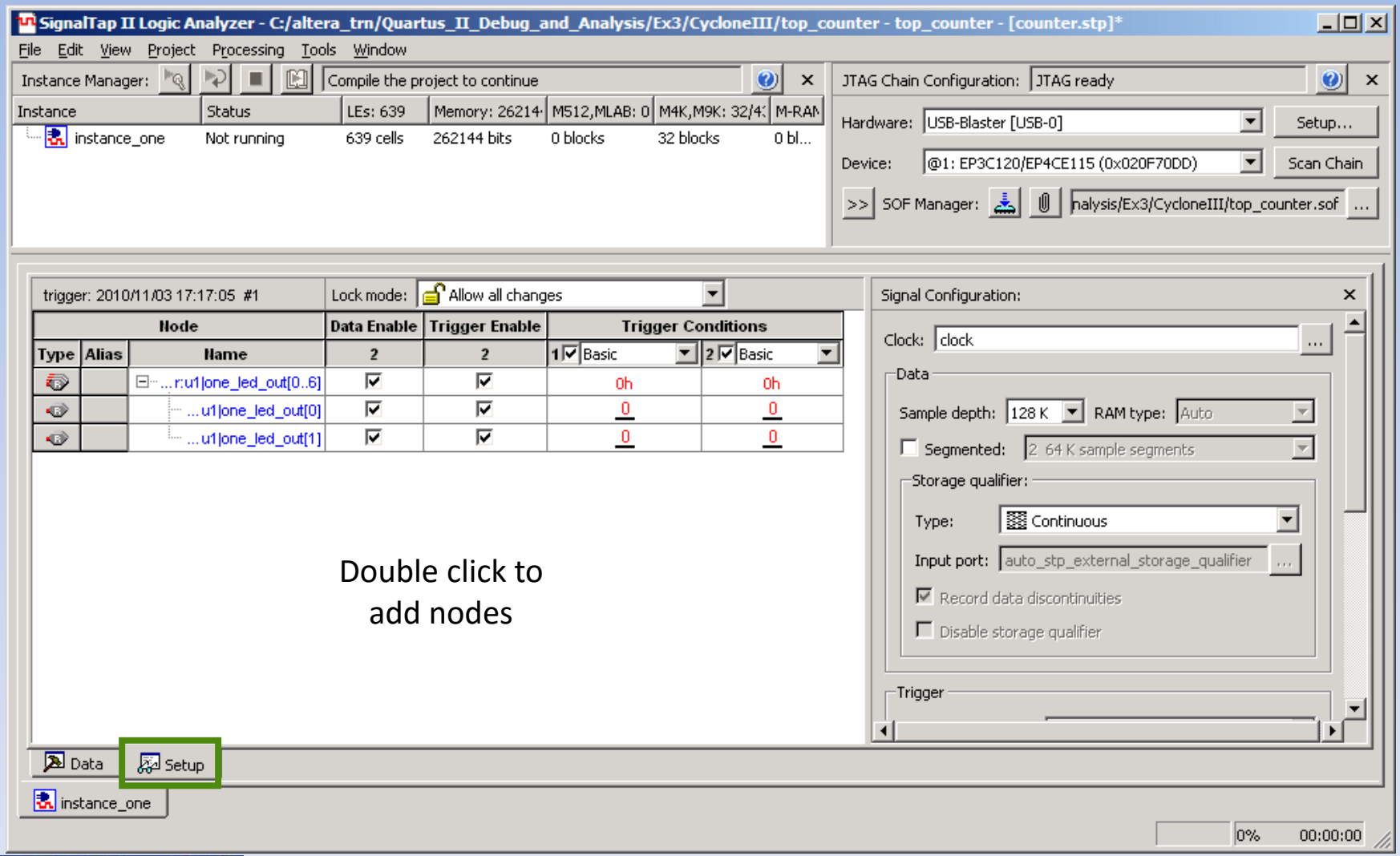


# Trigger In & Out

- Interface SignalTap II ELA with other devices



# Main .STP File Components



# Set Up Node List

- Add signals to Node List by double-clicking
- Two filters available in Node Finder
  - SignalTap II: Pre-Synthesis: Nodes available after analysis & elaboration, but before synthesis
  - SignalTap II: Post-Fitting: Nodes available after Fitter optimizations and place-and-route

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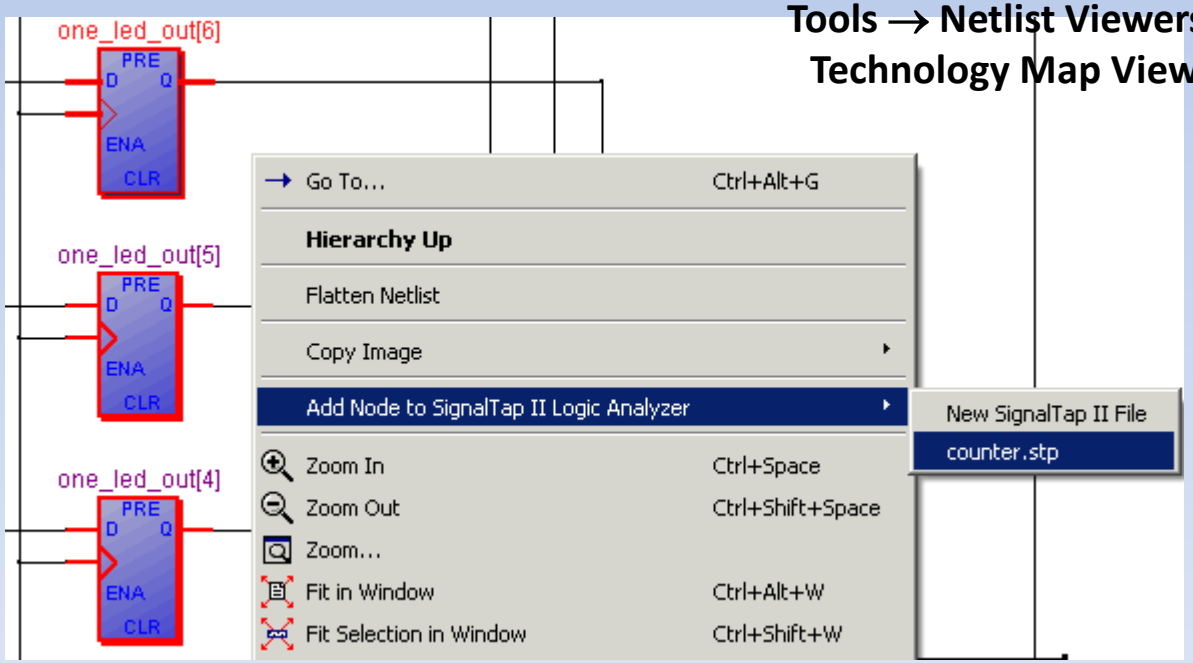
# Tapping from Technology Map Viewer

- Select nodes in Technology Map Viewer (Post Fitting)
- Quickly add to new or existing SignalTap file

**Tools → Netlist Viewers → Technology Map Viewer**

**Select and right-click on nodes**

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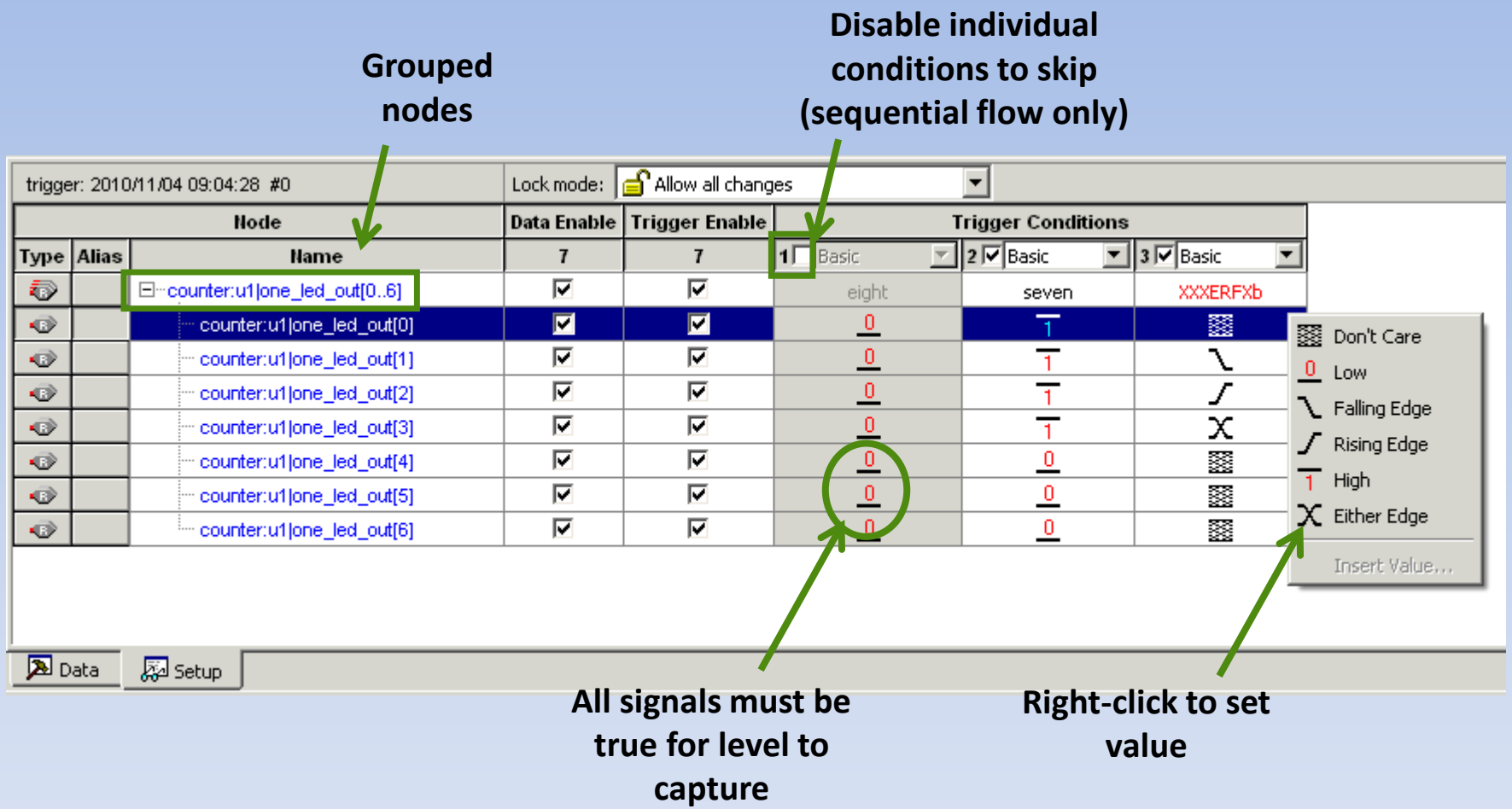
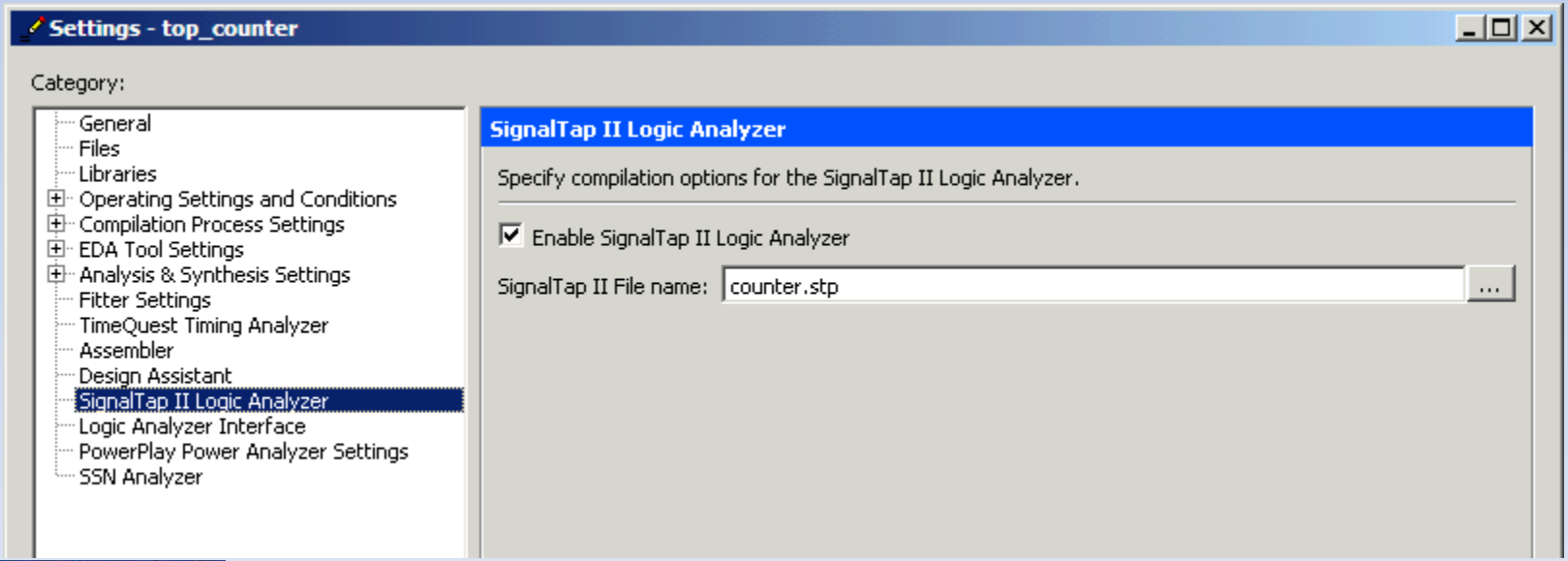
# Basic Triggering



# 2) Save .STP File & Compile

- SignalTap II Logic Analyzer control in Settings
  - **Assignments** menu → **Settings**
  - Specify the SignalTap II file to compile with project

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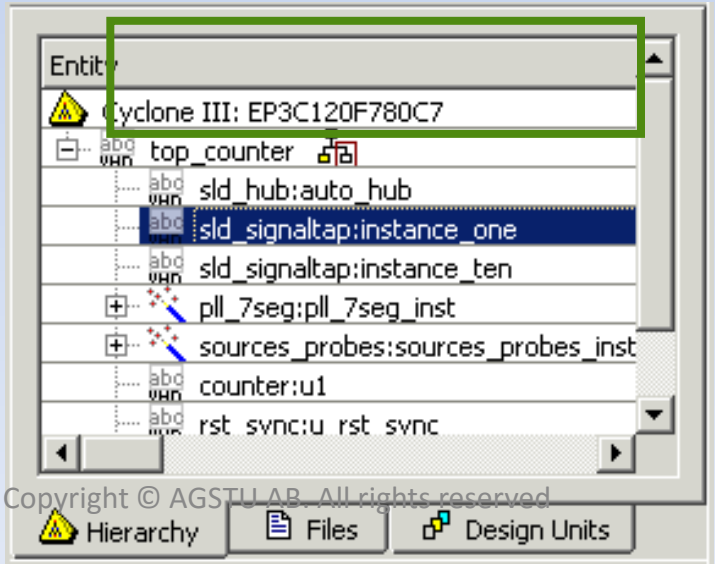
# Compile Project with SignalTap II ELA

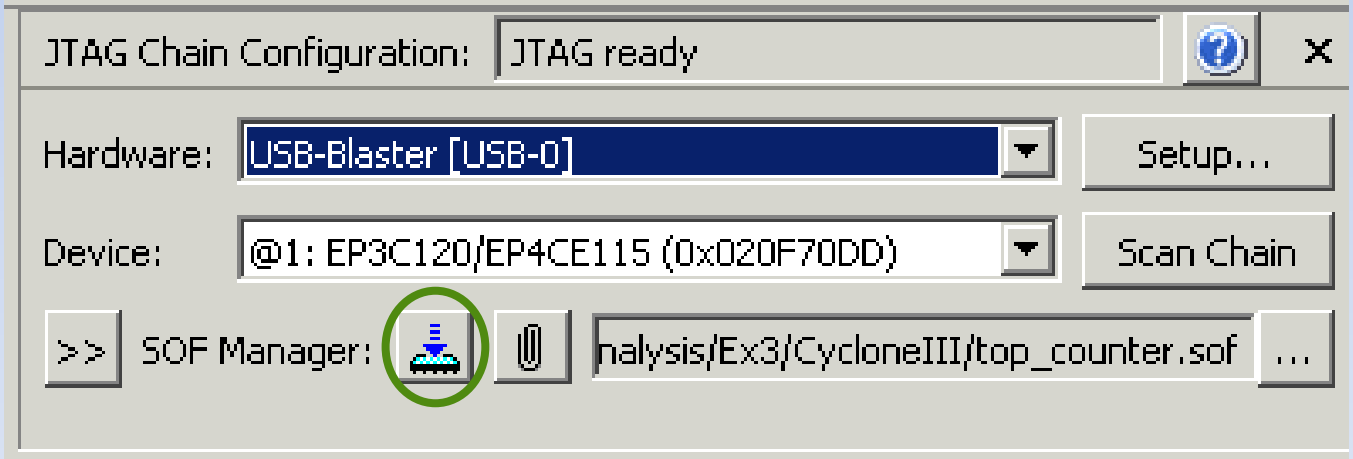
- Full compilation (Processing menu → Start Compilation) to integrate ELA into design

- sld_signaltap and sld_hub added to project to implement logic analyzer and JTAG hub connection



# 3) Program Device(s)

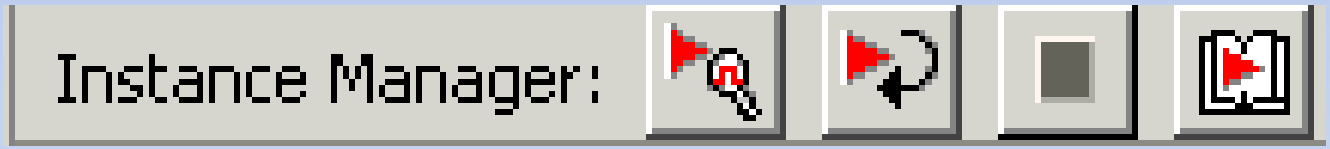
- Use Quartus II Programmer or SignalTap II file
  - Program button in the SignalTap II interface only configures the selected device in chain
  - Use Quartus II Programmer to program multiple devices
    - Can create a separate SignalTap II file for each device in the JTAG chain



# 4) Acquire Data

**Run Analysis**
**Run SignalTap II until trigger event occurs or logic analyzer stopped; multiple selected instances run simultaneously**

**Stop Analysis**
**Stops the logic analyzer; no data transferred if trigger event did not occur**




**Autorun Analysis**
**Run SignalTap II until logic analyzer is stopped, ignored trigger events**

**Read data**
**Transfers data currently stored in buffer to SignalTap file even if trigger event did not occur**

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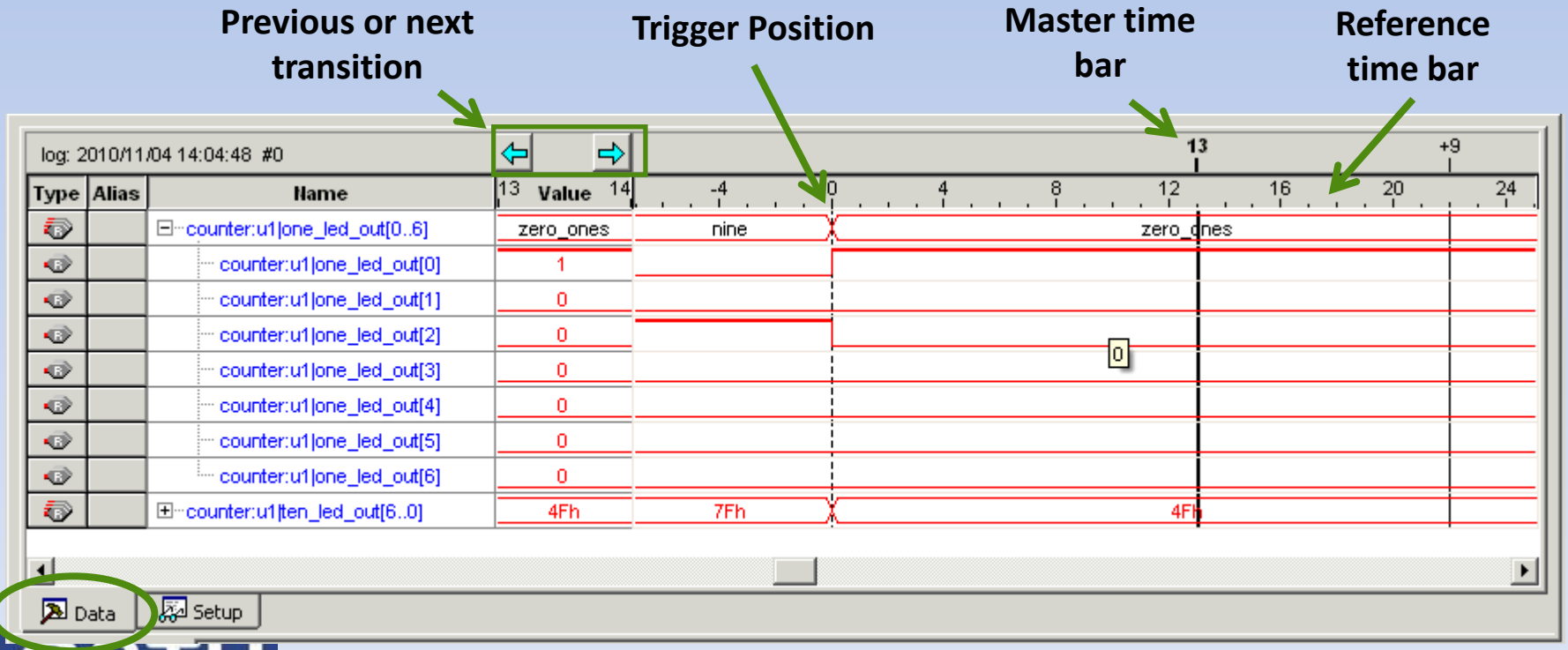
# Displaying Acquired Data (1)

- Display signal groups as standard waveforms in selected radix or as a bar or line chart



Dokumentation som kan vara bra att ha:
http://www.altera.com/literature/hb/qts/qts_qii53009.pdf
http://en.wikipedia.org/wiki/Logic_analyzer
ftp://ftp.altera.com/up/pub/Tutorials/DE2/Digital_Logic/tut_signaltapII_vhdlDE2.pdf