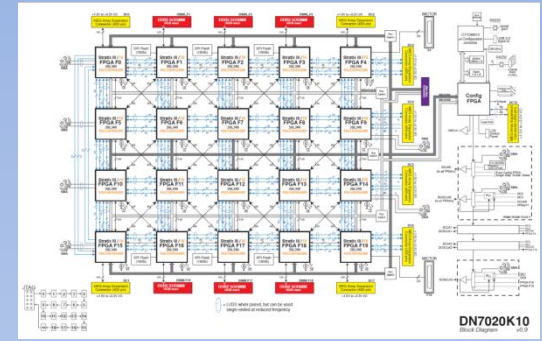


VHDL programmering för inbyggda system

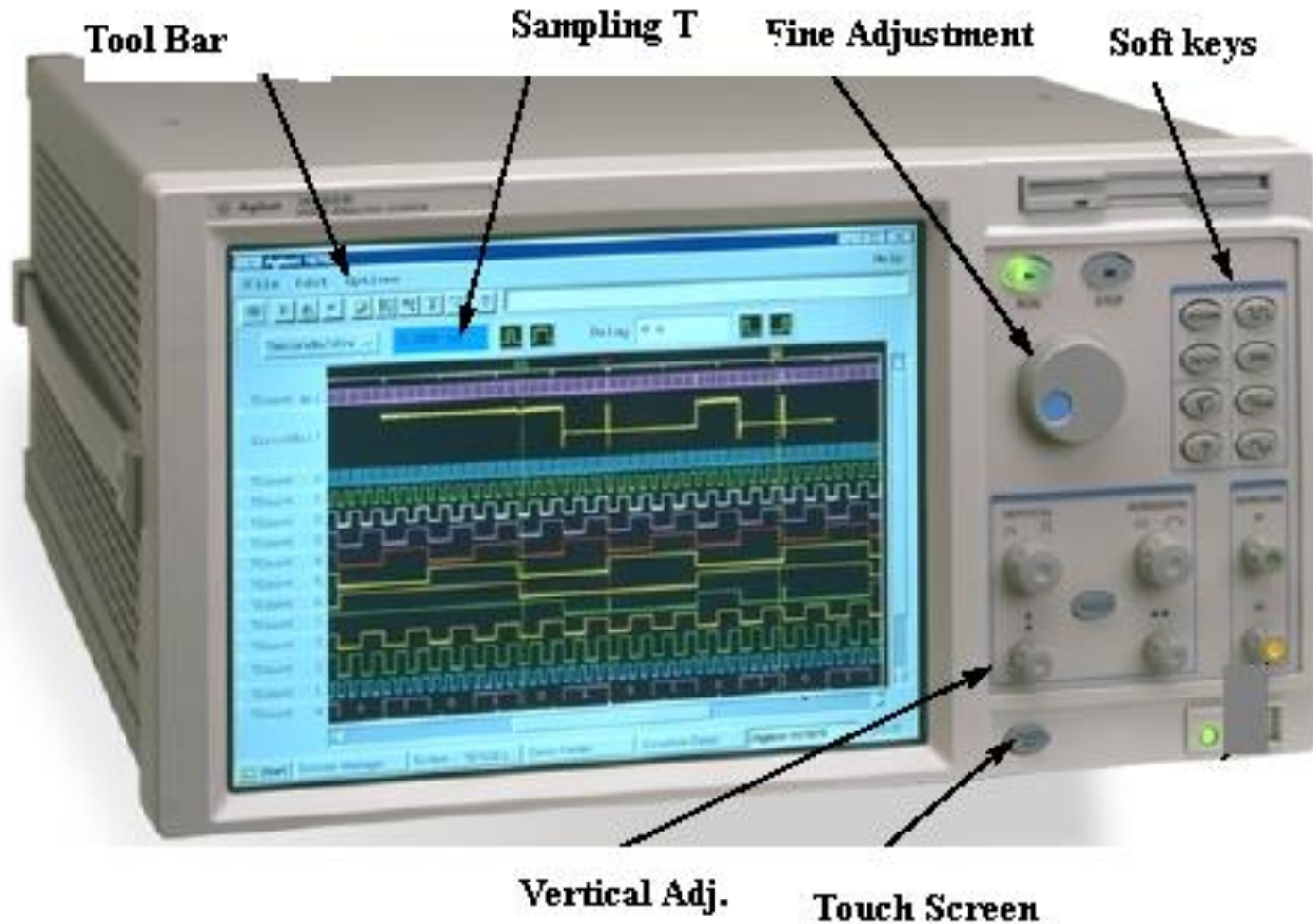
Välkommen



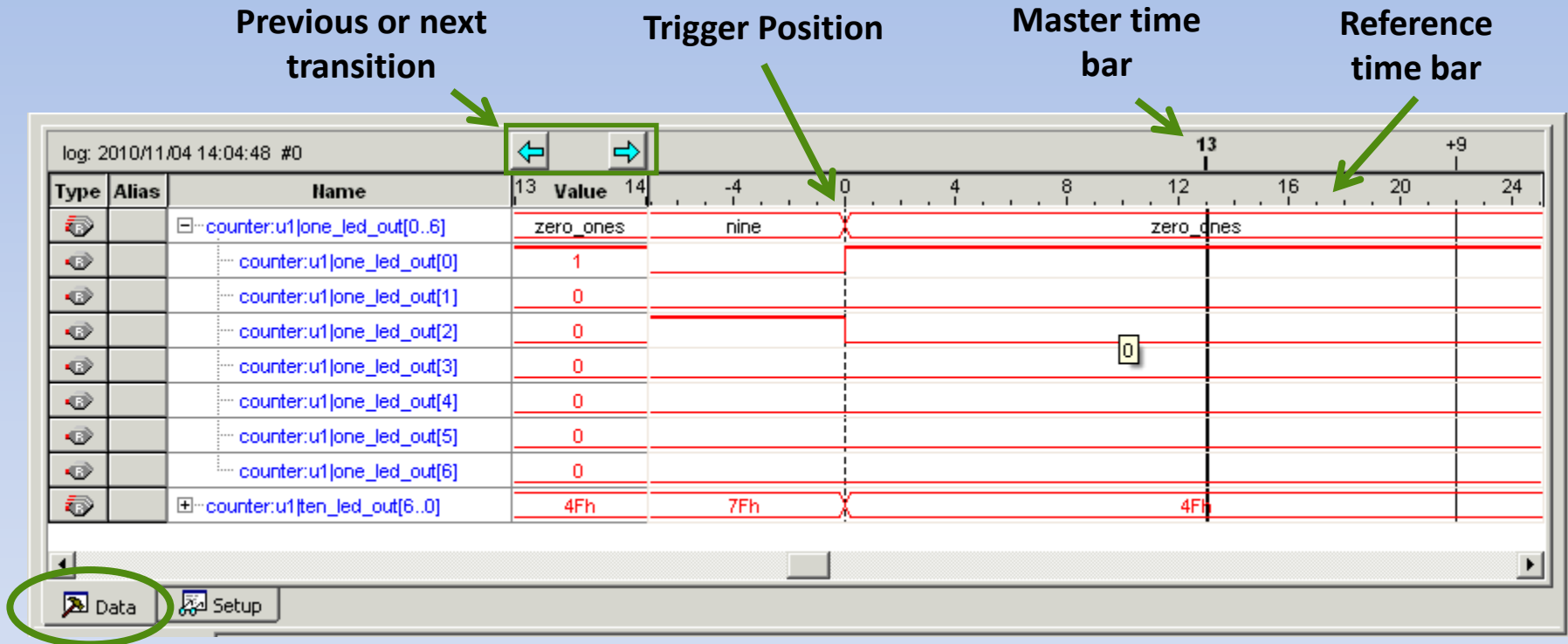
- Debugging Tools – SignalTap II Embedded Logic Analyze
- What is a glitch?
- Timing mode accuracy
- How Does it Work?
- SignalTap II Design Flow
- Dokumentation:

http://www.altera.com/literature/hb/qts/qts_qii53009.pdf

Logik Analysator



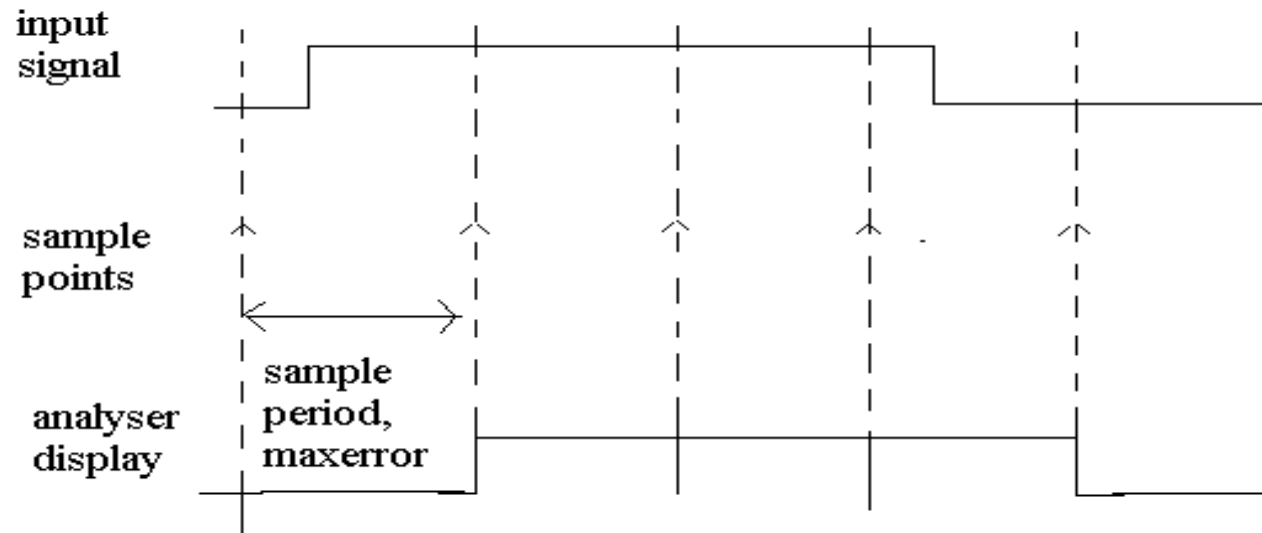
SignalTap II Embedded Logic Analyzer



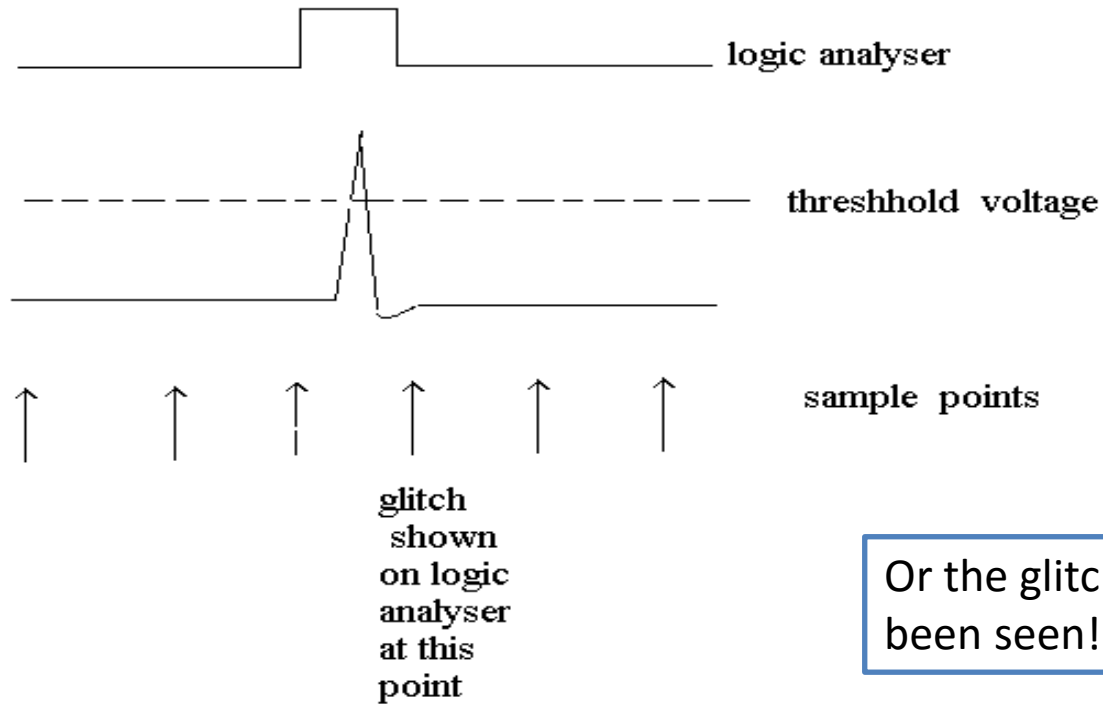
Timing mode accuracy

TIMING MODE ACCURACY

transition between sample points



What is a glitch?

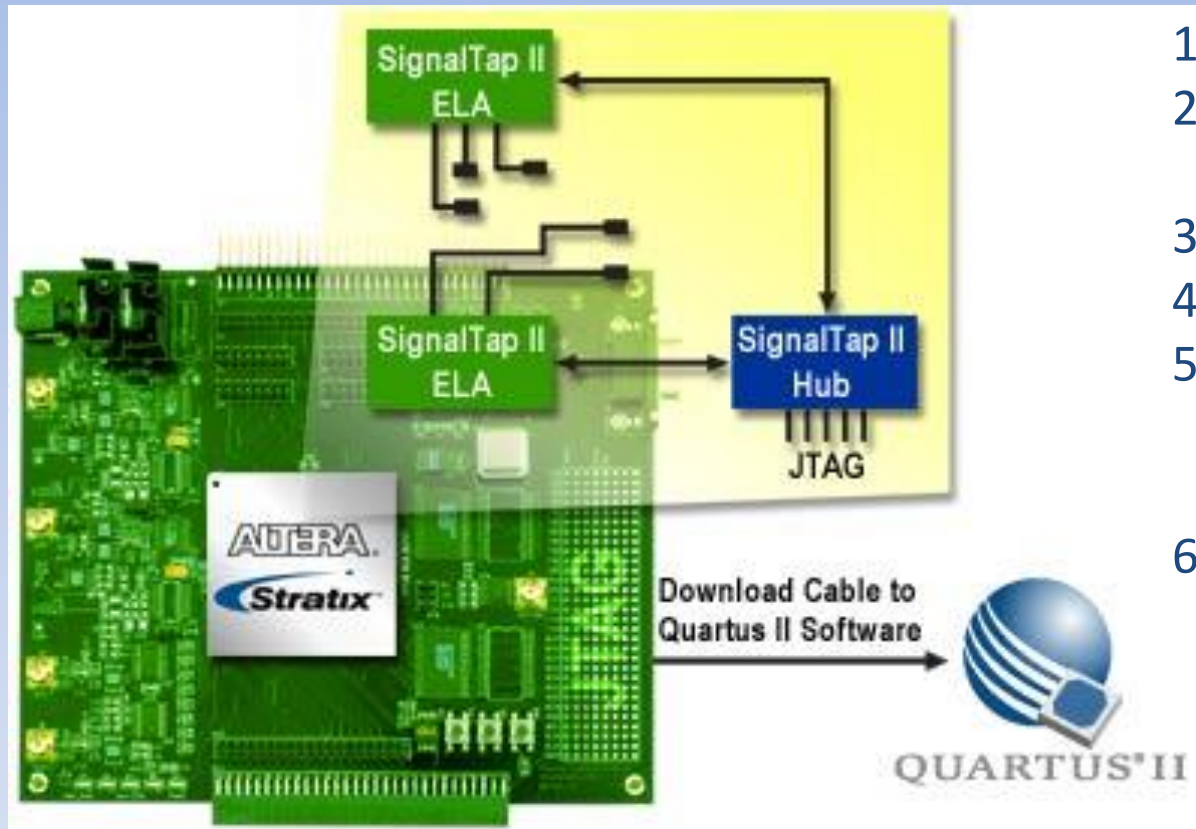


Or the glitch will not be seen!

SignalTap II ELA Agenda

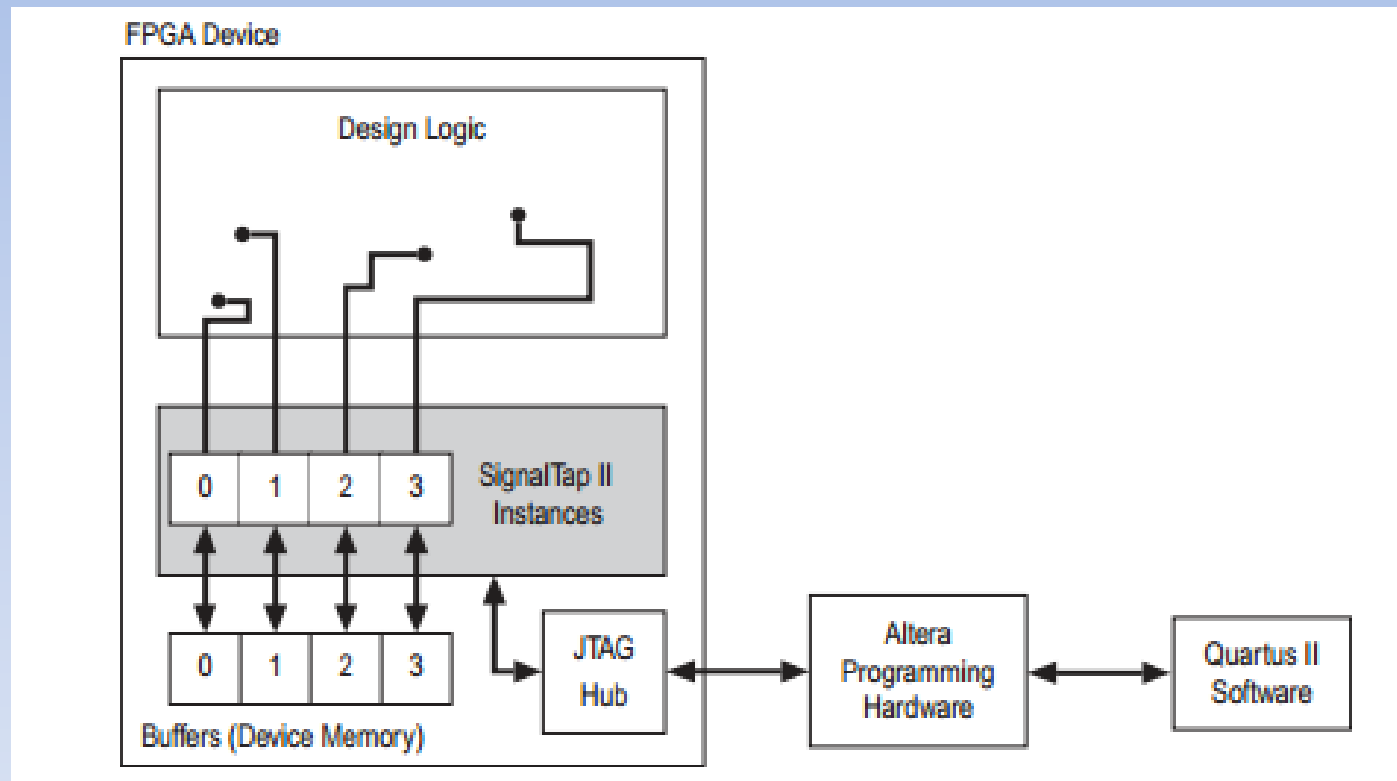
- **SignalTap II ELA overview & features**
- Using SignalTap II ELA interface
- ELA = Embedded Logic Analyzer

How Does it Work?



1. Configure ELA
2. Download ELA into FPGA along with design
3. Start running ELA
4. Defined trigger event(s)
5. Samples and stores internal signal states in device memory
6. Captured samples transferred to Quartus II software through JTAG

How Does it Work?



ELA Resource Utilization

- Logic elements
 - Number of channels
 - Trigger levels
- Memory block count
 - Number of channels
 - Sample depth
 - Selectable trade-off between depth & number of channels
 - 128K sample depth with 1024 channels not practical – 32,768 M4K blocks
- Estimated resource usage displayed and update during SignalTap II configuration

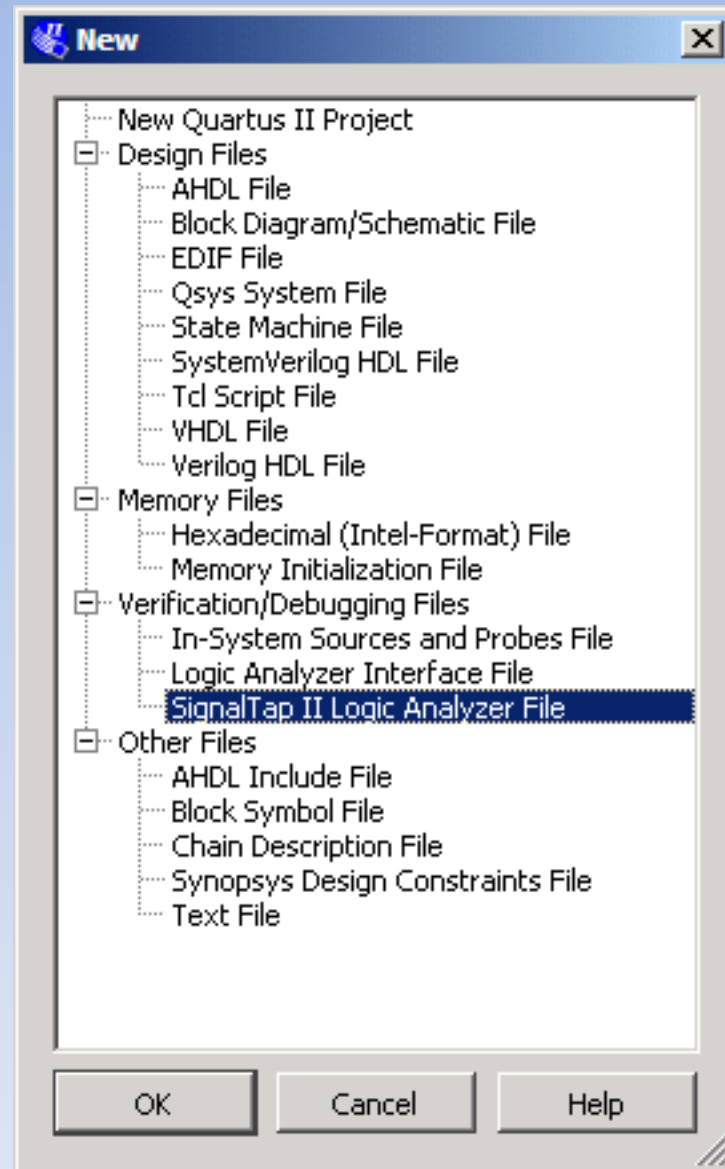
SignalTap II Agenda

- SignalTap II ELA overview & features
- **Using SignalTap II ELA interface**

Using STP File

1. Create .STP file
 - Assign sample clock
 - Specify sample depth
 - Assign signals to STP file
 - Specify triggering conditions and flow
 - Specify storage qualifier(s) (optional)
 - Setup JTAG
2. Save .STP file & compile with design
3. Program device
4. Acquire data

1) Create a New .STP File



Main .STP File Components

The screenshot displays the SignalTap II Logic Analyzer interface with the following components highlighted:









- Instance Manager:** A table showing the status of logic instances.

| Instance | Status | LEs: 1040 | Memory: 14336 | M512,MLAB: 0/0 | M4K,M9K: 2/43 | M-RAM,M144K: 0/0 |
|--------------|-------------|-----------|---------------|----------------|---------------|------------------|
| instance_one | Not running | 520 cells | 7168 bits | 0 blocks | 1 blocks | 0 blocks |
| instance_ten | Not running | 520 cells | 7168 bits | 0 blocks | 1 blocks | 0 blocks |
- JTAG Chain Configuration:** A panel showing JTAG settings, including hardware (USB-Blaster [USB-0]), device (@1: EP3C120/EP4CE115 (0x020F70DD)), and SOF Manager.
- Node List:** A table listing nodes and their trigger conditions.

| Type | Alias | Name | Data Enable | Trigger Enable | Trigger Conditions |
|------|-------|---------------------------|-------------------------------------|-------------------------------------|--------------------|
| | | ...r:u1 ten_led_out[0..6] | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | eight |
| | | ...u1 ten_led_out[0] | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | 0 |
| | | ...u1 ten_led_out[1] | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | 0 |
| | | ...u1 ten_led_out[2] | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | 0 |
| | | ...u1 ten_led_out[3] | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | 0 |
| | | ...u1 ten_led_out[4] | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | 0 |
| | | ...u1 ten_led_out[5] | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | 0 |
| | | ...u1 ten_led_out[6] | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | 0 |
- Trigger conditions & storage qualifiers:** A panel for configuring trigger conditions (Basic, Basic) and storage qualifiers (Continuous, Input port).
- Design Hierarchy:** A panel showing the hierarchy of the design, including instance_one and instance_ten.
- Data Log:** A panel showing the data log for instance_ten.

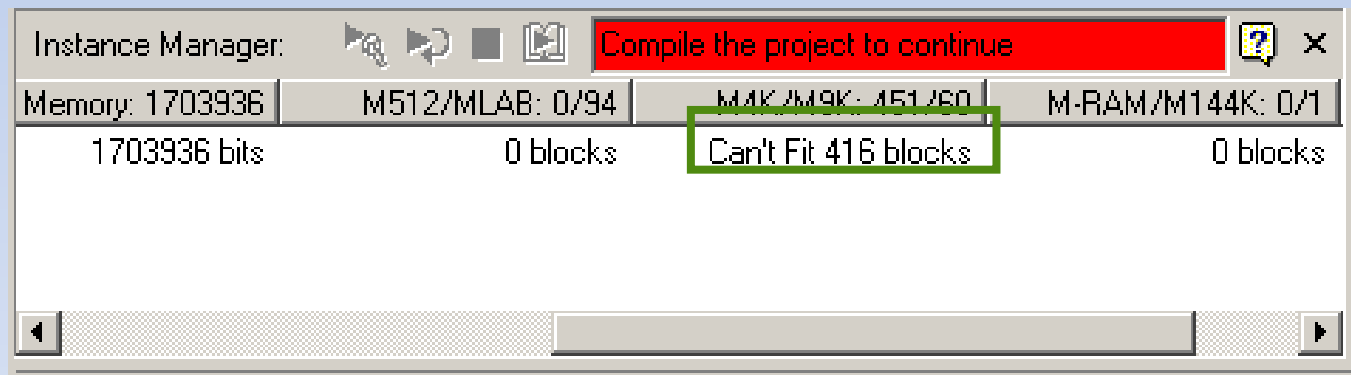
Instance Manager

- Create new instances (right-click)
- Displays the current status of each instance
- Run and control instances

| Instance Manager:     Compile the project to continue   | | | | | | |
|--|-------------|-----------|---------------|----------------|----------------|------------------|
| Instance | Status | LEs: 1040 | Memory: 14336 | M512,MLAB: 0/0 | M4K,M9K: 2/432 | M-RAM,M144K: 0/0 |
|  instance_one | Not running | 520 cells | 7168 bits | 0 blocks | 1 blocks | 0 blocks |
| Power-Up Trigger | | | | | | |
|  instance_ten | Not running | 520 cells | 7168 bits | 0 blocks | 1 blocks | 0 blocks |

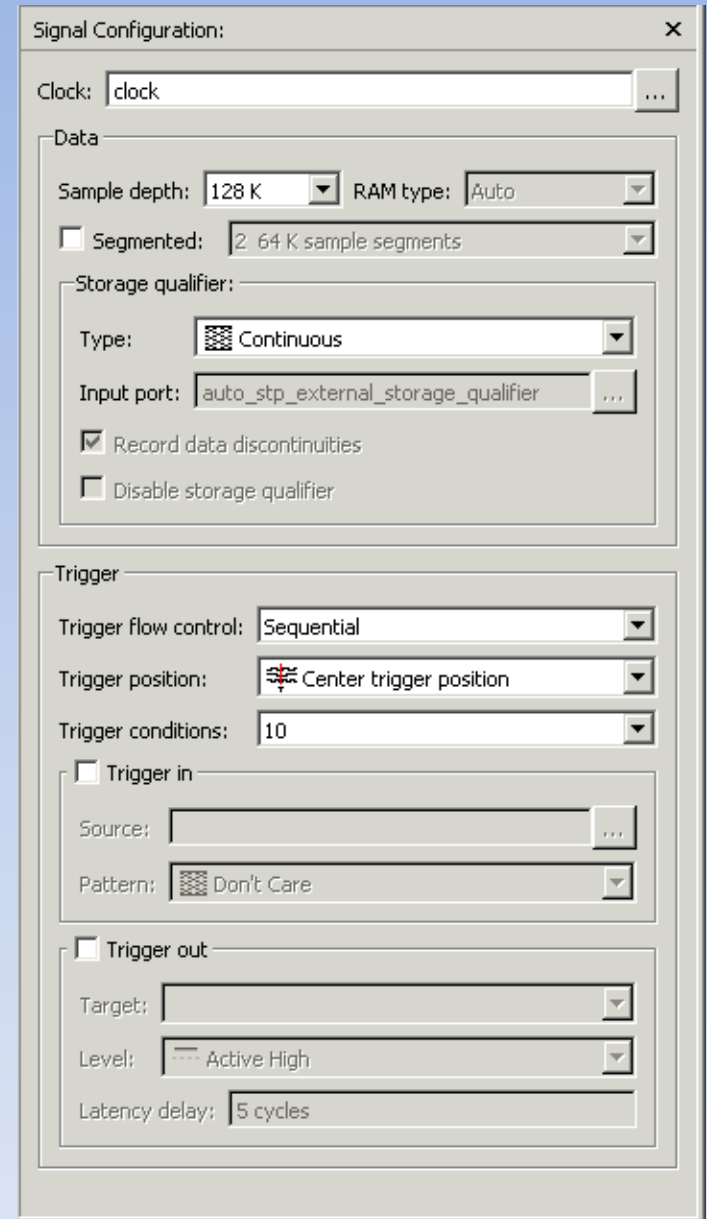
Fitting Prediction

- Predict whether current configuration can fit before lengthy compilation



Signal Configuration

- Manages data capture & signal configuration
 - Sample clock
 - Sample depth
 - Buffer type
 - Storage qualification
 - Trigger flow
 - Trigger position
 - Trigger-in & trigger-out
- Settings similar to external test equipment



The image shows a 'Signal Configuration' dialog box with the following settings:

- Clock:** clock
- Data:**
 - Sample depth: 128 K
 - RAM type: Auto
 - ☐ Segmented: 2 64 K sample segments
 - Storage qualifier:
 - Type: Continuous
 - Input port: auto_stp_external_storage_qualifier
 - ☒ Record data discontinuities
 - ☐ Disable storage qualifier
- Trigger:**
 - Trigger flow control: Sequential
 - Trigger position: Center trigger position
 - Trigger conditions: 10
 - ☐ Trigger in:
 - Source:
 - Pattern: Don't Care
 - ☐ Trigger out:
 - Target:
 - Level: Active High
 - Latency delay: 5 cycles

Sample Clock

Signal Configuration: [X]

Clock: [...]

Data

Sample depth: RAM type:

☐ Segmented:

Storage qualifier:

Type:

Input port: [...]

☒ Record data discontinuities

☐ Disable storage qualifier

Trigger

Trigger flow control:

Trigger position:

Trigger conditions:

☐ Trigger in

Source: [...]

Pattern:

☐ Trigger out

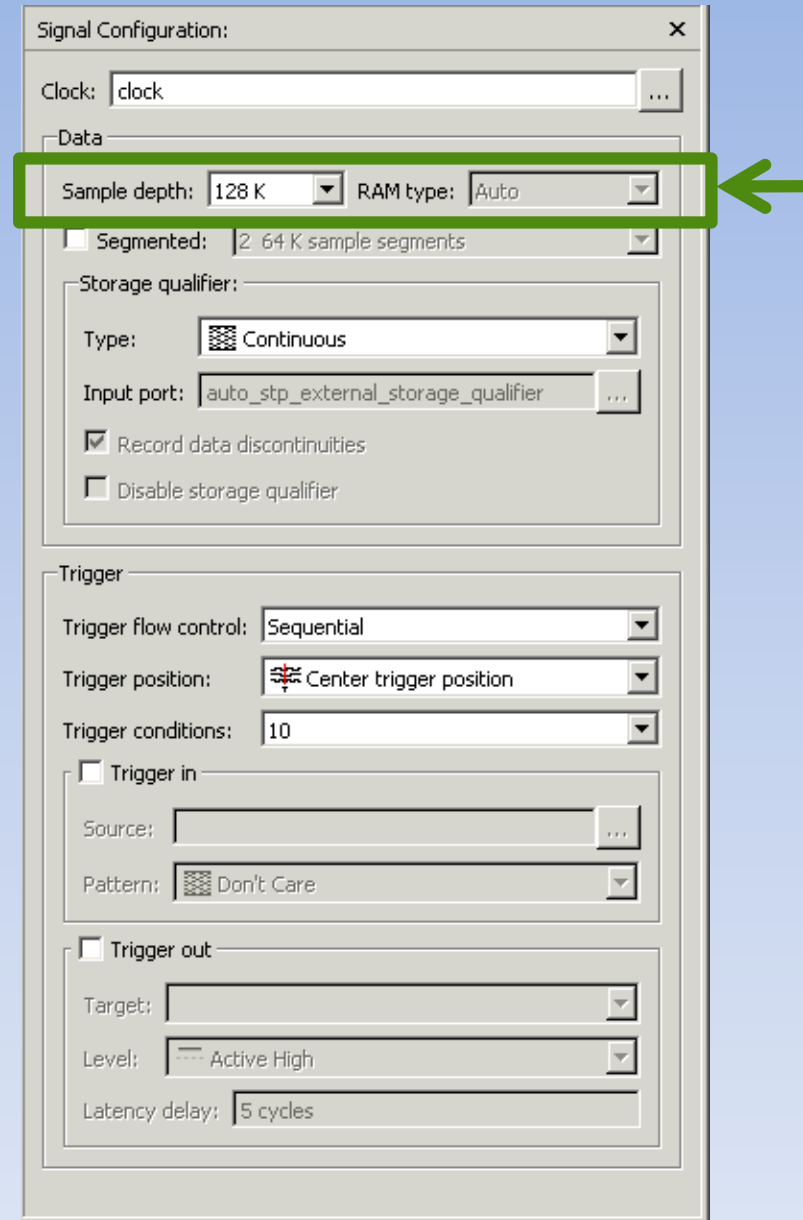
Target:

Level:

Latency delay:

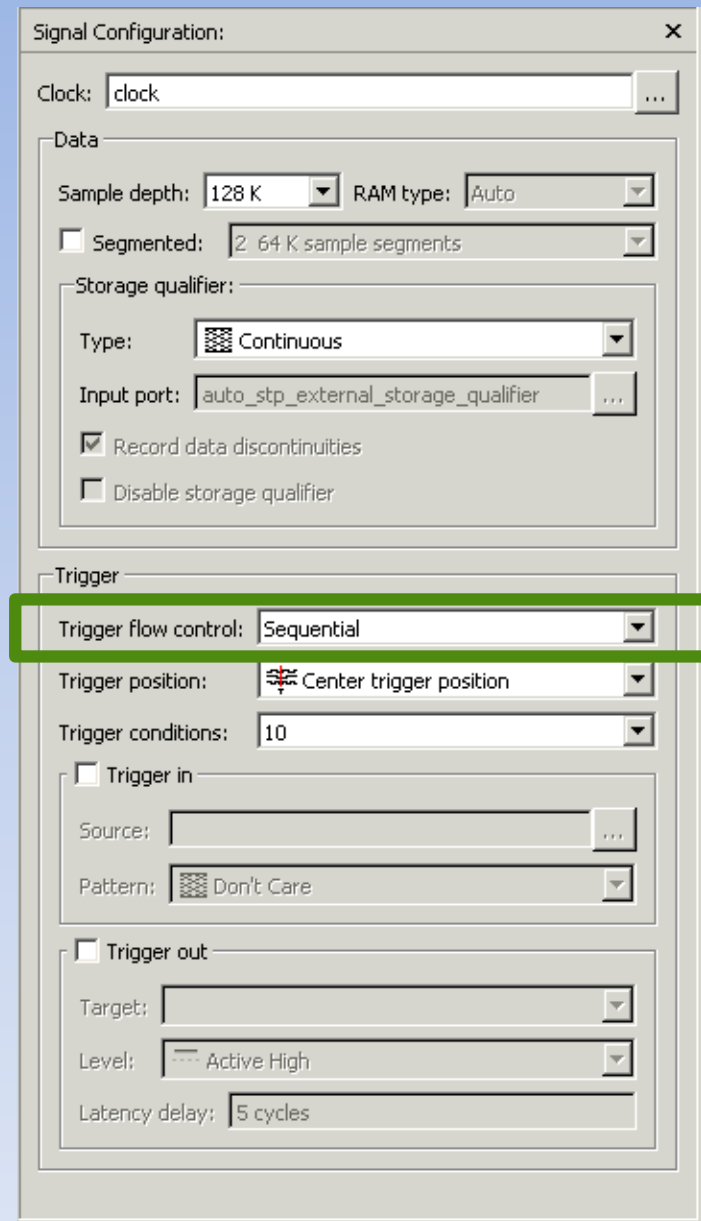
Sample Depth

- Sample depth
 - 0 to 128K sample depth
- Select RAM type for supported FPGAs
 - Defaults to Auto on unsupported device families



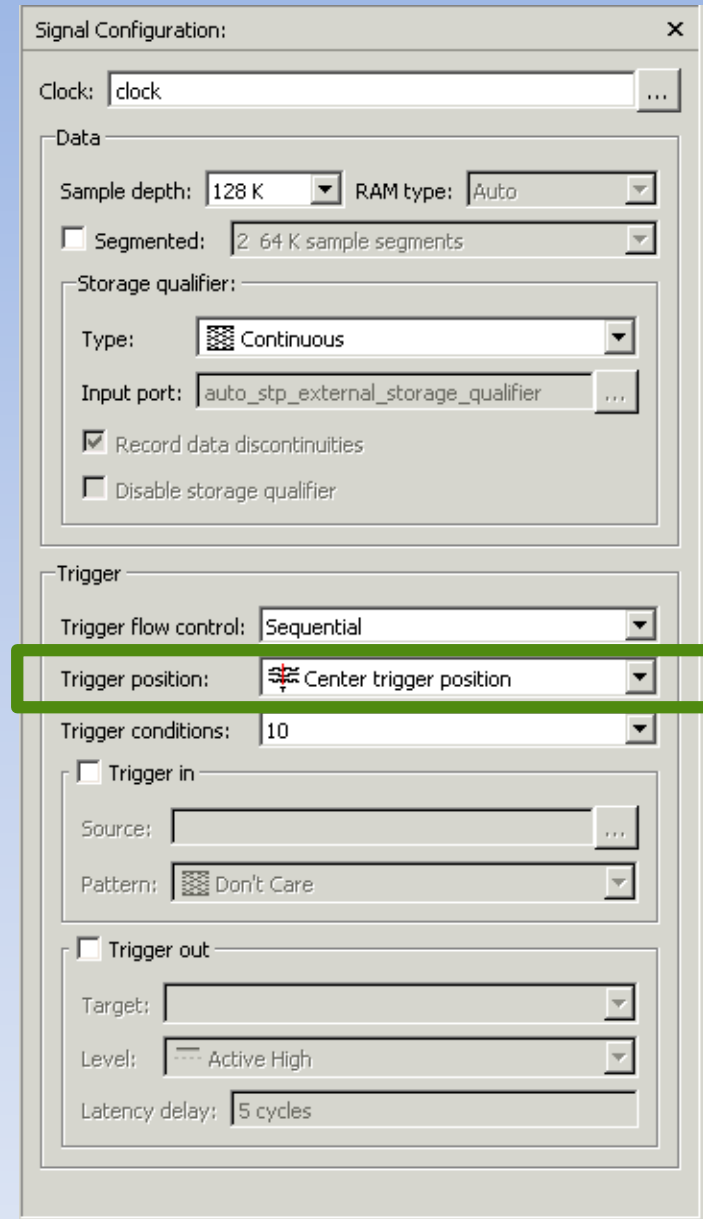
Trigger Flow Control

- Sequential
 - Trigger conditions evaluated in numerical order
 - Trigger in (condition “0”) followed by conditions 1, 2, 3, etc.
 - Buffer or 1st buffer segment filled on final condition
 - Subsequent segments filled only when final condition reoccurs



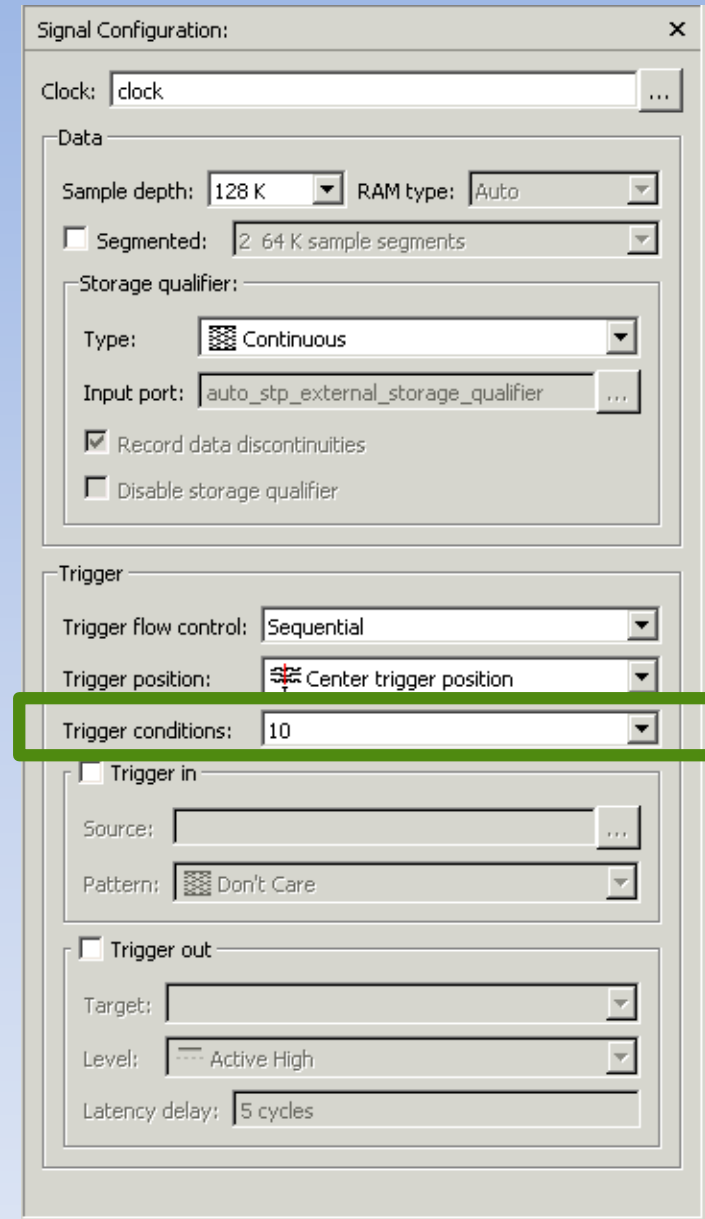
Trigger Position

- Location in buffer (or buffer segment) where trigger sample located
- Three default positions
 - Pre (12% before trigger, 88% after)
 - Center (50% before, 50% after)
 - Post (88% before, 12% after)



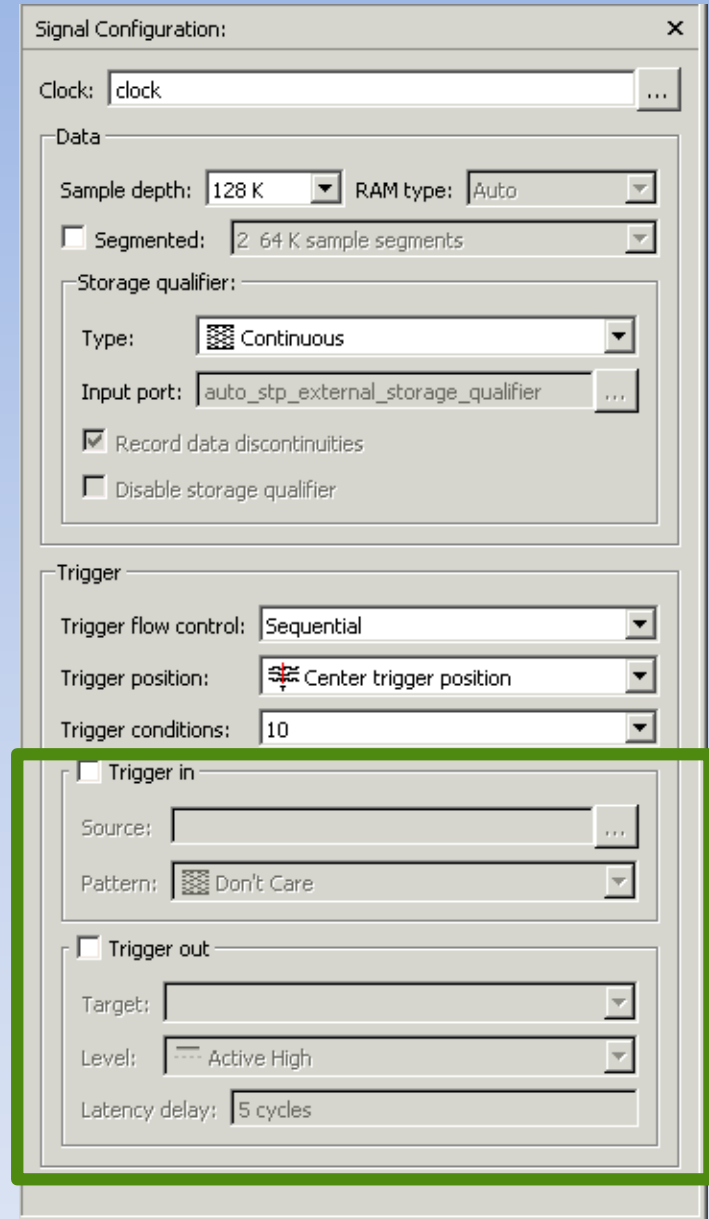
Trigger Conditions

- Create up to 10 trigger conditions for each SignalTap II instance
- Conditions appear as separate columns in node list
- Order and analysis of conditions depends on flow control setting



Trigger In & Out

- Interface SignalTap II ELA with other devices



The image shows a 'Signal Configuration' dialog box with the following settings:

- Clock:** clock
- Data:**
 - Sample depth: 128 K
 - RAM type: Auto
 - Segmented: ☐ 2 64 K sample segments
 - Storage qualifier:
 - Type: Continuous
 - Input port: auto_stp_external_storage_qualifier
 - ☒ Record data discontinuities
 - ☐ Disable storage qualifier
- Trigger:**
 - Trigger flow control: Sequential
 - Trigger position: Center trigger position
 - Trigger conditions: 10
 - Trigger in:**
 - Source:
 - Pattern: Don't Care
 - Trigger out:**
 - Target:
 - Level: Active High
 - Latency delay: 5 cycles

A green box highlights the 'Trigger in' and 'Trigger out' sections, and a green arrow points to the 'Trigger out' section.

Main .STP File Components

SignalTap II Logic Analyzer - C:/altera_trn/Quartus_II_Debug_and_Analysis/Ex3/CycloneIII/top_counter - top_counter - [counter.stp]*

File Edit View Project Processing Tools Window

Instance Manager: Compile the project to continue

| Instance | Status | LEs: 639 | Memory: 26214 | M512,MLAB: 0 | M4K,M9K: 32/4 | M-RAM |
|--------------|-------------|-----------|---------------|--------------|---------------|---------|
| instance_one | Not running | 639 cells | 262144 bits | 0 blocks | 32 blocks | 0 bl... |

JTAG Chain Configuration: JTAG ready

Hardware: USB-Blaster [USB-0] Setup...

Device: @1: EP3C120/EP4CE115 (0x020F70DD) Scan Chain

>> SOF Manager: nalysis/Ex3/CycloneIII/top_counter.sof ...

trigger: 2010/11/03 17:17:05 #1 Lock mode: Allow all changes

| Node | | Data Enable | Trigger Enable | Trigger Conditions | |
|------|-------|-------------------------------------|-------------------------------------|--------------------|---------|
| Type | Alias | 2 | 2 | 1 Basic | 2 Basic |
| | ... | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | 0h | 0h |
| | ... | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | 0 | 0 |
| | ... | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | 0 | 0 |

Signal Configuration:

Clock: clock

Data

Sample depth: 128 K RAM type: Auto

☐ Segmented: 2 64 K sample segments

Storage qualifier:

Type: Continuous

Input port: auto_stp_external_storage_qualifier

☒ Record data discontinuities

☐ Disable storage qualifier

Trigger

Double click to add nodes

Data Setup

instance_one

0% 00:00:00

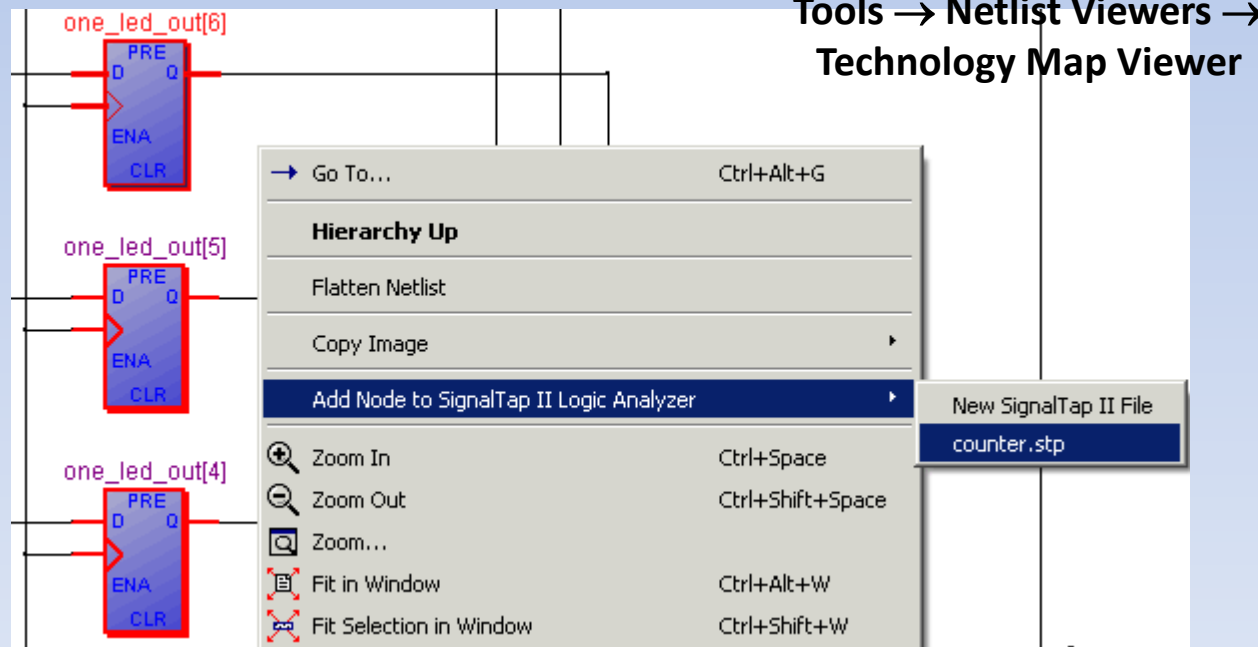
Set Up Node List

- Add signals to Node List by double-clicking
- Two filters available in Node Finder
 - SignalTap II: Pre-Synthesis: Nodes available after analysis & elaboration, but before synthesis
 - SignalTap II: Post-Fitting: Nodes available after Fitter optimizations and place-and-route

Tapping from Technology Map Viewer

- Select nodes in Technology Map Viewer (Post Fitting)
- Quickly add to new or existing SignalTap file

Select and right-click on nodes



Basic Triggering

trigger: 2010/11/04 09:04:28 #0 Lock mode: Allow all changes

Grouped nodes (points to the first node in the list)

Disable individual conditions to skip (sequential flow only) (points to the '1' in the Trigger Enable column)

| Type | Alias | Node | Data Enable | Trigger Enable | Trigger Conditions |
|------|-------|------------------------------|-------------------------------------|-------------------------------------|-------------------------------|
| | | Name | 7 | 7 | 1 Basic 2 Basic 3 Basic |
| | | counter:u1 one_led_out[0..6] | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | eight seven XXXERFXb |
| | | counter:u1 one_led_out[0] | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | 0 1 |
| | | counter:u1 one_led_out[1] | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | 0 1 |
| | | counter:u1 one_led_out[2] | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | 0 1 |
| | | counter:u1 one_led_out[3] | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | 0 1 |
| | | counter:u1 one_led_out[4] | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | 0 0 |
| | | counter:u1 one_led_out[5] | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | 0 0 |
| | | counter:u1 one_led_out[6] | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | 0 0 |

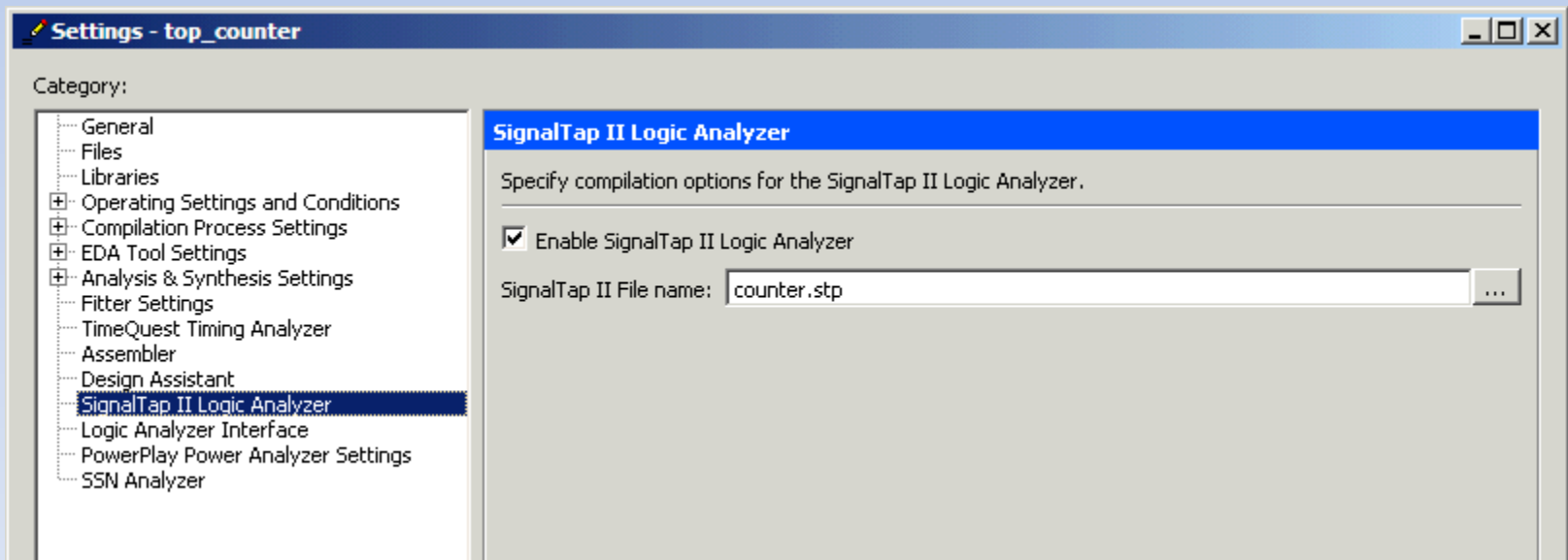
All signals must be true for level to capture (points to the '0' in the Trigger Enable column)

Right-click to set value (points to the right-click context menu)

Don't Care
 Low
 Falling Edge
 Rising Edge
 High
 Either Edge
 Insert Value...

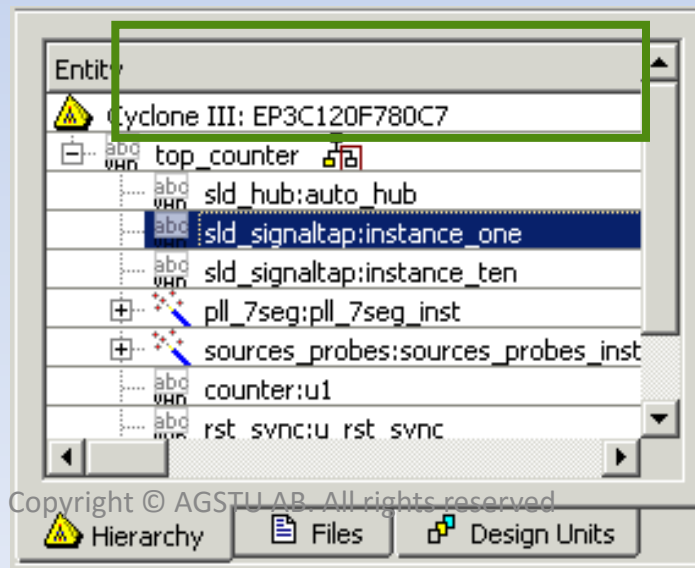
2) Save .STP File & Compile

- SignalTap II Logic Analyzer control in Settings
 - **Assignments** menu → **Settings**
 - Specify the SignalTap II file to compile with project



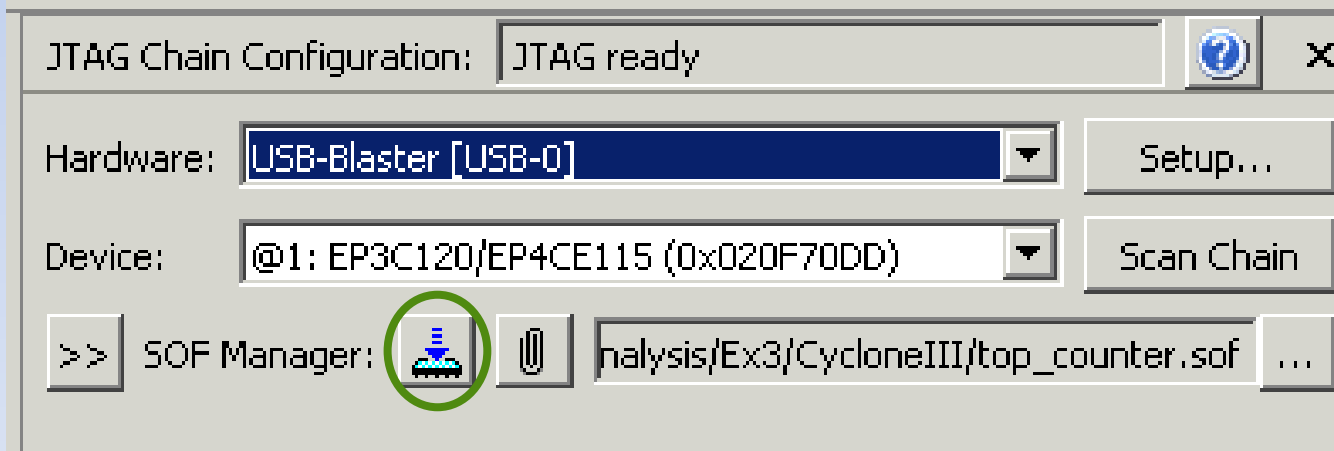
Compile Project with SignalTap II ELA

- Full compilation (Processing menu → Start Compilation) to integrate ELA into design
- sld_signaltap and sld_hub added to project to implement logic analyzer and JTAG hub connection



3) Program Device(s)

- Use Quartus II Programmer or SignalTap II file
 - Program button in the SignalTap II interface only configures the selected device in chain
 - Use Quartus II Programmer to program multiple devices
 - Can create a separate SignalTap II file for each device in the JTAG chain



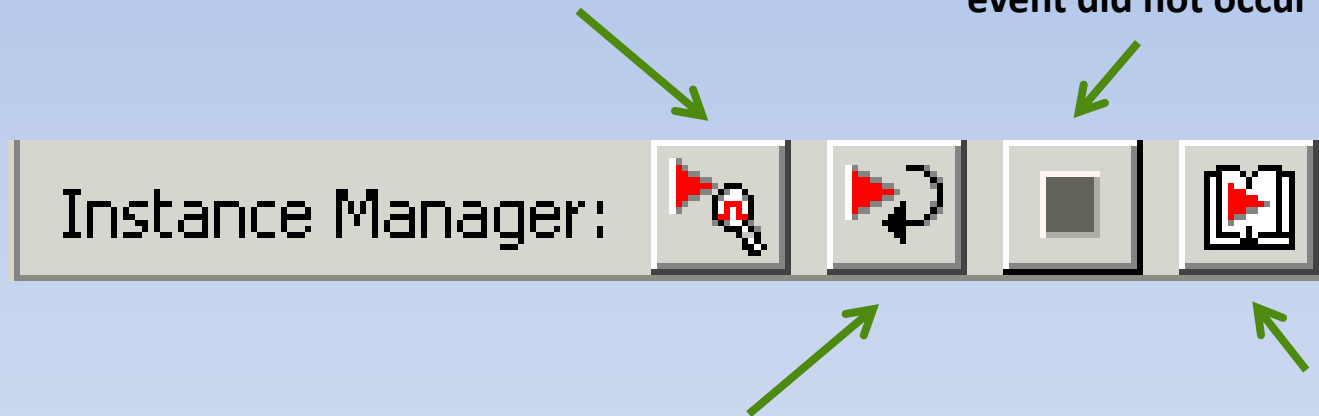
4) Acquire Data

Run Analysis

Run SignalTap II until trigger event occurs or logic analyzer stopped; multiple selected instances run simultaneously

Stop Analysis

Stops the logic analyzer; no data transferred if trigger event did not occur



Autorun Analysis

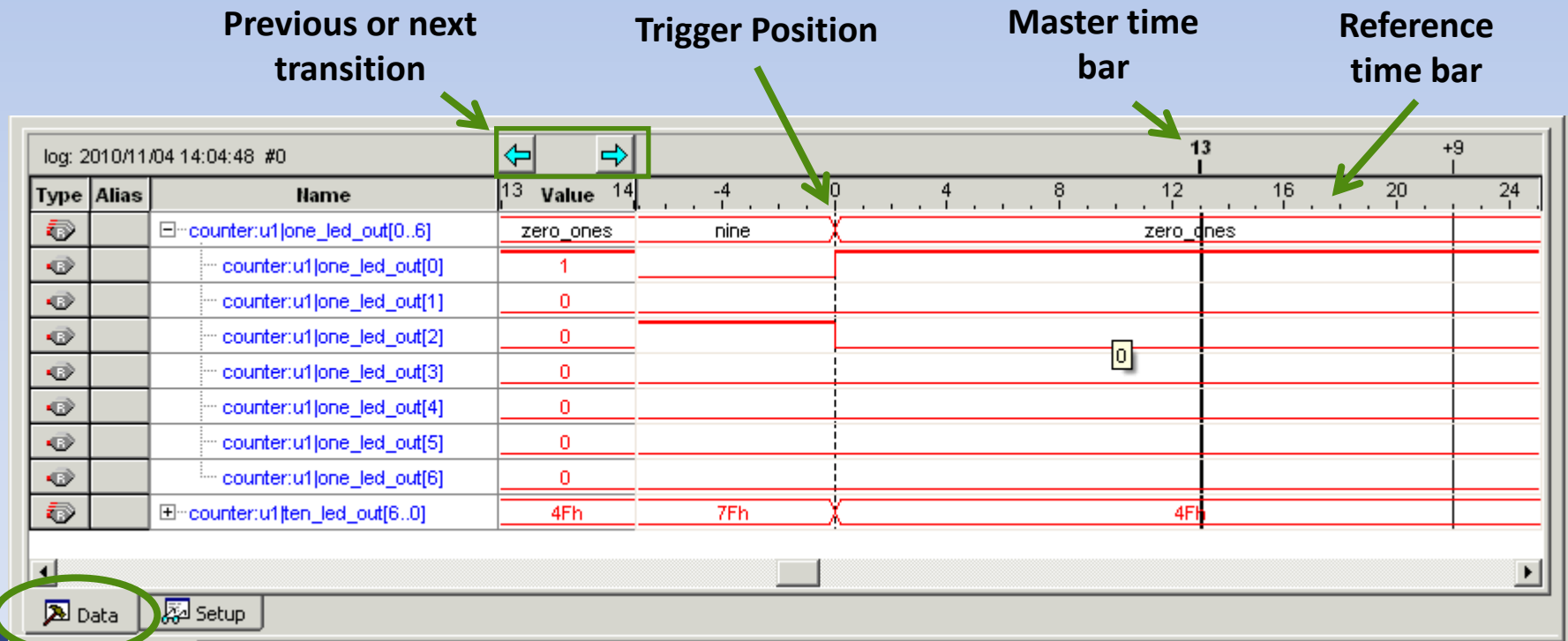
Run SignalTap II until logic analyzer is stopped, ignored trigger events

Read data

Transfers data currently stored in buffer to SignalTap file even if trigger event did not occur

Displaying Acquired Data (1)

- Display signal groups as standard waveforms in selected radix or as a bar or line chart



Dokumentation som kan vara bra att ha:

http://www.altera.com/literature/hb/qts/qts_qii53009.pdf

http://en.wikipedia.org/wiki/Logic_analyzer

ftp://ftp.altera.com/up/pub/Tutorials/DE2/Digital_Logic/tut_sign_altaII_vhdIDE2.pdf



S-L-C.



AGSTU
Utbildning

