Hybrid EV DC-DC Design Example Description rev 1

Introduction

This document describes the Design Example for a Hybrid EV DC-DC Converter ("Variable Voltage Control" or "VVC") digital controller. The architecture and theory are described for the Altera White Paper: "FPGA-Based Control for Electric Vehicle and Hybrid Electric Vehicle Power Electronics". The Design Example uses Altera Advanced DSP Builder to simulate and synthesize VHDL control. The VHDL is then targeted to a BeMicro MAX10 development board (available from Arrow) and results are shown.

Simulation and Code Generation Files

File**: vvc_simpower.slx** – This file is used to simulate a bi-directional dc-dc "Variable Voltage Control" converter using Matlab Simulink Simpower Systems.

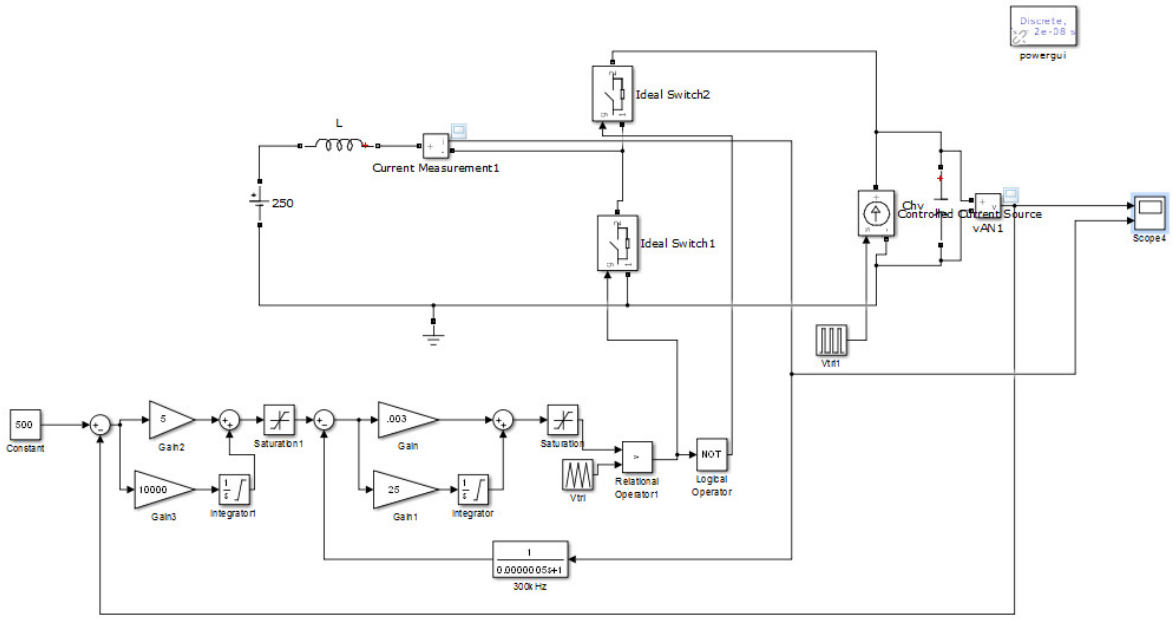


Fig 1 DC-DC Converter Simulation using Matlab Simulink Simpower Systems

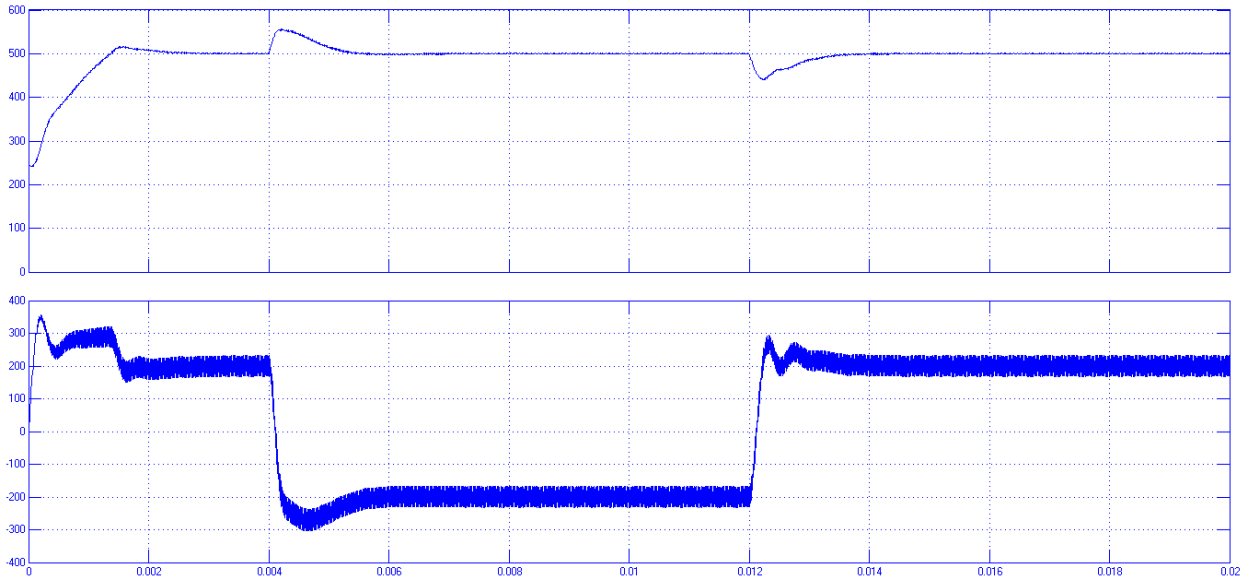


Fig 2 Top: Output Voltage [V], Bottom: Inductor Current [A]

File: **vvc_hwsim_adsp_vhdl.slx** - This file is used to simulate a bi-directional dc-dc "Variable Voltage Control" converter and generate vhdl. The file includes a hardware simulator (Hardware In Loop) so that the complete system can be run in real-time on one FPGA.

- Built with Matlab 2014a and ADSP Builder 14.1
  - Uses Altera Advanved DSP Builder Blocks

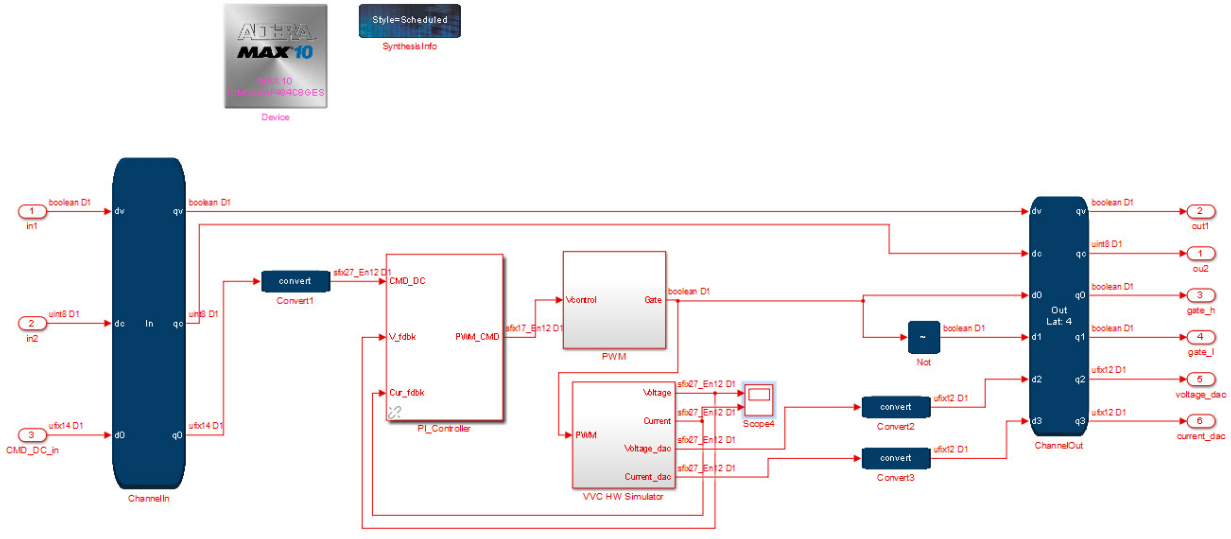


Fig 3 DC-DC Converter and HIL Simulation using Altera ADSPBuilder

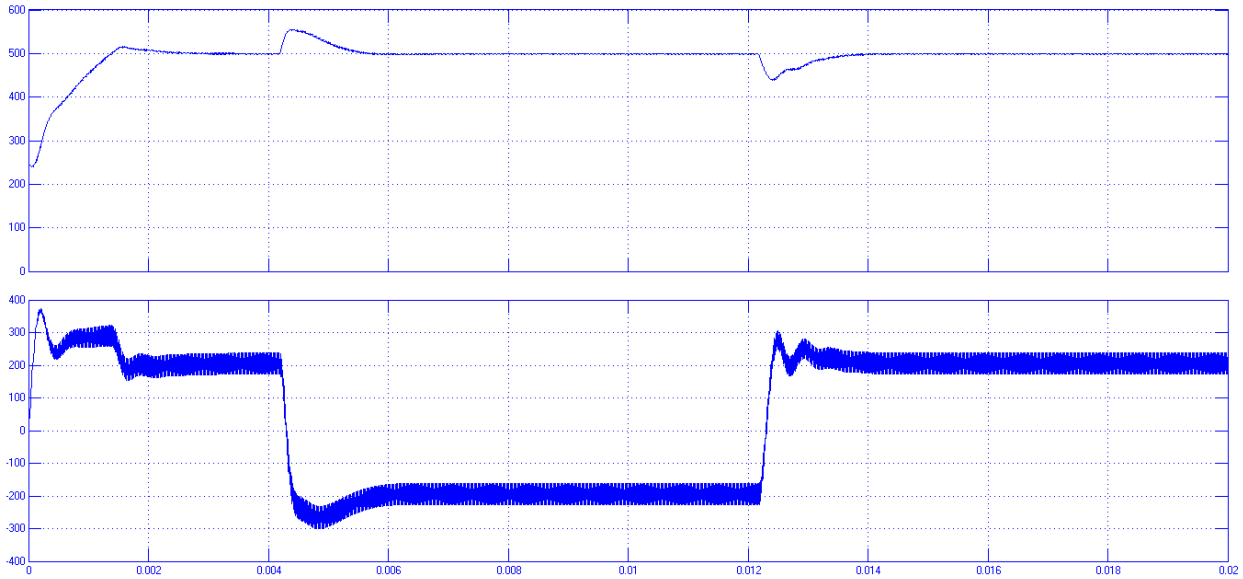


Fig 4 Top: Output Voltage [V], Bottom: Inductor Current [A]

Parameter Description

Inputs

CMD_DC_in	voltage command = 500	[V]

Output

Gate_h	gate drive	[binary]
Gate_l	Gate drive	[binary]

Scope outputs

output voltage
inductor current

Variables

PI_controller block	
Voltage_Pgain	5
Voltage_Igain	10000
Current_Pgain	.003
Current_Igain	25
PWM block	
Triangle freq	50000[Hz]*clk
Clocks	
Clk	20nS

Quartus Project and BeMicro MAX 10: The VVC dc-dc converter control and hardware simulator vhdl code was targeted to a MAX10 FPGA and implemented with the BeMicro MAX10 development kit.

To generate VHDL code, select “Generate Hardware” in “Control” block and specify a destination directory (e.g. “./rtl”). VHDL will automatically be generated when the model is run.

Quartus Project: vvc_bemicro/vvc_rev1

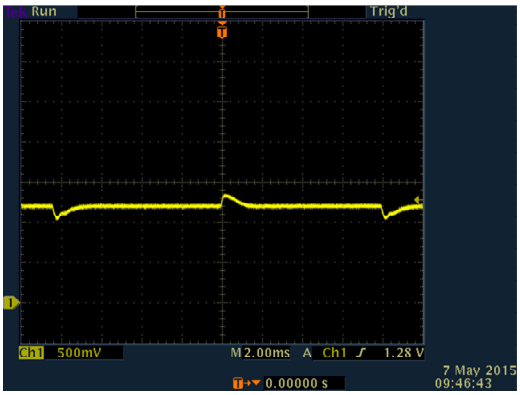
Resources: The following Resources are used for the MAX10 FPGA

Function	Logic Elements	Memory bits	M9 multipiers
VVC	3192	0	24

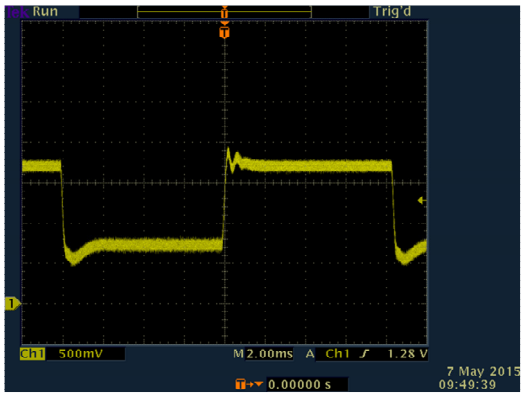
The output voltage and inductor current from the hardware simulator are connected to the BeMicro MAX10 DAC. Push-button SW1 is used to select voltage or current.

BeMicro MAX10 Board

DAC Output Waveforms



Output Voltage



Inductor Current (SW1 depressed)

Project Archive: (download from design store)

D:\vvc_bemicro\vvc_rev1.qar

Unpack archive

D:\vvc_bemicro>c:\altera\14.1\quartus\bin64\quartus_sh –platform –name vvc_rev1.qar

Matlab files:

D:\vvc_bemicro\matlab

vvc_simpower.slx and vvc_hwsim_adsp_vhdl.slx

ADSP generated vhdl files:

D:\vvc_bemicro\matlab\rtl