BeMicro Max 10  
FPGA Evaluation Kit

Getting Started User Guide

Version 14.0 9/4/2014 User Guide

Table of Contents

[1. Overview 2](#_Toc397633292)

[1.1 Board Features 2](#_Toc397633293)

[1.2 Block Diagram 3](#_Toc397633294)

[1.3 Getting To Know Your Kit 4](#_Toc397633295)

[2. Software Installation 5](#_Toc397633296)

[2.1 Install the Altera Design Software 5](#_Toc397633297)

[2.1.1 Download and Install Quartus II Web Edition v14.0 5](#_Toc397633298)

[2.1.2 Download and Install Update 2 which includes the MAX 10 FPGA device family support 11](#_Toc397633299)

[2.2 Enable TalkBack 12](#_Toc397633300)

[2.3 Install USB Blaster Driver 12](#_Toc397633301)

[2.4 Download and Extract a BeMicro Max 10 Kit Example Project 15](#_Toc397633302)

[3. Pinout Information for MAX 10 FPGA I/O 16](#_Toc397633303)

[3.1 Analog Devices External Peripherals 16](#_Toc397633304)

[3.1.1 Accelerometer, 3-Axis, SPI interface (ADXL362) 16](#_Toc397633305)

[3.1.2 DAC, 12-bit, SPI interface (AD5681) 16](#_Toc397633306)

[3.1.3 Temperature sensor, I2C interface (ADT7420) 17](#_Toc397633307)

[3.2 External Memory Devices 17](#_Toc397633308)

[3.2.1 8MB SDRAM 17](#_Toc397633309)

[3.2.2 Serial Flash 18](#_Toc397633310)

[3.3 User Interaction 18](#_Toc397633311)

[3.3.1 LEDs 18](#_Toc397633312)

[3.3.2 Push Buttons 18](#_Toc397633313)

[3.4 MAX 10 FPGA Analog Inputs 19](#_Toc397633314)

[3.4.1 Analog Input Header 19](#_Toc397633315)

[3.4.2 Photo Resistor 19](#_Toc397633316)

[3.4.3 Thermistor (Thermal Resistor) 19](#_Toc397633317)

[3.5 Expansion Headers and Connectors 20](#_Toc397633318)

[3.5.1 BeMicro Edge Connector 20](#_Toc397633319)

[3.5.2 Two 40-pin Expansion Headers 21](#_Toc397633320)

[3.5.3 PMOD Connectors 22](#_Toc397633321)

[3.6 Clock Inputs 22](#_Toc397633322)

[3.7 Boot Select 22](#_Toc397633323)

[4. Hands-On Tutorials and Example Designs 23](#_Toc397633324)

# LVDS loopback demo

The MAX 10 devices use registers and logic in the core fabric to implement LVDS input and output interfaces.

• For LVDS transmitters and receivers, MAX 10 devices use the the double data rate I/O (DDIO) registers that reside in the I/O elements (IOE). This architecture improves performance with regards to the receiver input skew margin (RSKM) or transmitter channel-to-channel skew (TCCS).

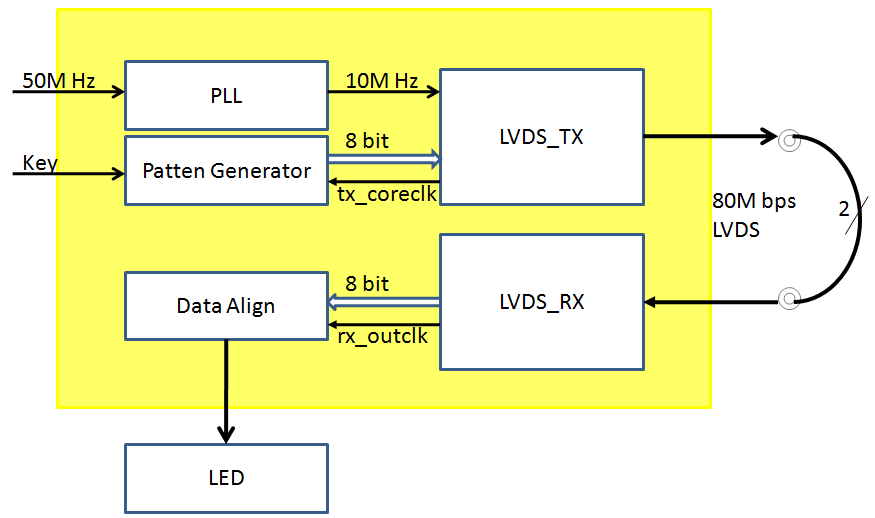
• For the LVDS serializer/deserializer (SERDES), MAX 10 devices use logic elements (LE) registers.

We set the demo for the LVDS loopback functions in the BeMicro Max 10.

The BeMicro Max 10 contains two 2x20 Pin headers(J4 and J5), many of them support LVDS, you can reference below list. we can use either of them for demo purpose.

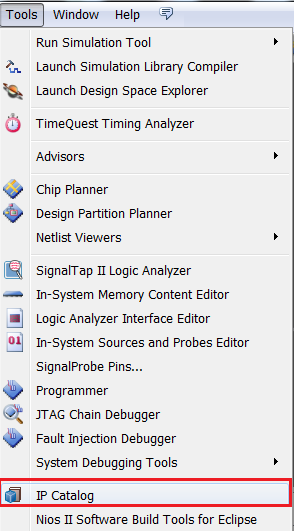
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  |  | | --- | --- | --- | | **Signal Name** | **MAX 10 Pin** | **J3 Pin** | | DIFF\_RX\_P[0] | K14 | 39 | | DIFF\_RX\_P[0](n) | K15 | 40 | | DIFF\_RX\_P[1] | E16 | 37 | | DIFF\_RX\_P[1](n) | E15 | 38 | | DIFF\_RX\_P[2] | D17 | 35 | | DIFF\_RX\_P[2](n) | C17 | 36 | | DIFF\_RX\_P[3] | H14 | 33 | | DIFF\_RX\_P[3](n) | J13 | 34 | | DIFF\_RX\_P[4] | C14 | 31 | | DIFF\_RX\_P[4](n) | C13 | 32 | | DIFF\_RX\_P[5] | A14 | 27 | | DIFF\_RX\_P[5](n) | B14 | 28 | | DIFF\_RX\_P[6] | D14 | 25 | | DIFF\_RX\_P[6](n) | E13 | 26 | | DIFF\_RX\_P[7] | E12 | 23 | | DIFF\_RX\_P[7](n) | D13 | 24 | | DIFF\_RX\_P[8] | H12 | 21 | | DIFF\_RX\_P[8](n) | J11 | 22 | | DIFF\_RX\_P[9] | B10 | 19 | | DIFF\_RX\_P[9](n) | C9 | 20 | | DIFF\_RX\_P[10] | A9 | 17 | | DIFF\_RX\_P[10](n) | B8 | 18 | | DIFF\_RX\_P[11] | A7 | 15 | | DIFF\_RX\_P[11](n) | A8 | 16 | | |  |  |  | | --- | --- | --- | | **Signal Name** | **MAX 10 Pin** | **J4 Pin** | | LVDS\_TX\_P[0] | V17 | 39 | | LVDS\_TX\_P[0](n) | W17 | 40 | | LVDS\_TX\_P[1] | V16 | 37 | | LVDS\_TX\_P[1](n) | U15 | 38 | | LVDS\_TX\_P[2] | W15 | 35 | | LVDS\_TX\_P[2](n) | V14 | 36 | | LVDS\_TX\_P[3] | W14 | 31 | | LVDS\_TX\_P[3](n) | V13 | 32 | | LVDS\_TX\_P[4] | Y14 | 29 | | LVDS\_TX\_P[4](n) | Y13 | 30 | | LVDS\_TX\_P[5] | AA10 | 27 | | LVDS\_TX\_P[5](n) | Y10 | 28 | | LVDS\_TX\_P[6] | V10 | 23 | | LVDS\_TX\_P[6](n) | V9 | 24 | | LVDS\_TX\_P[7] | AA7 | 21 | | LVDS\_TX\_P[7](n) | AA6 | 22 | | LVDS\_TX\_P[8] | W8 | 19 | | LVDS\_TX\_P[8](n) | W7 | 20 | | LVDS\_TX\_P[9] | U7 | 15 | | LVDS\_TX\_P[9](n) | U6 | 16 | | LVDS\_TX\_P[10] | W6 | 13 | | LVDS\_TX\_P[10](n) | W5 | 14 | | LVDS\_TX\_P[11] | W3 | 11 | | LVDS\_TX\_P[11](n) | W4 | 12 | |

## LVDS loopback simple demo chart

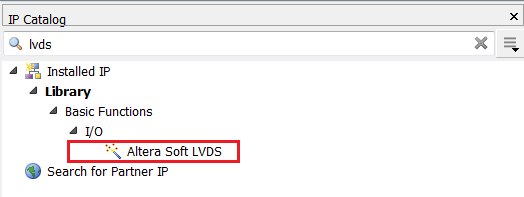


## Soft LVDS IP megawizard

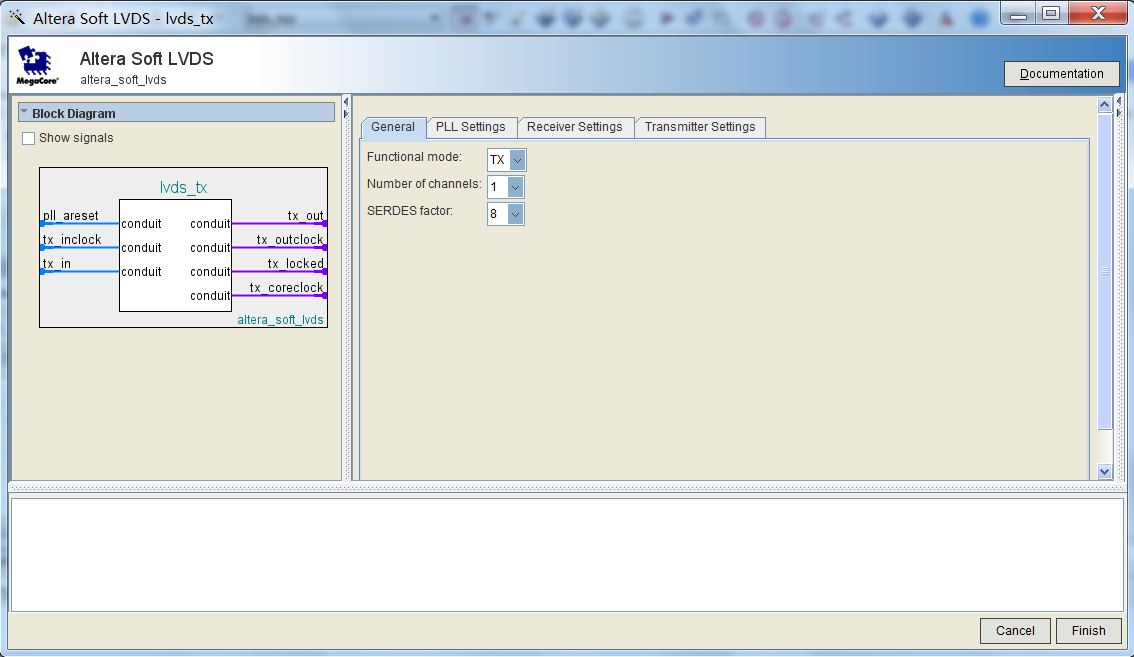
Open Quartus-Tool-IP Catalog



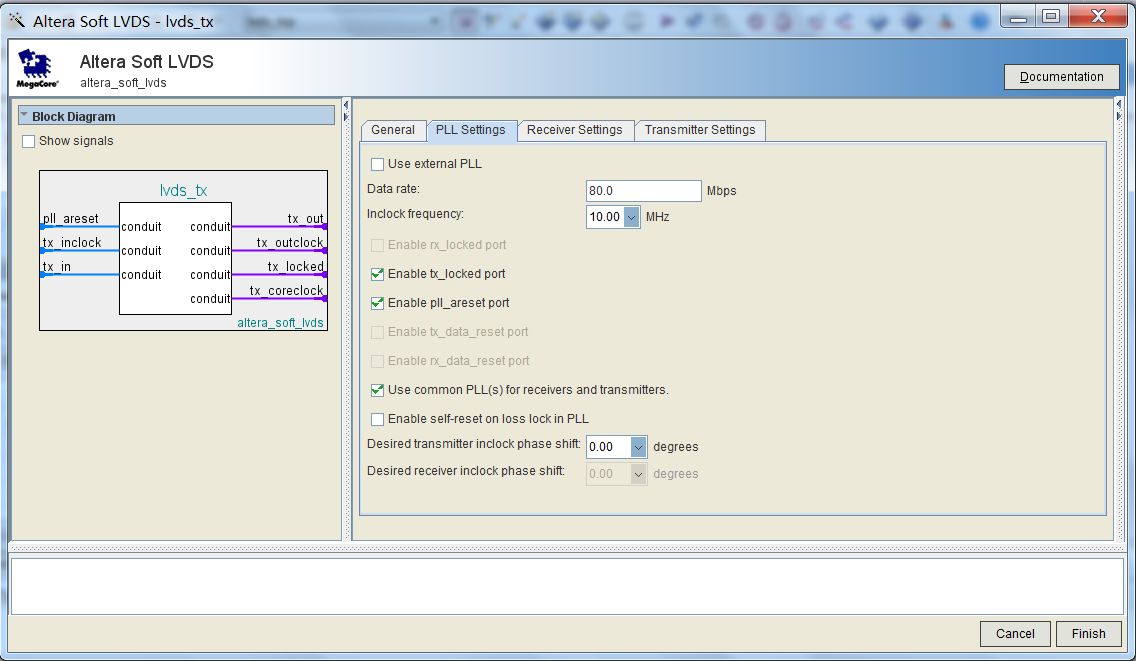
Browse the Altera Soft LVDS IP



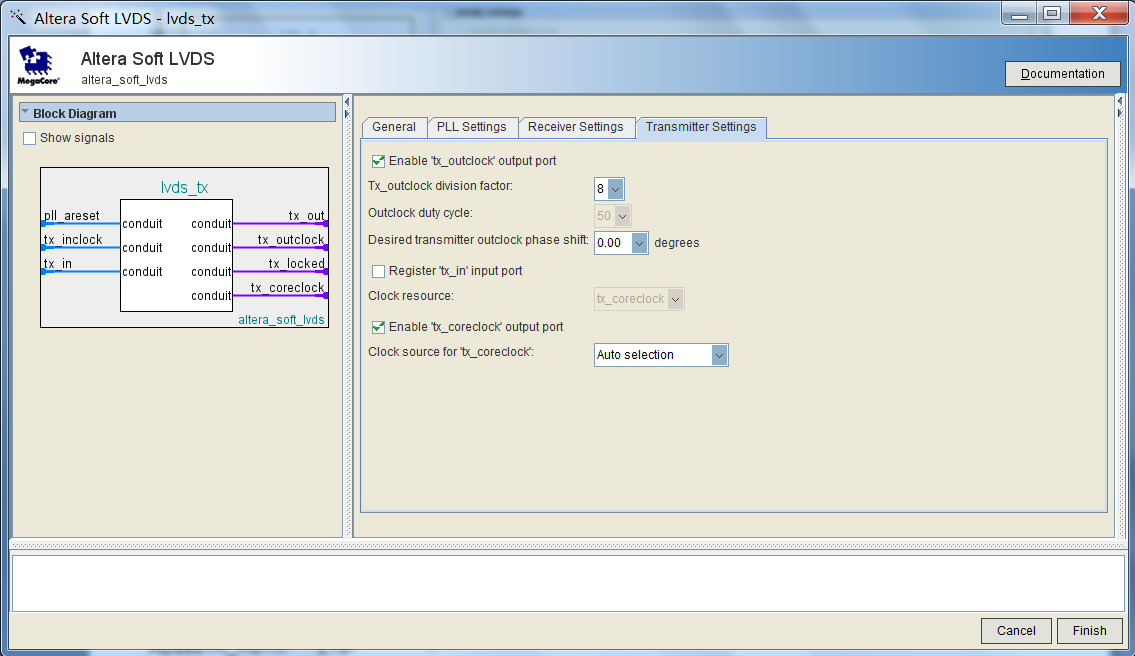
1. Altera Soft LVDS - lvds\_tx IPcore setting - Page1



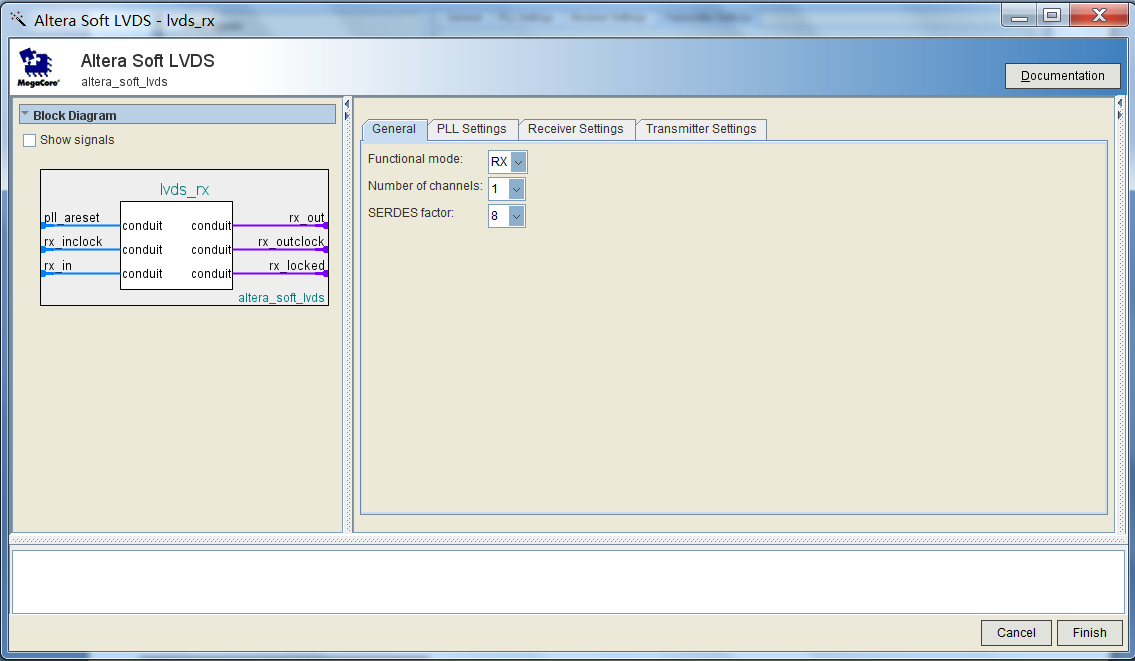
2. Altera Soft LVDS - lvds\_tx IPcore setting - Page2



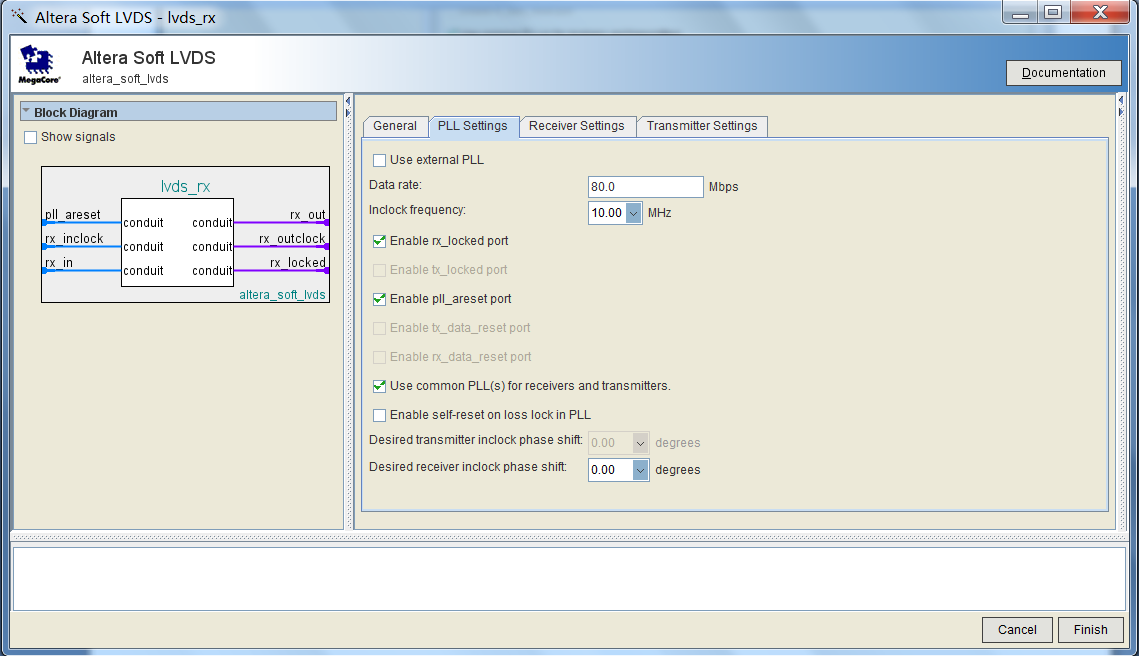
3. Altera Soft LVDS - lvds\_tx IPcore setting - Page4



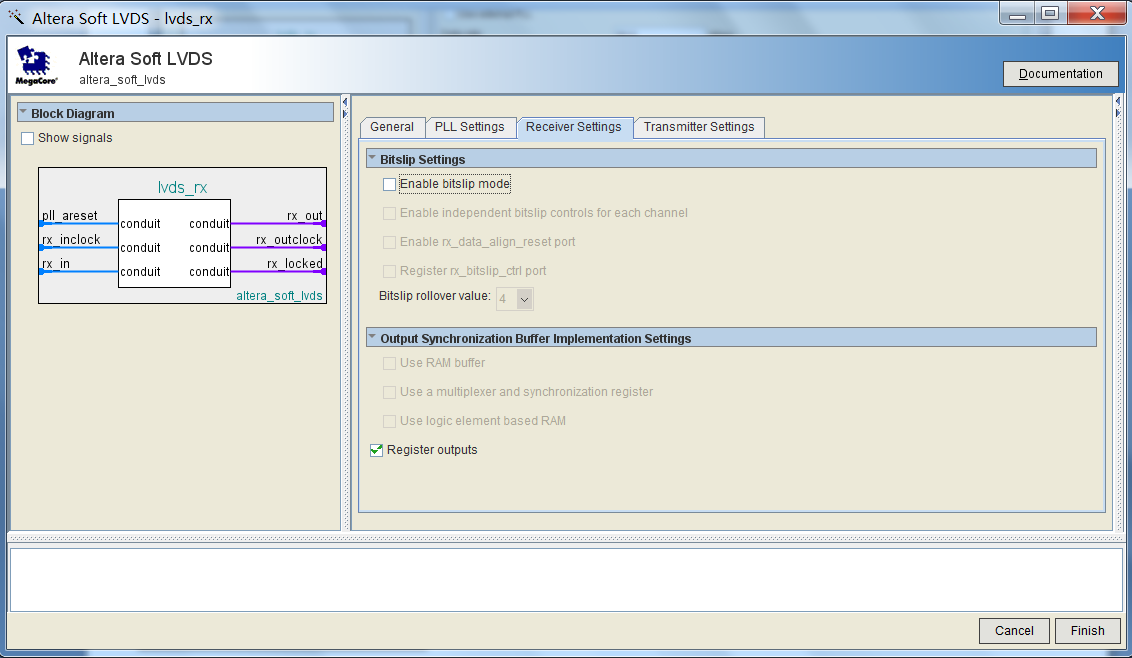
4. Altera Soft LVDS - lvds\_rx IPcore setting - Page1



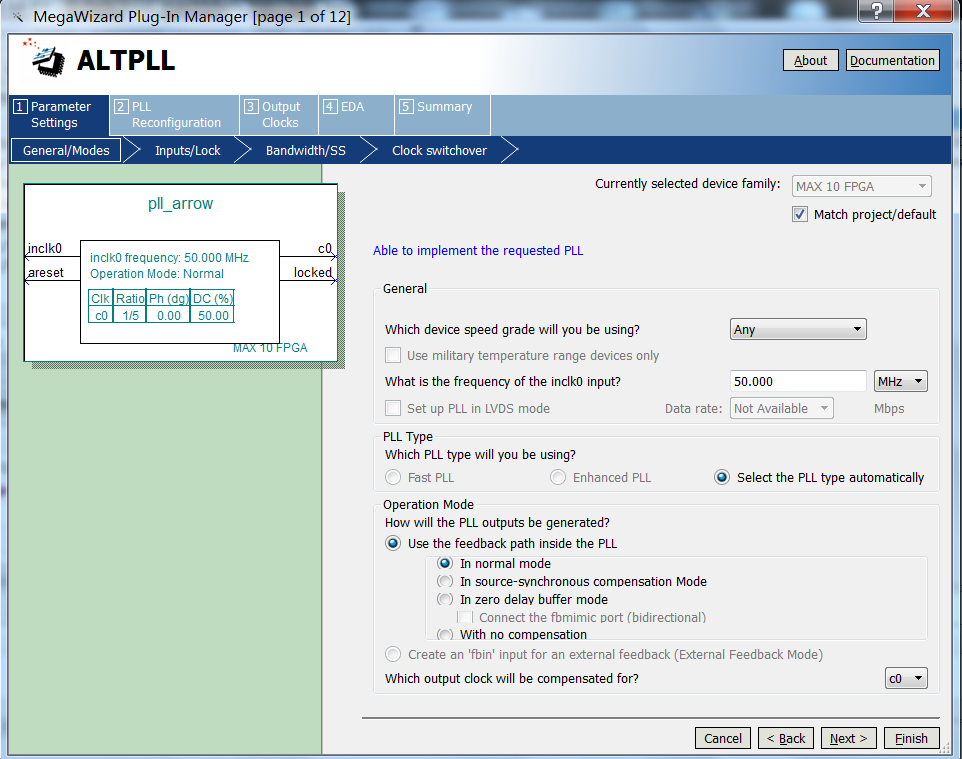
5. Altera Soft LVDS - lvds\_rx IPcore setting - Page2



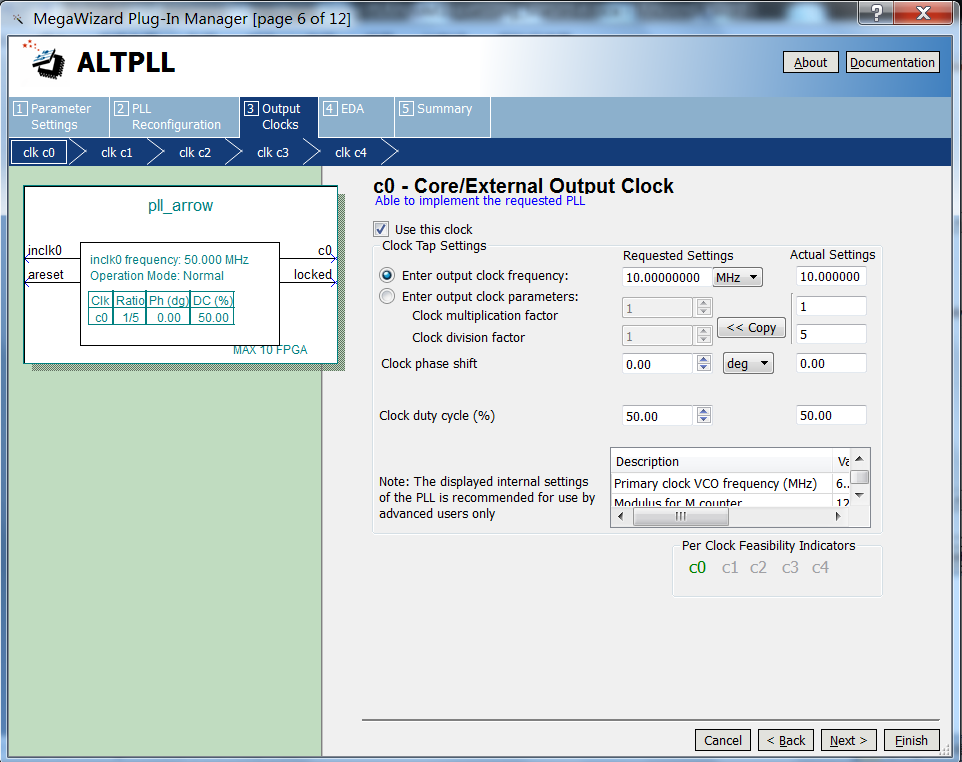
6.Altera Soft LVDS - lvds\_rx IPcore setting - Page3



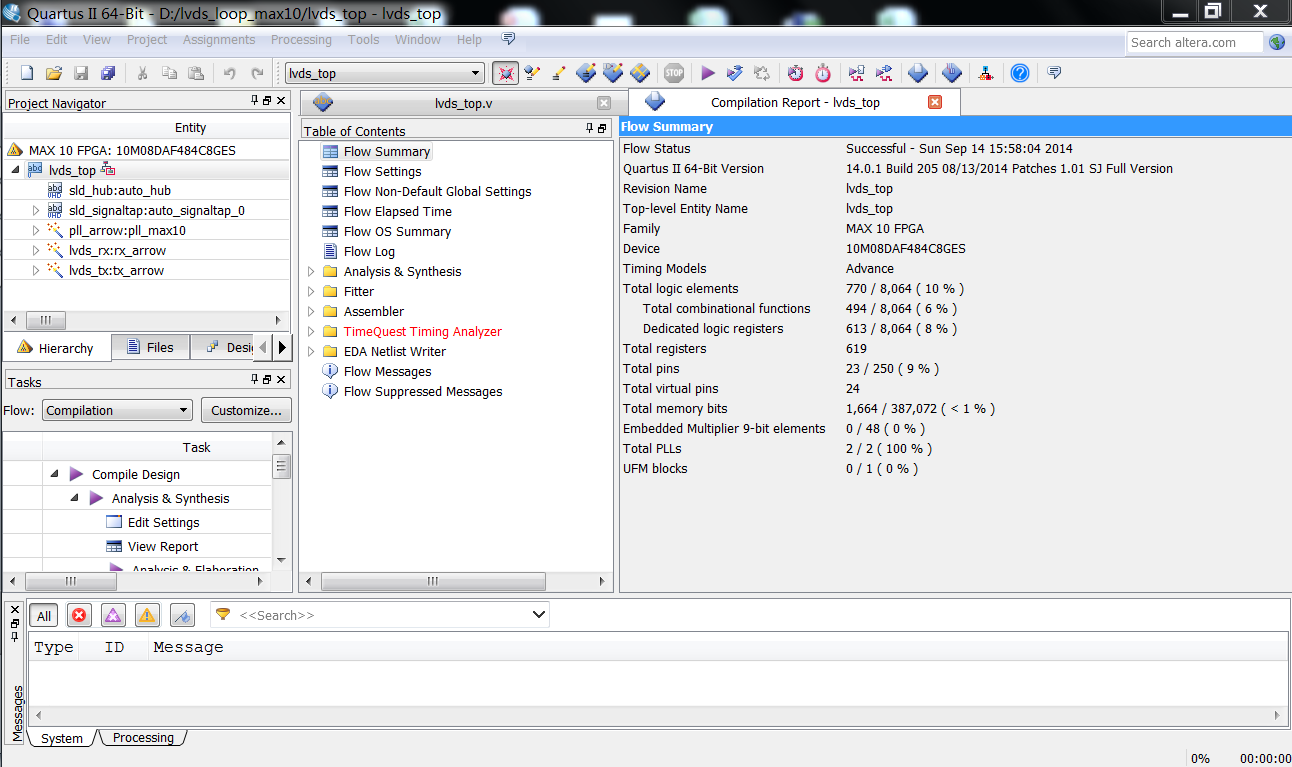
7.Altera PLL - Page1



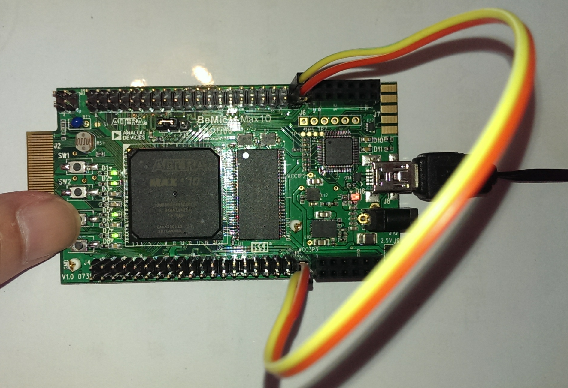
8.Altera PLL - Page2



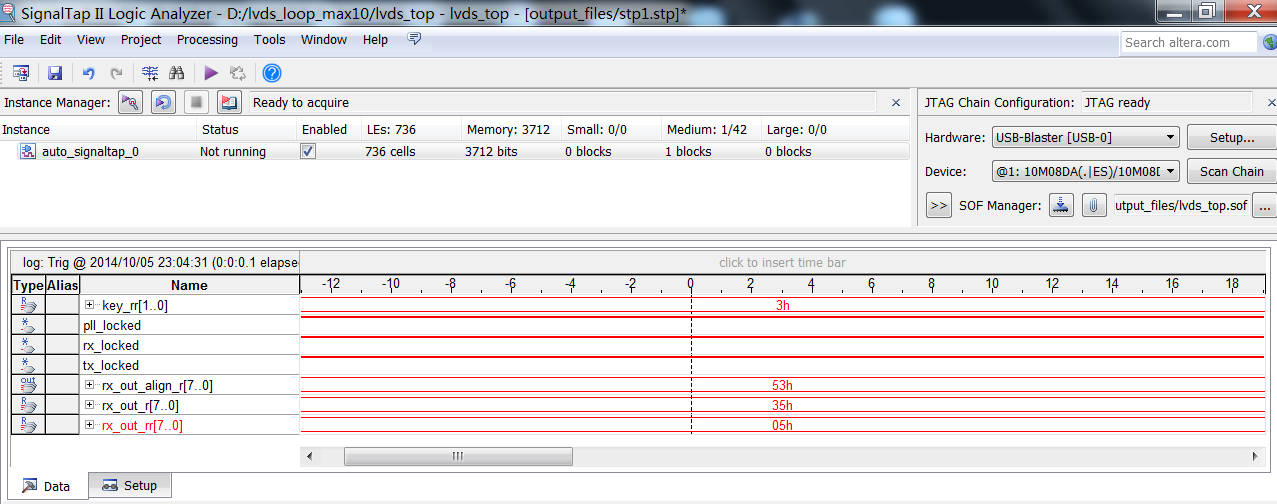
9.Finish the project looks like...



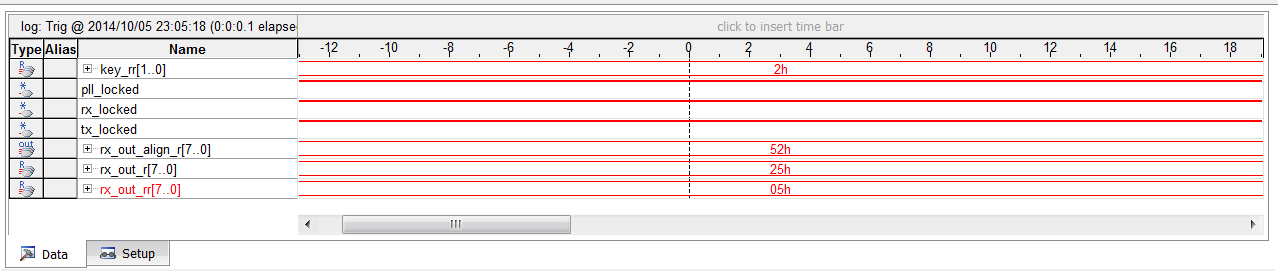
9.Connect the TX(P and N) with RX(P and N)



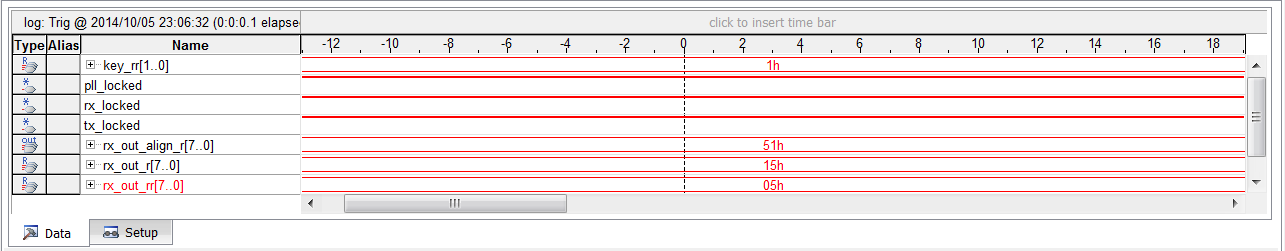
release all keys



push SW3



Push SW4



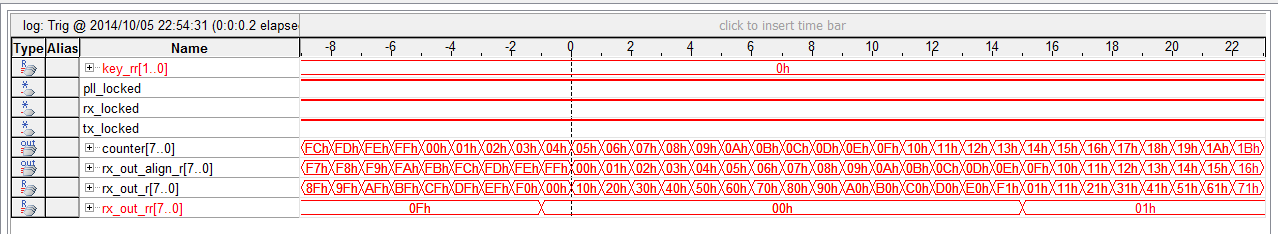
we can adjust the transmit data by below code

assign tx\_in\_custom = 8'hA1; // Display constant

assign tx\_in\_custom = counter; // Display Counter

assign tx\_in\_custom = {6'b010100,key\_rr}; // Display the SW3 and SW4 key value

use the counter in the transmit data



use the constant 0xA1 in the transmit data

