28V DC Power Distribution Modeling, Stability and Fault Detection (with reference with MIL-STD-704F)

Platform: MATLAB/Simulink + Simscape Electrical

Subsystems: Power Bus Model, Loads/Fault Injection, Sensor + ADC Chain, Fault Detection, Fault Classification, Stateflow Fault Manager, Test Sequence

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1. Introduction and Objectives

Aircraft and heavy-duty platforms widely use 28 V DC distribution networks for powering avionics, sensors, actuators and control units. In real systems, the bus can experience load variations, short circuits, open circuits, and ground faults. These faults may create voltage collapse, high currents, unstable transients, and may lead to unsafe operation if not detected quickly.

This project builds a simulation-based digital prototype of a 28 V DC distribution line using Simscape Electrical, and implements ECU-level fault monitoring logic using Simulink blocks, MATLAB Function, and Stateflow. The goal is to observe the physical behavior of the bus under fault conditions and to validate a structured fault handling strategy.

Main objectives

- Build a physical 28 V DC bus model with line resistance/inductance and configurable loads.
- Inject realistic fault conditions:
  - Normal load / Heavy load
  - Short circuit (bus-to-ground or near-zero resistance path)
  - Open circuit (load disconnected)
  - Ground fault (return path degradation / unintended ground path)
- Implement a realistic measurement chain:
  - Voltage sensing (Simscape sensor)
  - Signal conditioning concept (divider gain/offset model)
  - ADC quantization (12-bit)
  - Filtering (low-pass) and optional noise/EMI injection
- Develop fault detection logic aligned with MIL-STD-704F-oriented voltage limits:
  - Undervoltage detection (UV) with hysteresis and debounce
- Develop a fault classification block to identify Short/Open/Ground using V/I signatures.
- Implement a Stateflow Fault Manager to apply:
  - Priority rules (example: Short > Open > Ground)
  - Debounce timing (time qualification)

2. 28V DC Bus Physical Modeling (Simscape)

This project models a simplified 28 V DC power distribution bus in Simscape(Figure 1). The electrical source is represented by an ideal 28 V supply together with a source internal resistance (R_{source} = 0.1 Ω)**.** This internal resistance is used to emulate the non-ideal behavior of a real power supply and upstream distribution components. The distribution wiring is modeled using a line resistance (R_{line} = 0.2 Ω**)** and a small line inductance (L = 20 μH)**.** The line resistance represents copper losses and connector/contact resistances.

The inductance represents the natural inductive behavior of cables and harness loops, which becomes important during fast transients such as switching events and short circuits. A nominal load is modeled with R_{line} = 56 Ω**,** which draws approximately 0.5 A at 28 V (P=~14 W). This value provides a realistic "light/normal load" condition and helps observe small voltage drops across source and line impedances.

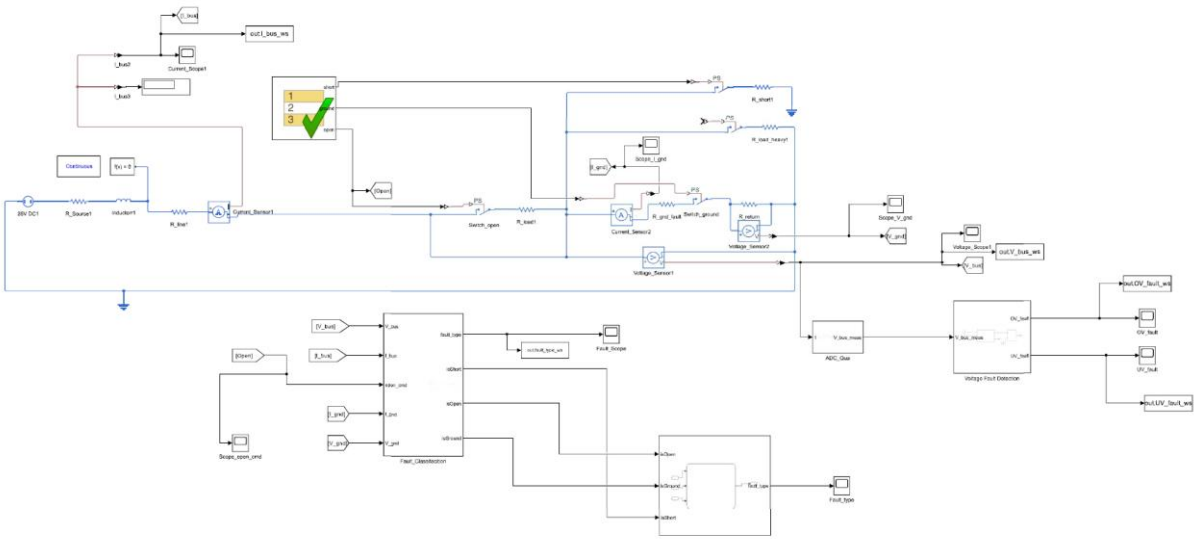

Figure 1: 28V DC bus modeling physical modeling

3. Fault Injection Scenarios (Heavy / Short / Open / Ground)

Fault scenarios are injected using controlled switches and dedicated resistive paths:

- **Heavy load (at 0-2 sec):** The heavy load is modeled by R_{load_heavy} = 14 Ω, which increases the current to about 2 A at 28 V (P ≈ 56 W). This scenario is used to observe bus voltage sag due to the voltage drop on R_{source} and R_{line} under higher current.
- **Short circuit (at 2-3 sec):** A short circuit is approximated by a very small resistance R_{line} = 0.001 Ω**.** In this case, the current becomes very high, and the bus voltage collapses mainly because the source and line impedances limit the current and create a large voltage drop (V_{drop} = I·(R_{source} + R_{line})). This is expected behavior in real systems: the supply cannot maintain 28 V under a severe short.
- **Open circuit (at 3-4 sec):** The open condition is created by opening the main load path. In an open circuit, the load current becomes near zero and the bus voltage returns close to the nominal value, except for measurement and numerical effects.
- **Ground fault (at 4-5 sec):** A ground fault is modeled using R_{gnd_fault} = 5 Ω to represent a resistive leakage path to ground. This creates an additional current path and can cause partial voltage drop depending on the total equivalent resistance. The value is chosen to create a measurable fault current without making the system behave like a hard short.

Why voltage collapses occur: Voltage collapse is mainly caused by high current flowing through the non-zero impedances (R_{source} and R_{line}). When the current increases (heavy load, short, or ground fault), the voltage drop increases and the measured bus voltage decreases accordingly.

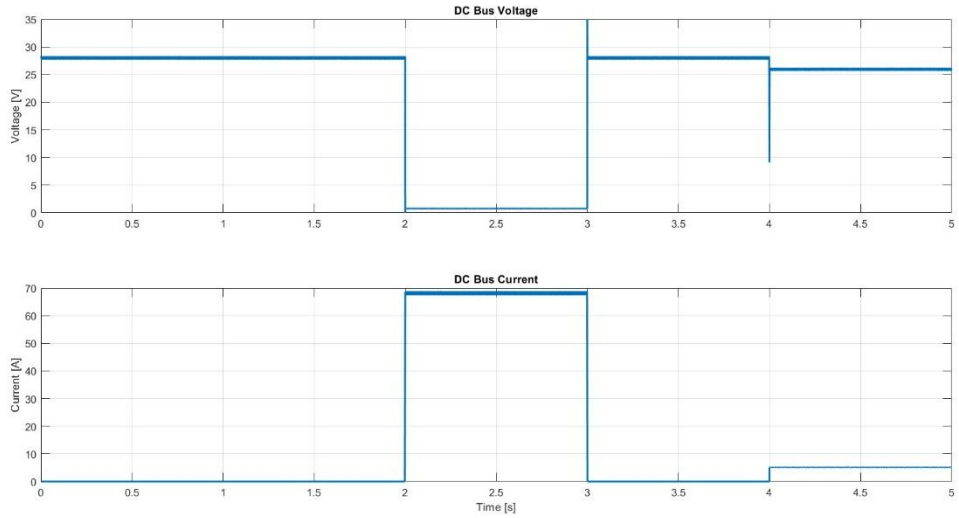

Figure 2: Fault injection scenarios (heavy, short, open, ground)

4. Sensor & Measurement Chain (Divider + ADC + LPF + Noise / EMI)

4.1 Purpose of the Measurement Chain

28 V DC power distribution systems, the bus voltage cannot be measured directly by an ECU due to ADC input limitations, noise sensitivity, and safety constraints. Therefore, a realistic sensor and measurement chain is implemented to represent how the DC bus voltage is conditioned before being processed by fault detection and classification logic.The objective of this section is to model:

- Voltage scaling suitable for ADC input range
- Quantization effects of a digital ADC
- Noise and EMI influence on measurements
- Signal conditioning using low-pass filtering

This approach ensures that fault detection logic is tested with realistic measurement behavior, not ideal signals.

4.2 Voltage Sensing and Divider Model

The DC bus voltage is first measured using a Voltage Sensor block placed directly on the 28 V DC bus. To represent practical ECU hardware, the measured voltage is passed through a voltage divider(Figure 2), reducing the signal amplitude to a level compatible with typical ADC input ranges (0–5 V or 0–3.3 V).

This divider does not affect system dynamics but ensures:

- Safe voltage levels at the ADC input
- Correct scaling for digital processing

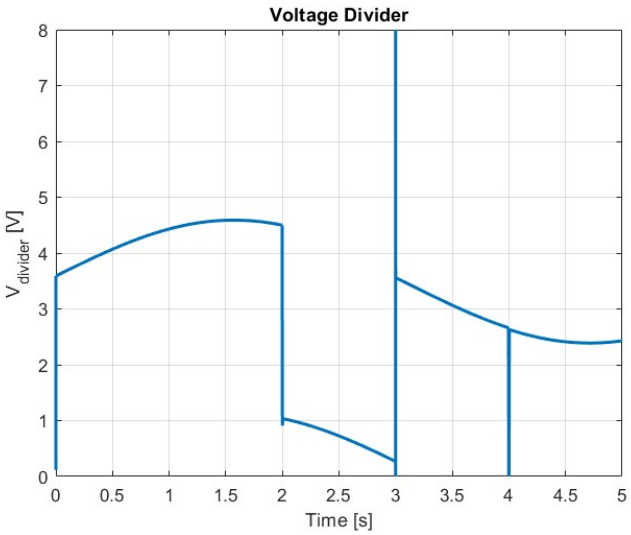

Figure 2: DC Bus Voltage (with divider)

4.3 ADC Quantization Modeling

After voltage scaling, the signal is converted into a digital representation using an ADC quantization model**.** A fixed-resolution ADC was assumed, introducing quantization steps that reflect real embedded systems behavior.

This stage introduces:

- Finite resolution effects
- Small measurement inaccuracies
- Step-like behavior in the digital signal

These effects are critical for testing threshold-based fault logic, especially near undervoltage and overvoltage limits.

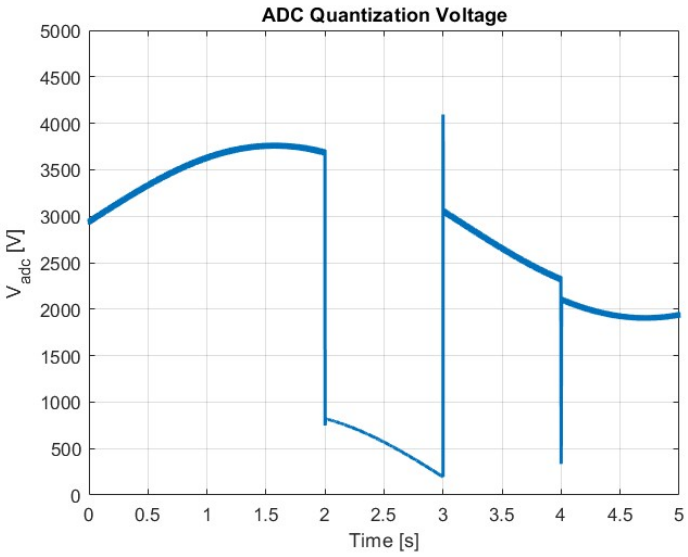

Figure 3: ADC Quantized Bus Voltage Signal

4.4 Noise and EMI Injection

In real aircraft electrical systems, voltage measurements are affected by:

- Switching noise from power electronics
- EMI coupling through wiring harnesses
- Ground reference disturbances

To represent these effects, noise and EMI components is injected into the measured voltage signal(Figure 4). This includes high-frequency ripple and low-amplitude random noise.

The purpose is not to model exact EMI physics, but to:

- Stress fault detection algorithms
- Prevent unrealistically clean signals
- Evaluate robustness of debounce and hysteresis logic

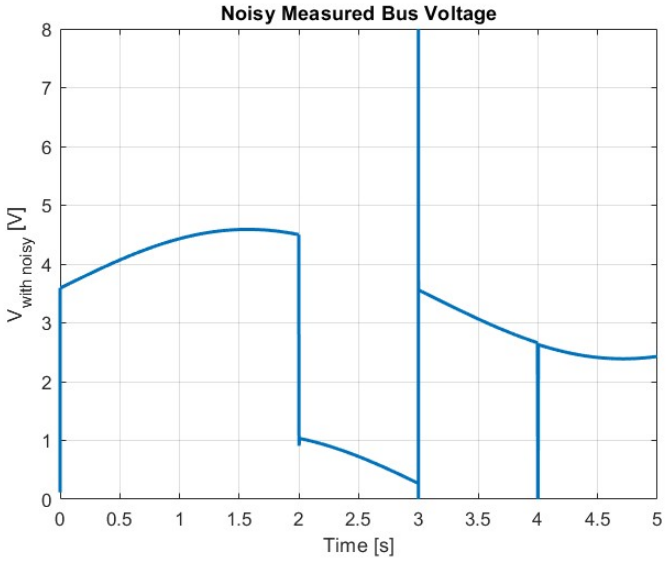

Figure 4: Noisy Measured Bus Dividing Voltage (Before Filtering)

4.5 Low-Pass Filtering (Signal Conditioning)

A low-pass filter (LPF) is applied to the noisy measurement signal to represent analog signal conditioning commonly used before ADC sampling or inside digital filtering stages.

The filter:

- Attenuates high-frequency noise
- Preserves slow voltage variations caused by load and fault events
- Improves stability of fault detection logic

This step is essential to avoid false fault triggering due to transient noise spikes.

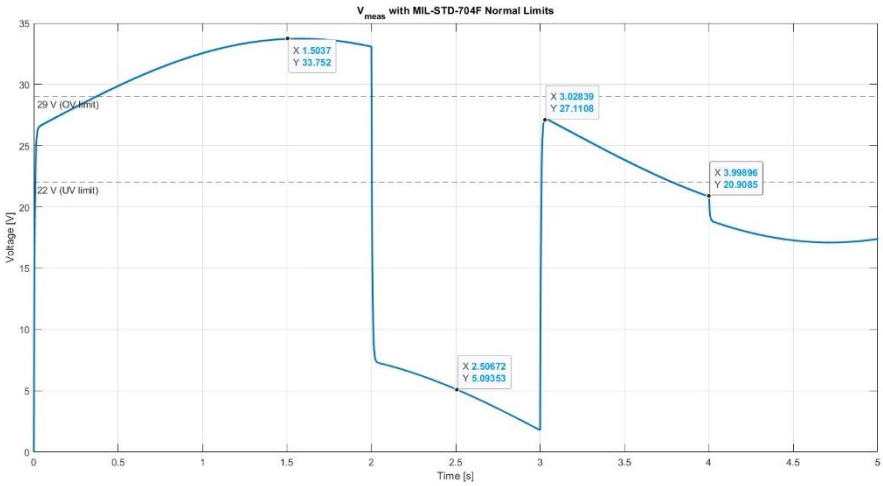

Figure 5: Filtered Bus Voltage Signal (V_{meas}) with MIL STD 704 tresholds

4.6 Low-Pass Filter Design for Voltage Measurement

To obtain a reliable DC bus voltage measurement, the raw voltage signal is passed through a low-pass filter (LPF). In aircraft DC power systems, voltage sensors are exposed to high-frequency noise caused by switching devices, wiring harness inductance, and electromagnetic interference (EMI).

A first-order low-pass filter is selected due to its simplicity, numerical stability, and suitability for real-time embedded systems.

The continuous-time transfer function of the low-pass filter is given by:

$$H(s) = \frac{1}{1 + s\tau}$$

where τ is the time constant of the filter.

The cutoff frequency is defined as:

$$f_c = \frac{1}{2\pi\tau}$$

In this study, the cutoff frequency is selected to attenuate high-frequency noise while preserving the dynamic behavior of the DC bus voltage during fault events. The filter ensures that short-duration noise spikes do not cause false undervoltage or overvoltage detections.

4.7 Output of the Measurement Chain

The final output of the sensor and measurement chain is the filtered digital voltage signal (V_{meas})**.**
This signal is used as the sole input for:

- Undervoltage / overvoltage detection
- Debounce and hysteresis logic
- Fault classification and Stateflow-based fault manager

By separating physical voltage (V_{bus}) and measured voltage (V_{meas}), the model clearly distinguishes between system behavior and ECU perception.

This separation is critical in safety-critical systems, where faults must be detected based on what the ECU measures**,** not the ideal physical value.

5. Voltage Fault Detection (Undervoltage / Overvoltage Logic with Hysteresis and Debounce)

5.1 Purpose of Voltage Fault Detection

In aircraft electrical power distribution systems, monitoring the DC bus voltage is a critical safety function. Sudden load changes, short circuits, ground faults, or generator transients may cause the bus voltage to move outside its safe operating range. The voltage fault detection subsystem monitors the measured DC bus voltage (V_meas) and generates stable undervoltage and overvoltage fault signals under dynamic load and fault conditions.

5.2 Undervoltage and Overvoltage Thresholds

Based on typical 28 V DC power system limits, the following thresholds are defined:

- **Undervoltage threshold (UV_ON):**
  The bus voltage is considered undervoltage when it drops below a predefined minimum level(Figure 7).
- **Overvoltage threshold (OV_ON):**
  The bus voltage is considered overvoltage when it exceeds a predefined maximum level(Figure 8).

These thresholds are selected to represent safe operational limits of a 28 V DC bus and are consistent with aircraft and heavy-duty vehicle electrical systems.

The measured bus voltage (V_{meas}) is continuously compared against these limits using comparator logic implemented in Simulink.

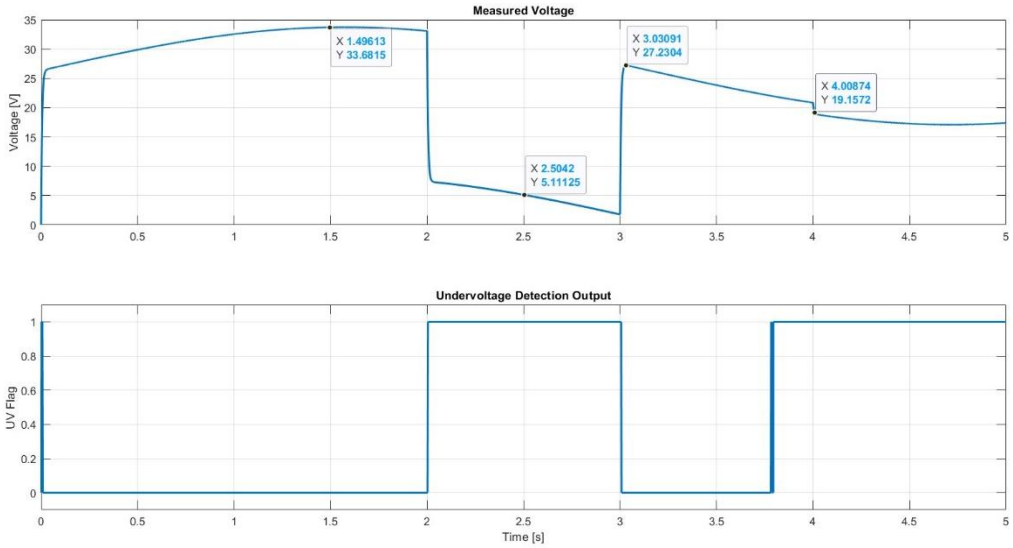

Figure 7: V_{meas} voltage vs time with UV

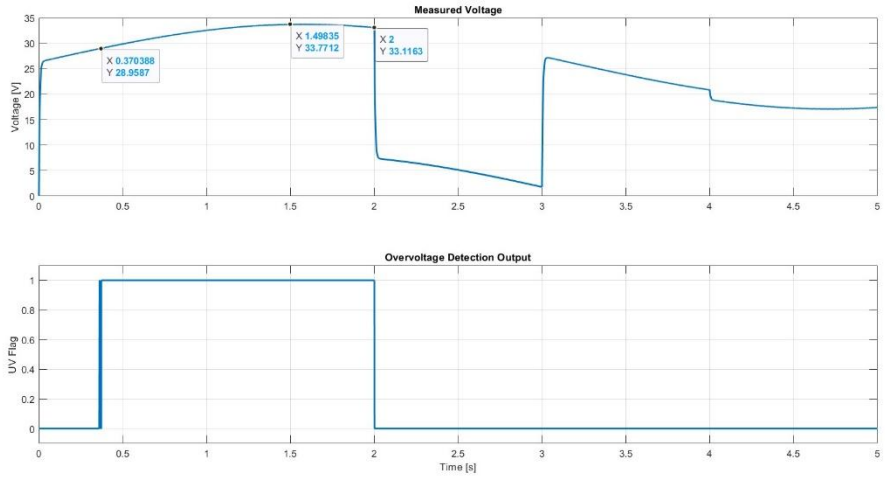

Figure 8: V_{meas} voltage vs time with OV

5.3 Hysteresis Implementation

In real aircraft power systems, the DC bus voltage may fluctuate around the threshold values due to load changes, noise, or transient conditions. If a fault detection logic reacts immediately at a single threshold, this may cause false triggering and unstable fault flags.

To avoid this behavior, a hysteresis mechanism is implemented in the voltage fault detection logic. Separate voltage levels are defined for fault entry and fault recovery. Once an undervoltage condition is detected, the system requires the voltage to rise above the recovery threshold before clearing the fault.

This hysteresis approach improves robustness and prevents rapid toggling of the undervoltage and overvoltage flags when the measured voltage oscillates near the MIL-STD-704F limits.

5.4 Debounce Logic

In addition to hysteresis, a time-based debounce logic is applied to the voltage fault detection. Short-duration voltage dips or spikes may occur during switching events or fault transitions, but these events do not always represent a real fault condition.

To filter out such transient effects, the voltage must remain below or above the defined threshold continuously for a predefined delay time before a fault flag is asserted.

In this model, a delay of 0.10 seconds is used for undervoltage detection and 0.05 seconds for overvoltage detection. This debounce mechanism ensures reliable fault detection and reduces sensitivity to short disturbances.

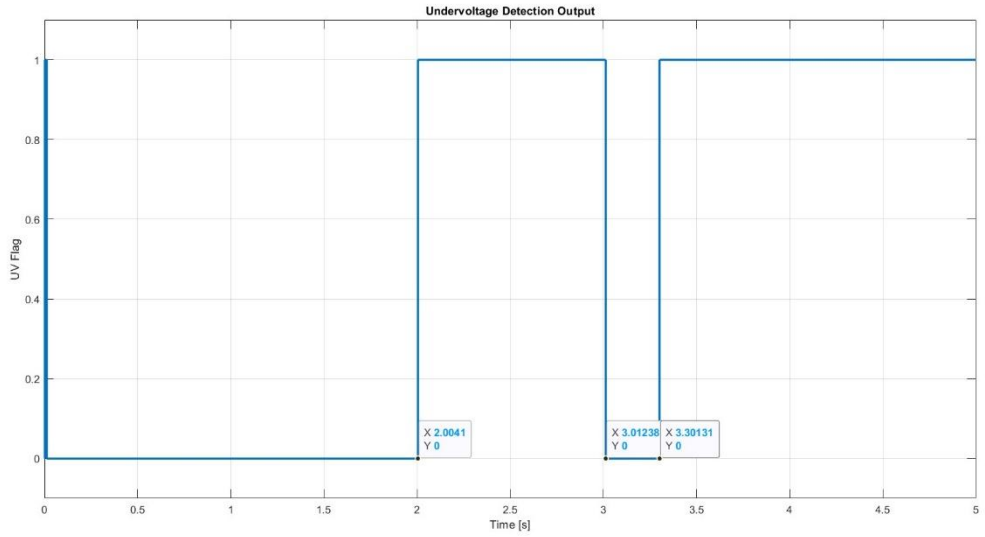

Figure 10: Debounce behavior during short-duration voltage transients

6. Fault Classification Logic (Short / Open / Ground)

In this section, a fault classification logic is developed to identify different electrical fault types on the 28 V DC power distribution bus. The purpose of this logic is to distinguish short circuit**,** open circuit**,** and ground fault conditions based on measured voltage and current behaviors.

The classification logic is implemented at ECU level using MATLAB/Simulink and operates after voltage measurement and basic signal conditioning stages.

6.1 Motivation for Fault Classification

In aircraft power distribution systems, different fault types may cause similar symptoms such as voltage drop or current increase. However, each fault has a different physical root cause and requires a different system response.Therefore, it is not sufficient to detect only an undervoltage or overvoltage condition. The system must also determine which type of fault occurred to support fault isolation, maintenance actions, and safety decisions.

6.2 Classification Implementation

The classification logic is implemented using a MATLAB Function block that evaluates voltage and current thresholds simultaneously. Logical conditions are used to assign a unique fault code to each fault type.

The output of the classification block is a single fault indicator signal representing:

- Normal / heavy operation
- Short circuit
- Open circuit
- Ground fault

This output is monitored using a Scope block to verify correct fault transitions during simulation.

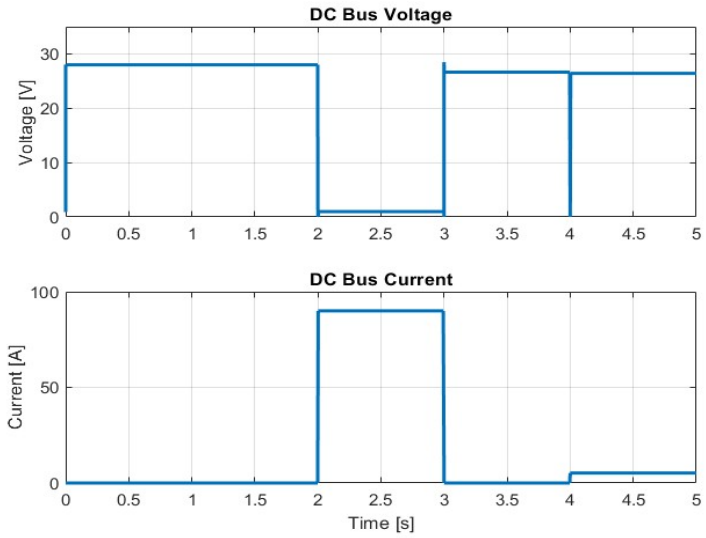

Figure 11: DC bus voltage and current at each fault level

7. Simulation Results and Validation

Bus Voltage Ripple and Measurement Noise Considerations

In the simulation model, voltage ripple (ripple $\leq$ 1.5V) is applied at the 28 V DC bus level to represent realistic power source behavior and load-induced variations. This ripple reflects the physical characteristics of the power distribution system rather than the ECU measurement process(Figure12).

For the ECU voltage measurement path, high-frequency noise and EMI effects are modeled separately using noise injection and signal conditioning blocks. A low-pass filter is applied to limit the measurement bandwidth and represent the analog front-end behavior of an ECU(Figure 13).

This separation allows the model to distinguish between system-level voltage ripple and measurement-level noise, providing a more realistic and physically meaningful simulation of aircraft power distribution and fault detection behavior(Figure 14).

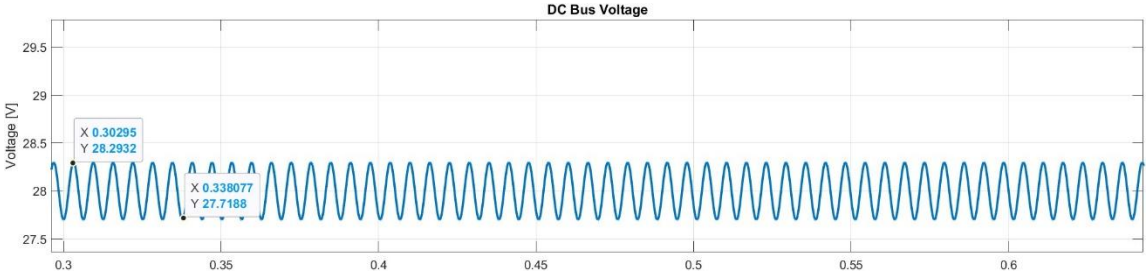

Figure 12: Voltage ripple referenced with MIL-STD-704F

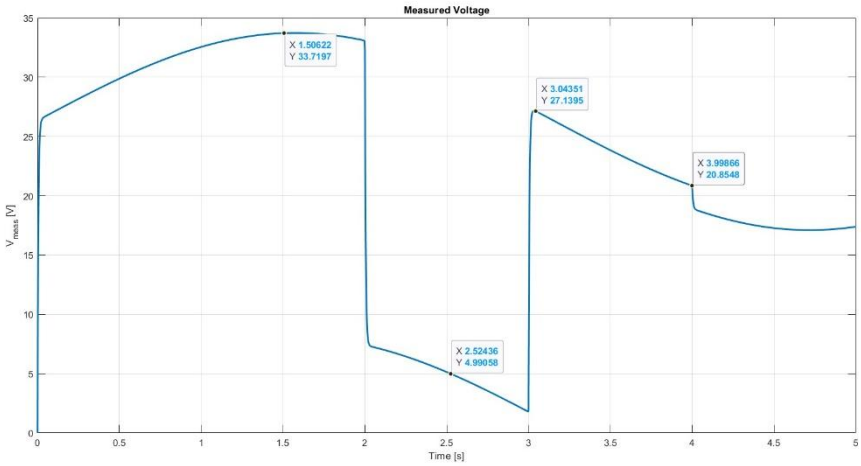

Figure 13: Measured voltage with noises

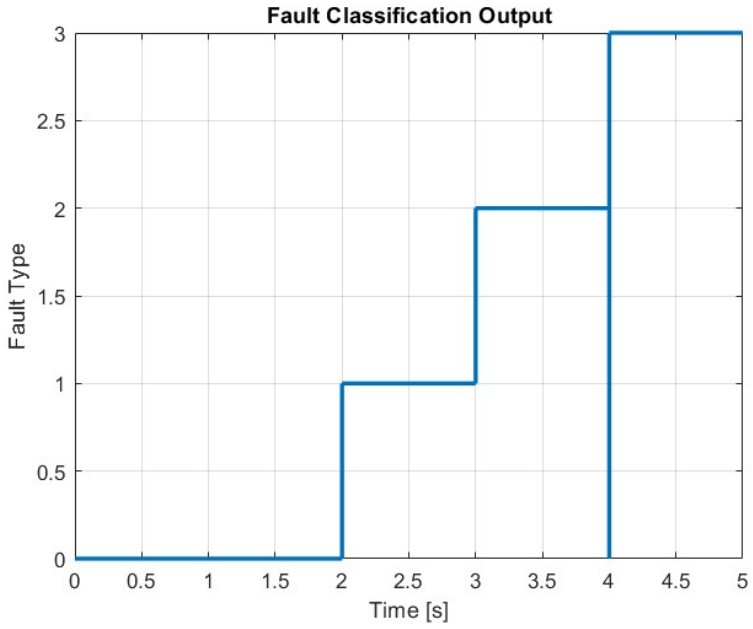

Figure 14: Fault Classification Output

8. Fault Manager with Stateflow

In this project, a Fault Manager was implemented using Stateflow to manage different fault conditions in a structured and deterministic way(Figure 13).

The Fault Manager receives fault signals (Short Circuit, Open Circuit, Ground Fault, Undervoltage, Overvoltage) from the fault detection and classification blocks. Each fault is handled according to a priority order, where critical faults (such as short circuit) have higher priority than non-critical ones.

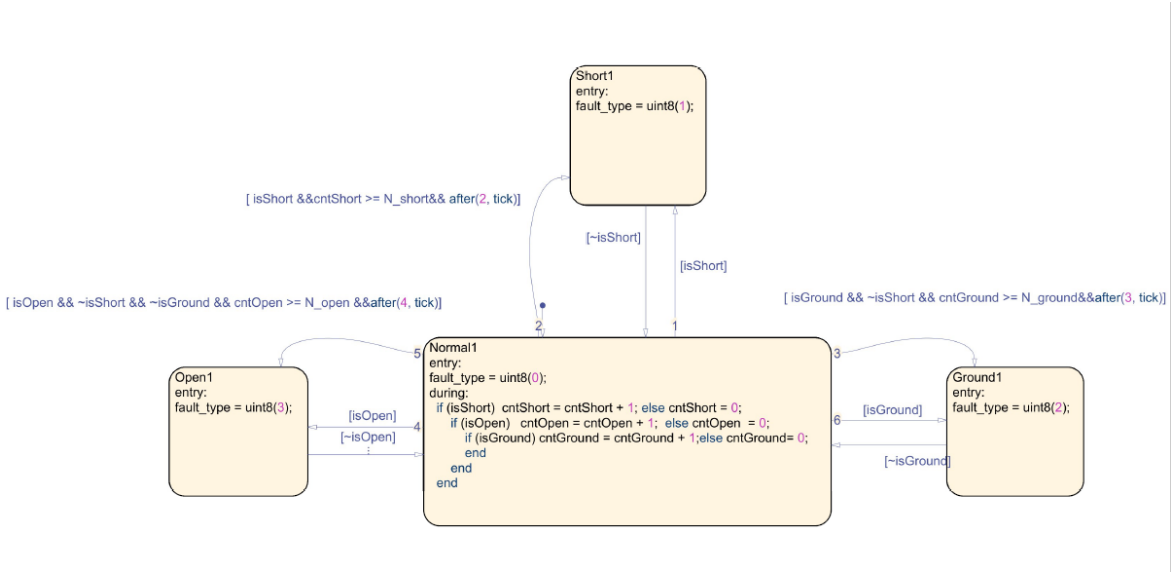

Figure 13: Fault Manager Chart

9. Conclusion

In this project, a 28 V DC power distribution system is successfully modeled and analyzed using MATLAB/Simulink. The electrical behavior of the DC bus is evaluated under normal operation as well as heavy load, short circuit, open circuit, and ground fault conditions. Voltage and current responses clearly showed the impact of each fault scenario on system stability and load behavior.

A voltage fault detection logic based on undervoltage (UV) and overvoltage (OV) thresholds is implemented in accordance with MIL-STD-704F normal operating limits. Hysteresis and debounce mechanisms is applied to prevent false fault triggering caused by noise, ripple, and transient events. The measurement chain, including voltage divider, ADC quantization, noise injection, and low-pass filtering, was shown to have a direct influence on the reliability of fault detection.

In addition, a fault classification algorithm is developed to distinguish between short circuit, open circuit, and ground fault conditions by analyzing voltage and current characteristics. A Stateflow-based fault manager is designed to handle fault prioritization, timing, and recovery behavior in a structured and scalable way.

Overall, the results demonstrate that a model-based design approach enables early verification of power distribution stability and fault handling strategies before real hardware testing. The developed simulation model provides a strong foundation for future extensions such as hardware-in-the-loop (HIL) testing or integration with real ECUs in aerospace or heavy-duty electrical systems.

10. References

[1]MIL-STD-704F, Aircraft Electric Power Characteristics, U.S. Department of Defense, 2016.

[2]MIL-STD-461F, Requirements for the Control of Electromagnetic Interference Characteristics of Subsystems and Equipment, U.S. Department of Defense, 2007.

[3]MathWorks, Simscape Electrical Documentation, MathWorks Inc.

[4]MathWorks, Stateflow User Guide, MathWorks Inc.

Appendix A – Key Parameters

Parameter	Value	Description
DC Bus Voltage	28 V	Nominal aircraft DC bus
R_source	0.1 Ω	Source internal resistance
R_line	0.2 Ω	Cable / line resistance
Inductor	20 µH	Line inductance
R_load	56 Ω	Nominal load
R_load_heavy	14 Ω	Heavy load condition
R_short	0.001 Ω	Short circuit simulation
R_gnd_fault	5 Ω	Ground fault resistance
Sampling Time	0.01 s	Discrete simulation step