Middle East Technical University - Department of Computer Engineering

CENG 232

Logic Design

Spring 2023-2024

Lab Assignment 2

Due date: Friday, April 5, 2024, 23:59

1 Introduction

This laboratory aims to familiarize you with some of the most important IC components, like multiplexers and decoders. You are expected to design your circuit using the CENG232 Logisim tool with the given gates below.

The Logisim submission will differ from the demo circuit you will build in the lab. It will contain an additional output and related IC components to generate that output.

2 IC Pool

- 74LS08 (AND)
- 74LS32 (OR)
- 74LS04 (NOT, Inverter)
- 74LS02 (NOR)
- 74LS00 (NAND)
- 74LS153 (Multiplexer)
- 74LS86 (XOR)
- 74LS138 (Decoder)

3 Lab Work

In this lab, you will be given three 2-bit numbers, A, B, and S, as inputs, and you are expected to implement the 3-bit output X. Additionally, for the **Logisim part**, you are expected to implement an 8-bit output Y. Requirements are given as follows:

- The digits of input **A** should be labelled as A1 and A0 where A0 is the least significant digit and A1 is the most significant digit.
- The digits of input **B** should be labelled as B1 and B0 where B0 is the least significant digit and B1 is the most significant digit.
- The digits of input **S** should be labelled as S1 and S0 where S0 is the least significant digit and S1 is the most significant digit.

- The output **X** is a 3-bit number which should be labelled as X2, X1 and X0 where X0 is the least significant digit and X2 is the most significant digit.
- The 8-bit output **Y** [Y7..Y0] will be used to display decimal numbers corresponding to the binary representation of X. Only one bit of Y is set at a time. For instance, Y0 corresponds to 0, and Y5 corresponds to 5 (or -3, please see Figure 1).

  If X is 110, Y is 01000000 or if X is 011, Y is 00001000
- Your design is expected to perform the following four operations depending on the value of S:
  - If S is 0, the X and Y outputs should display the result of A-B.
  - If S is 1, the X and Y outputs should display the result of max(A, B).
  - If S is 2, the X and Y outputs should display the result of 2*B.
  - If S is 3, the X and Y outputs should display the result of 2*A+1.

3.1 Implementation of A-B

This operation produces the result of A-B as a 3-bit number, and the X and Y outputs are used to represent it. For the negative values generated from A-B, you can use Figure- 1 for the mapping of negative values to positive values in 3-bit representation.

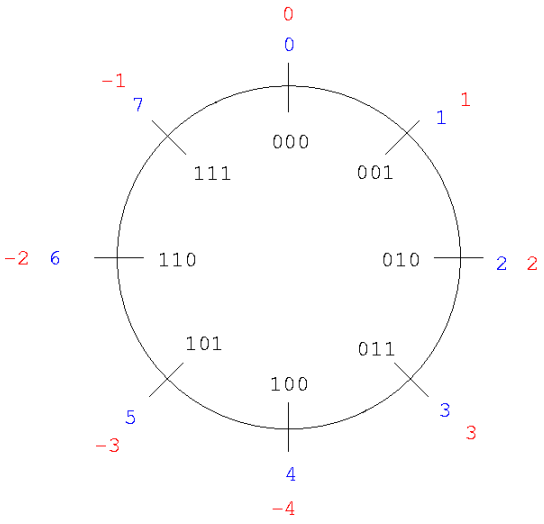

Figure 1: Mapping of negative numbers to positive numbers in 3-bit representation.

Input-Output Examples:

Inputs		Operation	Outputs	
A	B	A-B	X	Y
$(00)_2$	$(01)_2$	$(111)_2$	$(111)_2$	$(10000000)_2$
$(01)_2$	$(11)_2$	$(110)_2$	$(110)_2$	$(01000000)_2$
$(11)_2$	$(10)_2$	$(001)_2$	$(001)_2$	$(00000010)_2$
$(10)_2$	$(00)_2$	$(010)_2$	$(010)_2$	$(00000100)_2$

3.2 Implementation of max(A,B)

This operation produces a result depending on the larger number between A and B.
Input-Output Examples:

Inputs		Operation	Outputs	
A	B	max(A,B)	X	Y
$(10)_2$	$(01)_2$	$(010)_2$	$(010)_2$	$(00000100)_2$
$(00)_2$	$(11)_2$	$(011)_2$	$(011)_2$	$(00001000)_2$

3.3 Implementation of 2*A+1

This operation produces the result of 2*A+1.
Input-Output Examples:

Inputs	Operation	Outputs	
A	2*A+1	X	Y
$(10)_2$	$(101)_2$	$(101)_2$	$(00100000)_2$
$(01)_2$	$(011)_2$	$(011)_2$	$(00001000)_2$

3.4 Implementation of 2*B

This operation produces the result of 2*B.
Input-Output Examples:

Inputs	Operation	Outputs	
B	2*B	X	Y
$(10)_2$	$(100)_2$	$(100)_2$	$(00010000)_2$
$(01)_2$	$(010)_2$	$(010)_2$	$(00000100)_2$

Note: You are expected to implement your circuitry using only the ICs specified in the IC pool section.

4 Logisim-Only Part

In your Logisim submissions, you are expected to display the decimal conversion of X in the output Y for every operation. **Due to hardware restrictions**, **you will not build the circuit components that generate output Y in the lab.**

5 Free Session

After your homework is announced, there will be a *free session week*. You will have 2 hours in your free session slot. At the very beginning, a couple of the new ICs (for this assignment) will be introduced. In the remaining time of the free session, you may build your solution circuit on a breadboard by using IC components and practice how to handle possible problems related to a physical circuit on a breadboard.

6 Demo Session

There will be a 2-hour-long *demo session week* following the free session week. In the demo session:

- You will take a short quiz about the logic concepts that involve the coverage of this lab.
- You will reconstruct your circuit on your breadboard (without the output Y).
- You will show that the circuit drawn in Logisim works as specified (without the output Y).
- A sample solution will be published before the first demo session.

7 Labelling Specifications

- You have to use **pins** for your inputs and outputs. Please only set **label property** of the **pin** objects; do not add a **text object**.
- Your input pins should be labelled as A1, A0, B1, B0, S1 and S0.
- Your output pins should be labelled as X2, X1, X0, Y7, Y6, Y5, Y4, Y3, Y2, Y1 and Y0.
- Label properties are case-sensitive. Note that all labels consist of an uppercase letter followed by a number. **Please be very careful with the naming of labels.**
- If you need to feed any input with a constant value, you can use a constant gate. This gate is under the CENG232 Gates section. We will only set values for A1, A0, B1, B0, S1, and S0.
- You will receive a grade **penalty** unless labeling is done correctly.

8 Deliverables

- Please submit the circuit named e1234567.circ prepared in Logisim, which is your preliminary work, until the specified deadline. Please do not forget to replace e1234567 with your 7-digit student ID.
- The evaluation of the submission will be a **black-box test**.
- In the demo session, you will reconstruct and show that the circuit drawn in Logisim works. This part will be graded in the lab.
- You should use the CENG232 version of Logisim which is available on ODTUClass course page. Circuits designed with other Logisim versions, other tools, or that are not named properly **will not be graded**!

9 What to Bring in the Lab

- Circuit designs prepared with CENG232 Logisim (you can have them printed or downloaded on your phone/tablet, etc.).
- Data sheets of chips (you can have them printed or downloaded on your phone/tablet, etc.). www.alldatasheet.com
- Pencil and eraser, as you will have a quiz at the very beginning of demo sessions.

Note: The lab materials (gates, cables, etc.) will be distributed at the beginning of each lab session and will be collected at the end of the session. Therefore, you do not have to buy them. If you want to work out of the labs, you may still buy them. Moreover, if you would like to work with your own equipment (ICs, breadboard, cables, etc), you are free to bring them to the sessions as well.

10 Cheating Policy

All lab work should be done individually, and there is a zero-tolerance policy for cheating. Please see the course website for further information about the cheating policy.

11 References

- CENG 232 Logisim
- Discussions Page