A Laboratory Experiment in Linear Series Voltage Regulators

Jeffrey S. Franzone
University of Memphis

Abstract

Many advanced electronics courses cover linear voltage regulators from the *"black-box"* (or IC) perspective. Although this perspective is valid and useful, it doesn't give students much opportunity in a laboratory setting to deeply investigate the behavior of the major parts of the regulator, its characteristics, and the reinforcement of transistor theory. Many *"canned"* linear voltage regulator labs favor the *"quick-and-dirty"* approach. Students construct a power supply using a linear voltage regulator IC, make a few measurements, and observe empirically the stability of the output voltage with line and load changes. With these labs, students miss the opportunity to see what makes a regulator *"tick"* and how different elements of the regulator affect particular regulator characteristics. The laboratory experiment presented here tries to address some of the issues that are not covered in depth in common linear voltage regulator experiments. They include:

- Students build a real regulator circuit from discrete transistors. Students actually see the major parts of the regulator and the interaction between each section.

- Students learn the real meaning of terms such as line and load regulation, % efficiency, and maximum and minimum differential voltage by observing what factors in the regulator actually influence these parameters.

- In traditional experiments, constant-current limiting is the only protection scheme shown. This lab not only demonstrates this technique but also foldback-current limiting. The advantage of foldback-current limiting over constant-current limiting is illustrated by an empirical heatsink test. The regulator circuit is first designed with constant-current limiting. The regulator is shorted and students observe that a heatsink is required. Next, the same circuit is constructed with foldback-current limiting. The output is shorted and students observe that a heatsink is not required.

- Students get to simulate on PSPICE the regulator circuit with constant-current limiting and with foldback-current limiting. The waveforms generated from each circuit clearly emphasize the circuit action and effectiveness of each protection scheme and support the laboratory results.

- Extensive analysis questions are provided throughout the experiment to enhance the students problem solving skills. Many questions require detailed explanations using laboratory measurements, calculations, and simulation results.

The laboratory experiment has been successfully tested in an advanced solid-state course in community college and is currently taught in an advanced electronics course at the University of Memphis, Engineering Technology Department. Many positive responses were noted from students. Many commented that the depth and breadth of the experiment was difficult, at times, to digest but very useful in understanding linear voltage regulators and in improving their transistor theory and problem-solving skills. Many really appreciated the practical sections on current protection.

I. Introduction

The linear series voltage regulator lab experiment is divided into the following major sections:

1. BACKGROUND
2. OBJECTIVES
3. EQUIPMENT
4. PROCEDURE
5. ANALYSIS QUESTIONS
6. REFERENCES

This paper will briefly examine each of these sections providing relevant examples from the actual laboratory experiment. The complete experiment is provided at the end of this paper. Because the experiment relies heavily on solid state theory and extensive analysis, it is recommended that students should have completed at least one semester of solid state electronics and preferably some limited experience with PSpice for Windows to be successful with this experiment. The lab experiment should be completed within six hours, not including a laboratory report. For a three-hour lab that meets once a week, this experiment would be a two-week lab. The author recommends assigning PART I, II, and III for the first three hours of lab with PART IV and V for the last three hours. Since the Procedure is divided into separate sections each having its own set of analysis questions, the experiment can be easily adapted to fit the particular rigor of the instructor.

II. BACKGROUND

This section discusses many of the important concepts related to linear voltage regulators. The depth of this section is sufficient to be used as lecture material and provides important concepts and formulas necessary to successfully complete and understand the experiment.

The basic concepts and terminology necessary for understanding the overall operation of a series voltage regulator are discussed first before any detailed analysis. In particular, functional blocks are shown for each major section of a voltage regulator. This gives students the "big picture" and helps to emphasize the relationships between each block. Shown below is an excerpt:

- A voltage regulator is a device that maintains a constant voltage across a load even if the load current requirements change. Voltage regulators are a major building-block in power supplies. (NOTE: in some circuits, the voltage regulator is the actual power supply.)
- A linear series voltage regulator contains a *"control element"* (usually a transistor) that always operates in the active region, hence the term *"linear"*. The control element is in *"series"* between the unregulated line voltage and the regulated output voltage. When the control element is a transistor, it is often referred to as the *"pass transistor"* since it *"passes"* the required current to maintain a predetermined amount of regulated output voltage.

- The main elements of a linear series voltage regulator include:
  1. A control element.
  2. A reference voltage
  3. An error detector.
  4. A sample circuit.

  Figure 1 shows the interconnection of these elements.

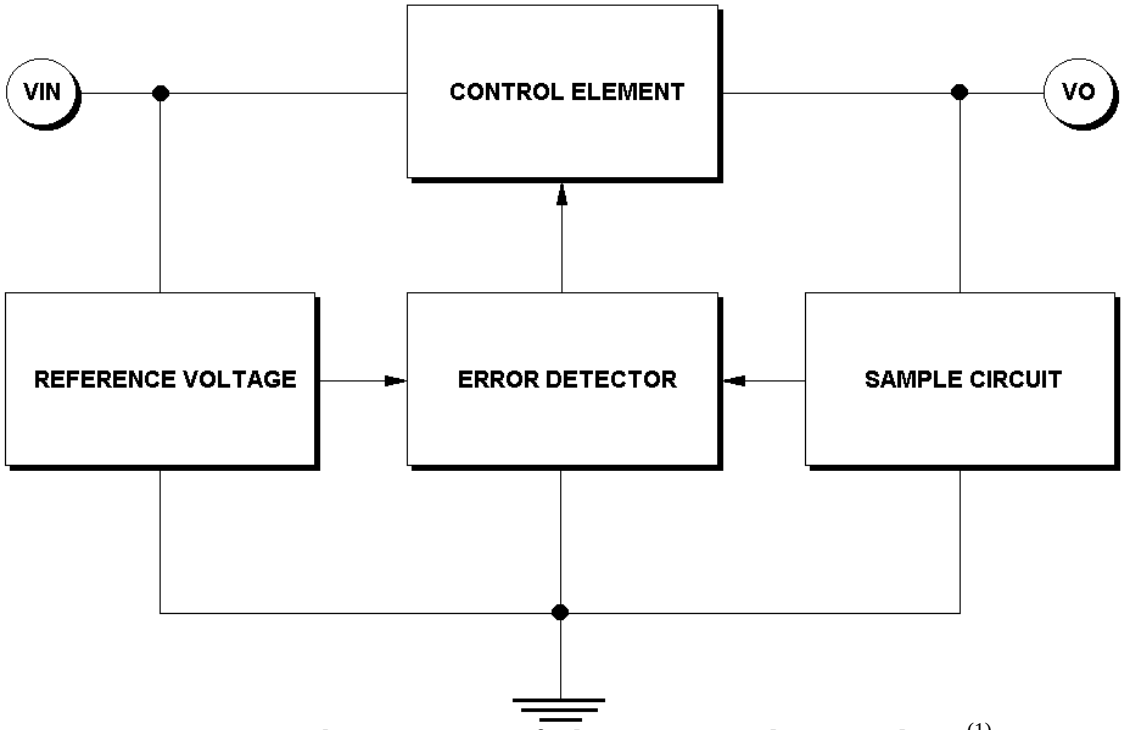


FIGURE 1. The major parts of a linear series voltage regulator.[1]

The basic operation of the linear series voltage regulator is as follows:

- An error detector compares a reference voltage with a sample of the output voltage. The output of the error detector is fed to a control element. The control element causes the output voltage to increase or decrease until the sample voltage equals the reference voltage. When this occurs, the error voltage is zero (or some other setpoint value) and the control element is held in a stable state. This keeps the output voltage relatively constant regardless of the load requirements (within specific limits, of course).

A detailed discussion of two voltage regulator circuit types are introduced; one built around transistors and the other built around an op-amp. Both circuits are used to identify the circuit components that compose each of the major functional blocks of a voltage regulator and to explain how these blocks interact. In addition, the advantage of an op-amp error-detector versus a transistor error-detector in improving the regulator's transient response is discussed.

Next, some important voltage regulator characteristics are examined such as load and line regulation, percent efficiency, and the relationship between the amount of differential voltage across the pass transistor and its ability to regulate. Students learn first-hand how to test and measure these characteristics in the experiment.

Finally, the concepts of constant-current limiting and foldback-current limiting are discussed. Each protection scheme is examined in depth, including transfer characteristics and all relevant design formulas. Students have the opportunity to design, test, and observe both protection schemes on the experimental voltage regulator circuit. Shown below are the transfer characteristics for each protection scheme. Students learn how to use PSpice to simulate these curves and how to interpret them.

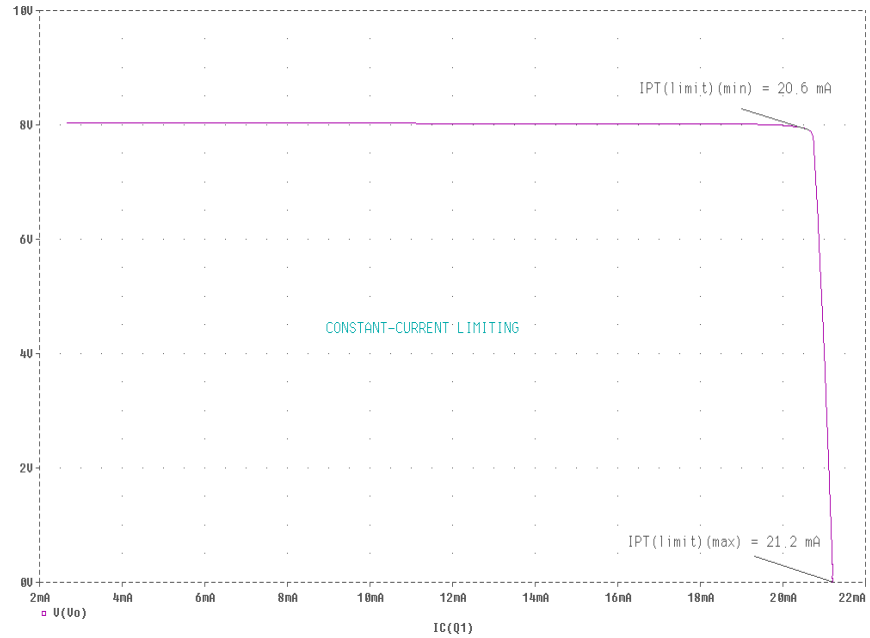


FIGURE 6. Vo vs. $I_{PT(limit)}$ for constant-current limiting protection scheme.

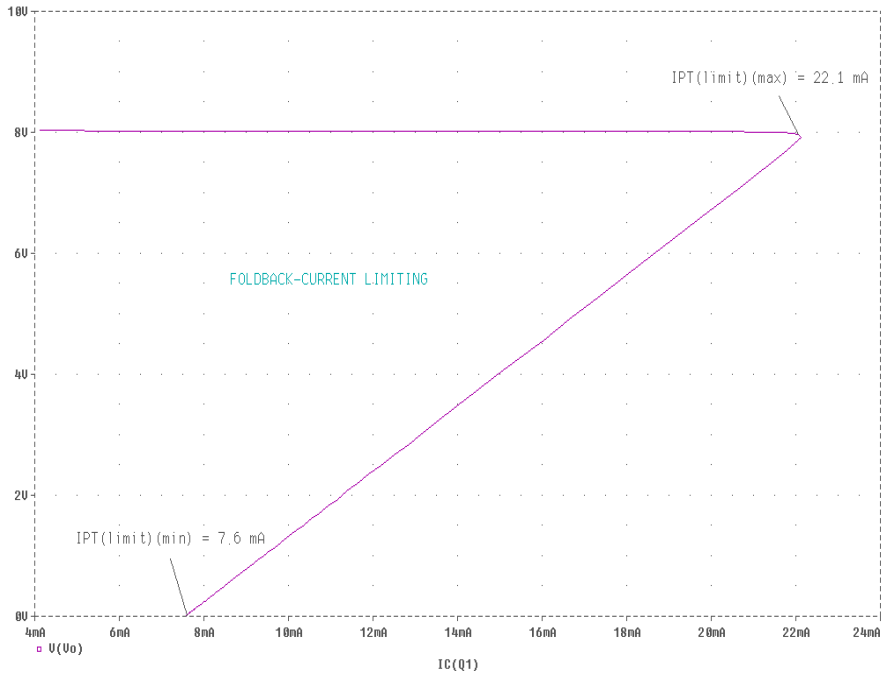


FIGURE 9. Vo vs. $I_{PT(limit)}$ for foldback-current limiting protection scheme.

III. OBJECTIVES

This section identifies the major concepts that will be examined in the experiment. Shown below is an excerpt:

> In this lab experiment, you will investigate some of the important characteristics of linear series voltage regulators such as
>
> - The major parts of the voltage regulator and how they work.
> - Load and line regulation ratings.
> - Percent efficiency rating.
> - Minimum differential voltage needed for regulation.
> - Heatsinking requirements.
> - Constant-current limiting and foldback-current limiting.

IV. EQUIPMENT

This section lists the necessary parts and test equipment needed for the experiment.

V. PROCEDURE

This section shows all pertinent experiment schematics and explains in detail the calculations, measurements, and simulations that need to be completed for each major regulator concept. The experimental voltage regulator circuit that students will build, modify, test, and measure is shown below:

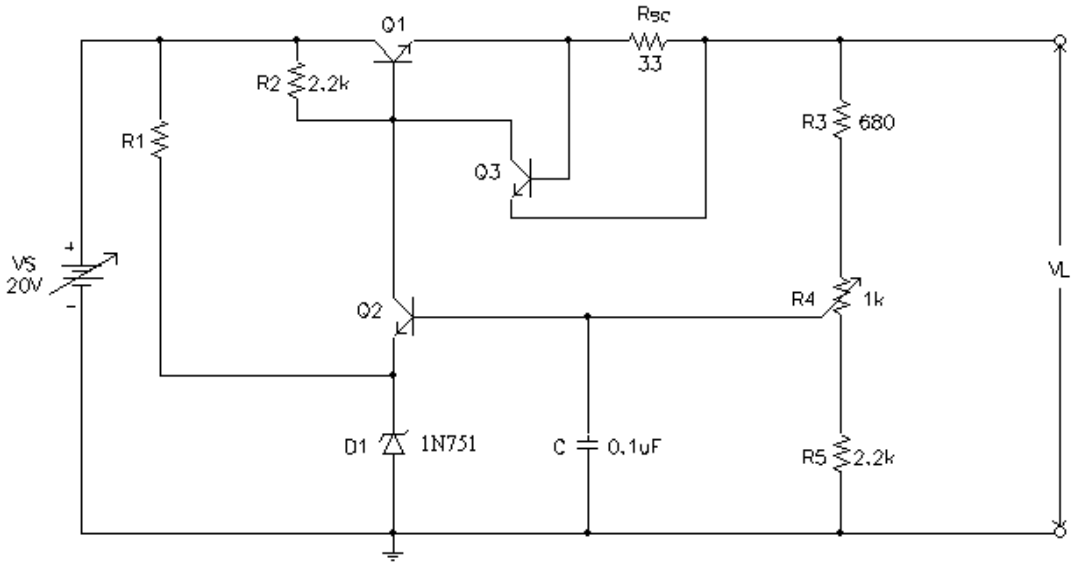


FIGURE 10. Experimental voltage regulator circuit.[2]

The procedure is divided into the following five subparts:

1. PART I - Zener diode biasing, output voltage range, and regulator gain.
2. PART II - Load and line regulation.
3. PART III - Constant-current limiting and heatsinking.
4. PART IV - Percent efficiency and differential voltage.
5. PART V - Foldback-current limiting.

In PART I, students design the biasing network for the zener diode reference voltage and measure the minimum and maximum output voltage produced by the regulator. From the theory presented in the BACKGROUND section, students determine the minimum and maximum closed-loop gain of the regulator. With this procedure, they learn how to apply the concepts of closed-loop gain to discrete transistor regulator circuits and the circuit equivalence of op-amp regulator circuits and transistor regulator circuits.

PART II investigates load and line regulation characteristics. Load regulation refers to a regulator's ability to maintain a constant output voltage when load requirements change. Students learn how to measure and calculate load regulation using several different no-load and full-load voltages. They observe that load regulation figures vary depending on the chosen no-load voltage and load requirements. (Many manufactures choose the best region of operation when listing load regulation figures.) Below is a sample excerpt:

4). Adjust R4 for a load voltage of +8V. Record this as the no-load voltage V_{NL}.

V_{NL} =

5). Connect a load resistance of 10kΩ. Measure the load voltage V_L. Record this value as the full-load voltage V_{FL}. Repeat this step with 1kΩ, 330Ω, and 100Ω.

$V_{FL\ (with\ 10k\Omega)}$ =

$V_{FL\ (with\ 1k\Omega)}$ =

$V_{FL\ (with\ 330\Omega)}$ =

$V_{FL\ (with\ 100\Omega)}$ =

6). Using measured values, calculate and record the percent load regulation for each of the load resistors using the following formula[4]:

$$\%L.R. = \frac{\mathbf{V_{NL} - V_{FL}}}{\mathbf{V_{FL}}} \times 100\%$$

$\%LR_{(\text{with } 10k\Omega)} =$

$\%LR_{(\text{with } 1k\Omega)} =$

$\%LR_{(\text{with } 330\Omega)} =$

$\%LR_{(\text{with } 100\Omega)} =$

Line regulation refers to a regulator's ability to maintain a constant output voltage with changes in input (or line) voltage. Students learn how to measure and calculate line regulation with a 20% line change. This percentage is chosen as a worst-case value and provides a good indication of the performance of a regulator when its line voltage contains a large ripple voltage.

PART III investigates the most common protection scheme used for voltage regulators: constant-current limiting. Before students modify the experimental circuit, they use PSpice to simulate the transfer curve for this protection scheme. Since constant-current limiting is new to most students, PSpice emphasizes how simulation can be used to see the operation of a concept before building a circuit. Armed with the transfer curve, students can visually see how constant-current limiting works making them better prepared to interpret lab data when they incorporate the protection scheme into the experimental circuit. Here is the experimental circuit modified with constant-current limiting and the PSpice procedure:

12). Figure 11 employs one of the most common regulator protection schemes: constant-current limiting.

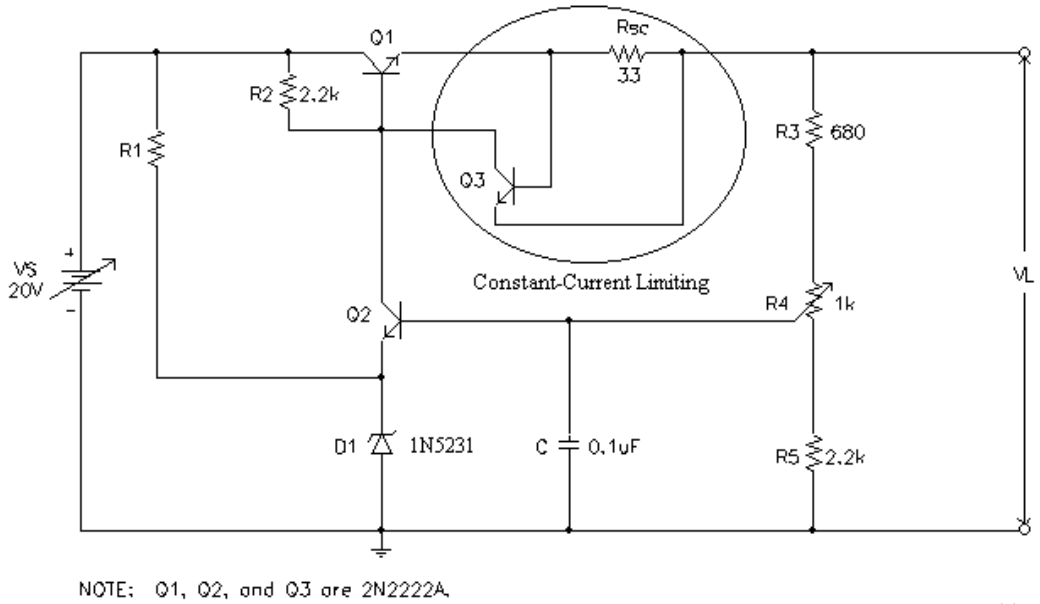


FIGURE 11. Series regulator with constant-current limiting (Q3 and R_{SC}).[2]

Draw and simulate the circuit of Figure 11 in PSpice Schematics with the following modifications:

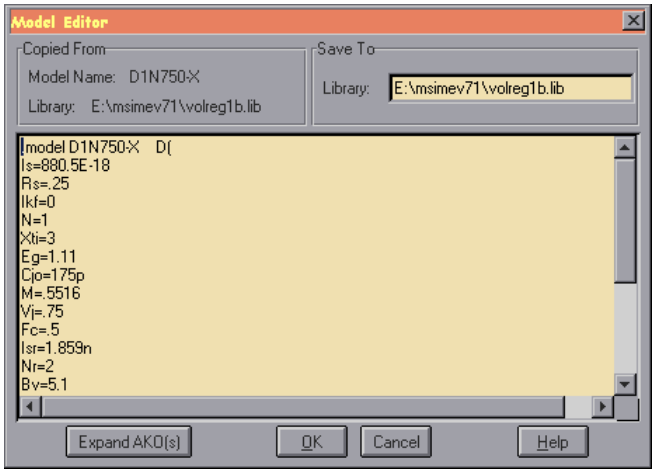
- Instead of using the PSpice potentiometer part, calculate the value of R4 that gives a V_L of + 8V using the following formula:

$$\left(1+\frac{\mathbf{R3}+\mathbf{R4}}{\mathbf{R5}}\right)\left(\mathbf{Vz}+\mathbf{0.7V}\right) = V_L$$

R4 =

Connect the base terminal of Q2 to the junction of R4 and R5.

- Select and place the zener diode part D1N750 in your circuit. Then, highlight the part and select the *'Edit Instance Model (Text)…'* option from the *Edit | Model* menu. You should see a dialog box similar to that shown on the next page:



Change the parameter *Bv* (zener breakdown voltage) to 5.1V. Press OK.

- Connect the VIEWPOINT part at the output terminal of the regulator. Run the simulation and read the VIEWPOINT value. It should be very close to the calculated V_L.

- Next, connect a resistor across the output terminals. Label the resistor name R_L. Label the value of the resistor *{RL_val}*. The resistor value is now a parameter that will be varied through a range during simulation.

To set the range of R_L, get the part named *PARAM* and place it near R_L. Double-click on *PARAM* and in the dialog box set *NAME1 = RL_val* and *VALUE1=10k*. Then, select *Analysis | Setup* and click on *DC Sweep*. Under *Swept Var. Type*, check the *Global*

Parameter option. Under *Sweep Type*, check the *Decade* option. In the *Name* field, type *RL_val*. In the *Start Value* field type 0.*1* (for 0.1 ohm), in the *End Value* field type *1MEG*, and in the *Pts/Decade* field type *40*.

- Place a voltage marker at the output terminal of the regulator. Run the simulation. When PROBE is invoked, change the X-Axis setting to *IC(Q1)* to generate a graph showing V_L vs. $I_{PT(limit)}$. Label $I_{PT(limit)(min)}$ and $I_{PT(limit)(max)}$. You will verify the accuracy of the graph in the next section.

HINTS:

- To change the X-Axis setting, select the *'X Axis Setting'* option from the Plot menu. On the dialog box, press the *'Axis Variable'* button and select the parameter *IC(Q1)*.

- $I_{PT(limit)(max)}$ occurs when V_L = 0V. $I_{PT(limit)(min)}$ occurs when Q3 just begins to turn on and V_L begins to decrease as indicated by the rounded corner on the graph.

Of particular interest in this section is the approach to heatsinking. Instead of laboring over heatsinking theory and calculations, students literally get to "feel" why heatsinking the pass transistor is typically required when employing constant-current limiting; one of its major disadvantages. Students first quickly short the output terminals of the regulator and measure the voltage across the pass transistor. They then calculate the power dissipation of the pass transistor and compare to the Data Book value. They observe from this calculation that without a heat sink, the pass transistor would be quickly destroyed (skeptics can also touch the transistor when the output is shorted to see how "untouchable" it is). Students then place a small hat-type transistor heatsink on the pass transistor and short the output terminals for a long period of time. During this period of time, students touch the pass transistor to empirically observe its temperature. Although the pass transistor gets hot, it is still "touchable" and operating within its safety zone. Shown below is the heatsinking procedure:

16). Connect a voltmeter across the pass transistor (from collector to emitter). Short the load terminals and quickly record the voltage across the pass transistor. Then, remove the short.

$V_{CE(SC)(measured)}$ =

17). Calculate and record the power dissipation of the pass transistor using $V_{CE(SC)(measured)}$ and $I_{L(limit)(min)(measured)}$. Calculate the difference in mW between $P_{DQ1(measured)}$ and the Data Book value: P_D for a 2N2222A is 500mW (TO-18 metal case) or 625mW (TO-92 plastic case).

$P_{DQ1(measured)}$ =

$P_{D(diff)}$ =

18). Place a transistor hat-type heatsink on Q1. Short the load terminals and touch Q1 with your fingers. Keep the load terminals shorted for a long period of time while recording your observations. Remove the short-circuit and the heatsink when done.

Pass transistor observations:

Later in the experiment, students will compare constant-current limiting to foldback-current limiting. They will perform the same heatsinking procedure as explained above and observe that foldback-current limiting does not require the pass transistor to be heatsinked; a major advantage of this type of protection scheme.

PART IV investigates the percent efficiency of a regulator and its relationship to the amount of differential voltage across the pass transistor. After completing this section, students learn that series voltage regulators have typically small efficiencies; it takes a large amount of input power to produce useful load power. Students learn those parts of the regulator that "waste" power and

those that contribute to producing useful load power. They learn how the percent efficiency is affected by changes in line voltage and load changes. Here is a sample excerpt:

19). Using ideal values, calculate the DC input power P_I of the voltage regulator circuit with a load resistance of 1kΩ, a load voltage of +8V, and an input line voltage of +20V. P_I is given by the following formula:

$$P_I = Vin(I_I)$$
$$\text{where } I_I = I_{R1} + I_{R2} + I_{DIVIDER} + I_L$$

I_{R1} =

I_{R2} =

$I_{DIVIDER}$ =

I_L =

I_I =

P_I =

20). Using ideal values, calculate the power absorbed by the load resistor P_L using the following formulas:

$$P_L = (I_L^2)R_L$$

P_L =

21). Using ideal values, calculate the power absorbed by the pass transistor P_{PT} using the following formula:

$$P_{PT} = (Vin - Vout)(I_L + I_{DIV})$$

P_{PT} =

22). Using ideal values, calculate the power across R_1 and the power across the zener diode. P_{D1} is calculated with the following formula:

$$P_{D1} = (V_Z)(I_{R1} + I_{R2})$$

P_{R1} =

P_{D1} =

23). Using ideal values, calculate the percent efficiency %η of the regulator using the following formula:

$$\%\eta = \frac{\mathbf{P_L}}{\mathbf{P_I}} \text{ x } 100\%$$

$\%\eta_{(Vin = +20V,\ Vo = +8V,\ RL = 1k\Omega)}$ =

Students investigate the effect the amount of differential voltage across the pass transistor has on the percent efficiency for a given load regulation. Through calculations and measurements, students learn that for a given load regulation, a larger differential voltage across the pass transistor decreases the percent efficiency. The importance of this parameter is seen when it is considered that a large enough differential voltage must be maintained across the pass transistor in order to maintain a specified load regulation when ripple is present on the line voltage. However, students also observe an important tradeoff; to maintain good load regulation, some regulator efficiency must usually be sacrificed.

PART V investigates the protection scheme called foldback-current limiting. As shown in the schematic below, students select the necessary components from given design parameters and test the validity of their design by measurement. Since foldback-current limiting actually decreases the current through the pass transistor once maximum load current is reached, students use PSpice to obtain the transfer curve and compare to the experimental measurements. Here, simulation is done after the measurements rather than before (as was done for constant-current limiting) to emphasize that simulation can also be used to verify the validity of a design after it is tested.

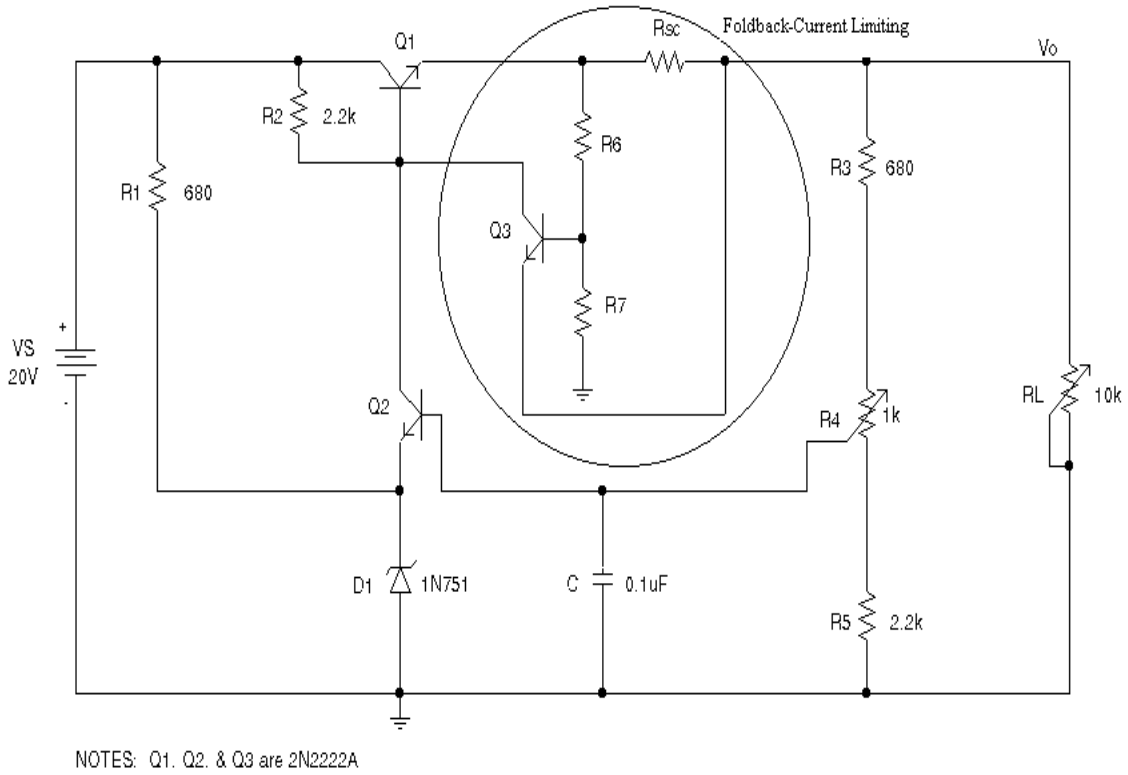


FIGURE 12. Series regulator with foldback-current limiting (Q3, R6, R7, and R_{SC}).[3]

One of the major advantages of foldback-current limiting is the absence of a heatsink for the pass transistor. Although this is clearly evident from the transfer curve, students also get to empirically verify that a heatsink is not required by shorting the output terminals of the regulator and observing that the pass transistor is only warm to the touch.

VI. ANALYSIS QUESTIONS

This section lists the analysis questions. The appropriate questions to each PART are also included after completion of each PART. This allows students to begin the thought process of analyzing the results before moving to the next PART. The analysis questions are of sufficient depth to be incorporated into a laboratory report. Some sample questions are listed below.

- Briefly explain the purpose of each element:

  a). Reference voltage.
  b). Control element.
  c). Error Detector.
  d). Sample circuit.

- From your load regulation measurements, how is %LR affected by differences in load requirements and V_{NL} settings? Are changes linear?

- Explain how Q3 and R_{SC} limit the output current. Why is I_{SC} different from $I_{L(limit)}$? Where does this extra current come from?

- Explain and show with calculations what would happen to the pass transistor without Q3 and R_{SC} if the output was shorted? The maximum power dissipation of a 2N2222A is 500mW (metal case) or 625mW (plastic case).

- Explain and show with calculations what would happen to the pass transistor and R_{SC} if Q3 was open and the output was shorted?

- Explain why the pass transistor without a heatsink is not a good choice for this design? (***HINT***: Derate the transistor power dissipation for a temperature of 30 °C.)

- Derating factor for 2N2222A (TO-18 metal case) = 2.28 mW / °C

- Derating factor for 2N2222A (TO-92 plastic case) = 5 mW / °C

- For a constant load resistance and output voltage, how is %η affected by a decrease in line voltage?

- For a constant line and output voltage, how is %η affected by a decrease in load resistance?

- Assuming an unregulated line voltage and constant load resistance, is the regulator a *"better"* regulator at higher efficiencies? (***HINT***: as ΔV_{DIFF} decreases, the pass transistor is more susceptible to line voltage changes (such as ripple) decreasing its ability to regulate at a specified load regulation.) Use calculations and measurements for support.

- When does the pass transistor dissipate more power: at higher or lower efficiencies? Use calculations and measurements for support.

- By lowering the regulated output voltage and drawing larger currents, the regulator can operate at higher efficiencies with increased load regulation (smaller %L.R.). What is the major disadvantage of this method?

- Explain why I_{Q1} is slightly larger than $I_{PT(limit)(min)}$. Why is there a difference when both values are supposed to represent the same pass transistor current? Is accurate to say that I_{Q1} is practically equal to $I_{PT(limit)(min)}$?

- Conceptually explain the principle of foldback-current limiting. Use the PSpice graph to illustrate.

VII. REFERENCES

This section lists external sources of information that were instrumental in verifying the accuracy of many of the linear voltage regulator concepts and providing many of the pertinent formulas.

VIII. CONCLUSION

Many voltage regulator laboratory experiments tend to emphasize the "black-box" approach in studying the characteristics of voltage regulators. Although using a voltage regulator IC has its advantages, it does not adequately address the fundamental concepts of what makes a voltage regulator "tick" or provide insight into many of its characteristics. When students can construct, analyze, and test a discrete voltage regulator, they can see the important interactions and relationships inherent in voltage regulator circuits such as load and line regulation, percent efficiency, and the effectiveness of different current-limiting protection schemes. This approach reinforces circuit analysis and solid-state theory (which many engineering students continually need) and it puts students in a better position to appreciate and understand power supply problems and interfacing issues between voltage regulator IC circuits and other electronic circuitry.

Bibliography

1. Floyd, Thomas L. *"Electronic Devices, 5th Ed."* Prentice Hall, 1999. *"Chapter 18: Voltage Regulators"*, pgs. 912 – 920.
2. Malvino, Albert Paul. *"Experiments for Malvino Electronic Principles, 6th Ed."* Glencoe/McGraw-Hill, 1999. *"Experiment 60: Series Regulators"*, pgs. 281 – 286.
3. Malvino, Albert Paul. *"Electronic Principles, 5th Ed."* Glencoe/McGraw-Hill, 1995. *"Chapter 23: Regulated Power Supplies"*, pgs. 842 – 879.

JEFFREY FRANZONE

Jeffrey Franzone currently teaches in the Engineering Technology Department at the University of Memphis as an Assistant Professor. He teaches C, C++, Java, and solid-state electronics courses. He has 7 years industrial experience working as an engineering technologist both in hardware and software design and testing. Jeff received a Bachelor's degree in Electronics Engineering Technology at California State University at Long Beach in 1991 and received a Master's degree in Computer Technology at Arizona State University in 1996. Before teaching at the University of Memphis, Jeff was an Electronics Professor at Linn-Benton Community College in Oregon for 3 years.

LAB EXPERIMENT
LINEAR SERIES VOLTAGE REGULATORS

Written by Jeffrey Franzone
Original - 3/96, Updated - 8/00
Rev. 1

BACKGROUND

Proceedings of the 2001 American Society for Engineering Education Annual Conference & Exposition

- **A voltage regulator is a device that maintains a constant voltage across a load even if the load current requirements change. Voltage regulators are a major building-block in power supplies. (NOTE: in some circuits, the voltage regulator is the actual power supply.)**

- **A linear series voltage regulator contains a *"control element"* (usually a transistor) that always operates in the active region, hence the term *"linear"*. The control element is in *"series"* between the unregulated line voltage and the regulated output voltage. When the control element is a transistor, it is often referred to as the *"pass transistor"* since it *"passes"* the required current to maintain a predetermined amount of regulated output voltage.**

- **The main elements of a linear series voltage regulator include:**
  1. **A control element.**
  2. **A reference voltage**
  3. **An error detector.**
  4. **A sample circuit.**

  Figure 1 shows the interconnection of these elements.

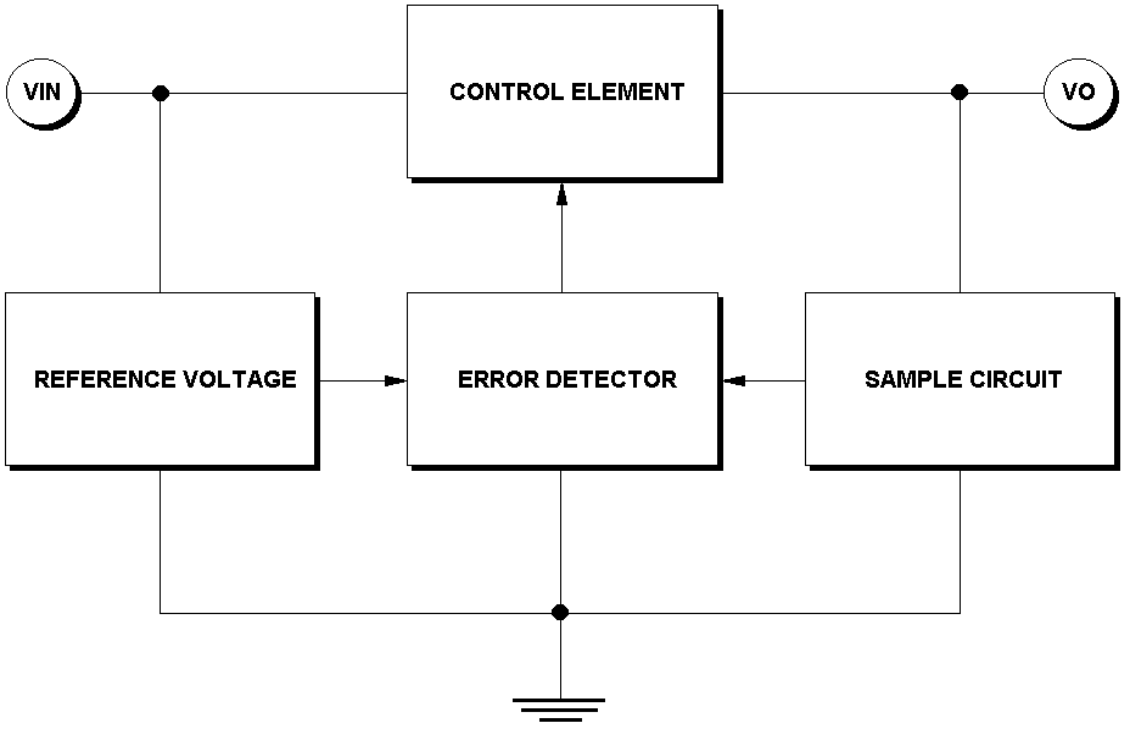


FIGURE 1. The major parts of a linear series voltage regulator.[(1)]

- **The basic operation of the linear series voltage regulator is as follows:**

An error detector compares a reference voltage with a sample of the output voltage. The output of the error detector is fed to a control element. The control element causes the output voltage to increase or decrease until the sample voltage equals the reference voltage. When this occurs, the error voltage is zero (or some other setpoint value) and the control element is held in a stable state. This keeps the output voltage relatively constant regardless of the load requirements (within specific limits, of course).

- **Figure 2 shows a linear series voltage regulator built with discreet components. A single transistor error-detector Q2 amplifies the differential voltage between its inputs (V_Z and V_{BQ2}) causing an immediate change in the base drive of the pass transistor Q1. When the output voltage decreases for some reason, V_{BQ2} decreases. This reduces the differential voltage of the error amplifier (since V_Z is fixed), causing I_{CQ2} to decrease. A smaller I_{CQ2} reduces the voltage across R2 causing the base voltage of the pass transistor to increase. This action brings the output voltage back to its original level. Likewise, if the output voltage increases for some reason, V_{BQ2} increases. This increases the differential voltage of the error amplifier causing its collector current to increase. More collector current increases the voltage drop across R2, causing an increase in the base voltage of the pass transistor. This action reduces the output voltage to its original level.**

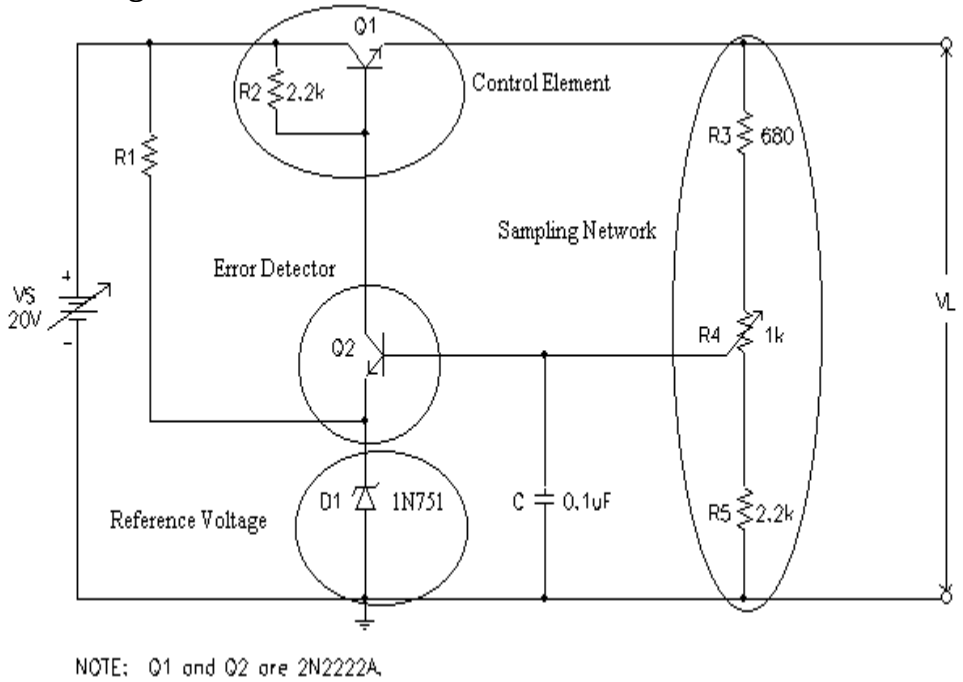


FIGURE 2. Linear series voltage regulator with discreet components.[(2)] The capacitor suppresses any circuit oscillations that could occur from quick line or load changes.

- **The error amplifier improves the regulation of the regulator by amplifying any changes in the output voltage caused by line changes or load demands. These changes cause the base drive of the pass transistor to change in the opposite direction**

counteracting any original output voltage change. The effectiveness of the error amplifier to counteract any output voltage changes mainly depends upon its amplification as given by the following formula[3]:

$$Av_{(EA)} = \frac{\Delta Vs}{\Delta Vo}$$

The larger the gain of the error amplifier, a larger change in Vo can be amplified to counteract the change in line voltage (or load demand).

- **A single transistor error amplifier suffers from a relatively low gain which reduces its transient response-how quickly the regulator can respond to output voltage changes. However, we can view a single transistor error amplifier as an equivalent op-amp noninverting amplifier as shown in Figure 3. This is useful since it clearly depicts the function of the error amplifier in relation to the rest of the regulator and gives an important clue as to how to improve the effectiveness of the error amplifier.**

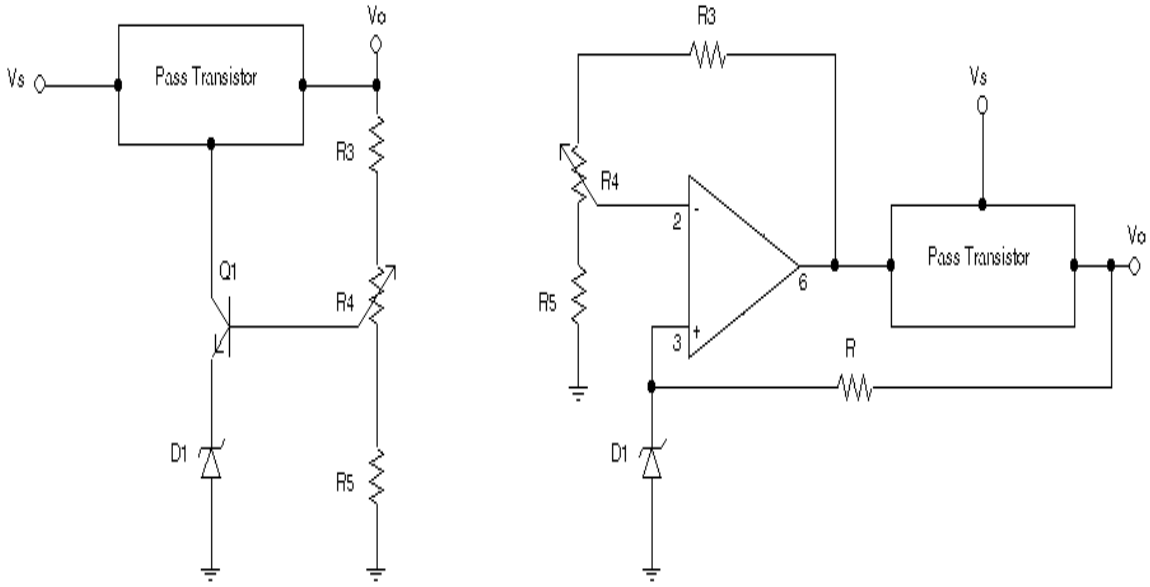


FIGURE 3. Op-amp noninverting amplifier equivalent.

- **Using an op-amp as the error amplifier greatly increases the effectiveness of the regulator to maintain a constant output voltage. The large *"open-loop"* gain of the op-amp greatly increases the transient response of the regulator. As in the single-transistor error amplifier, the stability of the *"closed-loop"* gain is used to adjust the output voltage via R4.**

- **Figure 4 shows a voltage regulator circuit that uses an op-amp as the error detector. The large *"open-loop"* gain of the error-detection circuitry is essential in determining how quickly the regulator can respond to transient changes in output voltage. The**

faster the response, the more effective the regulator is in counteracting adverse changes in the output voltage (caused by either line or load changes).

- **The following discussion will focus on the operation of the voltage regulator shown in Figure 4. The concepts presented here can be applied to most linear series voltage regulators.**

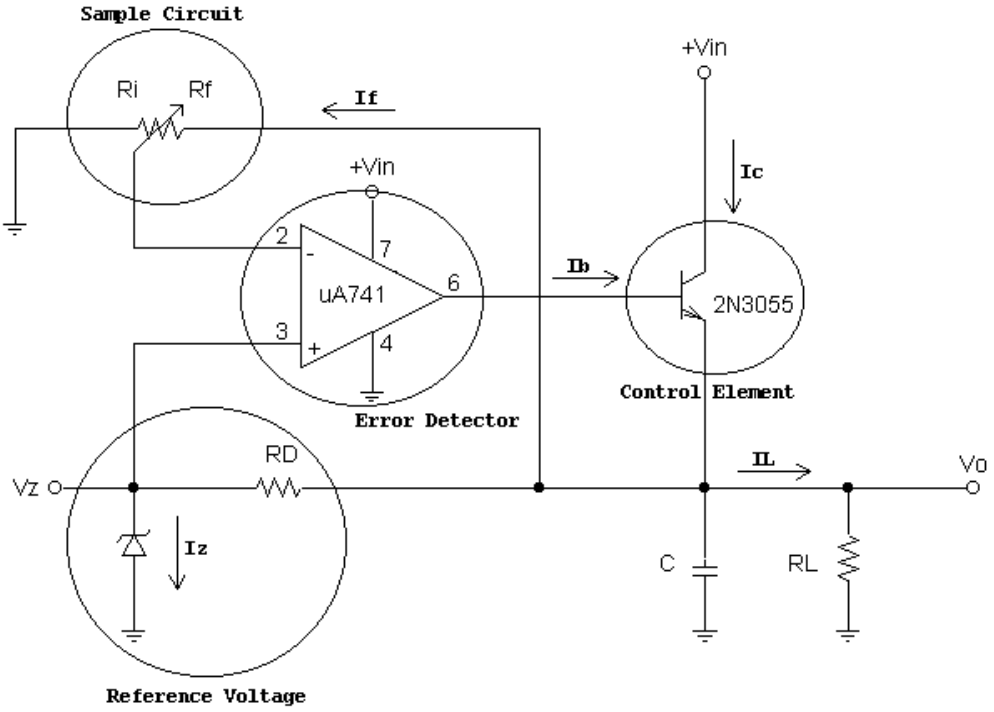


FIGURE 4. A typical *"real-world"* voltage regulator.

A zener diode with a V_Z between 5V and 6V is used as the reference voltage. A zener within this range of V_Z has a temperature coefficient near 0° and consequently maintains an extremely stable reference voltage over changes in temperature[(4)]. The reference voltage is applied to the noninverting input of an op-amp. The sample circuit is a potentiometer that acts as a variable voltage divider. The input to the potentiometer is the output voltage across the load. The sample voltage is taken from the wiper lead and applied to the inverting input of the op-amp. Since the reference voltage remains constant, any change in the output voltage will cause a corresponding change in the sample voltage. For example, if the load changes to a smaller value, more current will be drawn from the unregulated supply. This lowers the unregulated supply voltage causing less voltage to be developed across the load. This in turn, causes the sample voltage to decrease. Since the sample voltage is connected to the inverting input, less sample voltage creates a larger positive differential voltage between the op-amp input terminals. Because of negative feedback and the large internal *"open-loop"* gain, the op-amp responds by swinging its output voltage in a

positive direction very quickly. This increases the base drive to the control element (the pass transistor) causing it to turn on more. This forces more current to flow through the load bringing the output voltage to its nominal value. Similarly, if the load changes to a larger value, less current will be drawn from the unregulated supply. This increases the unregulated supply voltage causing more voltage to be developed across the load. This causes the sample voltage to increase and creates a smaller positive differential voltage across the op-amp input terminals. To maintain stability, the op-amp responds by swinging its output voltage in a less positive direction reducing the current through the control element. This results in less load current thereby decreasing the output voltage to its nominal value.

- **<u>Load regulation</u> refers to the amount the output voltage changes between the no-load and full-load conditions. Load regulation is one method used to determine the relative quality or effectiveness of a voltage regulator to maintain nominal (or no-load) regulation. The lower the load regulation, the better the regulator is in keeping the output voltage at its nominal value (the no-load voltage) for a particular load.**

$$\% \text{ L.R.}^{(4)} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\%$$

where V_{NL} **= no-load voltage.**
V_{FL} **= full-load voltage.**

<u>EXAMPLE</u>:

A dc voltage supply provides 60V when the output is unloaded. When connected to a load, the output drops to 56V. Calculate the percentage of load regulation.

$$\% \text{ L.R.} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\% = \frac{60V - 56V}{56V} \times 100\% = \underline{7.1\%}$$

- **Another method of measurement that is commonly used to determine the relative quality or effectiveness of regulation is <u>source or line regulation</u>. Line regulation is the variation in output voltage (ΔVo) that occurs when the line voltage (the unregulated input voltage V_{LN}) increases or decreases by a specified amount, usually 10%. The lower the line regulation, the better the regulator is at keeping the output voltage constant when changes in line voltage occur.**

$$\%\text{S.R.}^{(1)} = \frac{\Delta Vo}{\Delta V_{LN}} \times 100\%$$

When rating voltage regulators, the following formula[(4)] is commonly used:

$$\%S.R. = \frac{\Delta Vo}{Vo_{(nom)}} \times 100\%$$

where $Vo_{(nom)}$ is the nominal or no-load voltage.

EXAMPLES:

A voltage regulator experiences a 20μV change in its output voltage when its input voltage changes by 4V. What is the percentage of source regulation?

$$\%S.R. = \frac{20\mu V}{4V} \times 100\% = \underline{0.0005\%}$$

A voltage regulator has a nominal output voltage of 18V. When the line voltage changes by +-10%, Vo fluctuates from 19.8V to 16.2V. What is the percentage of source regulation?

$$\Delta Vo = (19.8V - 16.2V) = 3.6V.$$

$$\%S.R. = \frac{3.6V}{18V} \times 100 = \underline{20\%}$$

- **The percent efficiency %η of a linear series voltage regulator is the ratio of the load power to the input power.**

$$\% \eta = \frac{P_L}{P_I} \times 100\%$$

For a particular load power, a low efficiency (< 60%) means that the regulator absorbs most of the input power. Since this power is not transformed into useful load power, the regulator wastes a large amount of input power while only providing a small fraction of useful load power. Similarly, a high efficiency (≥ 60%) means that the regulator is transforming a large amount of input power into useful load power. Because the pass transistor is always ON and the other elements must be properly biased, this type of regulator typically performs at low efficiencies. With larger load currents, the series regulator operates more efficiently than at smaller load currents (assuming the regulator can maintain a constant output voltage at that load current). Even though the power dissipation of the pass transistor is larger than at small load currents, more power is delivered to the load and efficiencies can exceed 40%. With smaller load currents, efficiencies can be as small as 1%.

- **A large difference in the differential voltage across the pass transistor (from**

input to output) increases the power absorbed by the pass transistor and decreases the efficiency of the regulator. However, the load regulation is greatly improved with a large differential voltage. If the load resistance decreases, the pass transistor must supply more current to the load. This reduces the unregulated supply voltage, causing the output voltage to drop. With a large differential voltage, the pass transistor can drop less voltage across itself, maintaining the original output voltage. Likewise, if the load resistance increases, the pass transistor must supply less current to the load. This increases the unregulated supply voltage, causing the output voltage to increase. Again, with a large differential voltage, the pass transistor can drop more voltage across itself, maintaining the original output voltage. As the differential voltage is decreased, higher efficiencies are possible. However, care must be taken because any voltage regulator circuit needs a minimum differential voltage across the pass transistor to maintain regulation at a desired load voltage and load resistance. This minimum differential voltage is a major factor that usually limits the pass transistor from operating at high efficiencies (≥ 60%).

- **Figure 5 shows a discreet series regulator with constant-current limiting (Q3 and R_{SC}). Constant-current limiting is a protection scheme that prevents damage to the pass transistor if a short-circuit or large current demand occurs. The value of R_{SC} is chosen to limit the pass transistor current to a specified (and safe) level:**

$$R_{SC} \approx \frac{0.7V}{I_{PT(limit)}} \approx \frac{0.7V}{I_{RSC(limit)}}$$

where $I_{PT(limit)}$ is the limiting current through the pass transistor and $I_{RSC(limit)}$ is the limiting current through the current limit resistor, R_{SC}.

When the pass transistor current reaches $I_{PT(limit)}$ ($\approx I_{RSC(limit)}$), Q3 turns ON and base drive is diverted away from the pass transistor, limiting the current through it to $I_{PT(limit)}$. If a short-circuit occurs, the collector-emitter voltage of Q3 will be approximately equal to two diode drops (1.4V). Since $I_{PT(limit)}$ keeps Q3 on with a base-emitter voltage of 0.7V, the current through R_{SC} and Q1 remains relatively constant.

The major disadvantage of constant-current limiting is a heatsink is usually required on the pass transistor to prevent damage. When a short-circuit occurs, the entire line voltage is dropped across the pass transistor. At large line voltages, even small values of $I_{PT(limit)}$ may require a heatsink. Heatsinking usually increases the cost and board space of series voltage regulators. Note that Q3 generally does not require a heatsink since its differential voltage is small (1.4V) and it only needs to divert a relatively small current away from Q1 to maintain $I_{PT(limit)}$. Figure 6 illustrates the relationship between the output voltage and $I_{PT(limit)}$ when constant-current limiting is employed.

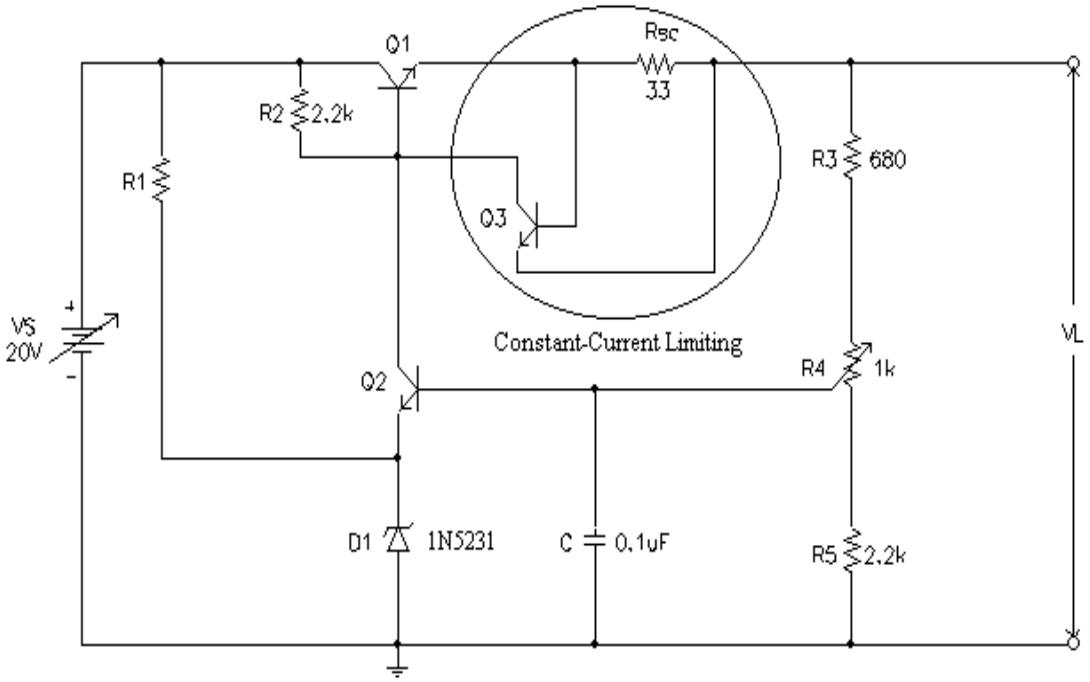


FIGURE 5. Series regulator with constant-current limiting (Q3 and R_{SC}).[2]

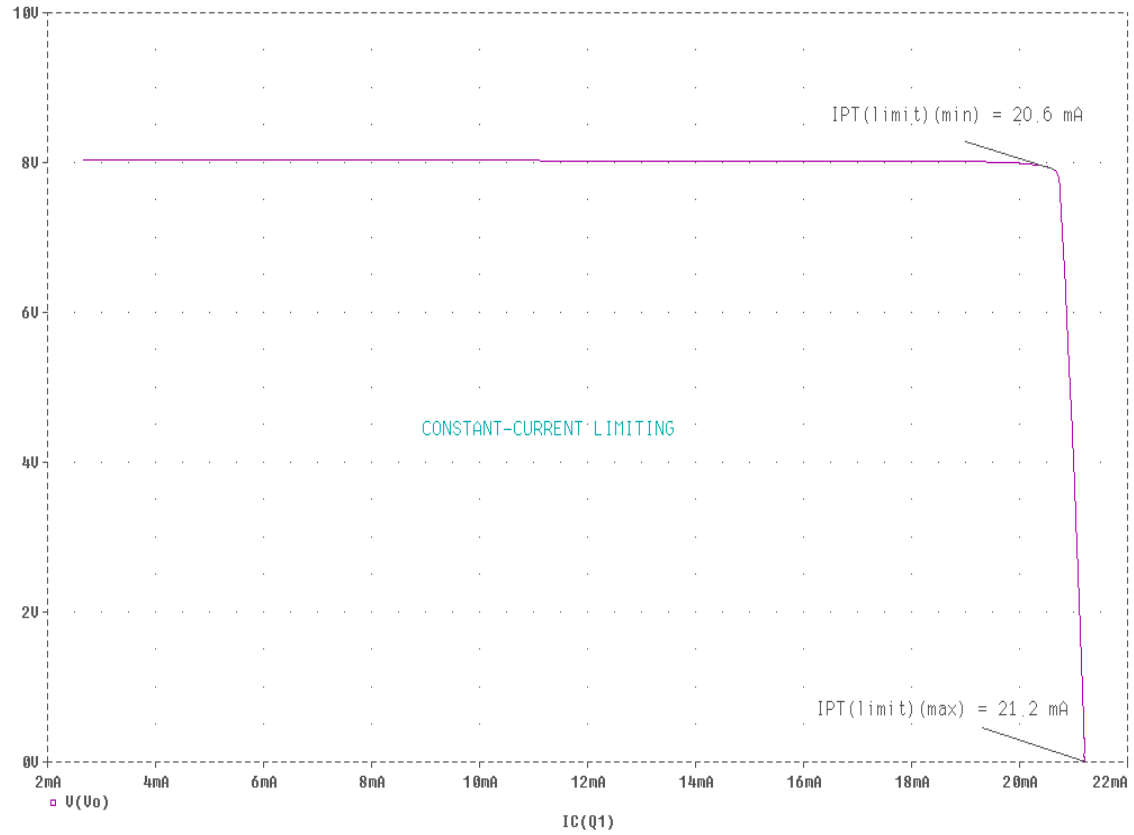


FIGURE 6. Vo vs. $I_{PT(limit)}$ for constant-current limiting protection scheme.

- **Figure 7 shows a discreet series regulator with foldback-current limiting (Q3, R6, R7, and R_{SC}). Foldback-current limiting is another protection scheme that prevents damage to the pass transistor if a short-circuit or large current demand occurs. The values of R6, R7, and R_{SC} are chosen to limit the pass transistor current to a much smaller value during short-circuit conditions than the maximum pass transistor current produced under normal operating conditions.**

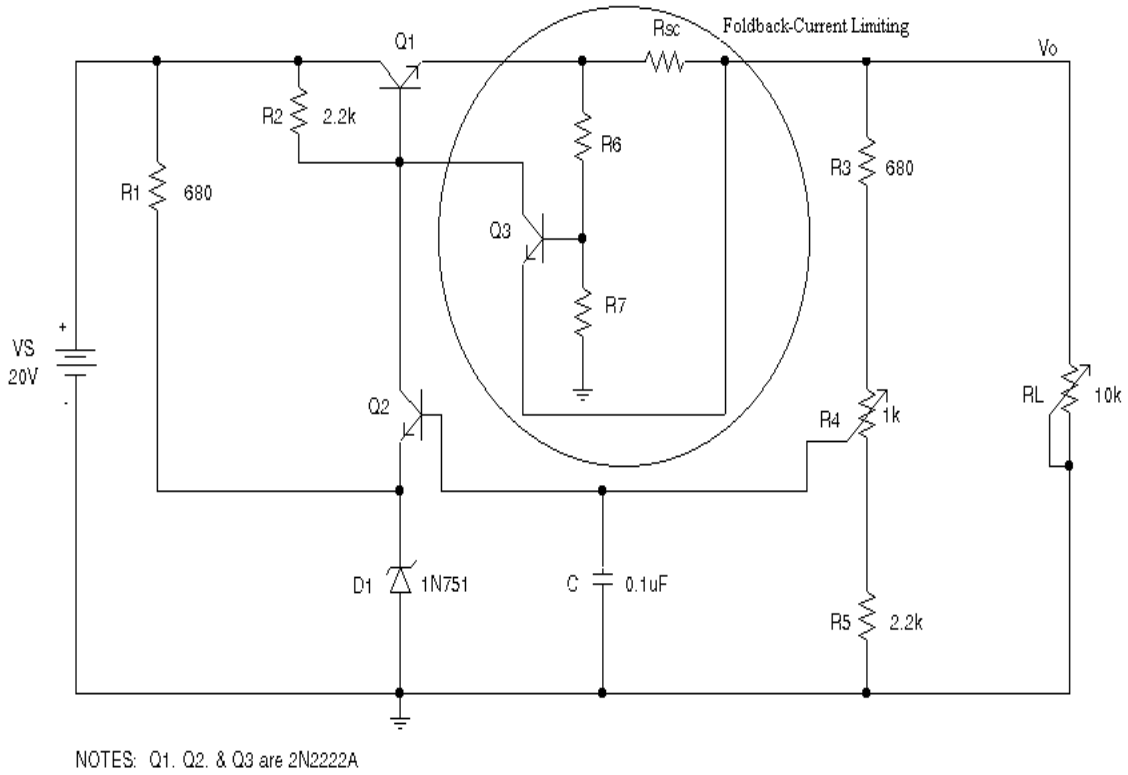


FIGURE 7. Series regulator with foldback-current limiting (Q3, R6, R7, and R_{SC}).[4]

The foldback circuitry is designed to turn Q3 ON when a short-circuit occurs. During a short-circuit, the pass transistor current is much smaller than the maximum pass transistor current. This causes a large decrease in its power dissipation. Typically, the pass transistor does not need to be heatsinked when short-circuits occur due to the lower power dissipation of the pass transistor. This is a significant advantage over the constant-current limiting protection scheme.

Under short-circuit conditions, the minimum current through the pass transistor is given by the following formula[4]:

$$I_{PT(limit)(min)} \approx I_{RSC(min)} = \frac{V_{BE(Q3)}}{KR_{SC}}$$

$$\text{where } K = \frac{R7}{R6 + R7}\text{, the feedback fraction.}$$

The derivation of this formula is as follows:

When Vo is shorted, we have the equivalent diagram in Figure 8. Note that the voltage across the current limit resistor R_{SC} must overcome the voltage across R6 as well as the V_{BE} drop of Q3 before Q3 turns on.

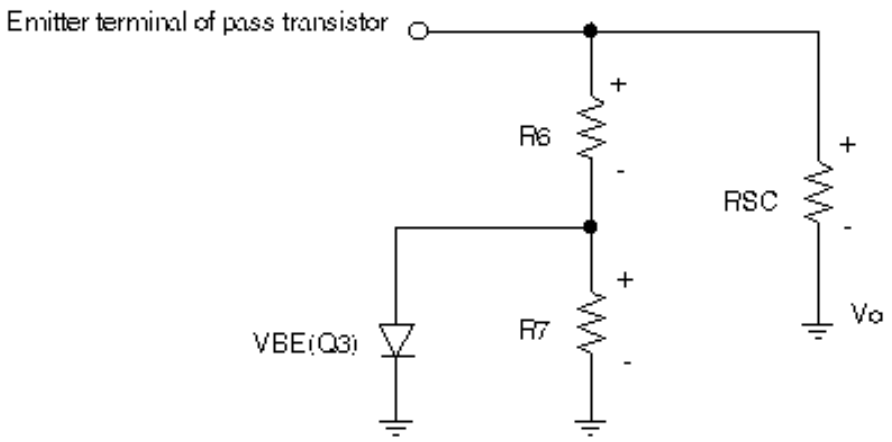


FIGURE 8. Equivalent diagram when Vo is shorted.

$$I_{PT(limit)(min)} = \frac{V_{RSC}}{R_{SC}}$$

$$V_{RSC} = V_{BE(Q3)} + V_{R6}$$

$$V_{R6} + V_{BE(Q3)} = \frac{R7}{R6 + R7} V_{RSC} + V_{R6}$$

$$V_{BE(Q3)} = \frac{R7}{R6 + R7} V_{RSC}$$

$$V_{RSC} = \frac{V_{BE(Q3)}}{\frac{R7}{R6 + R7}} = \frac{V_{BE(Q3)}}{K}$$, **where K is the feedback fraction.**

Substituting $\frac{V_{BE(Q3)}}{K}$ **for** V_{RSC}**, we have:**

$$I_{PT(limit)(min)} = \frac{V_{BE(Q3)}}{KR_{SC}}$$

As Vo increases from 0V, V_{R6} **increases. Consequently, more current is required through** R_{SC} **to maintain a sufficient voltage drop to keep Q3 forward-biased. An increase in current through** R_{SC} **increases the current through the pass transistor until some maximum is reached.**

The maximum pass transistor current can be derived as follows:

When Vo is 0V, $I_{PT(limit)(min)} = \frac{V_{BE(Q3)}}{KR_{SC}}$**. As Vo increases, the voltage drop across** $V_{BE(Q3)}$ **is given as,**

$$V_{BE(Q3)} = V_{RSC} - V_{R6}$$

$$V_{BE(Q3)} = R_{SC}I_{max} - \left(\frac{Vo + R_{SC}I_{max}}{R6 + R7}\right)R6$$

Solving for I_{max}**,**

$$V_{BE(Q3)} = \frac{R_{SC}I_{max}(R6 + R7) - [Vo + R_{SC}I_{max}]R6}{R6 + R7}$$

$$V_{BE(Q3)} = \frac{R_{SC}I_{max}(R6 + R7) - [VoR6 + R_{SC}I_{max}R6]}{R6 + R7}$$

$$V_{BE(Q3)} = \frac{R_{SC}I_{max}(R6 + R7 - R6) - VoR6}{R6 + R7}$$

$$I_{max} = \frac{V_{BE(Q3)}(R6 + R7) - VoR6}{R_{SC}R7}$$

Since $\frac{V_{BE(Q3)}(R6 + R7) - VoR6}{R_{SC}R7} = \frac{V_{BE(Q3)}}{KR_{SC}} = I_{PT(limit)(min)}$**,**

$$I_{max} = I_{PT(limit)(min)} + \frac{VoR6}{R_{SC}R7}$$

Dividing the numerator and denominator of $\frac{VoR6}{R_{SC}R7}$ **by (R6 + R7) leaves,**

$$I_{max} = I_{PT(limit)(min)} + \frac{\left(\frac{VoR6}{R6 + R7}\right)}{\left(\frac{R_{SC}R7}{R6 + R7}\right)}$$

$$I_{max}^{(4)} = I_{PT(limit)(min)} + \frac{Vo(1 - K)}{KR_{SC}}$$

$I_{max} = I_{RSC(max)} \approx I_{PT(limit)(max)}$

Typically, values for R_{SC}, R6, and R7 are chosen such that

$$I_{PT(limit)(max)} \approx 3I_{PT(limit)(min)}. \quad (4)$$

Figure 9 shows the relationship between Vo and $I_{PT(limit)}$ for a foldback-current limiting protection scheme.

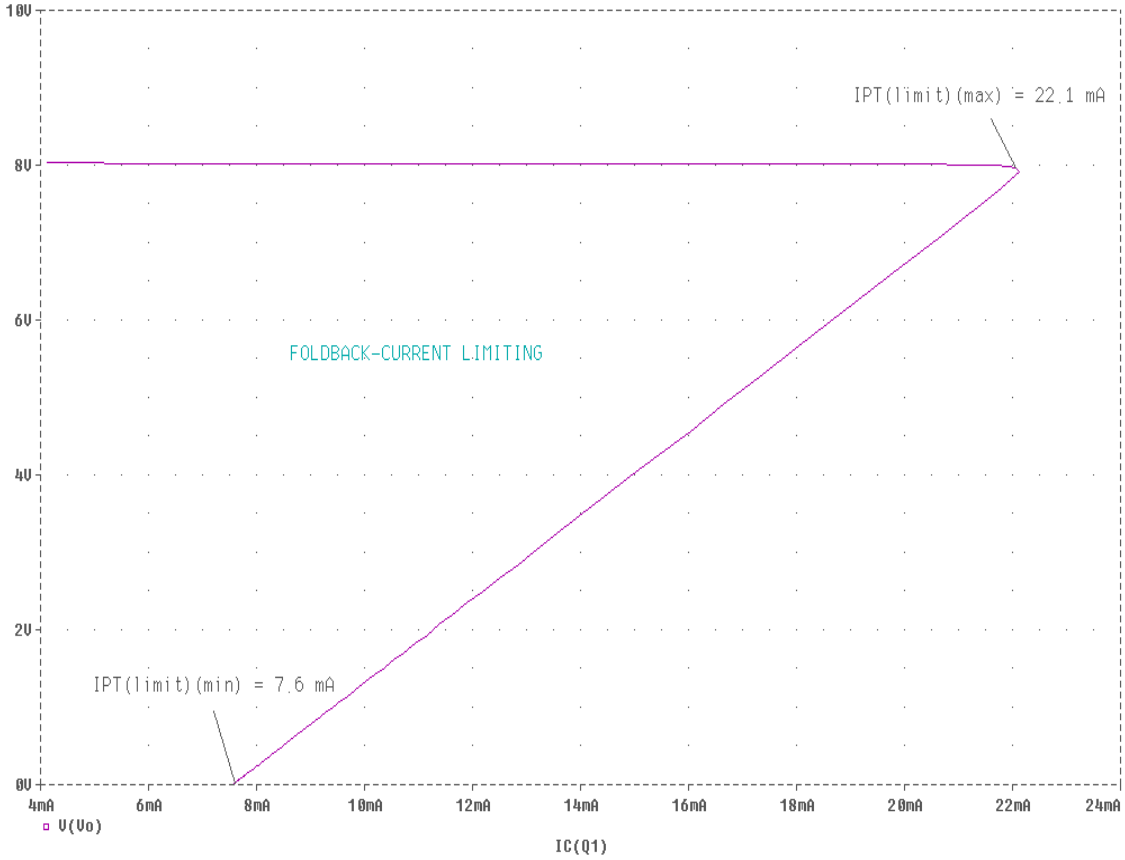


FIGURE 9. Vo vs. $I_{PT(limit)}$ for foldback-current limiting protection scheme.

OBJECTIVES

A voltage regulator is one that maintains a constant voltage across a load even though the load current requirements may change. Most applications of voltage regulators are in power supply circuits. When load current demand on an unregulated DC power supply changes, the amplitude of the supply decreases and the AC ripple voltage increases. These are undesirable changes that can be minimized by adding a regulator circuit. A Linear Series Voltage Regulator is one in which the control element (normally a pass transistor) is in series with the unregulated DC supply voltage and the load. When there are changes in the load demand, the drive on the pass transistor changes. This results in meeting the new load demand while maintaining a constant voltage across the load. Since the pass transistor is always on (or operating in its linear region), these types of voltage regulators have very low efficiencies (typically 1 to 40%). However, they are a good choice for low power demands and are relatively simple to build and operate.

In this lab experiment, you will investigate some of the important characteristics of linear series voltage regulators such as

- **The major parts of the voltage regulator and how they work.**
- **Load and line regulation ratings.**
- **Percent efficiency rating.**
- **Minimum differential voltage needed for regulation.**
- **Heatsinking requirements.**
- **Constant current-limiting and foldback current-limiting.**

EQUIPMENT

- **1 power supply : +-20V.**
- **3 NPN BJTs: 2N2222A (or equivalent), TO-18 metal case.**
- **1 zener diode: 1N751 (+5.1V).**
- **¼ W resistors: 2 2.2kΩ, 1 1kΩ, 1 680Ω, 1 33Ω, 1 4.7kΩ, 1 10kΩ, 1 560Ω, 1 330Ω, 1 100Ω, and two values to be determined.**
- **½ W resistor: to be determined.**
- **2N2222A Heat Sink (transistor *"hat-type"*.)**
- **1 1kΩ, 10-turn PC-mount potentiometers. (Will need adjustment tool.)**
- **1 10kΩ standard carbon-type potentiometer.**
- **1 capacitor: 0.1uF**
- **2 DMMs.**

PROCEDURE

SCHEMATIC:

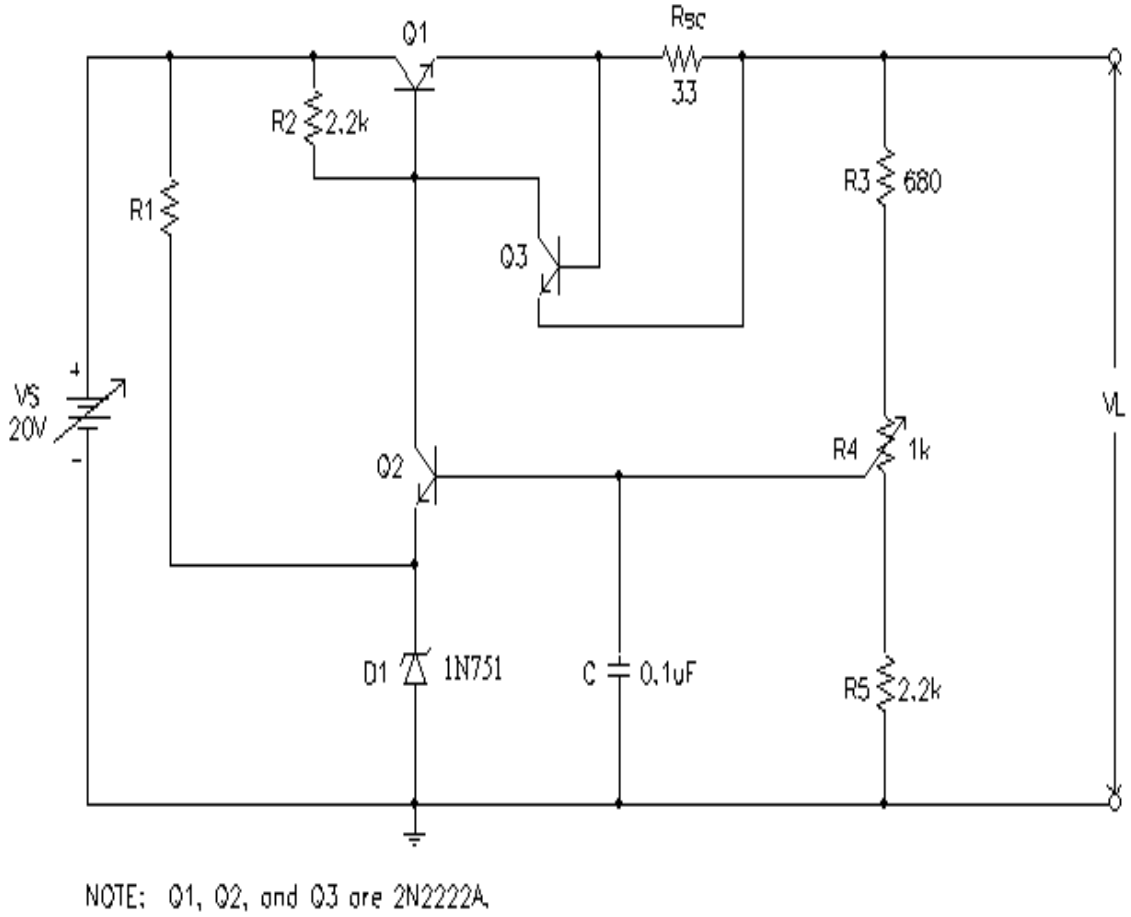


FIGURE 10. Experimental voltage regulator circuit.[(2)]

RESISTOR VALUES TABLE

Record the measured resistor values in the table below. Measured values should be within +-10% of the ideal values.

IDEAL		MEASURED
R2	2.2kΩ	
R3	680Ω	
$R4_{(MAX)}$	1kΩ	
R5	2.2kΩ	
R7 (Figure 11)	4.7kΩ	
Rsc	33Ω	
RL	10kΩ	
RL	1kΩ	
RL	560Ω	
RL	330Ω	
RL	100Ω	
When available:		
R1 (Figure 10)		
R6 (Figure 11)		
R_{SC} (Figure 11)		

TABLE 1.

PART I:

Zener-diode biasing, output voltage range, and regulator gain.

CALCULATIONS:

SELECTING R1 (ZENER DIODE BIASING RESISTOR)

1). Assuming a +5.1V zener diode, a zener current of 20mA, and an input voltage of +20V, calculate and record the value of R_1. (Refer to Figure 10 for reference.)

R_1 =

Select the nearest lower standard value if applicable and use the ideal value to calculate the required power dissipation. Select the next highest power rating (¼W, ½W, 1W, etc.).

P_{R1} =

Record the ideal and measured values for R1 in TABLE 1.

MINIMUM & MAXIMUM LOAD VOLTAGE

2). Using ideal resistor values, calculate and record the minimum and maximum load voltage V_L and the minimum and maximum "*closed-loop*" gain of the regulator when R4 is varied. Determine the range of output voltage and "*closed-loop*" regulator gain.

$V_{L(min)}$ =

$V_{L(max)}$ =

$V_{L(range)}$ =

$Av_{(CL)(min)}$ =

$Av_{(CL)(max)}$ =

$Av_{(CL)(range)}$ =

- **Explain how Q1 and the R3-R4-R5 voltage divider represent an equivalent op-amp noninverting amplifier. Draw the equivalent diagram and use the calculations from "*Minimum and Maximum Load Voltage*" for support.**
    - **What differences exist, if any, between the error-detection circuit in Figure 10 and the equivalent op-amp circuit? Are the output voltage ranges and "*closed-loop*" regulator gains identical? Explain why an op-amp error-detector is more desirable than a transistor error-detector.**
    - **Explain the meaning of $Av_{(CL)(range)}$. What does it tell us about the regulator?**

- **Draw a block diagram that shows the basic elements of linear series voltage regulators.**

- **Briefly explain the purpose of each element:**

  a). Reference voltage.
  b). Control element.
  c). Error Detector.
  d). Sample circuit.

MEASUREMENTS:

3). Obtain the appropriate value and power rating for R1 and construct the circuit of Figure 10. Adjust the DC input voltage to +20V. Measure and record the zener voltage. Then, adjust R4 through its range recording the minimum and maximum values of V_L. Use measured resistance values and $V_{Z(measured)}$ to calculate the minimum and maximum measured *"closed-loop"* regulator gain. Verify that all measurements are within +-10% of the calculations.

$V_{Z\ (measured)}$ =

$V_{L\ (min)(measured)}$ =

$V_{L\ (max)(measured)}$ =

$V_{L(range)(measured)}$ =

$Av_{(CL)(min)(measured)}$ =

$Av_{(CL)(max)(measured)}$ =

$Av_{(CL)(range)(measured)}$ =

PART II:
Load and Line Regulation

MEASUREMENTS:

LOAD REGULATION

4). Adjust R4 for a load voltage of +8V. Record this as the no-load voltage V_{NL}.

V_{NL} =

5). Connect a load resistance of 10kΩ. Measure the load voltage V_L. Record this value as the full-load voltage V_{FL}. Repeat this step with 1kΩ, 330Ω, and 100Ω.

$V_{FL\ (with\ 10k\Omega)}$ =

$V_{FL\ (with\ 1k\Omega)}$ =

$V_{FL\ (with\ 330\Omega)}$ =

$V_{FL\ (with\ 100\Omega)}$ =

6). Using measured values, calculate and record the percent load regulation for each of the load resistors using the following formula[(4)]:

$$\%L.R. = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\%$$

$\%LR_{(with\ 10k\Omega)}$ =

$\%LR_{(with\ 1k\Omega)}$ =

$\%LR_{(with\ 330\Omega)}$ =

$\%LR_{(with\ 100\Omega)}$ =

7). Repeat steps 4 through 6 with a V_{NL} = <u>+9V</u>.

$V_{FL\ (with\ 10k\Omega)}$ =

$V_{FL\ (with\ 1k\Omega)}$ =

$V_{FL\ (with\ 330\Omega)}$ =

$V_{FL\ (with\ 100\Omega)}$ =

$\%LR_{(with\ 10k\Omega)}$ =

$\%LR_{(with\ 1k\Omega)}$ =

$\%LR_{(with\ 330\Omega)}$ =

$\%LR_{(with\ 100\Omega)}$ =

8). Repeat steps 4 through 6 with a $V_{NL} = V_{L(min)(measured)}$.

$V_{NL} = V_{L(min)(measured)}$ =

$V_{FL\ (with\ 10k\Omega)}$ =

$V_{FL\ (with\ 1k\Omega)}$ =

$V_{FL\ (with\ 330\Omega)}$ =

$V_{FL\ (with\ 100\Omega)}$ =

$\%LR_{(\text{with } 10k\Omega)}$ =

$\%LR_{(\text{with } 1k\Omega)}$ =

$\%LR_{(\text{with } 330\Omega)}$ =

$\%LR_{(\text{with } 100\Omega)}$ =

LINE (OR SOURCE) REGULATION

9). Reconnect the 10kΩ load resistor and record the load voltage as V_{NOM} (nominal output voltage).

V_{NOM} =

10). Decrease the DC input voltage from +20V to +16V. This represents a line voltage change of 20%. Measure and record the load voltage as $V_{L(min)}$.

$V_{L(min)}$ =

11). Using measured values, calculate and record the percent line (or source) regulation using the formula[1] below. Also, calculate Av of the error amplifier.

$$\%S.R. = \frac{\Delta Vo}{Vo_{(nom)}} \times 100\%$$

ΔVout =

$\%SR_{(20\%)}$ =

$Av_{(EA)}$ =

- **Explain the concepts of load and line regulation. Use measurements for support. What do these terms tell you about voltage regulators?**

- **Explain the meaning of a %LR specification. Which is better: high or low percentages? Explain.**

- **Explain the meaning of a %SR specification assuming a 20% line voltage change. Which is better: high or low percentages? Explain.**

- **From your load regulation measurements, how is %LR affected by differences in load requirements and V_{NL} settings? Are changes linear?**

PART III:
Constant-Current Limiting and Heatsinking

PSPICE SIMULATION:

CONSTANT-CURRENT LIMITING

12). Figure 11 employs one of the most common regulator protection schemes: constant-current limiting.

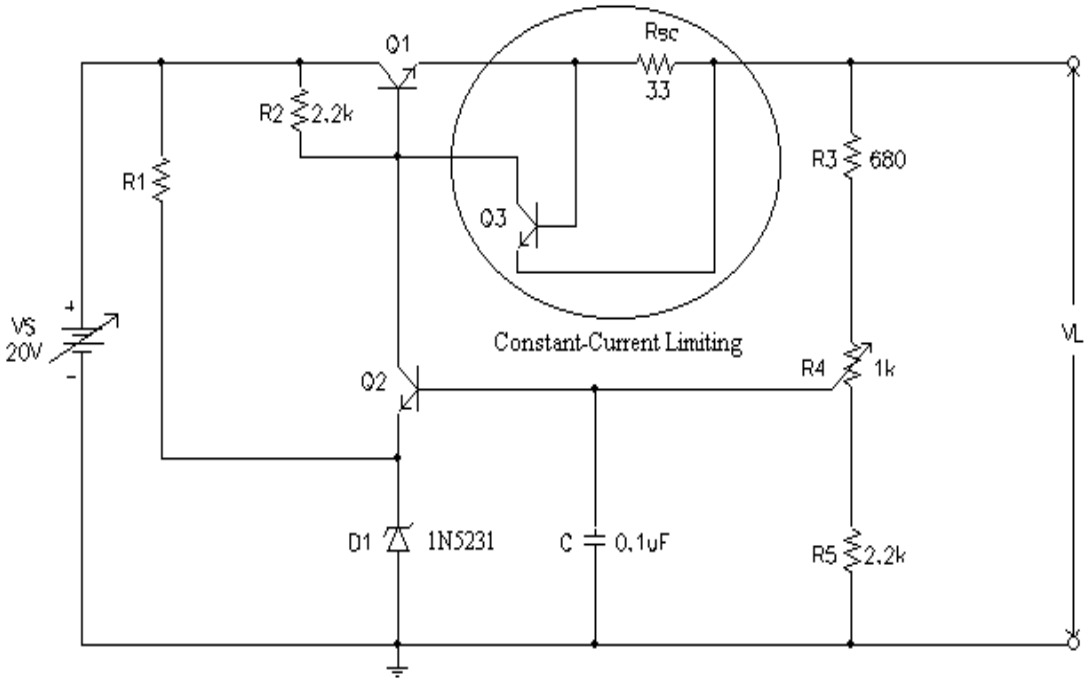


FIGURE 11. Series regulator with constant-current limiting (Q3 and R_{SC}).[2]

Draw and simulate the circuit of Figure 11 in PSpice Schematics with the following modifications:

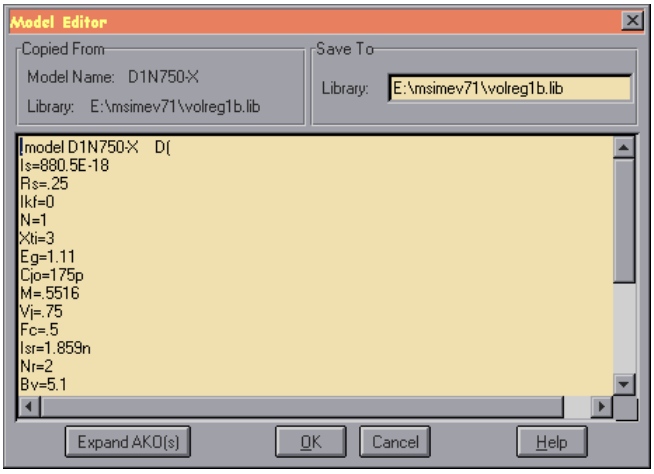
- **Instead of using the PSpice potentiometer part, calculate the value of R4 that gives a V_L of + 8V using the following formula:**

$$\left(1+\frac{R3+R4}{R5}\right)(Vz+0.7V) = V_L$$

R4 =

Connect the base terminal of Q2 to the junction of R4 and R5.

- **Select and place the zener diode part D1N750 in your circuit. Then, highlight the part and select the '*Edit Instance Model (Text)…*' option from the *Edit* | *Model* menu. You should see a dialog box similar to that shown on the next page:**



Change the parameter *Bv* (zener breakdown voltage) to 5.1V. Press OK.

- **Connect the VIEWPOINT part at the output terminal of the regulator. Run the simulation and read the VIEWPOINT value. It should be very close to the calculated V_L.**

- **Next, connect a resistor across the output terminals. Label the resistor name R_L. Label the value of the resistor *{RL_val}*. The resistor value is now a parameter that will be varied through a range during simulation.**

  To set the range of R_L, get the part named *PARAM* and place it near R_L. Double-click on *PARAM* and in the dialog box set *NAME1 = RL_val* and *VALUE1=10k*. Then, select *Analysis | Setup* and click on *DC Sweep*. Under *Swept Var. Type*, check the *Global Parameter* option. Under *Sweep Type*, check the *Decade* option. In the *Name* field, type *RL_val*. In the *Start Value* field type 0.*1* (for 0.1 ohm), in the *End Value* field type *1MEG*, and in the *Pts/Decade* field type *40*.

- **Place a voltage marker at the output terminal of the regulator. Run the simulation. When PROBE is invoked, change the X-Axis setting to *IC(Q1)* to generate a graph showing V_L vs. $I_{PT(limit)}$. Label $I_{PT(limit)(min)}$ and $I_{PT(limit)(max)}$. You will verify the accuracy of the graph in the next section.**

  HINTS:

  - **To change the X-Axis setting, select the *'X Axis Setting'* option from the Plot menu. On the dialog box, press the *'Axis Variable'* button and select the parameter *IC(Q1)*.**

- **$I_{PT(limit)(max)}$ occurs when V_L = 0V. $I_{PT(limit)(min)}$ occurs when Q3 just begins to turn on and V_L begins to decrease as indicated by the rounded corner on the graph.**

CALCULATIONS & MEASUREMENTS:

CONSTANT-CURRENT LIMITING

13). Assume that Q3 turns on when V_{BE} = 0.7V. Calculate and record the load current where current limiting begins.

$I_{L(limit)(min)}$ =

14). Modify the circuit in Figure 10 to that of Figure 11. Set the input line voltage to +20V and adjust R4 for a V_{NL} of +8V. Next, short the load terminals by directly connecting an ammeter across the load terminals. Record the short-circuit current I_{SC} displayed by the ammeter.
(NOTE: don't leave the load terminals shorted for too long.)

I_{SC} =

Remove the ammeter across the load terminals and place it in series with the emitter terminal of Q3. Next, place a wire across the load terminals. Measure and record the current through Q3 with an ammeter. Then, touch the pass transistor Q1 with your fingers. Record your observations. Remove the short across the load terminals when done. (NOTE: don't leave the load terminals shorted for too long.)

I_{Q3} =

Pass transistor observations:

15). Subtract I_{Q3} from I_{SC}. Verify that this difference is within +-5% of $I_{L(limit)(min)}$.

$I_{L(limit)(min)(measured)}$ =

- **What is meant by constant-current limiting. Use PSpice graph to illustrate.**

- **Is it accurate to say that $I_{L(limit)}$ is practically identical to I_{PT} for constant-current limiting? Explain.**

  - **Explain how Q3 and R_{SC} limit the output current. Why is I_{SC} different from $I_{L(limit)}$? Where does this extra current come from?**

  - **Explain and show with calculations what would happen to the pass transistor without Q3 and R_{SC} if the output was shorted? The maximum power dissipation of a 2N2222A is 500mW (metal case) or 625mW (plastic case).**

  - **Explain and show with calculations what would happen to the pass transistor and R_{SC} if Q3 was open and the output was shorted?**

- **What are some advantages and disadvantages of constant-current limiting?**

HEATSINKING

16). Connect a voltmeter across the pass transistor (from collector to emitter). Short the load terminals and quickly record the voltage across the pass transistor. Then, remove the short.

$V_{CE(SC)(measured)}$ =

17). Calculate and record the power dissipation of the pass transistor using $V_{CE(SC)(measured)}$ and $I_{L(limit)(min)(measured)}$. Calculate the difference in mW between $P_{DQ1(measured)}$ and the Data Book value: P_D for a 2N2222A is 500mW (TO-18 metal case) or 625mW (TO-92 plastic case).

$P_{DQ1(measured)}$ =

$P_{D(diff)}$ =

18). Place a transistor hat-type heatsink on Q1. Short the load terminals and touch Q1 with your fingers. Keep the load terminals shorted for a long period of time while recording your observations. Remove the short-circuit and the heatsink when done.

Pass transistor observations:

- **Discuss any differences in the relative temperature of the pass transistor with and without a heatsink.**

- **Explain why the pass transistor without a heatsink was much *"hotter"* than with a heatsink.**

- **Explain why the pass transistor without a heatsink is not a good choice for this design? (*HINT*: Derate the transistor power dissipation for a temperature of 30 °C.)**

  - **Derating factor for 2N2222A (TO-18 metal case) = 2.28 mW / °C**

  - **Derating factor for 2N2222A (TO-92 plastic case) = 5 mW / °C**

- **One alternative to using a heatsink is to select another transistor type with a larger power dissipation. Are there any disadvantages that need to be considered?**

PART IV:
Percent Efficiency and Differential Voltage

CALCULATIONS:

PERCENT EFFICIENCY OF THE REGULATOR

19). Using ideal values, calculate the DC input power P_I of the voltage regulator circuit with a load resistance of 1kΩ, a load voltage of +8V, and an input line voltage of +20V. P_I is given by the following formula:

$$P_I = Vin(I_I)$$
$$\text{where } I_I = I_{R1} + I_{R2} + I_{DIVIDER} + I_L$$

I_{R1} =

I_{R2} =

$I_{DIVIDER}$ =

I_L =

I_I =

P_I =

20). Using ideal values, calculate the power absorbed by the load resistor P_L using the following formulas:

$$P_L = (I_L^2)R_L$$

P_L =

21). Using ideal values, calculate the power absorbed by the pass transistor P_{PT} using the following formula:

$$P_{PT} = (Vin - Vout)(I_L + I_{DIV})$$

P_{PT} =

22). Using ideal values, calculate the power across R_1 and the power across the zener diode. P_{D1} is calculated with the following formula:

$$P_{D1} = (V_Z)(I_{R1} + I_{R2})$$

P_{R1} =

P_{D1} =

23). Using ideal values, calculate the percent efficiency %η of the regulator using the following formula:

$$\%\eta = \frac{P_L}{P_I} \text{ x } 100\%$$

$\%\eta_{(Vin = +20V,\ Vo = +8V,\ RL = 1k\Omega)}$ =

24). Repeat Steps #19 through #23 with a load resistance of 1kΩ, a load voltage of +8V, and an input line voltage of +12V. Assume V_Z = 5.1V.

I_{R1} =

I_{R2} =

$I_{DIVIDER}$ =

I_L =

I_I =

P_I =

P_L =

P_{PT} =

P_{R1} =

P_{D1} =

$\%\eta_{(Vin = +12V,\ Vo = +8V,\ RL = 1k\Omega)}$ =

25). Repeat Steps #19 through #23 with a load resistance of 560Ω, a load voltage of +8V, and an input line voltage of +20V.

I_{R1} =

I_{R2} =

$I_{DIVIDER}$ =

I_L =

I_I =

P_I =

P_L =

P_{PT} =

P_{R1} =

P_{D1} =

$\%\eta_{(Vin = +20V, Vo = +8V, RL = 560\Omega)}$ =

MEASUREMENTS:

26). Connect a load resistance of 1kΩ to the circuit in Figure 10. Adjust R4 for a load voltage of +8V. Verify that the DC input voltage is +20V. With an ammeter, measure and record I_I and I_L. From the measured values, determine P_I, P_L, and %η. Compare to the calculated values in Steps #19 through #23. Measured and calculated values should be within +-10%.

$I_{I(measured)}$ =

$I_{L(measured)}$ =

$P_{I(measured)}$ =

$P_{L(measured)}$ =

$\%\eta_{(Vin = +20V,\ Vo = +8V,\ RL = 1k\Omega)(measured)}$ =

27). Repeat Step #26 for a DC input voltage of <u>+12V</u> and a load voltage of <u>+8V</u>. (Keep the <u>1kΩ</u> load resistor connected.) Compare measured values to the calculated values in Step #24. Measured and calculated values should be within +-10%.

$I_{I(measured)}$ =

$I_{L(measured)}$ =

$P_{I(measured)}$ =

$P_{L(measured)}$ =

$\%\eta_{(Vin = +12V,\ Vo = +8V,\ RL = 1k\Omega)(measured)}$ =

28). Repeat Step #26 for a load resistance of <u>560Ω</u>, a DC input voltage of <u>+20V</u>, and a load voltage of <u>+8V</u>. Compare measured values to the calculated values in Step #25. Measured and calculated values should be within +-10%.

$I_{I(measured)}$ =

$I_{L(measured)}$ =

$P_{I(measured)}$ =

$P_{L(measured)}$ =

$\%\eta_{(Vin = +12V,\ Vo = +8V,\ RL = 560\Omega)(measured)}$ =

- **Percent Efficiency is a figure of merit for a voltage regulator. The larger the %η, the more efficient the regulator is in converting input power to useful load power.**
  - **When the line voltage is +20V and the load resistance is 1kΩ, what components *"waste"* most of the input power?**
  - **For a constant load resistance and output voltage, how is %η affected by a decrease in line voltage?**
  - **For a constant line and output voltage, how is %η affected by a decrease in load resistance?**
  - **How does the reference voltage network (R_1 and V_{D1}) affect %η?**

CALCULATIONS & MEASUREMENTS:

DIFFERENTIAL VOLTAGE OF THE PASS TRANSISTOR & PERCENT EFFICIENCY

MAXIMUM DIFFERENTIAL VOLTAGE

- **The maximum differential voltage is the maximum voltage that can be safely applied across the pass transistor. In most transistor Data Books, the parameter V_{CEO} specifies the maximum differential voltage. For a 2N2222A, V_{CEO} is 40V (metal and plastic case).**

MINIMUM DIFFERENTIAL VOLTAGE

(NOTE: Be very meticulous with measurements in this section.)

29). Calculate the output voltage V_{FL} for a 1% Load Regulation when V_{NL} = +9V.

$V_{FL(1\%\ L.R.,\ VNL\ =\ +9V)}$ =

30). Connect a load resistance of 1kΩ and verify a +20V line voltage. Adjust R4 for a V_L = V_{NL} of +9V. Next, reduce the input line voltage until the output voltage is set to V_{FL}.

Measure and record the new line voltage V_{LINE} and the voltage across the pass transistor $V_{DIFF(min)}$. This voltage represents the minimum differential voltage needed for a load regulation of 1%. Measure and record I_I and I_L. Calculate P_I, P_L, and %η of the regulator from the measured values.

$V_{LINE(1\%\ L.R.,\ VNL\ =\ +9V)(measured)}$ =

$V_{DIFF(min)(1\%\ L.R.,\ VNL\ =\ +9V)(measured)}$ =

$I_{I(measured)}$ =

$I_{L(measured)}$ =

$P_{I(measured)}$ =

$P_{L(measured)}$ =

$\%\eta_{(1\%\ L.R.,\ VNL\ =\ +9V)(measured)}$ =

31). Using measured values, calculate the change in differential voltage ΔV_{DIFF} for the pass transistor using the following formula:

$$\Delta V_{DIFF} = V_{DIFF(VNL)} - V_{DIFF(1\%\ L.R.)}$$

$\Delta V_{DIFF(1\%\ L.R.,\ VNL\ =\ +9V)(measured)}$ =

32). Repeat Steps #29 through #31 for a $V_L = V_{NL}$ = of <u>+10V</u>. (*<u>NOTE</u>*: The value of ΔV_{DIFF} should be <u>smaller</u> than ΔV_{DIFF} in Step #31 and the value of V_{LINE} should be <u>slightly larger</u> than V_{LINE} in Step #30.)

$V_{FL(1\%\ L.R.,\ VNL\ =\ +10V)}$ =

$V_{LINE(1\%\ L.R.,\ VNL\ =\ +10V)(measured)}$ =

$V_{DIFFmin(1\%\ L.R.,\ VNL\ =\ +10V)(measured)}$ =

$I_{I(measured)}$ =

$I_{L(measured)}$ =

$P_{I(measured)}$ =

$P_{L(measured)}$ =

$\%\eta_{(1\%\ L.R.,\ VNL\ =\ +10V)(measured)}$ =

$\Delta V_{DIFF(1\%\ L.R.,\ VNL\ =\ +10V)(measured)}$ =

33). Repeat Steps #29 through #31 for a $V_L = V_{NL}$ = of <u>+8V</u>. (*<u>NOTE</u>*: The value of ΔV_{DIFF} should be <u>larger</u> than ΔV_{DIFF} in Step #31 and the value of V_{LINE} should be <u>slightly smaller</u> than V_{LINE} in Step #32.)

$V_{FL(1\%\ L.R.,\ VNL\ =\ +8V)}$ =

$V_{LINE(1\%\ L.R.,\ VNL\ =\ +8V)(measured)}$ =

$V_{DIFFmin(1\%\ L.R.,\ VNL\ =\ +8V)(measured)}$ =

$I_{I(measured)}$ =

$I_{L(measured)}$ =

$P_{I(measured)}$ =

$P_{L(measured)}$ =

$\%\eta_{(1\%\ L.R.,\ VNL\ =\ +8V)(measured)}$ =

$\Delta V_{DIFF(1\%\ L.R.,\ VNL\ =\ +8V)(measured)}$ =

- **Explain the concept of percent efficiency.**
- **What are the advantages and disadvantages of maintaining large differential voltages across the pass transistor? Use calculations and measurements for support.**
- **What are the advantages and disadvantages of maintaining smaller differential voltages across the pass transistor? Use calculations and measurements for support. (*HINT*: your measurements should show that for a constant load regulation, larger changes in ΔV_{DIFF} result in larger changes in line voltage.**
- **What effect does the relative value of load current have on percent efficiency assuming a constant load regulation?**
- **Assuming an unregulated line voltage and constant load resistance, is the regulator a *"better"* regulator at higher efficiencies? (*HINT*: as ΔV_{DIFF} decreases, the pass transistor is more susceptible to line voltage changes (such as ripple) decreasing its ability to regulate at a specified load regulation.) Use calculations and measurements for support.**
- **When does the pass transistor dissipate more power: at higher or lower efficiencies? Use calculations and measurements for support.**
- **By lowering the regulated output voltage and drawing larger currents, the regulator can operate at higher efficiencies with increased load regulation (smaller %L.R.). What is the major disadvantage of this method?**

PART V:
Foldback-Current Limiting

CALCULATIONS:

FOLDBACK-CURRENT LIMITING

34). The circuit in Figure 12 employs a current limiting technique known as *foldback-current limiting*. When current-limiting begins, the peak load current $I_{L(limit)}$ through R_{SC} in both circuits (Figure 11 and Figure 12) are identical and approximately equal to 21mA. When the regulator output in Figure 11 is shorted, Q3 draws most of the extra base current away from the pass transistor, keeping $I_{L(limit)}$ and $I_{PT(limit)}$ essentially constant. However, the power dissipation of the pass transistor becomes exceedingly close to its rated value at room temperature since its differential voltage approaches 20V. To prevent the destruction of the pass transistor, it must be heatsinked. In contrast, the circuit in Figure 12 (with values you will design), *"foldback"* to an $I_{PT(limit)}$ of approximately 7mA when the regulator output is shorted. This greatly reduces the power dissipation of the pass transistor and eliminates the heatsink.

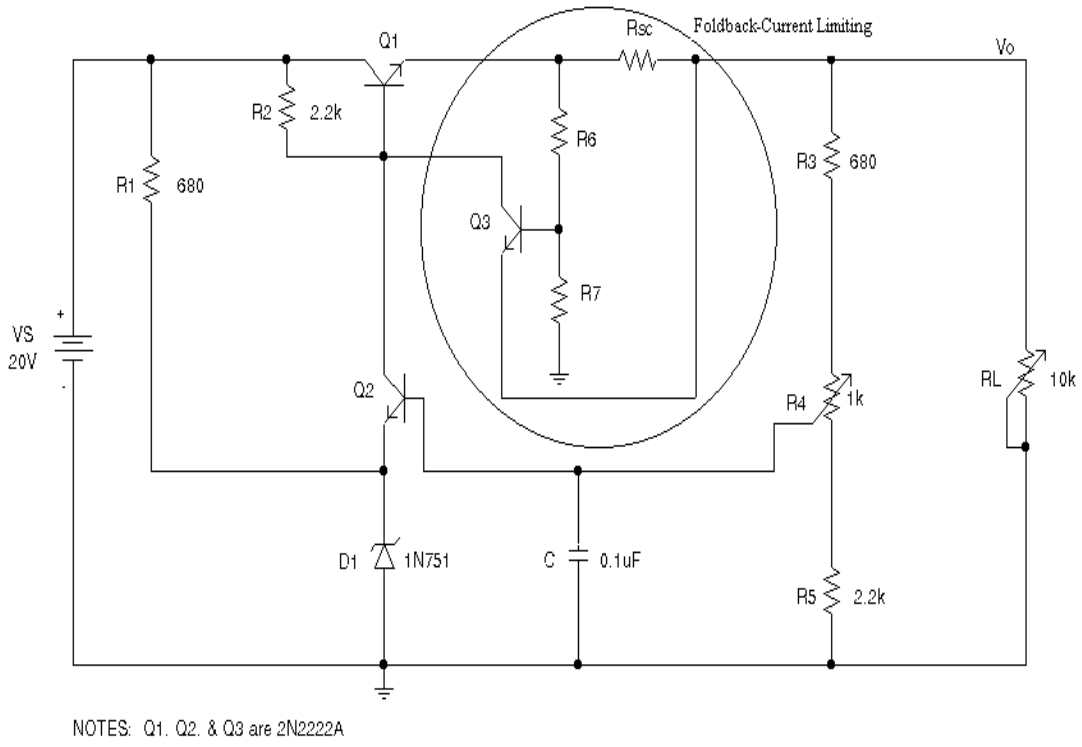


FIGURE 12. Series regulator with foldback-current limiting (Q3, R6, R7, and R_{SC}).[4]

K represents the feedback fraction of $\frac{R7}{R6+R7}$. K is chosen to be <u>0.83</u>. This makes $I_{PT(limit)(max)} \approx 3I_{PT(limit)(min)}$.[4] Calculate R_{SC} and R6 if <u>R7 = 4.7k</u> using the following formula. <u>Select the nearest standard resistor values and record their measured values in TABLE 1.</u>

(<u>IMPORTANT</u>: select a resistor value for R_{SC} as close as possible to the calculated R_{SC} even if you have to connect multiple resistor values together.)

$$I_{PT(limit)(min)}^{(4)} \approx I_{RSC(limit)(min)} = \frac{V_{BE(Q3)}}{KR_{SC}}$$

R_{SC} =

R6 =

35). Calculate and verify the value of $I_{PT(limit)(max)}$ (approximately 21mA, +-10%) with the following equation. $I_{PT(limit)(min)}$ = <u>7mA</u> and V_L = <u>+8V</u>. Use the closest value you can build using standard resistor values for R_{SC}.

$$I_{PT(limit)(max)}^{(4)} = I_{PT(limit)(min)} + \frac{Vo(1-K)}{KR_{SC}}$$

$I_{PT(limit)(max)}$ =

36). Modify the circuit in Figure 10 to that in Figure 12. Adjust R4 for a V_L of <u>+8V</u>. Connect a 10kΩ potentiometer across the output terminals making sure that the resistance between the wiper and the potentiometer terminal connected to Vo is 10kΩ. Next, insert an ammeter in the R_{SC} branch and <u>slowly</u> adjust R_L for $I_{PT(limit)(max)(measured)}$. Record its value. Next, continue rotating R_L and observe how I_{RSC} decreases. Record the smallest value of I_{RSC} when R_L is shorted (call this $I_{PT(limit)(min)(measured)}$). $I_{PT(limit)(max)(measured)}$ and $I_{PT(limit)(min)(measured)}$ should be within +-10% of the calculated values.

$I_{PT(limit)(max)(measured)}$ =

$I_{PT(limit)(min)(measured)}$ =

37). Measure and record I_{Q1} with an ammeter with R_L shorted. Its value should be within +-10% of $I_{PT(limit)(min)(measured)}$. Next, measure and record the voltage across the pass transistor when R_L is a short. Calculate P_{DQ1}.

I_{Q1} =

$V_{Q1(diff)}$ =

P_{DQ1} =

38). Touch the pass transistor with your fingers when R_L is a short. Note your observations.

Pass transistor observations:

- **Does the pass transistor feel as *"hot"* with foldback current-limiting as it does with constant current-limiting? Why or why not?**
- **How does the power dissipation of the pass transistor in Figure 12 differ from the power dissipation of the pass transistor in Figure 11?**
- **Explain why I_{Q1} is slightly larger than $I_{PT(limit)(min)}$. Why is there a difference when both values are supposed to represent the same pass transistor current? Is accurate to say that I_{Q1} is practically equal to $I_{PT(limit)(min)}$?**

PSPICE SIMULATION:

FOLDBACK-CURRENT LIMITING

39). Simulate the circuit in Figure 12 in PSpice. Generate a graph showing V_L vs. $I_{PT(limit)}$. Label $I_{PT(limit)(max)}$ and $I_{PT(limit)(min)}$. Refer to PART III for PSpice setup parameters. Use the same value for R4 and V_L as in PART III. Use 4.7kΩ for R7 and the calculated resistor values for R6 and R_{SC}.

R4 =

R6 =

R7 =

R_{SC} =

- **Conceptually explain the principle of foldback-current limiting. Use the PSpice graph to illustrate.**
- **What is the main advantage of foldback-current limiting as compared to constant-current limiting? Use lab data and PSpice graphs for support.**

ANALYSIS QUESTIONS

(Listed here for convenience)

Questions 40 through 48 refer to Figure 10.

40). Explain how Q1 and the R3-R4-R5 voltage divider represent an equivalent op-amp noninverting amplifier. Draw the equivalent diagram and use the calculations from "*Minimum and Maximum Load Voltage*" for support.

41). What differences exist, if any, between the error-detection circuit in Figure 10 and the equivalent op-amp circuit? Are the output voltage ranges and "*closed-loop*" regulator gains identical? Explain why an op-amp error-detector is more desirable than a transistor error-detector.

42). Explain the meaning of $Av_{(CL)(range)}$. What does it tell us about the regulator?

43). Draw a block diagram that shows the basic elements of linear series voltage regulators.

44). Briefly explain the purpose of each element:

a). Reference voltage.
b). Control element.
c). Error Detector.
d). Sample circuit.

45). Explain the concepts of load and line regulation. Use measurements for support. What do these terms tell you about voltage regulators?

46). Explain the meaning of a %LR specification. Which is better: high or low percentages? Explain.

47). Explain the meaning of a %SR specification assuming a 10% line voltage change. Which is better: high or low percentages? Explain.

48). From your load regulation measurements, how is %LR affected by differences in load requirements and V_{NL} settings? Are changes linear?

Questions 49 through 69 refer to Figure 11.

49). What is meant by constant-current limiting. Use PSpice graph to illustrate.

50). Is it accurate to say that $I_{L(limit)}$ is practically identical to I_{PT} for constant-current limiting? Explain.

51). Explain how Q3 and R_{SC} limit the output current. Why is I_{SC} different from $I_{L(limit)}$? Where does this extra current come from?

52). Explain and show with calculations what would happen to the pass transistor without Q3 and R_{SC} if the output was shorted? The maximum power dissipation of a 2N2222A is 500mW (TO-18 metal case) or 625mW (TO-92 plastic case).

53). Explain and show with calculations what would happen to the pass transistor and R_{SC} if Q3 was open and the output was shorted?

54). What are some advantages and disadvantages of constant-current limiting?

55). Discuss any differences in the relative temperature of the pass transistor with and without a heatsink.

56). Explain why the pass transistor without a heatsink was much "hotter" than with a heatsink.

57). Explain why the pass transistor without a heatsink is not a good choice for this design? (*HINT*: Derate the transistor power dissipation for a temperature of 30 °C.)

- **Derating factor for 2N2222A (TO-18 metal case) = 2.28 mW / °C**
- **Derating factor for 2N2222A (TO-92 plastic case) = 5 mW / °C**

58). One alternative to using a heatsink is to select another transistor type with a larger power dissipation. Are there any disadvantages that need to be considered?

59). When the line voltage is +20V and the load resistance is 1kΩ, what components *"waste"* most of the input power?

60). For a constant load resistance and output voltage, how is %η affected by a decrease in line voltage?

61). For a constant line and output voltage, how is %η affected by a decrease in load resistance?

62). How does the reference voltage network (R_1 and V_{D1}) affect the %η?

63). Explain the concept of percent efficiency.

64). What are the advantages and disadvantages of maintaining large differential voltages across the pass transistor? Use calculations and measurements for support.

65). What are the advantages and disadvantages of maintaining smaller differential voltages across the pass transistor? Use calculations and measurements for support.

(*HINT*: your measurements should show that for a constant load regulation, larger changes in ΔV_{DIFF} result in larger changes in line voltage.

66). What effect does the relative value of load current have on percent efficiency assuming a constant load regulation?

67). Assuming an unregulated line voltage and constant load resistance, is the regulator a *"better"* regulator at higher efficiencies? (*HINT*: as ΔV_{DIFF} decreases, the pass transistor is more susceptible to line voltage changes (such as ripple) decreasing its ability to regulate at a specified load regulation.) Use calculations and measurements for support.

68). When does the pass transistor dissipate more power: at higher or lower efficiencies? Use calculations and measurements for support.

69). By lowering the regulated output voltage and drawing larger currents, the regulator can operate at higher efficiencies with increased load regulation (smaller %L.R.). What is the major disadvantage of this method?

Questions 70 – 73 refer to Figure 12.

70). Does the pass transistor feel as *"hot"* with foldback current-limiting as it does with constant current-limiting? Why or why not?

71). How does the power dissipation of the pass transistor in Figure 12 differ from the power dissipation of the pas transistor in Figure 11?

72). Explain why I_{Q1} is slightly larger than $I_{PT(limit)(min)}$. Why is there a difference when both values are supposed to represent the same pass transistor current? Is accurate to say that I_{Q1} is practically equal to $I_{PT(limit)(min)}$?

73). Conceptually explain the principle of foldback-current limiting. Use the PSpice graph to illustrate.

74). What is the main advantage of foldback-current limiting as compared to constant-current limiting? Use lab data and PSpice graphs for support.

REFERENCES:

This lab experiment was mainly inspired from Malvino's *"Series Regulators"* lab experiment contained in the manual *"Experiments for Malvino Electronic Principles, 5th & 6th Editions"*. Although Malvino's lab experiment is quite simple, it fostered a deeper interest in the subject to the author. The goal was to provide a more comprehensive study and depth to the subject of series voltage regulators without an integrated circuit perspective. The other sources listed here also provided important concepts and formulas to the *"BACKGROUND"* section of this experiment.

4. **Floyd, Thomas L. *"Electronic Devices, 5th Ed."* Prentice Hall, 1999. *"Chapter 18: Voltage Regulators"*, pgs. 912 – 920.**

5. **Malvino, Albert Paul. *"Experiments for Malvino Electronic Principles, 6th Ed."* Glencoe/McGraw-Hill, 1999. *"Experiment 60: Series Regulators"*, pgs. 281 – 286.**

6. **Bell, David. *"Electronic Devices and Circuits, 3rd Ed."* Prentice Hall, 1996. *"Chapter 16: Power Supplies, Breakdown Diodes, and Voltage Regulators"*, pgs. 486 – 498.**

7. **Malvino, Albert Paul. *"Electronic Principles, 5th Ed."* Glencoe/McGraw-Hill, 1995. *"Chapter 23: Regulated Power Supplies"*, pgs. 842 – 879.**