AN3320
Application note

Getting started with STM32F20xxx/21xxx MCU hardware development

Introduction

This application note is intended for system designers who require a hardware implementation overview of the development board features such as the power supply, the clock management, the reset control, the boot mode settings and the debug management. It shows how to use the high-density performance line STM32F20xxx/21xxx product families and describes the minimum hardware resources required to develop an STM32F20xxx/21xxx application.

Detailed reference design schematics are also contained in this document with descriptions of the main components, interfaces and modes.

Contents

List of tables

List of figures

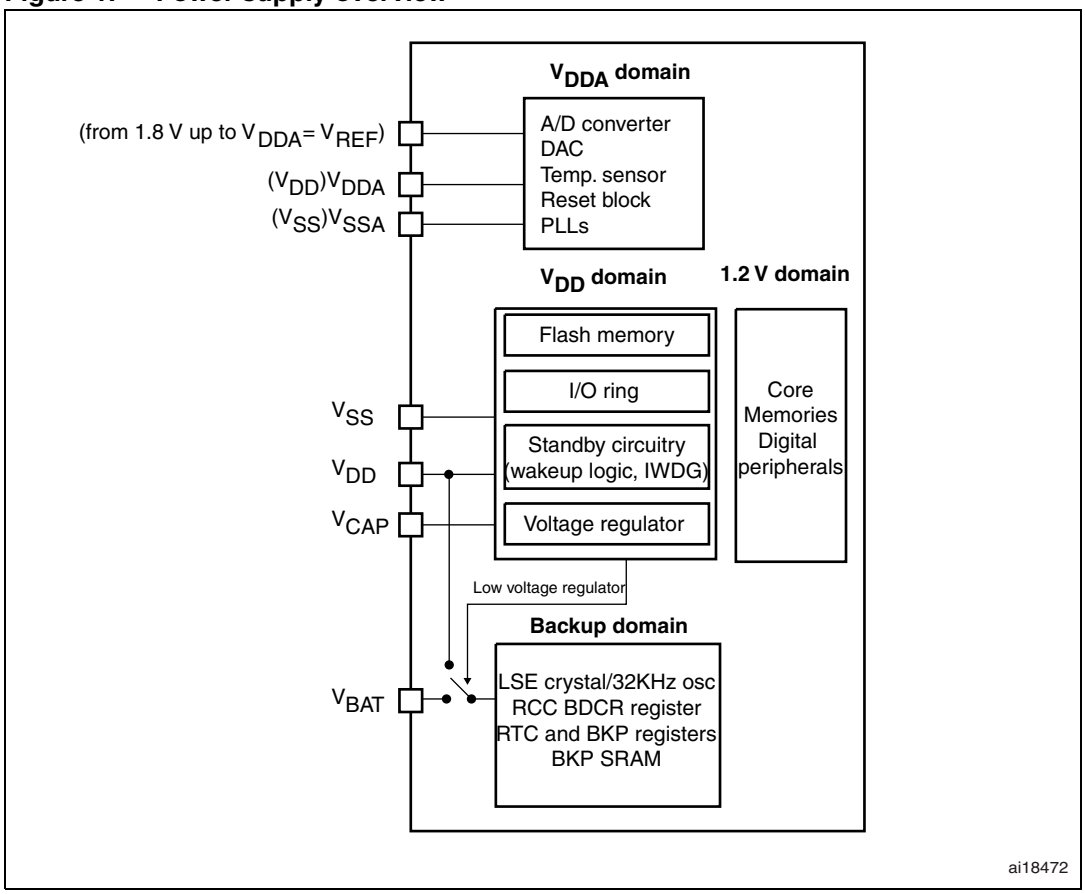
1 Power supplies

1.1 Introduction

The device requires a 1.8 V to 3.6 V operating voltage supply (V_{DD}), excepted the WLCSP package witch requires 1.65 V to 3.6 V. An embedded regulator is used to supply the internal 1.2 V digital power.

The real-time clock (RTC) and backup registers can be powered from the V_{BAT} voltage when the main V_{DD} supply is powered off.

Figure 1. Power supply overview



1. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
2. The voltage on V_{REF} ranges from 1.65 V to V_{DDA} for WLCSP64+2 packages.

1.1.1 Independent A/D converter supply and reference voltage

To improve conversion accuracy, the ADC has an independent power supply that can be filtered separately, and shielded from noise on the PCB.

- the ADC voltage supply input is available on a separate V_{DDA} pin
- an isolated supply ground connection is provided on the V_{SSA} pin

When available (depending on package), V_{REF-} must be tied to V_{SSA}.

On 100-pin package and above and on WLCSP64+2

To ensure a better accuracy on low-voltage inputs, the user can connect a separate external reference voltage ADC input on V_{REF+}. The voltage on V_{REF+} may range from 1.8 V to V_{DDA}. On WLCSP64+2, the V_{REF-} pin is not available, it is internally connected to the ADC ground (V_{SSA}).

On 64-pin packages

The V_{REF+} and V_{REF-} pins are not available, they are internally connected to the ADC voltage supply (V_{DDA}) and ground (V_{SSA}).

1.1.2 Battery backup

To retain the content of the Backup registers when V_{DD} is turned off, the V_{BAT} pin can be connected to an optional standby voltage supplied by a battery or another source.

The V_{BAT} pin also powers the RTC unit, allowing the RTC to operate even when the main digital supply (V_{DD}) is turned off. The switch to the V_{BAT} supply is controlled by the power down reset (PDR) circuitry embedded in the Reset block.

If no external battery is used in the application, it is highly recommended to connect V_{BAT} externally to V_{DD}.

1.1.3 Voltage regulator

The voltage regulator is always enabled after reset. It works in three different modes depending on the application modes.

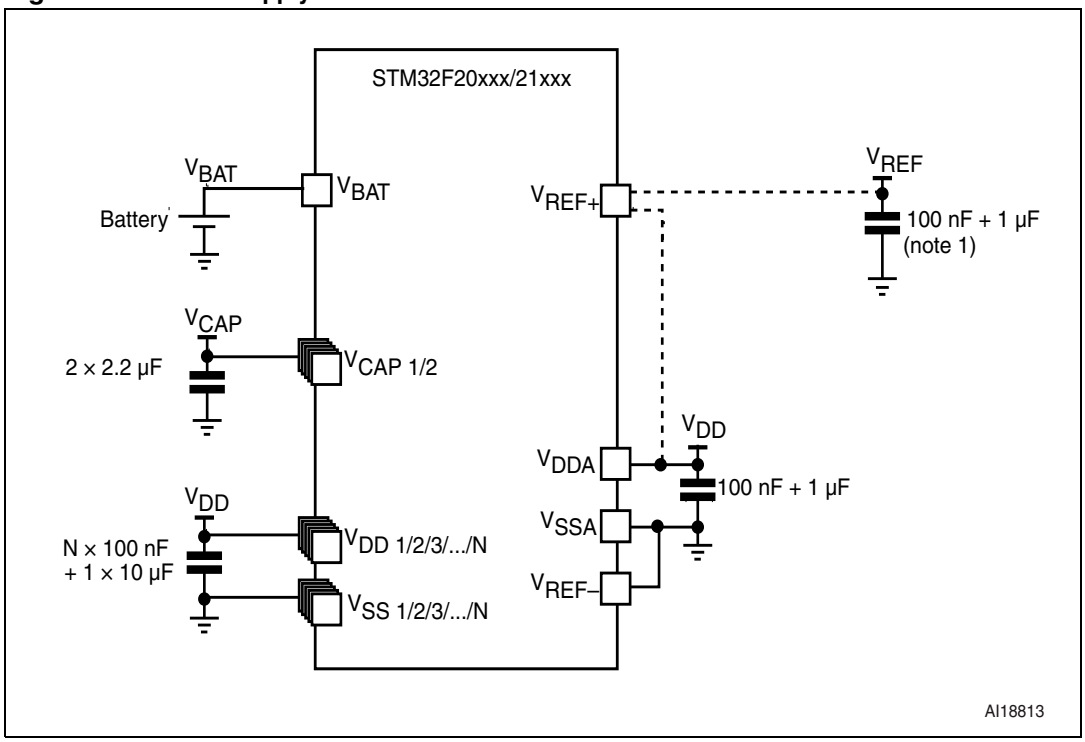
- in Run mode, the regulator supplies full power to the 1.2 V domain (core, memories and digital peripherals)
- in Stop mode, the regulator supplies low power to the 1.2 V domain, preserving the contents of the registers and SRAM
- in Standby mode, the regulator is powered off. The contents of the registers and SRAM are lost except for those concerned with the Standby circuitry and the Backup domain.

1.2 Power supply schemes

The circuit is powered by a stabilized power supply, V_{DD}.

- Caution:
  - The V_{DD} voltage range is 1.8 V to 3.6 V (and 1.65 V to 3.6 V for WLCSP64+2 package)
- The V_{DD} pins must be connected to V_{DD} with external decoupling capacitors: one single Tantalum or Ceramic capacitor (min. 4.7 µF typ.10 µF) for the package + one 100 nF Ceramic capacitor for each V_{DD} pin.
- The V_{BAT} pin can be connected to the external battery (1.65 V < V_{BAT} < 3.6 V). If no external battery is used, it is recommended to connect this pin to V_{DD} with a 100 nF external ceramic decoupling capacitor.
- The V_{DDA} pin must be connected to two external decoupling capacitors (100 nF Ceramic + 1 µF Tantalum or Ceramic).
- The V_{REF+} pin can be connected to the V_{DDA} external power supply. If a separate, external reference voltage is applied on V_{REF+}, a 100 nF and a 1 µF capacitors must be connected on this pin. In all cases, V_{REF+} must be kept between 1.65 V and V_{DDA}.
- Additional precautions can be taken to filter analog noise:
  - V_{DDA} can be connected to V_{DD} through a ferrite bead.
  - The V_{REF+} pin can be connected to V_{DDA} through a resistor (typ. 47 Ω).
- The V_{CAPx} pin are usually connected only to a capacitor. On WLCSP66 and UFBGA176 package, those pins can be connected to an external 1.2 V power supply when the REGOFF pin is activated (this will avoid some power loss in the internal regulator), see STM32F20xxx/21xxx datasheet for details.

Figure 2. Power supply scheme



1. Optional. If a separate, external reference voltage is connected on V_{REF+}, the two capacitors (100 nF and 1 µF) must be connected.
2. V_{REF+} is either connected to V_{REF} or to V_{DDA}.
3. N is the number of V_{DD} and V_{SS} inputs.

1.3 Reset & power supply supervisor

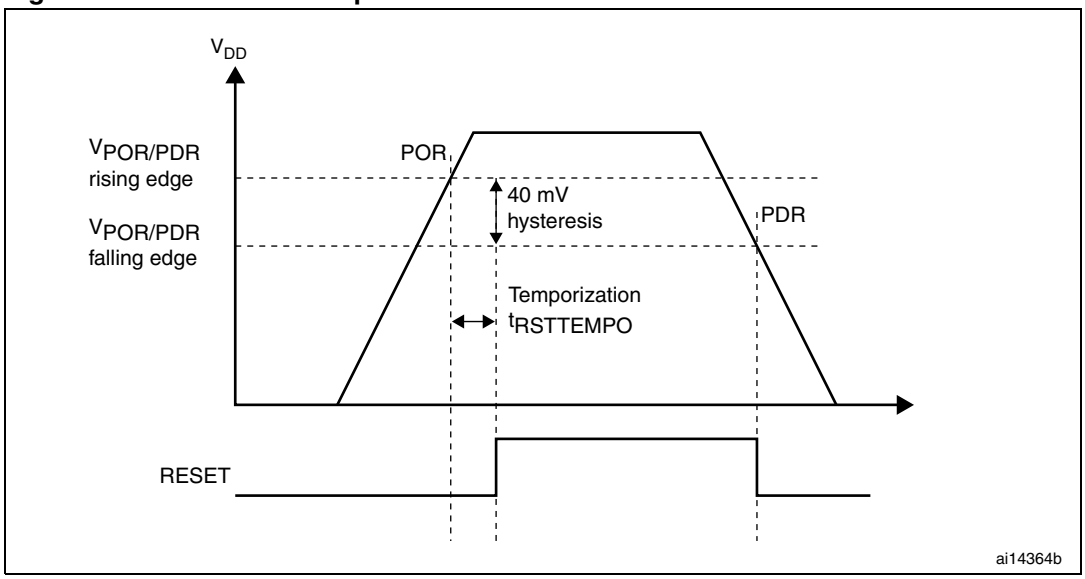
1.3.1 Power on reset (POR) / power down reset (PDR)

The device has an integrated POR/PDR circuitry that allows proper operation starting from 1.8 V.

The device remains in the Reset mode as long as V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit. For more details concerning the power on/power down reset threshold, refer to the electrical characteristics in STM32F20xxx/21xxx datasheets.

On WLCSP66 package if IRROFF pin is set to V_{DD} (in that case REGOFF pin must not be activated, see *Chapter 1.2: Power supply schemes*), the PDR is not functional. Then the V_{DD} can lower below 1.8 V, but the external circuitry must ensure that reset pin is activated when V_{DD}/V_{DDA} becomes below 1.65 V.

Figure 3. Power-on reset/power-down reset waveform



1. $t_{RSTTEMPO}$ is approximately 2.6 ms. $V_{POR/PDR}$ rising edge is 1.74 V (typ.) and $V_{POR/PDR}$ falling edge is 1.70 V (typ.). Refer to STM32F20xxx/21xxx datasheets for actual value.

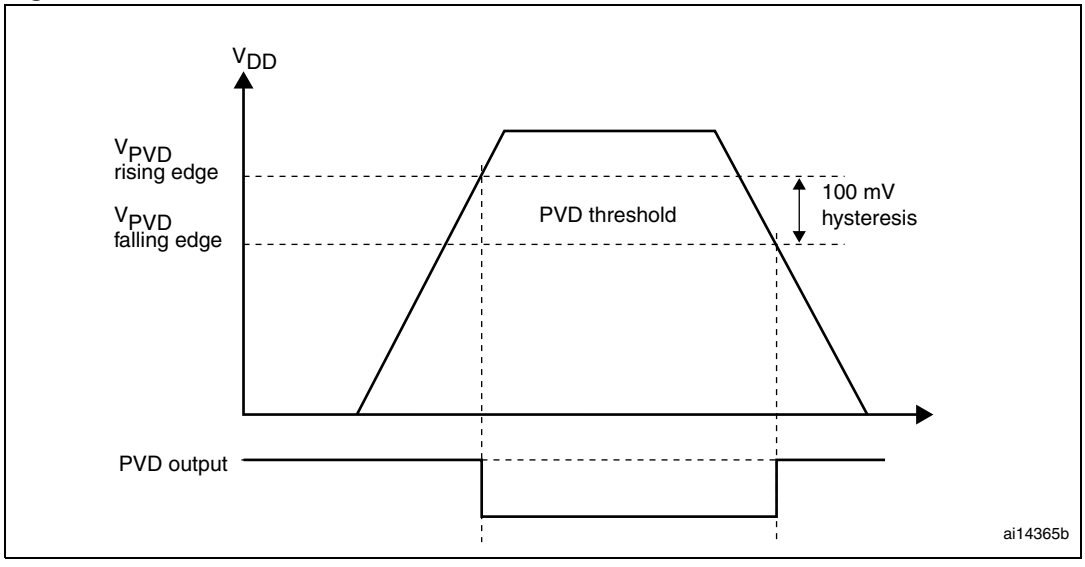
1.3.2 Programmable voltage detector (PVD)

You can use the PVD to monitor the V_{DD} power supply by comparing it to a threshold selected by the PLS[2:0] bits in the Power control register (PWR_CR).

The PVD is enabled by setting the PVDE bit.

A PVDO flag is available, in the Power control/status register (PWR_CSR), to indicate whether V_{DD} is higher or lower than the PVD threshold. This event is internally connected to EXTI Line16 and can generate an interrupt if enabled through the EXTI registers. The PVD output interrupt can be generated when V_{DD} drops below the PVD threshold and/or when V_{DD} rises above the PVD threshold depending on the EXTI Line16 rising/falling edge configuration. As an example the service routine can perform emergency shutdown tasks.

Figure 4. PVD thresholds



1.3.3 System reset

A system reset sets all registers to their reset values except for the reset flags in the clock controller CSR register and the registers in the Backup domain (see *Figure 1*).

A system reset is generated when one of the following events occurs:

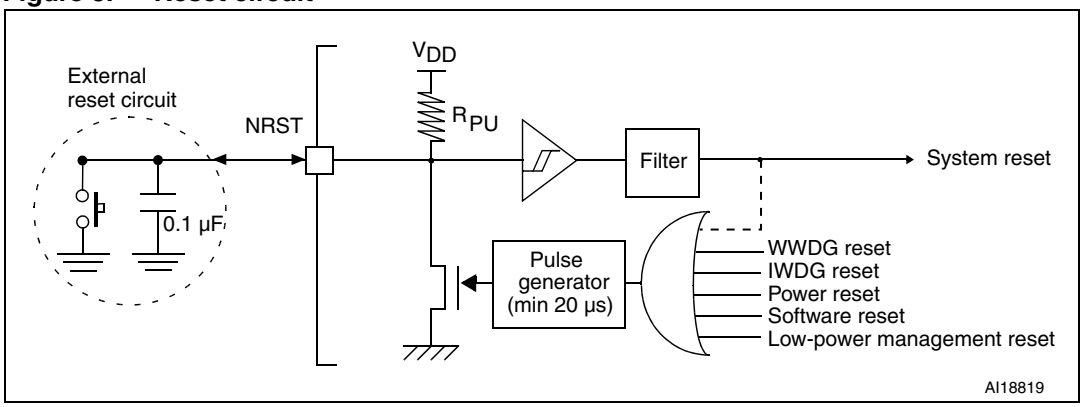
1. A low level on the NRST pin (external reset)
2. window watchdog end-of-count condition (WWDG reset)
3. Independent watchdog end-of-count condition (IWDG reset)
4. A software reset (SW reset)
5. Low-power management reset

The reset source can be identified by checking the reset flags in the Control/Status register, RCC_CSR.

The STM32F20xxx/21xxx does not require an external reset circuit to power-up correctly. Only a pull-down capacitor is recommended to improve EMS performance by protecting the device against parasitic resets. See *Figure 5*.

Charging and discharging a pull-down capacitor through an internal resistor increases the device power consumption. The capacitor recommended value (100 nF) can be reduced to 10 nF to limit this power consumption;

Figure 5. Reset circuit



2 Clocks

Three different clock sources can be used to drive the system clock (SYSCLK):

- HSI oscillator clock (high-speed internal clock signal)
- HSE oscillator clock (high-speed external clock signal)
- PLL clock

The devices have two secondary clock sources:

- 32 kHz low-speed internal RC (LSI RC) that drives the independent watchdog and, optionally, the RTC used for Auto-wakeup from the Stop/Standby modes.
- 32.768 kHz low-speed external crystal (LSE crystal) that optionally drives the real-time clock (RTCCLK)

Each clock source can be switched on or off independently when it is not used, to optimize the power consumption.

Refer to the STM32F20xxx/21xxx reference manual RM0033 for the description of the clock tree.

2.1 HSE OSC clock

The high-speed external clock signal (HSE) can be generated from two possible clock sources:

- HSE external crystal/ceramic resonator (see *Figure 7*)
- HSE user external clock (see *Figure 6*)

Figure 6. HSE external clock

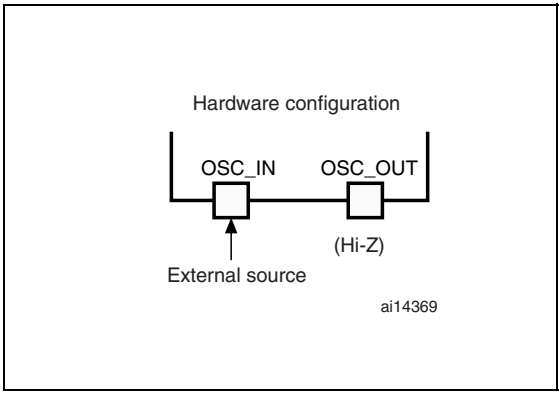
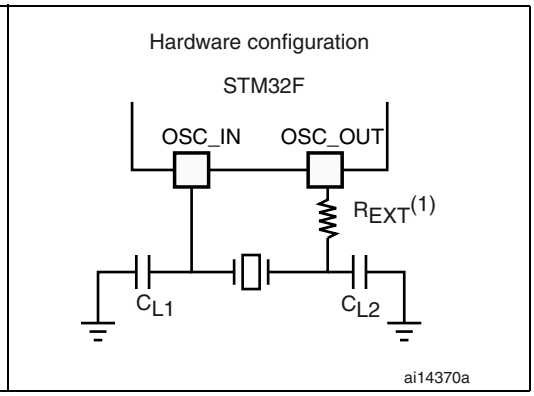


Figure 7. HSE crystal/ceramic resonators



1. The value of R_{EXT} depends on the crystal characteristics. Typical value is in the range of 5 to 6 R_S (resonator series resistance).
2. Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where: C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF. Please refer to *Section 5: Recommendations on page 21* to minimize its value.

2.1.1 External source (HSE bypass)

In this mode, an external clock source must be provided. It can have a frequency from 1 to 16 MHz (refer to STM32F20xxx/21xxx datasheets for actual max value).

The external clock signal (square, sine or triangle) with a duty cycle of about 50%, has to drive the OSC_IN pin while the OSC_OUT pin must be left in the high impedance state (see *Figure 7* and *Figure 6*).

2.1.2 External crystal/ceramic resonator (HSE crystal)

The external oscillator frequency ranges from 4 to 26 MHz.

The external oscillator has the advantage of producing a very accurate rate on the main clock. The associated hardware configuration is shown in *Figure 7*. Using a 25 MHz oscillator frequency is a good choice to get accurate Ethernet, USB OTG high-speed peripheral, and I^2S.

The resonator and the load capacitors have to be connected as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The load capacitance values must be adjusted according to the selected oscillator.

For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors in the 5 pF-to-25 pF range (typ.), designed for high-frequency applications and selected to meet the requirements of the crystal or resonator. C_{L1} and $C_{L2,}$ are usually the same value. The crystal manufacturer typically specifies a load capacitance that is the series combination of C_{L1} and C_{L2}. The PCB and MCU pin capacitances must be included when sizing C_{L1} and C_{L2} (10 pF can be used as a rough estimate of the combined pin and board capacitance).

Refer to the electrical characteristics sections in the datasheet of your product for more details.

2.2 LSE OSC clock

The low-speed external clock signal (LSE) can be generated from two possible clock sources:

- LSE external crystal/ceramic resonator (see *Figure 9*)
- LSE user external clock (see *Figure 8*)

Figure 8. LSE external clock

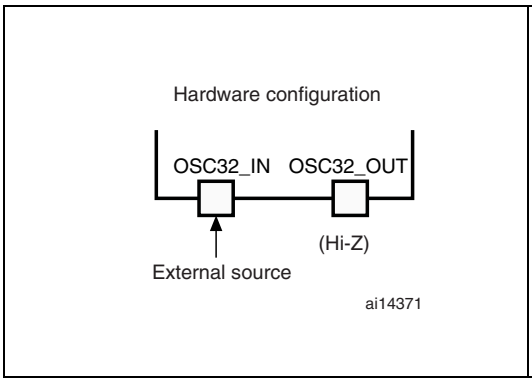
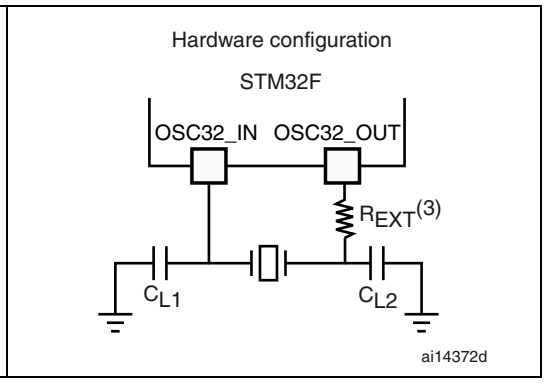


Figure 9. LSE crystal/ceramic resonators



1. **"LSE crystal/ceramic resonators" figure:**
To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leq 7$ pF. Never use a resonator with a load capacitance of 12.5 pF.
2. **"LSE external clock" and "LSE crystal/ceramic resonators" figures:**
OSC32_IN and OSC32_OUT pins can be used also as GPIO, but it is recommended not to use them as both RTC and GPIO pins in the same application.
3. **"LSE crystal/ceramic resonators" figure:**
The value of R_{EXT} depends on the crystal characteristics. A 0 Ω resistor would work but would not be optimal. To fine tube R_S value, refer to AN2867 - Oscillator design guide for ST microcontrollers.

2.2.1 External source (LSE bypass)

In this mode, an external clock source must be provided. It can have a frequency of up to 1 MHz. The external clock signal (square, sine or triangle) with a duty cycle of about 50% has to drive the OSC32_IN pin while the OSC32_OUT pin must be left high impedance (see *Figure 8*).

2.2.2 External crystal/ceramic resonator (LSE crystal)

The LSE crystal is a 32.768 kHz low-speed external crystal or ceramic resonator. It has the advantage of providing a low-power, but highly accurate clock source to the real-time clock peripheral (RTC) for clock/calendar or other timing functions.

The resonator and the load capacitors have to be connected as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The load capacitance values must be adjusted according to the selected oscillator.

2.3 Clock security system (CSS)

The clock security system can be activated by software. In this case, the clock detector is enabled after the HSE oscillator startup delay, and disabled when this oscillator is stopped.

- If a failure is detected on the HSE oscillator clock, the oscillator is automatically disabled. A clock failure event is sent to the break input of the TIM1 advanced control timer and an interrupt is generated to inform the software about the failure (clock security system interrupt CSSI), allowing the MCU to perform rescue operations. The CSSI is linked to the Cortex™-M3 NMI (non-maskable interrupt) exception vector.
- If the HSE oscillator is used directly or indirectly as the system clock (indirectly means that it is used as the PLL input clock, and the PLL clock is used as the system clock), a detected failure causes a switch of the system clock to the HSI oscillator and the disabling of the external HSE oscillator. If the HSE oscillator clock (divided or not) is the clock entry of the PLL used as system clock when the failure occurs, the PLL is disabled too.

For details, see the STM32F20xxx/21xxx (RM0033) reference manuals available from the STMicroelectronics website *www.st.com*.

3 Boot configuration

3.1 Boot mode selection

In the STM32F20xxx/21xxx, three different boot modes can be selected by means of the BOOT[1:0] pins as shown in *Table 1*.

Table 1. Boot modes

BOOT mode selection pins		Boot mode	Aliasing
BOOT1	BOOT0		
x	0	Main Flash memory	Main Flash memory is selected as boot space
0	1	System memory	System memory is selected as boot space
1	1	Embedded SRAM	Embedded SRAM is selected as boot space

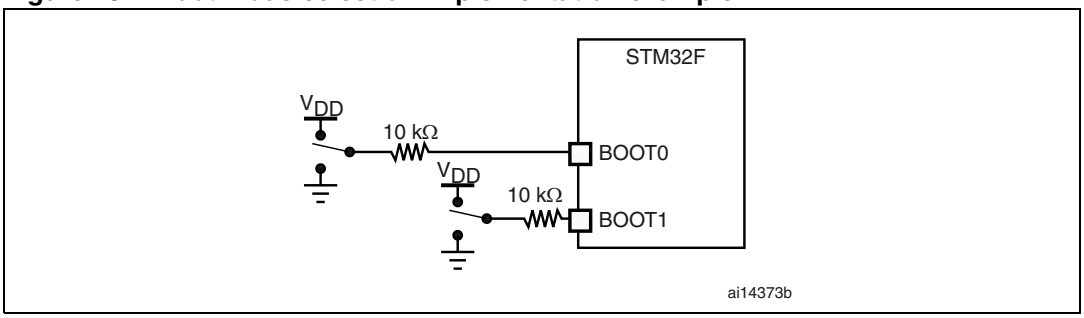
The values on the BOOT pins are latched on the 4th rising edge of SYSCLK after a reset. It is up to the user to set the BOOT1 and BOOT0 pins after reset to select the required boot mode.

The BOOT pins are also resampled when exiting the Standby mode. Consequently, they must be kept in the required Boot mode configuration in the Standby mode. After this startup delay has elapsed, the CPU fetches the top-of-stack value from address 0x0000 0000, and starts code execution from the boot memory starting from 0x0000 0004.

3.2 Boot pin connection

Figure 10 shows the external connection required to select the boot memory of the STM32F20xxx/21xxx.

Figure 10. Boot mode selection implementation example



1. Resistor values are given only as a typical example.

3.3 Embedded boot loader mode

The Embedded boot loader mode is used to reprogram the Flash memory using one of the available serial USART1(PA9/PA10), USART3(PB10/11 & PC10/11), CAN2(PB5/13) or USB OTG FS(PA11/12) in Device mode (DFU: device firmware upgrade).

The USART peripheral operates with the internal 16 MHz oscillator (HSI). The CAN and USB OTG FS, however, can only function if an external 8 MHz-26 MHz clock (HSE) is present.

This embedded boot loader is located in the System memory and is programmed by ST during production.

For additional information, refer to AN2606.

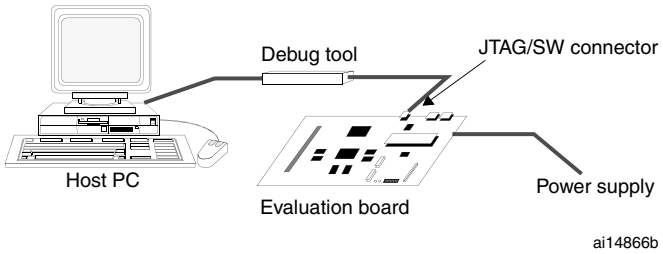
4 Debug management

4.1 Introduction

The Host/Target interface is the hardware equipment that connects the host to the application board. This interface is made of three components: a hardware debug tool, a JTAG or SW connector and a cable connecting the host to the debug tool.

Figure 11 shows the connection of the host to the evaluation board STM3220G-EVAL.

Figure 11. Host-to-board connection



4.2 SWJ debug port (serial wire and JTAG)

The STM32F20xxx/21xxx core integrates the serial wire / JTAG debug port (SWJ-DP). It is an ARM® standard CoreSight™ debug port that combines a JTAG-DP (5-pin) interface and a SW-DP (2-pin) interface.

- The JTAG debug port (JTAG-DP) provides a 5-pin standard JTAG interface to the AHP-AP port
- The serial wire debug port (SW-DP) provides a 2-pin (clock + data) interface to the AHP-AP port

In the SWJ-DP, the two JTAG pins of the SW-DP are multiplexed with some of the five JTAG pins of the JTAG-DP.

4.3 Pinout and debug port pins

The STM32F20xxx/21xxx MCU is offered in various packages with different numbers of available pins. As a result, some functionality related to the pin availability may differ from one package to another.

4.3.1 SWJ debug port pins

Five pins are used as outputs for the SWJ-DP as *alternate functions* of general-purpose I/Os (GPIOs). These pins, shown in *Table 2*, are available on all packages.

Table 2. Debug port pin assignment

SWJ-DP pin name	JTAG debug port		SW debug port		Pin assignment
	Type	Description	Type	Debug assignment	
JTMS/SWDIO	I	JTAG test mode selection	I/O	Serial wire data input/output	PA13
JTCK/SWCLK	I	JTAG test clock	I	Serial wire clock	PA14
JTDI	I	JTAG test data input	-	-	PA15
JTDO/TRACESWO	O	JTAG test data output	-	TRACESWO if async trace is enabled	PB3
JNTRST	I	JTAG test nReset	-	-	PB4

4.3.2 Flexible SWJ-DP pin assignment

After reset (SYSRESETn or PORESETn), all five pins used for the SWJ-DP are assigned as dedicated pins immediately usable by the debugger host (note that the trace outputs are not assigned except if explicitly programmed by the debugger host).

However, some of the JTAG pins shown in *Table 3* can be configured to an alternate function through the GPIOx_AFRx registers.

Table 3. SWJ I/O pin availability

Available Debug ports	SWJ I/O pin assigned				
	PA13 / JTMS/ SWDIO	PA14 / JTCK/ SWCLK	PA15 / JTDI	PB3 / JTDO	PB4/ JNTRST
Full SWJ (JTAG-DP + SW-DP) - reset state	X	X	X	X	X
Full SWJ (JTAG-DP + SW-DP) but without JNTRST	X	X	X	X	
JTAG-DP disabled and SW-DP enabled	X	X			
JTAG-DP disabled and SW-DP disabled	Released				

Table 3 shows the different possibilities to release some pins.

For more details, see the STM32F20xxx/21xxx (RM0033) reference manual, available from the STMicroelectronics website *www.st.com*.

4.3.3 Internal pull-up and pull-down resistors on JTAG pins

The JTAG input pins must *not* be floating since they are directly connected to flip-flops to control the debug mode features. Special care must be taken with the SWCLK/TCK pin that is directly connected to the clock of some of these flip-flops.

To avoid any uncontrolled I/O levels, the STM32F20xxx/21xxx embeds internal pull-up and pull-down resistors on JTAG input pins:

- JNTRST: Internal pull-up
- JTDI: Internal pull-up
- JTMS/SWDIO: Internal pull-up
- TCK/SWCLK: Internal pull-down

Once a JTAG I/O is released by the user software, the GPIO controller takes control again. The reset states of the GPIO control registers put the I/Os in the equivalent state:

- JNTRST: Input pull-up
- JTDI: Input pull-up
- JTMS/SWDIO: Input pull-up
- JTCK/SWCLK: Input pull-down
- JTDO: Input floating

The software can then use these I/Os as standard GPIOs.

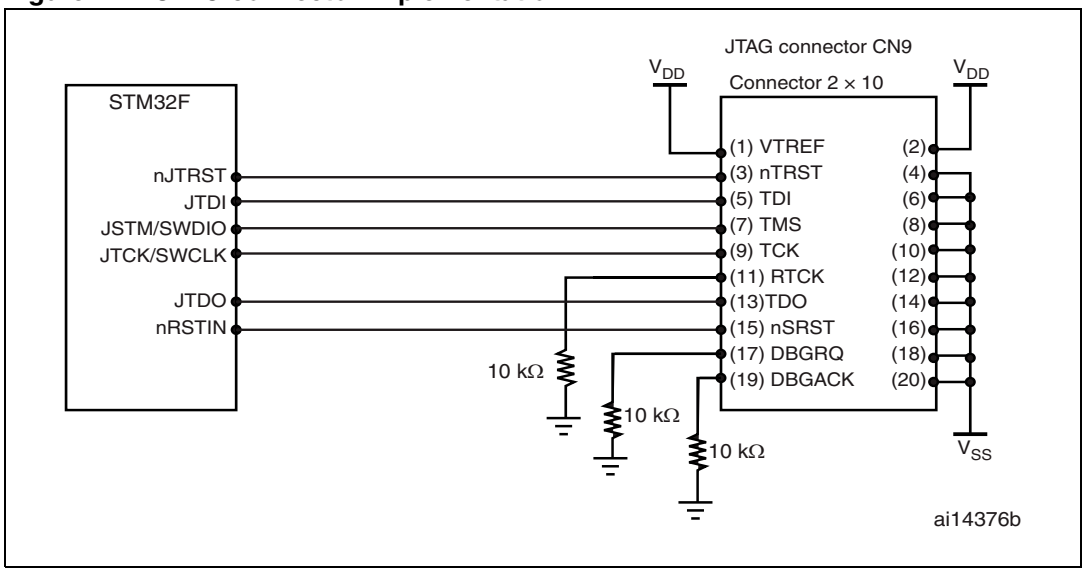
Note: The JTAG IEEE standard recommends to add pull-up resistors on TDI, TMS and nTRST but there is no special recommendation for TCK. However, for the STM32F20xxx/21xxx*, an integrated pull-down resistor is used for JTCK.*

Having embedded pull-up and pull-down resistors removes the need to add external resistors.

4.3.4 SWJ debug port connection with standard JTAG connector

Figure 12 shows the connection between the STM32F20xxx/21xxx and a standard JTAG connector.

Figure 12. JTAG connector implementation



5 Recommendations

5.1 Printed circuit board

For technical reasons, it is best to use a multilayer printed circuit board (PCB) with a separate layer dedicated to ground (V_{SS}) and another dedicated to the V_{DD} supply. This provides good decoupling and a good shielding effect. For many applications, economical reasons prohibit the use of this type of board. In this case, the major requirement is to ensure a good structure for ground and for the power supply.

5.2 Component position

A preliminary layout of the PCB must separate the different circuits according to their EMI contribution in order to reduce cross-coupling on the PCB, that is noisy, high-current circuits, low-voltage circuits, and digital components.

5.3 Ground and power supply (V_{SS}, V_{DD})

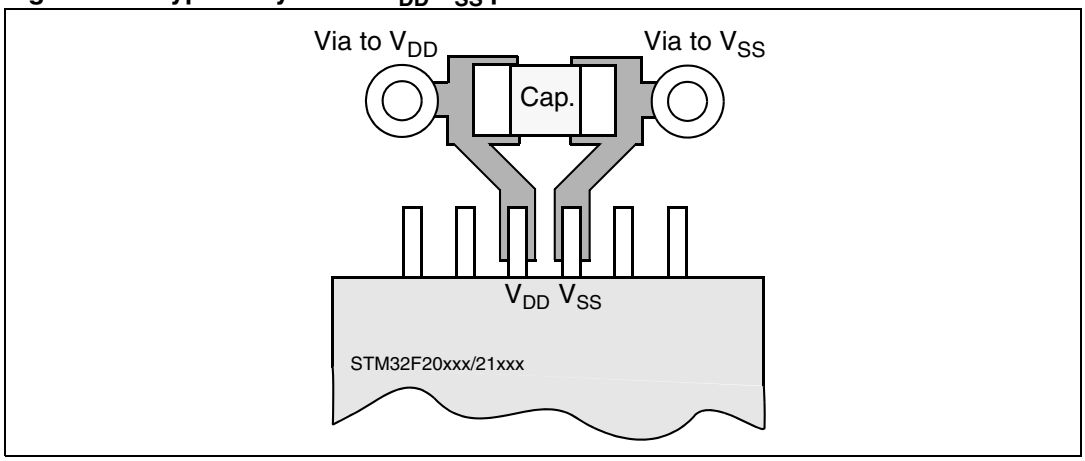
Every block (noisy, low-level sensitive, digital, etc.) should be grounded individually and all ground returns should be to a single point. Loops must be avoided or have a minimum area. The power supply should be implemented close to the ground line to minimize the area of the supply loop. This is due to the fact that the supply loop acts as an antenna, and is therefore the main transmitter and receiver of EMI. All component-free PCB areas must be filled with additional grounding to create a kind of shielding (especially when using single-layer PCBs).

5.4 Decoupling

All power supply and ground pins must be properly connected to the power supplies. These connections, including pads, tracks and vias should have as low impedance as possible. This is typically achieved with thick track widths and, preferably, the use of dedicated power supply planes in multilayer PCBs.

In addition, each power supply pair should be decoupled with filtering Ceramic capacitors C (100 nF) and one single Tantalum or Ceramic capacitor (min. 4.7 µF typ.10 µF) connected in parallel on the STM32F20xxx/21xxx device. These capacitors need to be placed as close as possible to, or below, the appropriate pins on the underside of the PCB. Typical values are 10 nF to 100 nF, but exact values depend on the application needs. *Figure 13* shows the typical layout of such a V_{DD}/V_{SS} pair.

Figure 13. Typical layout for V_{DD}/V_{SS} pair



5.5 Other signals

When designing an application, the EMC performance can be improved by closely studying:

- Signals for which a temporary disturbance affects the running process permanently (the case of interrupts and handshaking strobe signals, and not the case for LED commands).
  For these signals, a surrounding ground trace, shorter lengths and the absence of noisy and sensitive traces nearby (crosstalk effect) improve EMC performance.
  For digital signals, the best possible electrical margin must be reached for the two logical states and slow Schmitt triggers are recommended to eliminate parasitic states.
- Noisy signals (clock, etc.)
- Sensitive signals (high impedance, etc.)

5.6 Unused I/Os and features

All microcontrollers are designed for a variety of applications and often a particular application does not use 100% of the MCU resources.

To increase EMC performance, unused clocks, counters or I/Os, should not be left free, e.g. I/Os should be set to “0” or “1”(pull-up or pull-down to the unused I/O pins.) and unused features should be “frozen” or disabled.

6 Reference design

6.1 Description

The reference design shown in *Figure 14*, is based on the STM32F207IF(H6), a highly integrated microcontroller running at 120 MHz, that combines the Cortex™-M3 32-bit RISC CPU core with 1 Mbyte of embedded Flash memory and up to 128 + 4 Kbytes of high-speed SRAM.

This reference design can be tailored to any other STM32F20xxx/21xxx device with different package, using the pins correspondence given in *Table 6: Reference connection for all packages*.

6.1.1 Clock

Two clock sources are used for the microcontroller:

- LSE: X1– 32.768 kHz crystal for the embedded RTC
- HSE: X2– 25 MHz crystal for the STM32F20xxx/21xxx microcontroller

Refer to *Section 2: Clocks on page 12*.

6.1.2 Reset

The reset signal in *Figure 14* is active low. The reset sources include:

- Reset button (B1)
- Debugging tools via the connector CN1

Refer to *Section 1.3: Reset & power supply supervisor on page 9*.

6.1.3 Boot mode

The boot option is configured by setting switches SW2 (Boot 0) and SW1 (Boot 1). Refer to *Section 3: Boot configuration on page 16*.

Note: In low-power mode (more specially in Standby mode) the boot mode is mandatory to be able to connect to tools (the device should boot from the SRAM).

6.1.4 SWJ interface

The reference design shows the connection between the STM32F20xxx/21xxx and a standard JTAG connector. Refer to *Section 4: Debug management on page 18*.

Note: It is recommended to connect the reset pins so as to be able to reset the application from the tools.

6.1.5 Power supply

Refer to *Section 1: Power supplies on page 6*.

6.2 Component references

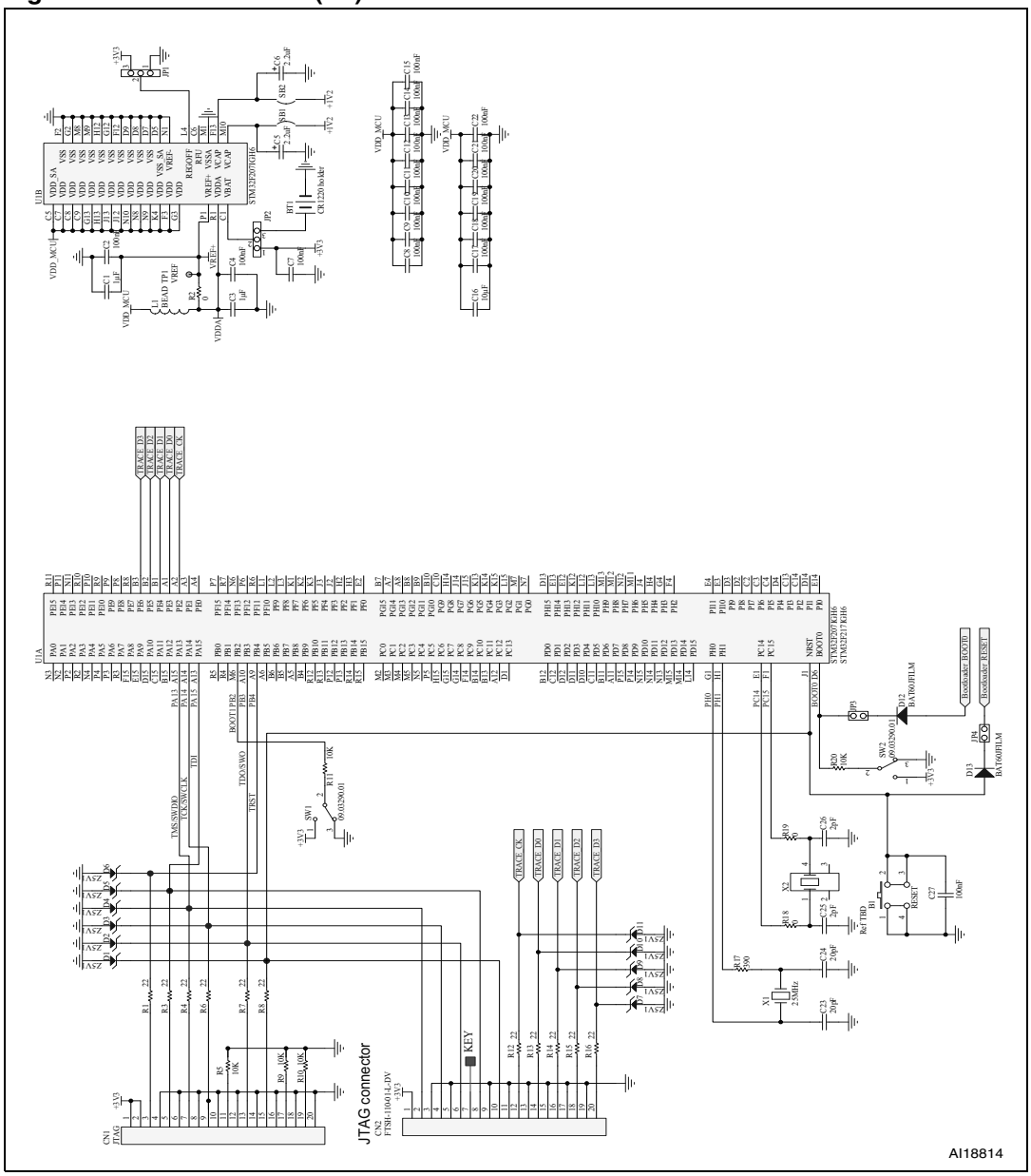
Table 4. Mandatory components

Id	Components name	Reference	Quantity	Comments
1	Microcontroller	STM32F207IG(H6)	1	176-pin package
2	Capacitors	100 nF	16	Ceramic capacitors (decoupling capacitors)
3	Capacitor	10 µF	1	Ceramic capacitor (decoupling capacitor)

Table 5. Optional components

Id	Components name	Reference	Quantity	Comments
1	Resistor	10 kΩ	5	pull-up and pull-down for JTAG and Boot mode.
2	Resistor	390 Ω	1	Used for HSE: the value depends on the crystal characteristics. This resistor value is given only as a typical example.
3	Resistor	0 Ω	1	Used for LSE: the value depends on the crystal characteristics. This resistor value is given only as a typical example.
4	Capacitor	100 nF	2	Ceramic capacitor.
5	Capacitor	2 pF	2	Used for LSE: the value depends on the crystal characteristics.
6	Capacitor	1 µF	2	Used for V_{DDA} and V_{REF}
7	Capacitor	2.2 µF	2	Used for internal regulator when it is on.
8	Capacitor	20 pF	2	Used for HSE: the value depends on the crystal characteristics.
9	Quartz	25 MHz	1	Used for HSE.
10	Quartz	32 kHz	1	Used for LSE.
11	JTAG connector	HE10	1	
12	Transil diode	5 V-400 W	11	For JTAG protection.
13	Resistor	22 Ohm	11	For JTAG protection.
14	Battery	3V3	1	If no external battery is used in the application, it is recommended to connect V_{BAT} externally to V_{DD}.
15	Switch	3V3	2	Used to select the right boot mode.
16	Push-button	B1	1	
17	Jumper	3 pins	2	Used to select V_{BAT} source, and REGOFF pin.
18	Debug trace connector	FTSH-110-01-L-DV	1	Used for JTAG/SWD and debug trace.

Figure 14. STM32F207IG(H6) microcontroller reference schematic



1. If no external battery is used in the application, it is recommended to connect V_{BAT} externally to V_{DD}.
2. To be able to reset the device from the tools this resistor has to be kept.

Table 6. Reference connection for all packages

Pin name	Pin numbers for LQFP packages				Pin numbers for BGA package	Pin numbers for WLCSP package
	176 pins	144 pins	100 pins	64 pins	176 pins	64+2 pins
OSC_IN	29	23	12	5	G1	E9
OSC_OUT	30	24	13	6	H1	F9
PC15-OSC32_OUT	10	9	9	4	F1	C9
PC14-OSC32_IN	9	8	8	3	E1	B9
BOOT0	166	138	94	60	D6	B6
PB2-BOOT1	58	48	37	28	M6	J4
NRST	31	25	14	7	J1	E8
PA13	124	105	72	46	A15	B2
PA14	137	109	76	49	A14	A1
PA15	138	110	77	50	A13	A2
PB4	162	134	90	56	A9	B4
PB3	161	133	89	55	A10	A4
V_{CAP_1}	81	71	49	31	M10	J3
V_{CAP_2}	125	106	73	47	F13	C2
V_{SS_2}	126	107	74	-	F12	B1
V_{SS_3}	-	-	-	63	-	D8
V_{SS_4}	48	38	27	18	-	F1
V_{SS_5}	22	16	10	-	G2	H9
V_{SS_6}	61	51	-	-	M8	-
V_{SS_7}	71	61	-	-	M9	-
V_{SS_8}	102	83	-	-	-	-
V_{SS_9}	113	94	-	-	G12	-
V_{SS_10}	148	120	-	-	D8	-
V_{SS_11}	158	130	-	-	D7	-
V_{SS_13}	14	-	-	-	F2	-
V_{SS_14}	90	-	-	-	H12	-
V_{SS_15}	135	-	-	-	D9	-
V_{DD_1}	82	72	50	32	N10	-
V_{DD_2}	127	108	75	48	G13	A8
V_{DD_3}	172	144	100	64	C5	D9

Table 6. Reference connection for all packages (continued)

Pin name	Pin numbers for LQFP packages				Pin numbers for BGA package	Pin numbers for WLCSP package
	176 pins	144 pins	100 pins	64 pins	176 pins	64+2 pins
V_{DD_4}	49	39	28	19	K4	E1
V_{DD_5}	23	17	11	-	G3	-
V_{DD_6}	62	52	-	-	N8	-
V_{DD_7}	72	62	-	-	N9	-
V_{DD_8}	103	84	-	-	J13	-
V_{DD_9}	114	95	-	-	H13	-
V_{DD_10}	149	121	-	-	C8	-
V_{DD_11}	159	131	-	-	C7	-
V_{DD_12}	36	30	19	-	-	-
V_{DD_13}	15	-	-	-	F3	-
V_{DD_14}	91	-	-	-	J12	-
V_{DD_15}	136	-	-	-	C9	-
V_{REF+}	38	32	21	-	P1	F7
V_{REF-}	-	-	-	-	N1	-
V_{SS}	-	-	-	-	D5	-
V_{SSA}	37	31	20	12	M1	-
V_{DDA}	39	33	22	13	R1	-
V_{BAT}	6	6	6	1	C1	A9

7 Revision history

Table 7. Document revision history

Date	Revision	Changes
25-Feb-2011	1	Initial release.