Two Wired Interface (TWI) / Inter IC (I^2C)

November 4, 2019

Microprocessor Laboratory EE 337

Department of Electrical Engineering
IIT Bombay

Table of Contents

I^2C

DS1307

AT89C5131A I^2C

Question/Comments

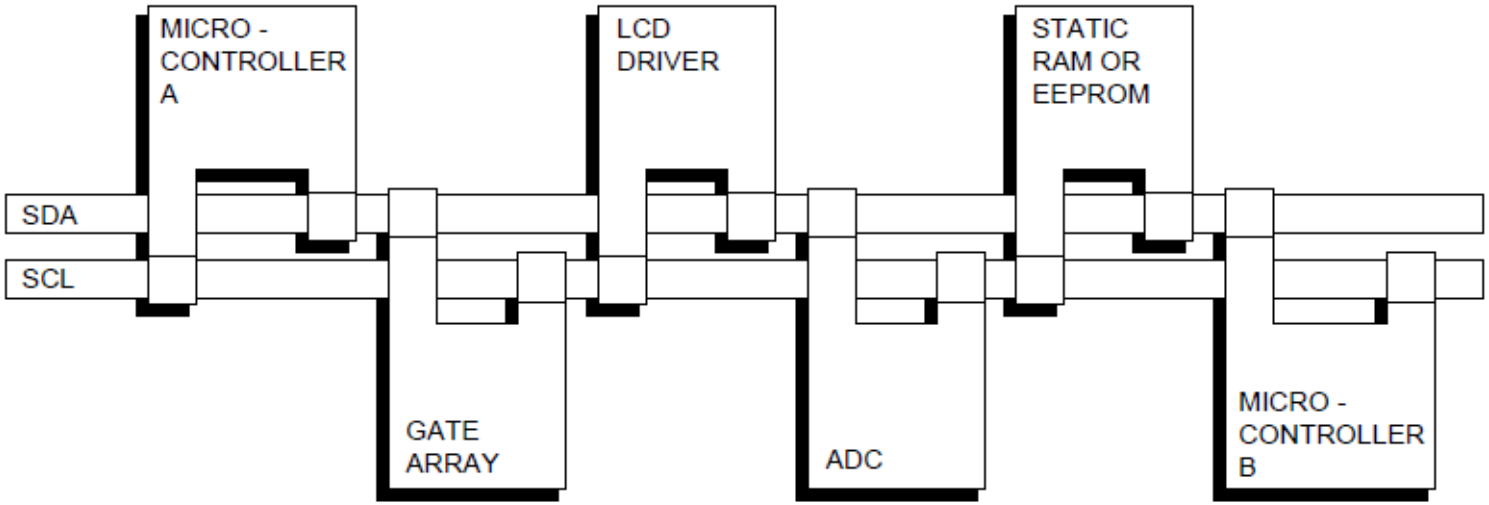
I^2C

I^2C is a two-wired, half-duplex serial mode of communication.

Here are some of the features of the I^2C-(Inter IC):

- Only **two** bus lines are required; a serial data line (SDA) and a serial clock line (SCL).
- **Master** alone determines the clock speed.
- It is **Multi-master** – **Multi-slave** type of communication.
- 8-bit oriented, **bidirectional** data transfers up to:
  - 100 kbps in Standard-mode.
  - 400 kbps in Fast-mode.
  - 1 Mbps in Fast-mode Plus.
  - 3.4 Mbps in High-speed mode.
- **Unidirectional** data transfers up to 5 Mbps in Ultra Fast-mode
- Clock synchronization using **clock stretching**.

I²C Network



7/10 bit addressing modes. The number of ICs that can be connected to the same bus is limited only by the maximum bus capacitance.

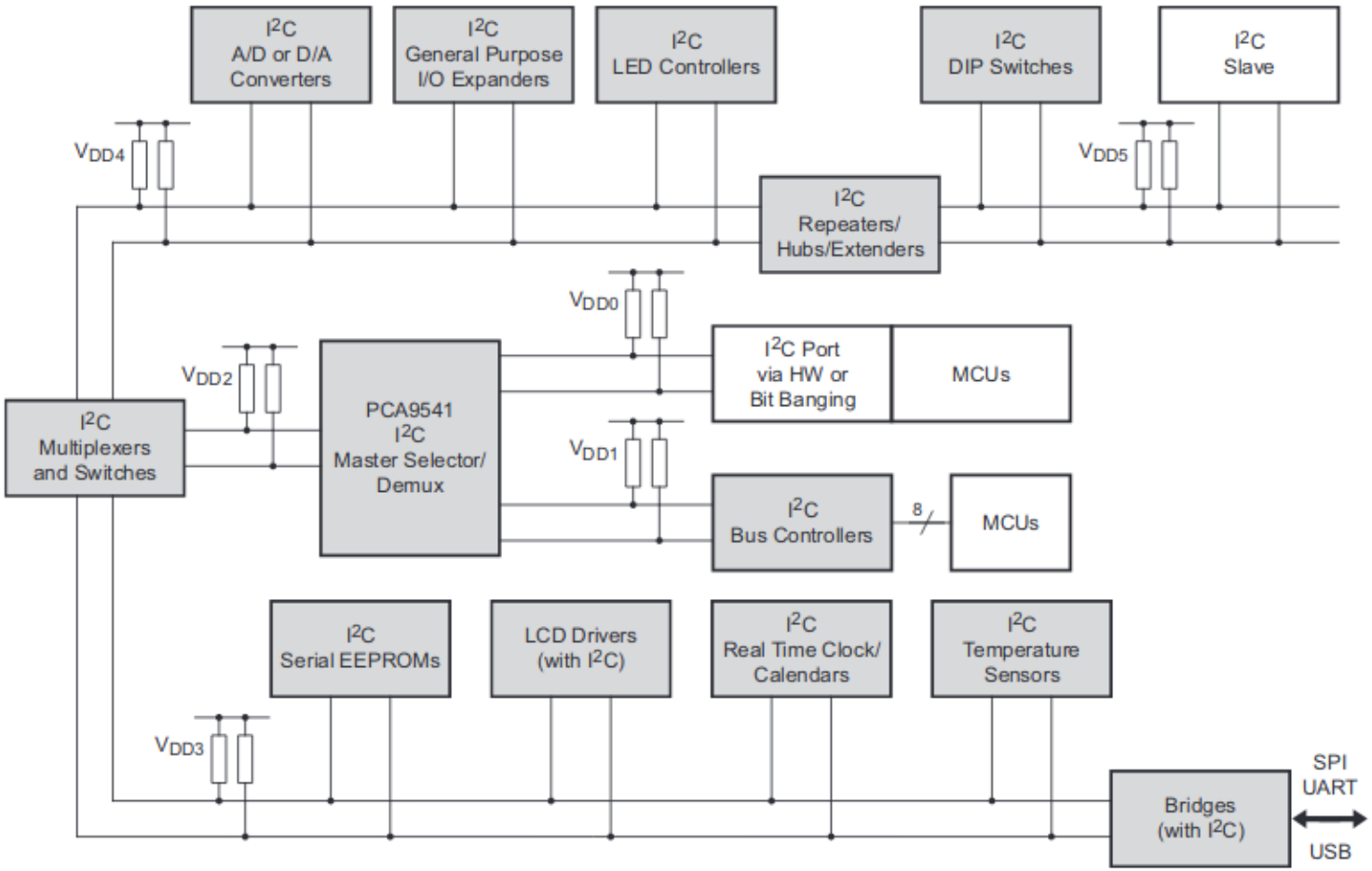
Comparison with UART and SPI

Speed: SPI > I^2C > UART

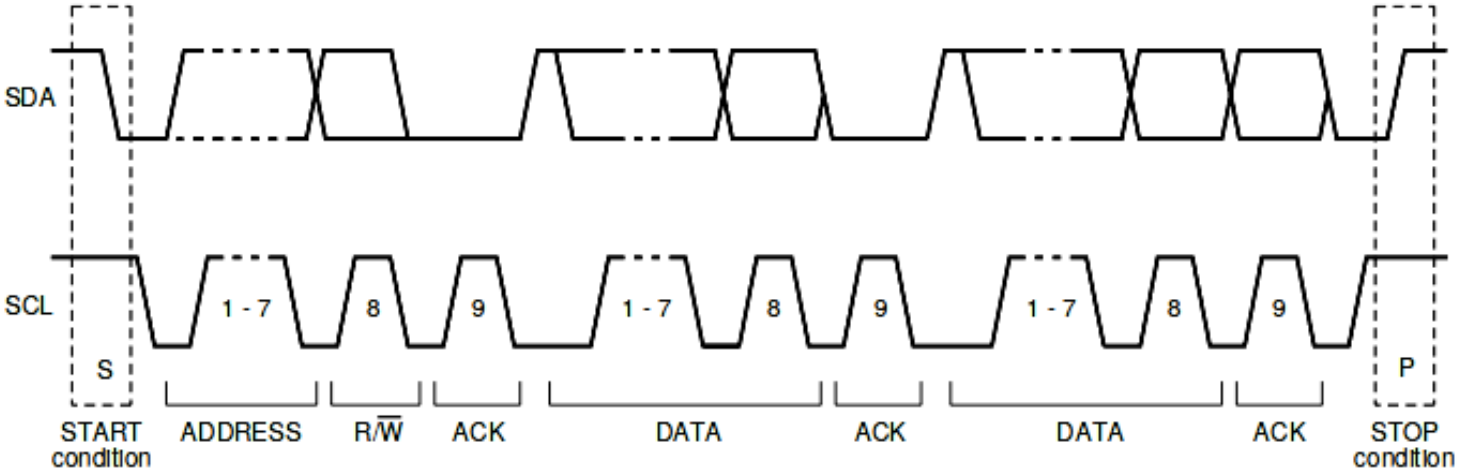
Doesn't require slave-select lines

Multiple Master and Multiple Slave all at once !

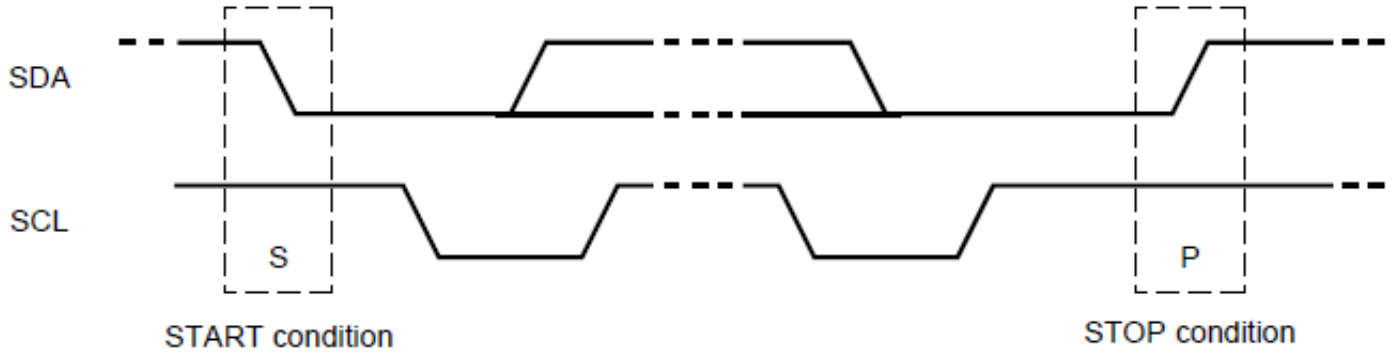
Applications



Data Transfer



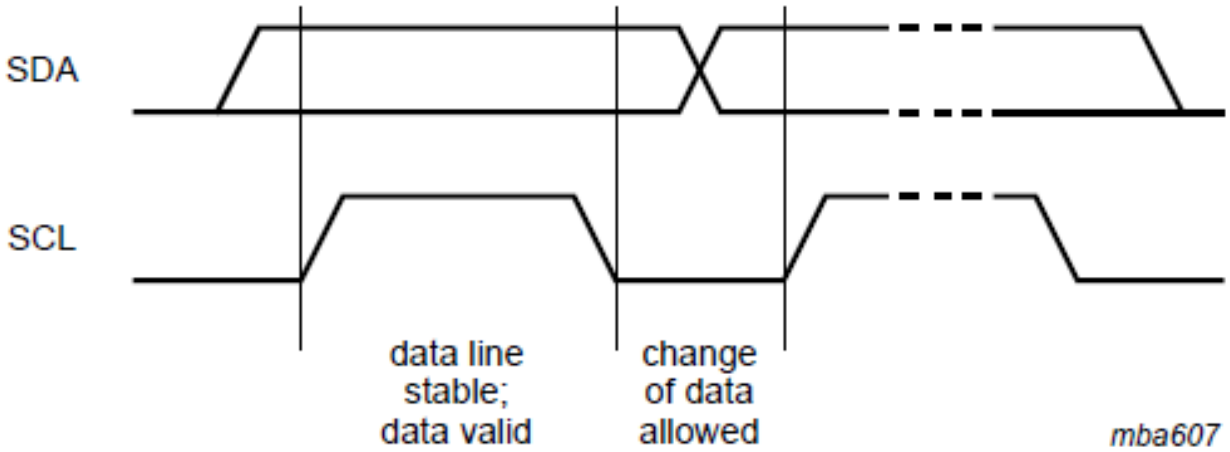
Start and Stop Condition



Transitions on SDA only when SCL is held High.

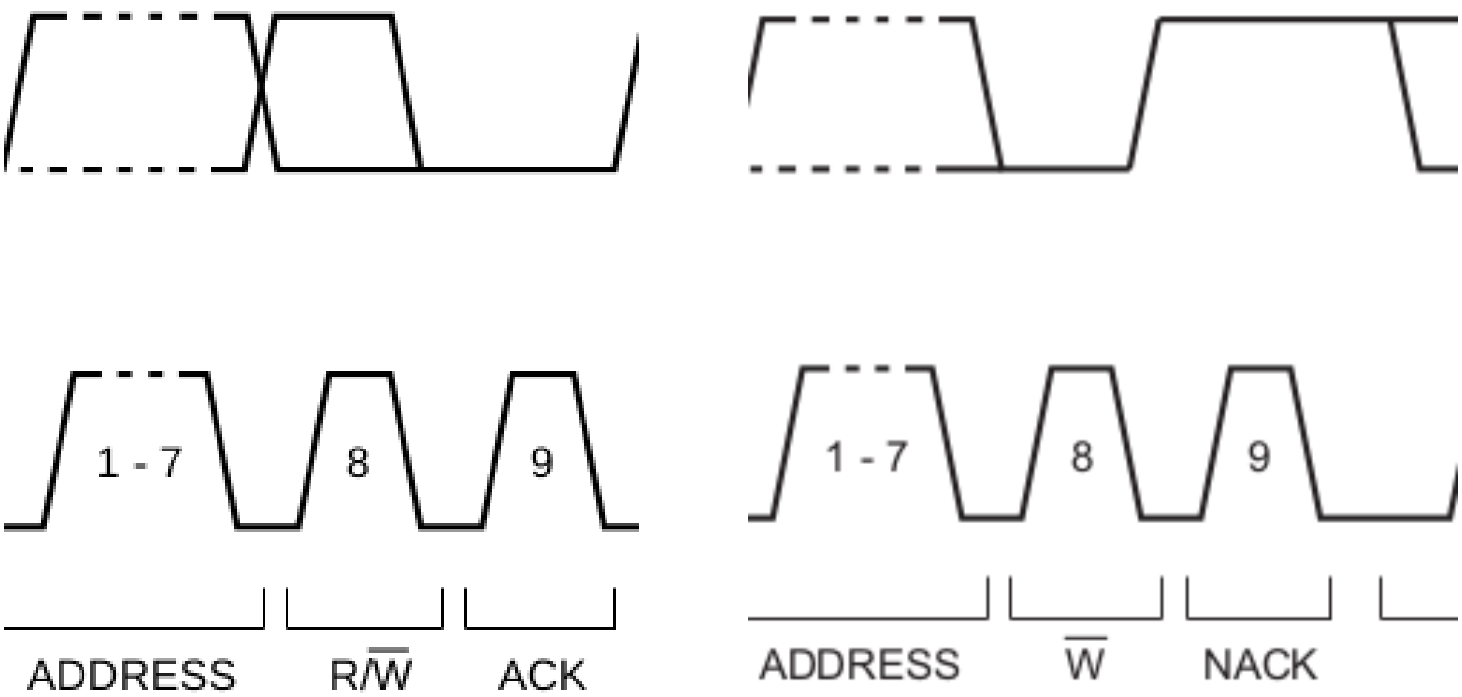
- High -> Low : Start bit
- Low -> High : Stop bit

Data Validity



Transitions on SDA only when SCL is held Low.

Acknowledge and Not Acknowledge



SDA line held Low and High respectively for ACK and NACK on the **9th** clock pulse on SCL line.

Data READ and WRITE

Figure 4. Data Write—Slave Receiver Mode

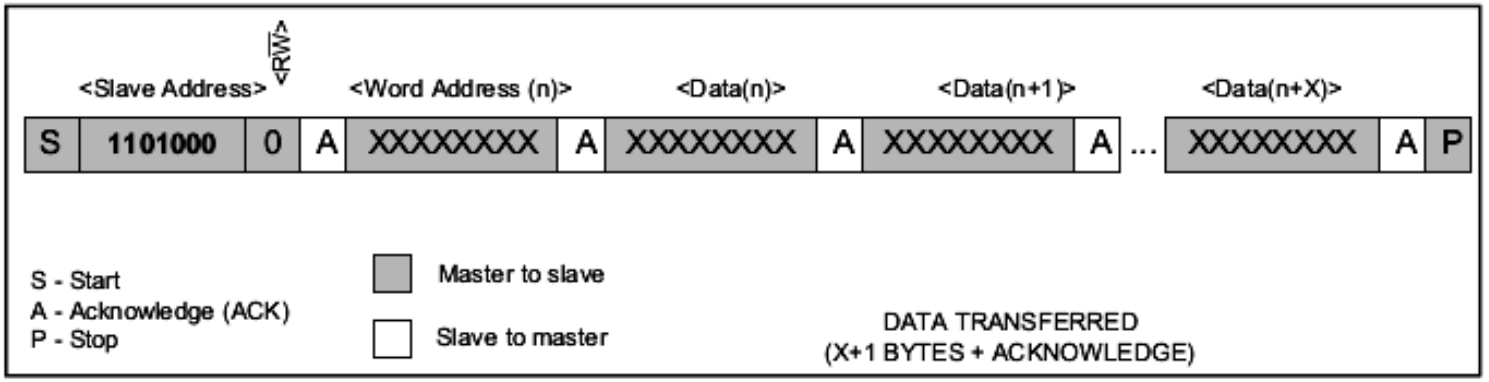
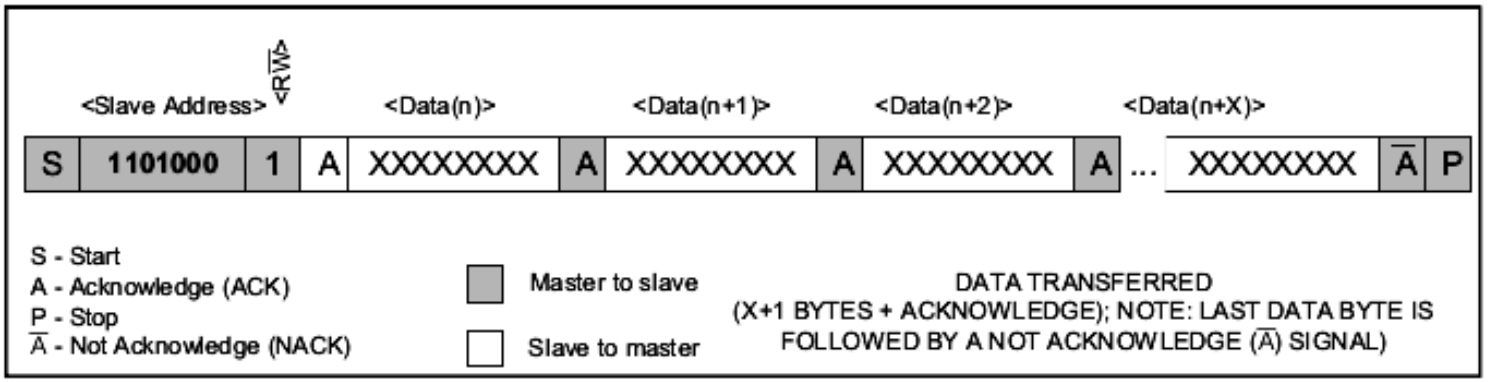


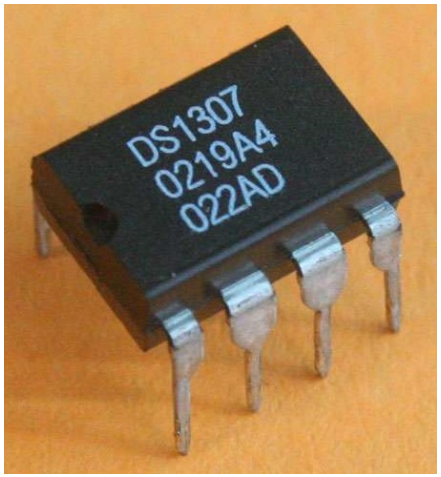
Figure 5. Data Read—Slave Transmitter Mode



We need to **relocate the pointer** to the memory location which we want to access for **READ** or **WRITE** operation.

DS1307

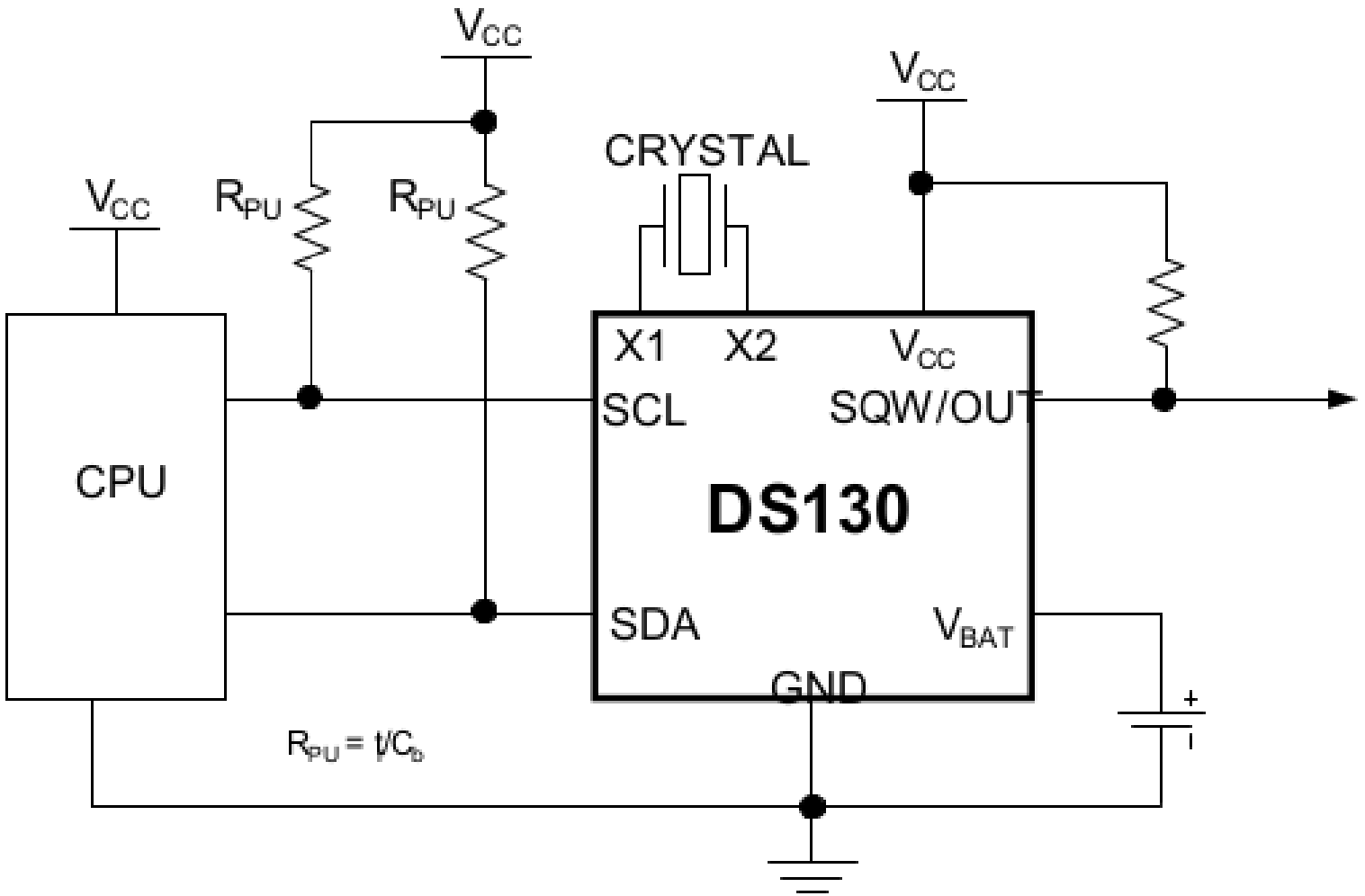
DS1307 is 64 x 8, Serial, I2C Real-Time Clock IC.



Features:

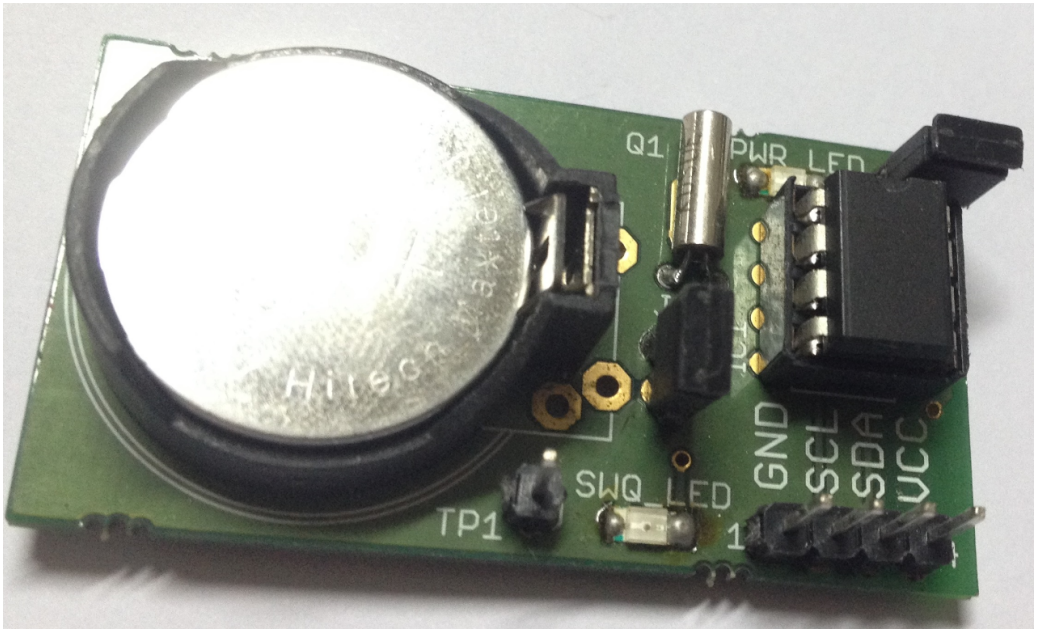
- A full **binary-coded decimal** (BCD) clock/calendar.
- Automatic date adjustment for months with fewer than 31 days, including corrections for leap year up-to year 2100.
- 24-hour or 12- hour format with AM/PM indicator.
- Values corresponding to the days of week are user-defined but must be sequential.

DS1307 Operating circuit



All Registers used are of value 10kΩ.

DS1307 Specifications



Parameter	Symbol	Typical Value
Supply Voltage	V_{cc}	5V
Battery Voltage(Back-up)	V_{BAT}	3V
SCL Clock Frequency	f_{SCL}	100 kHz
START and STOP time-gap	t_{BUF}	$4.7\mu s$
Pin Capacitance(SDA,SCL)	$C_{I/O}$	10pF

DS1307 Memorymap

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
00h	CH	10 Seconds			Seconds				Seconds	00–59
01h	0	10 Minutes			Minutes				Minutes	00–59
02h	0	12	10 Hour	10 Hour	Hours				Hours	1–12 +AM/PM 00–23
		24	PM/ AM							
03h	0	0	0	0	0	DAY			Day	01–07
04h	0	0	10 Date		Date				Date	01–31
05h	0	0	0	10 Month	Month				Month	01–12
06h	10 Year				Year				Year	00–99
07h	OUT	0	0	SQWE	0	0	RS1	RS0	Control	—
08h–3Fh									RAM 56 x 8	00h–FFh

0 = Always reads back as 0.

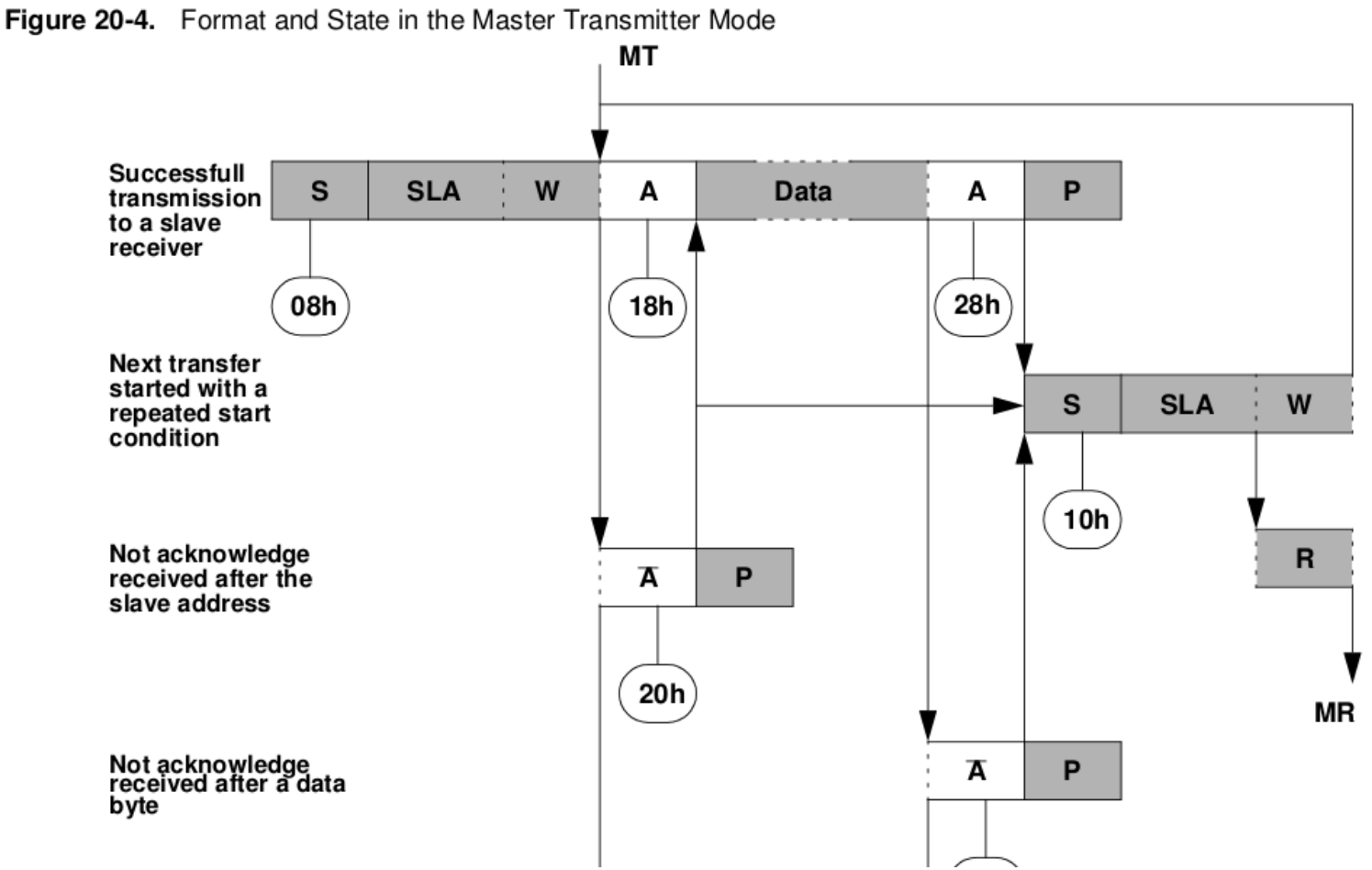
You can use memory locations from 08h-3Fh for storage.
The **7-bit slave address of DS1307 is 1101000**.

AT89C5131A I^{2}C Interfacing

Refer Page 102 of AT895131A Datasheet.

- Configure SDA and SCL pins as inputs.
- Initialize the following AT89c5131A Registers:
  - SSCON - to enable the TWI interface, to program the bit rate, to enable slave modes, to acknowledge or not a received data, to send a START or a STOP condition on the 2-wire bus, and to acknowledge a serial interrupt.
  - Interrupt SFR's - To enable and decide priority of external interrupt from OPT and TWI interrupt
  - TCON - To decide nature of interrupt to be served
- Read SSCS register to figure-out what type of TWI interrupt occurred(refer SSCS register map)
- SSDAT contains the Data to be transmitted/Received

SSCS Register



SSCS Register

Table 20-5. Status in Master Transmitter Mode

SSCS Status Code SSSTA	Status of the Two-wire Bus and Two-wire Hardware	Application software response					Next Action Taken by Two-wire Hardware
		To/From SSDAT	To SSCON				
			SSSTA	SSSTO	SSI	SSAA	
08h	A START condition has been transmitted	Write SLA+W	X	0	0	X	SLA+W will be transmitted.
10h	A repeated START condition has been transmitted	Write SLA+W	X	0	0	X	SLA+W will be transmitted.
		Write SLA+R	X	0	0	X	SLA+R will be transmitted. Logic will switch to master receiver mode
18h	SLA+W has been transmitted; ACK has been received	Write data byte	0	0	0	X	Data byte will be transmitted.
		No SSDAT action	1	0	0	X	Repeated START will be transmitted.
		No SSDAT action	0	1	0	X	STOP condition will be transmitted and SSSTO flag will be reset.
		No SSDAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and SSSTO flag will be reset.
20h	SLA+W has been transmitted; NOT ACK has been received	Write data byte	0	0	0	X	Data byte will be transmitted.
		No SSDAT action	1	0	0	X	Repeated START will be transmitted.
		No SSDAT action	0	1	0	X	STOP condition will be transmitted and SSSTO flag will be reset.

Question/Comments

For any queries regarding I^2C feel free to contact us.

THANK YOU !