Paper / Subject Code: 50394 / Digital Logic & Computer Architecture

DSE/SEM III/ COMP/AIDS/C SCHEME/MAY 2023/ 01.06.23

	(3 hours)		Total Marks: 80	
		 N.B. 1. Question No. 1 is compulsory 2. Attempt any three questions from remaining five questions 3. Assume suitable data if necessary and justify the assumptions 4. Figures to the right indicate full marks 	*05	
Q1	A	Differentiate between Computer organization and computer architecture	05	
	В	By the for of Pestoring division algorithm	05	
	С	Differentiate between Hardwired control unit and Micro programmed control	init 05	
	ıD	Explain IEEE 754 floating point representations.	03	
	•		10	
Q2	A	Draw the flow chart Booths algorithm for multiplication and Perform 6 X 2	05	
	В	Describe the detailed Von-Neumann Model with a neat block diagram	05	
	C	Explain Cache coherence		
Q3	Α	Explain the different addressing modes.	10	
		Define Instruction cycle and draw the state diagram of instruction cycle	05 05	
	C	Explain Bus arbitrations	03	
Q4	A	Explain Micro instruction format and write a micro program for the instruction		
	В	MUL R_1 , R_2 Explain Hardwired Control Unit and the various design methods associated with	th it. 10	
Q5	A	Explain various Memory mapping techniques	10	
	В	Explain the concept of Locality of reference	05	
	C	List & Explain the Characteristics of Memory	05	
Q6	Α	Explain Flynn's classification.	10	
		Describe Instruction Pipelining and its hazards.	10	
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