Date: 1/11/2023

<u>Lab Experiment-6</u> (Batch-1)

- 1. Implement and demonstrate 2 1-bit input ALU using mux and combinational circuits, which can perform AND, OR, NAND, XOR, ADD/SUB (use full adder circuit that can perform both tasks Add/Sub).
- 2. Implement and demonstrate Common Bus System using 8, 4-bit registers and appropriate number of multiplexers.