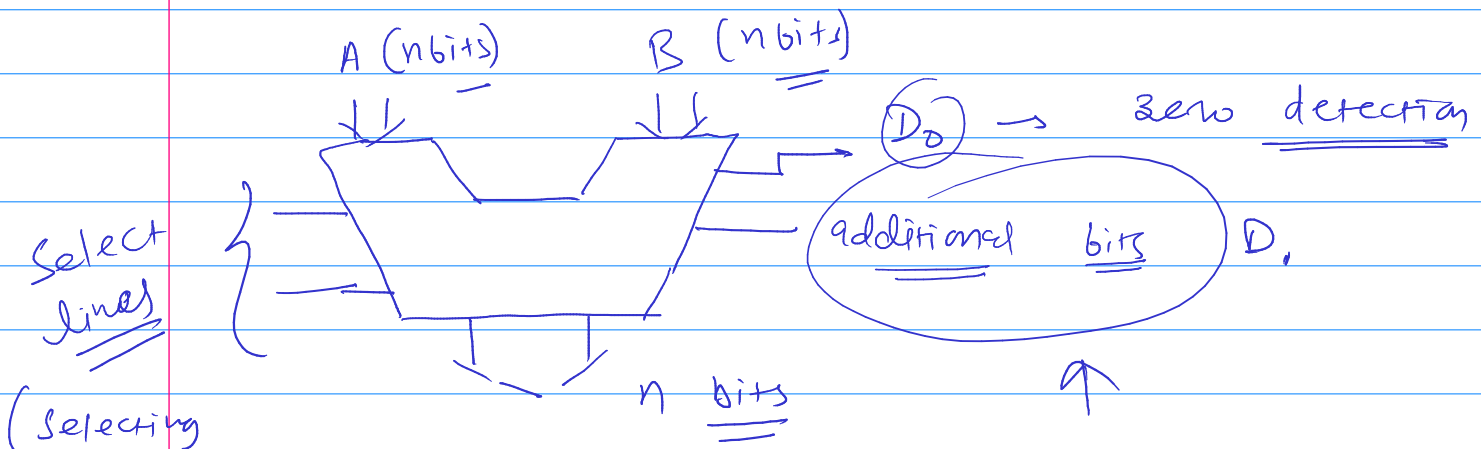
12 - 05 - 2022

Lecture # 17.

"ALU"

- # Addition → '+'
- # Subtraction → '-'
- # Multiplication → '*'
- # Shifting → >> <<
- # equal to or ! (equal to)
- # Mod.



110

111

State - S_0 → A + B

S_1 → A - B

S_2 → >> A

S_3 → << A

S_4 → >> B

S_5 → << B

S_6 = A && B (Bit wise operators)

S_7 = ! A

S_8 = ! B

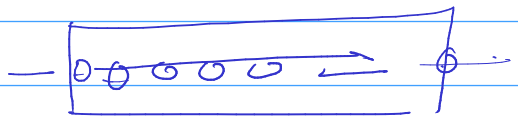
S_9 = A || B

#

50 Mhz

20 loop hz

50



50 Mhz

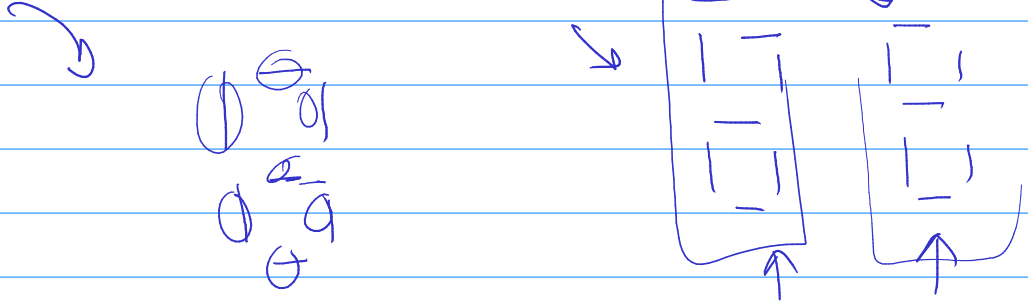
1 Hz

50×10^6

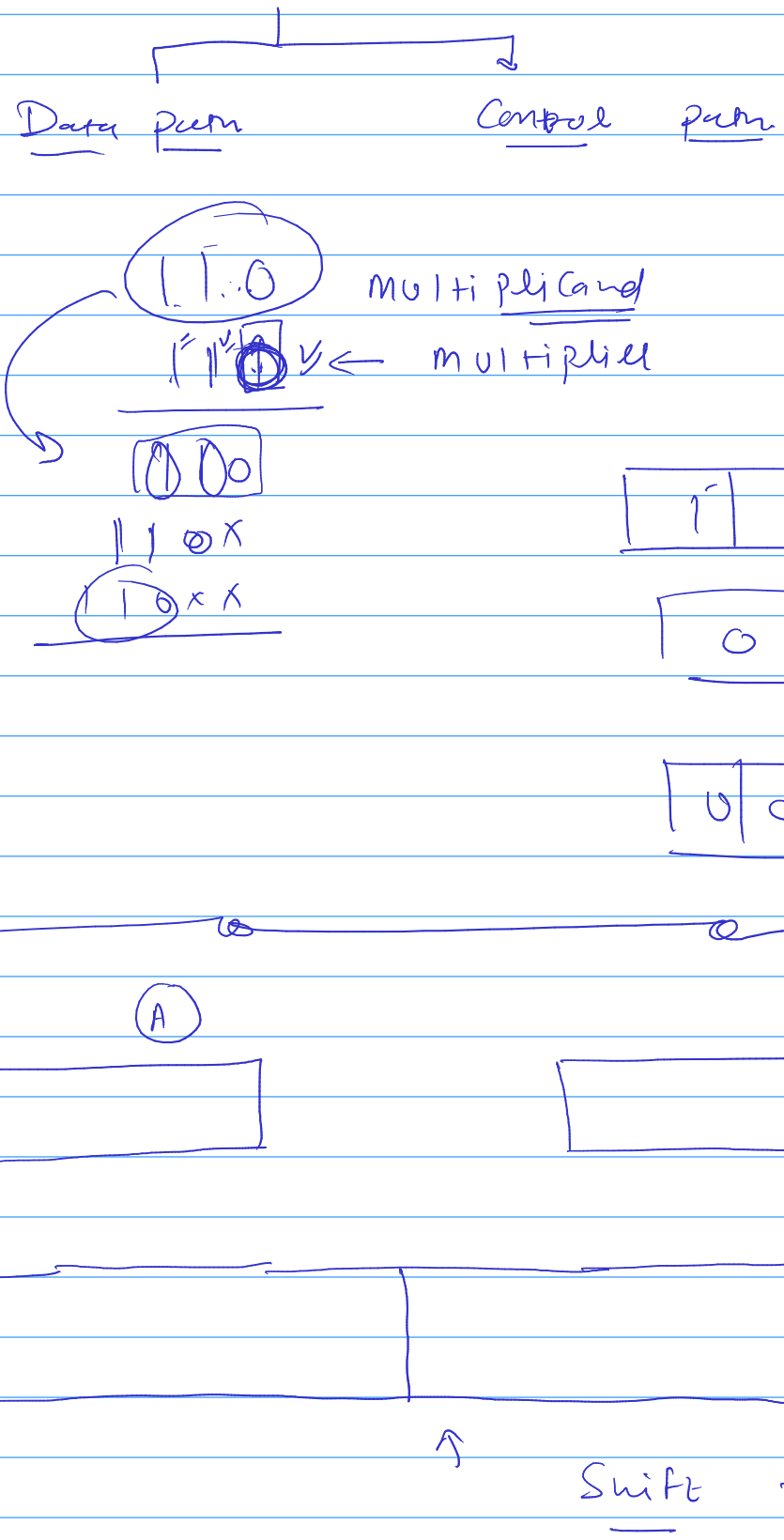
@ (Posedge clk)

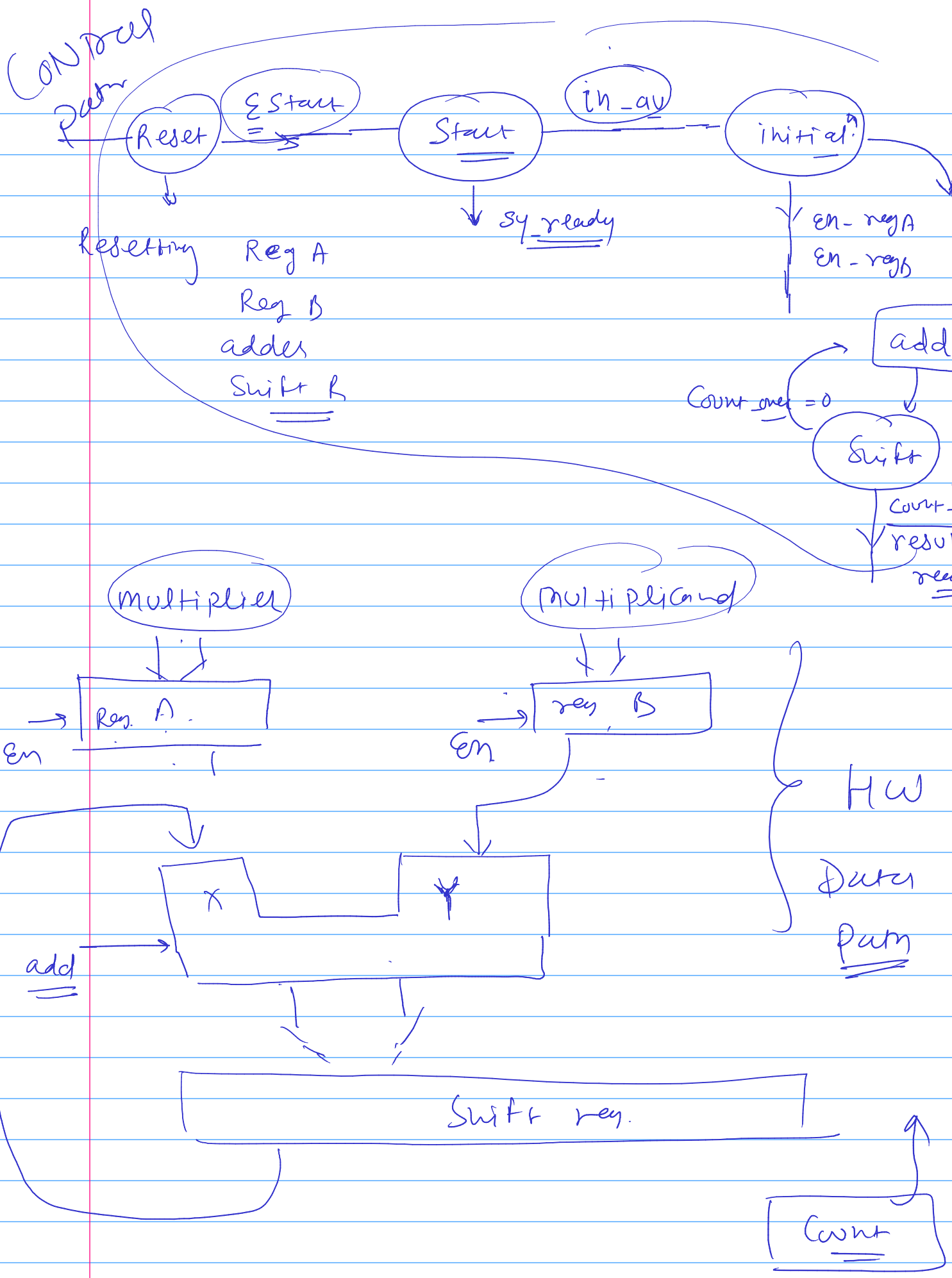
```
{ if (i < 100)
  i = i+1;

Else
  i = 0
  Count = ! Count.
```



System Design




Control Path
Reset
Estart
Start
in_av
initial
sy_ready
Resetting
Reg A
Reg B
adder
Shift R
en_regA
en_regB
add.
Count_one = 0
Shift
Count_one = 1
result_ready
Multiplier
Multiplicand
Reg A
reg B
en
en
HW
Data
Path
X
Y
add
Shift reg.
Count