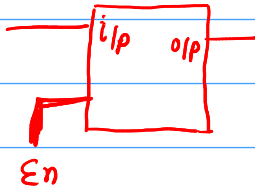


Lecture # 9

→

LATCH

(1) →



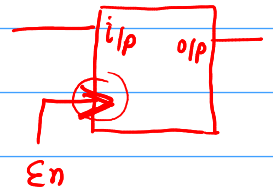
(2) :-

Level triggered.

(3) :-

Less no gates are required.

Flip-Flop



Edge triggered.

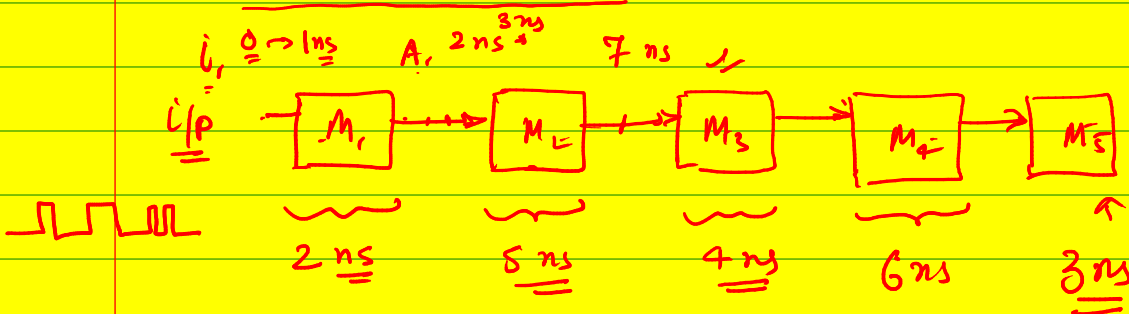
→ Comprises of
2 LATCHES.

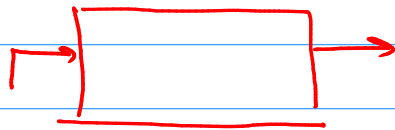
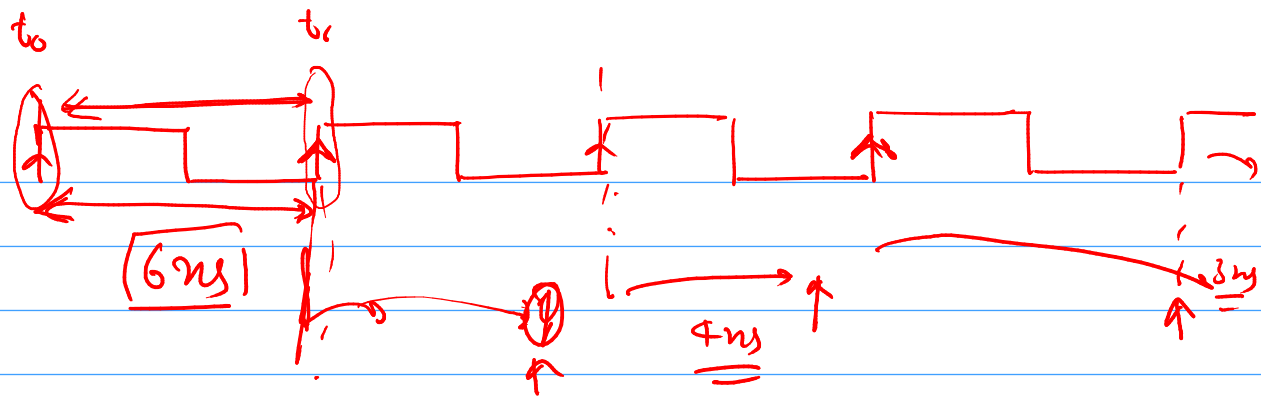
MASTER-SLAVE ARCH.

(4) →

$$\frac{dv}{dt} = \frac{I}{C}$$

→

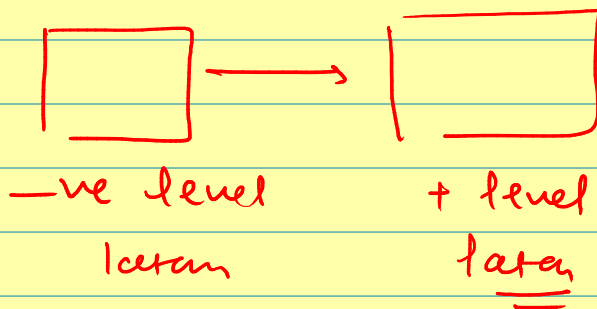
"SYNCHRONIZATION"



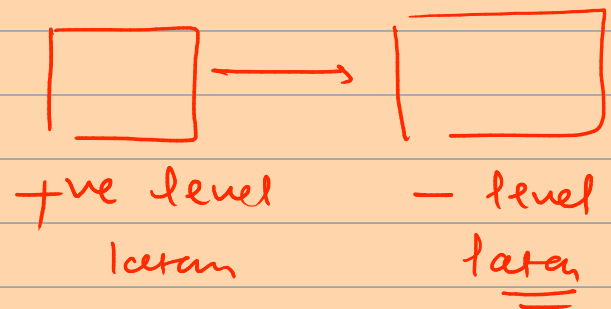
$$\boxed{3 \text{ GHz}} =$$

$$\frac{1}{3 \text{ GHz}} \rightarrow \frac{5 \text{ GHz}}{10 \text{ GHz}}$$

(-ve) edge triggered.



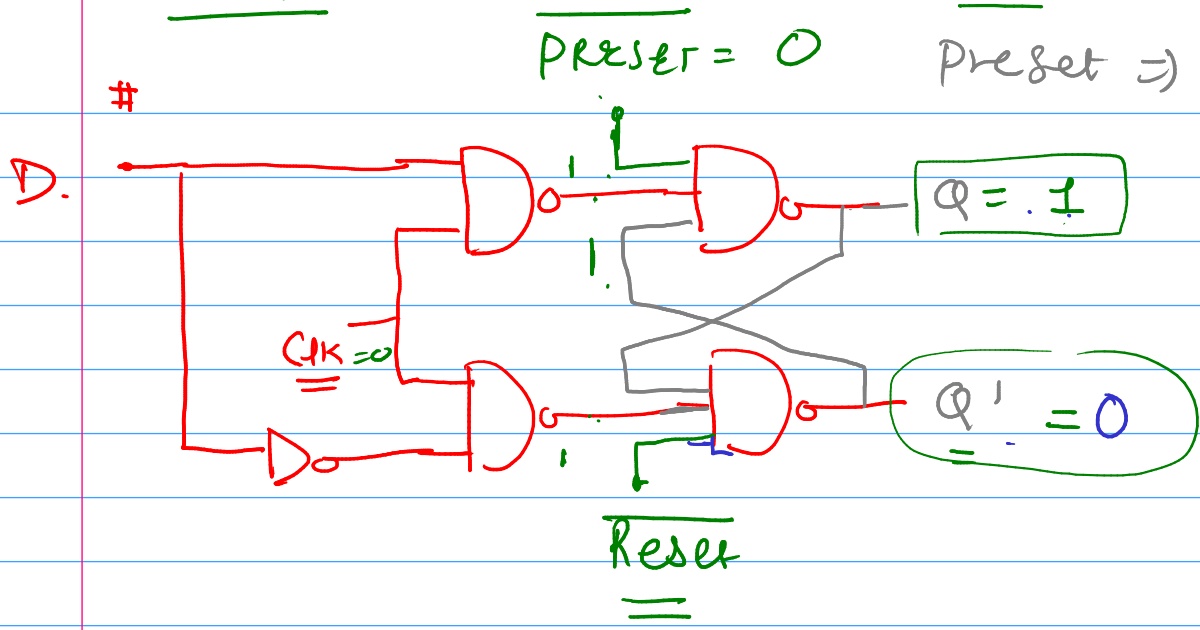
(+ve) edge triggered.



LATCH

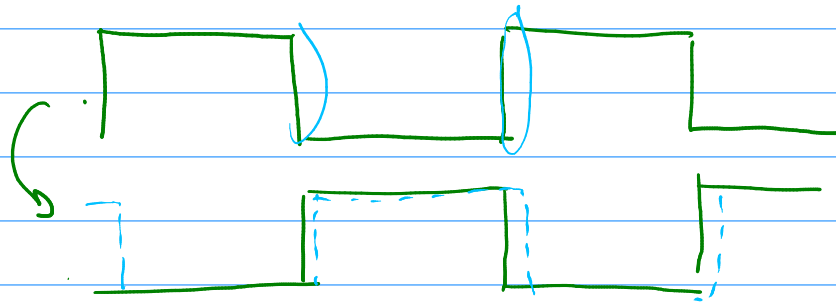
Reset \Rightarrow $Q = 0$

Preset \Rightarrow $Q = 1$



$$\text{RESET} = \overline{\text{PRESET}}$$

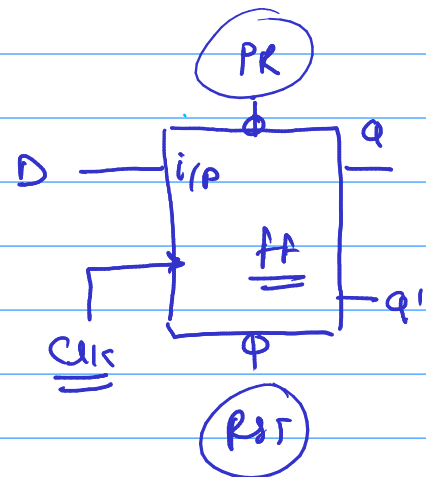
$$\text{RESET} = ! \text{PRESET}$$

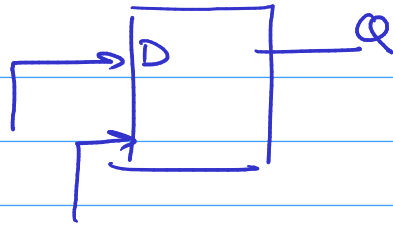


Always (a) (Pos edge clk)

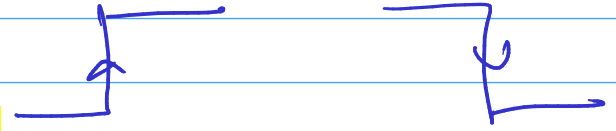
if ($\text{PR} == 0$; $\text{PR} == 1$) then
 $Q = 0$;

$Q = D$;





$D = 0$	$D = 1$
$Q = 0$	$Q = 1$



→ $RST = \text{not } PR;$

WON'T WORK

Always @ (Pos edge clk)

if ($RST == 0$)
 $Q = 0$; $Q' = 1$;
 else if ($RST == 1$)

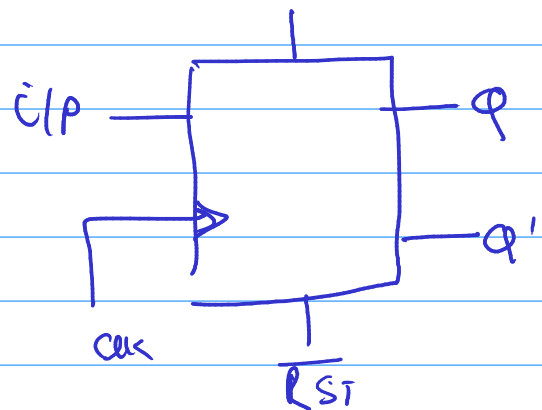
$Q = 1$; $Q' = 0$;

else

$Q = D$;

RST	PR
0	0
0	1 → Presu
1	0 → Pre Set
1	1

$\overline{PR} =$



$$PR = \overline{RST}$$

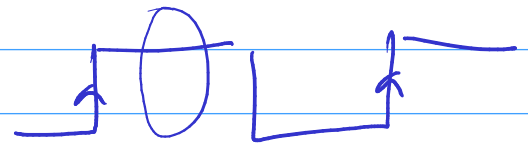
Always @ (Pos edge clk, RST, PR)

```

if (RST == 1; PR == 0) then
    Q = 0; Q' = 1;
else if (RST == 0, PR == 1) then
    Q = 1; Q' = 0;
else if (RST = 1, PR = 1) then
    Q = D;
End if;

```

PR	<u>RST</u>	clk	Q
0	1	X	0
1	0	X	1
1	1	↓	D



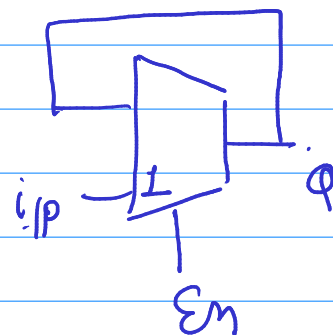
$$Q = \text{En} \cdot i$$

```

if (En = 1) then
    Q = i;
End if;

```

iP — Q



$$\text{En} = 1$$

$$Q = iP$$

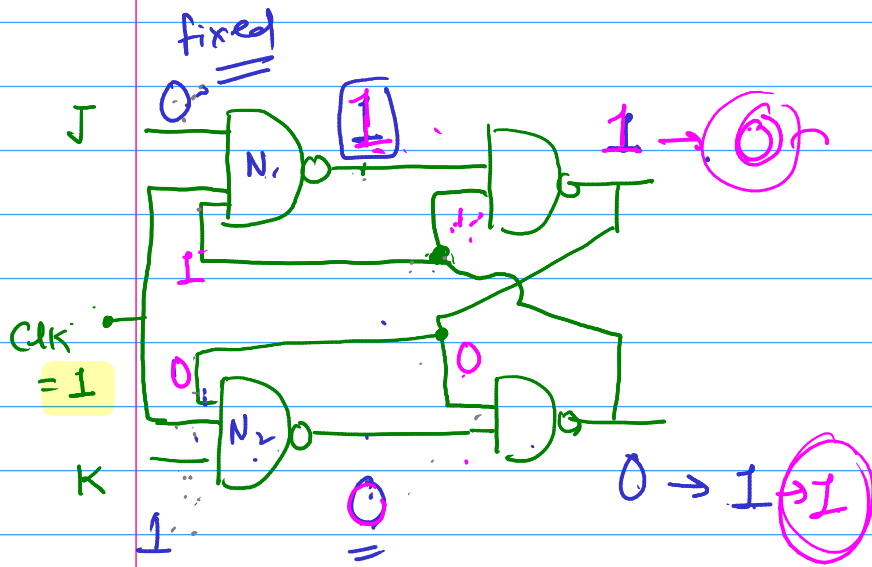
Else

$$Q = Q;$$

J-K LATCH

T-LATCH

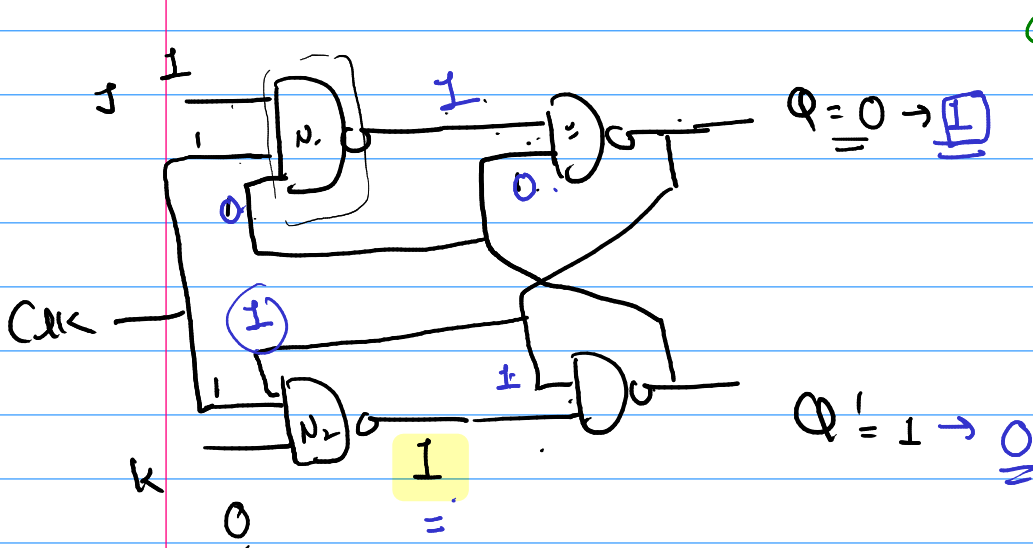
#



CLK	J	K	Q_n	Q_{n+1}
0	X	X	Q_n	Q_n

(No change)

1	0	1	0	→ 0
1	0	1	1	→ 0



CLK	J	K	Q_n	Q_{n+1}
1	1	0	0	→ 1
1	1	0	1	→ 1

J = 1 , K = 1

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