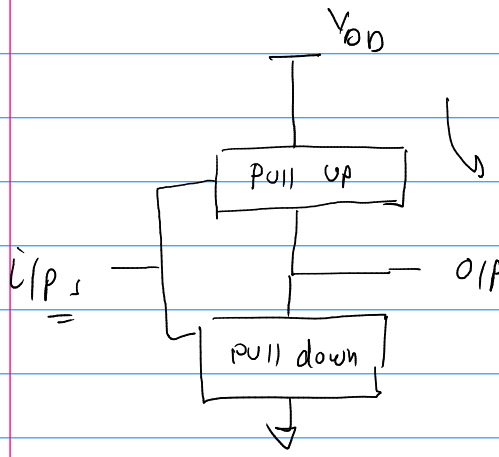
11- MAY - 2022.

# Lecture # 16

## Switch level logic Design.

Pmos → Good conductor for passing logic '1' or $V_{DD}$

Nmos → Good conductor for passing logic '0' or ground




When pull-up is "ON" ⇒ o/p = '1'

When pull-down is ON ⇒ o/p = '0'

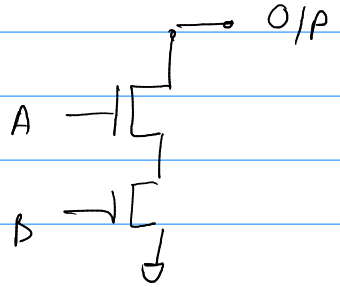
At a time Either pull-up is "ON" or pull-down is ON

---

Pmos → ON when i/p = '0'

Nmos → ON when i/p = '1'

---



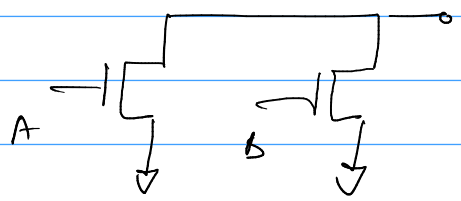

When N mos transistors (switches) are in series →

⇒ o/p is going to connect with ground terminal only & only when both

A = B = '1'

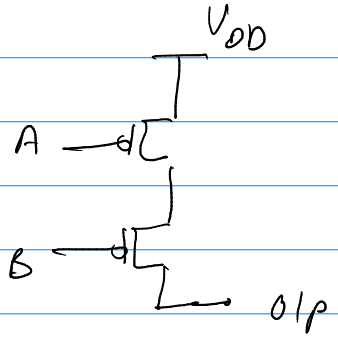
⇒

⇒ ! (AND)



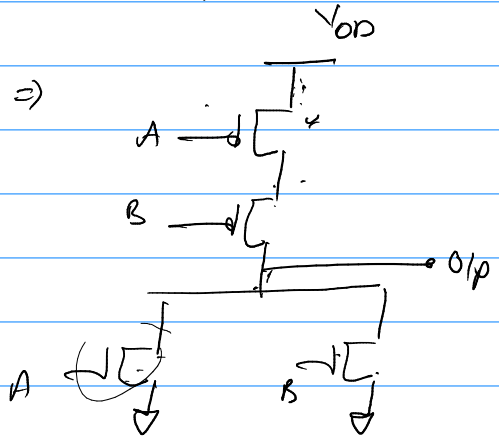

Either 'A' or 'B' is '1' then O/p = '0'

$\Rightarrow$ !(OR)



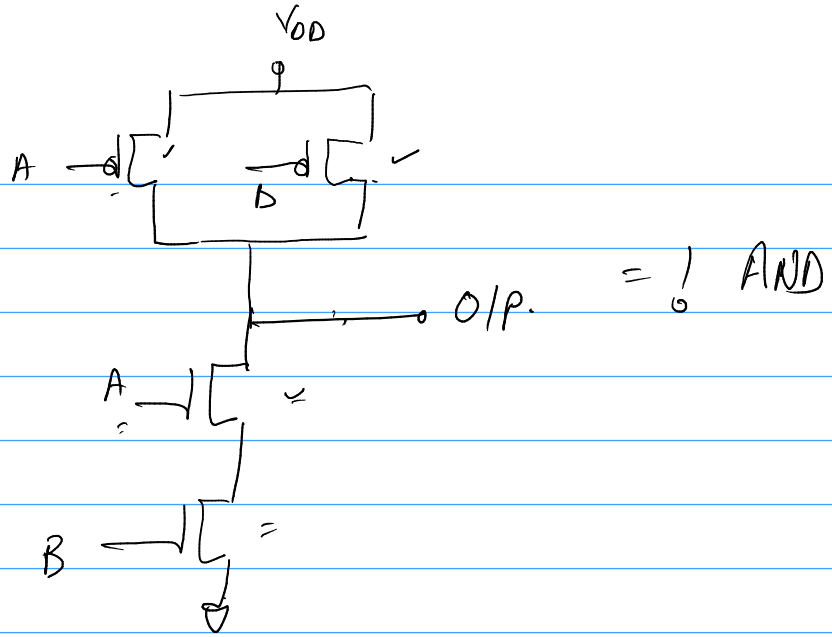

When Both 'A' & 'B' are '0' → then only O/p = '1'

$\Rightarrow$




NOR GATE

| A | B | | O/p |
|---|---|---|---|
| 0 | 0 | → | 1 |
| 0 | 1 | → | 0 |
| 1 | 0 | → | 0 |
| 1 | 1 | → | 0 |




$= 1$ AND

---

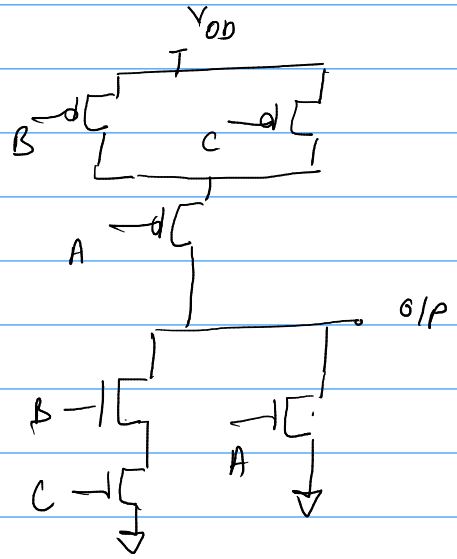
# $Y = (A + B C)'$

for O/P = 0

① ⇒ When Both B & C are '1'.

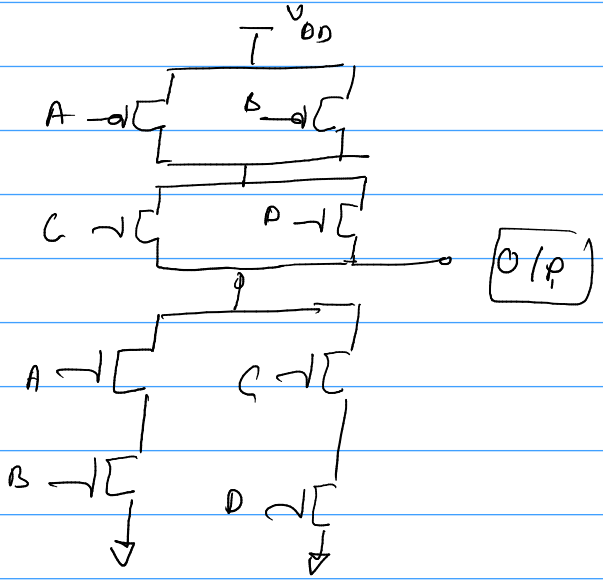
OR

② ⇒ A = 1




---

$Y = [AB + CD]'$




$Y = A + B'C'$

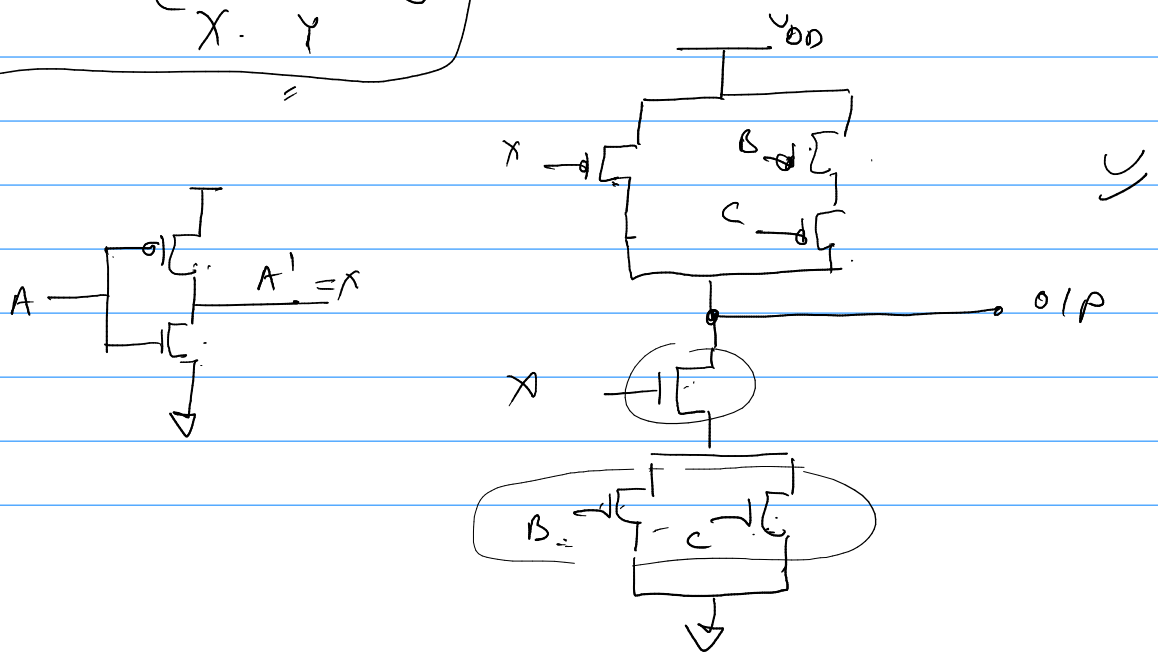
$Y' = [A + B'C']' = A' \cdot (B + C)$

$Y = [A' \cdot (B+C)]'$

$Y = [X \cdot (B+C)]'$

$X \cdot Y$

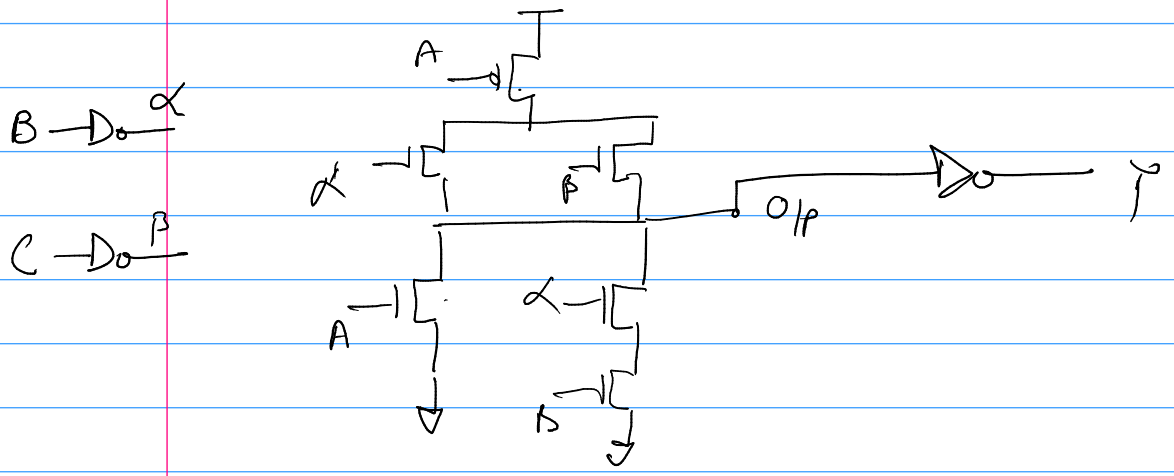
$A' = X$



$Y = A + B'C'$

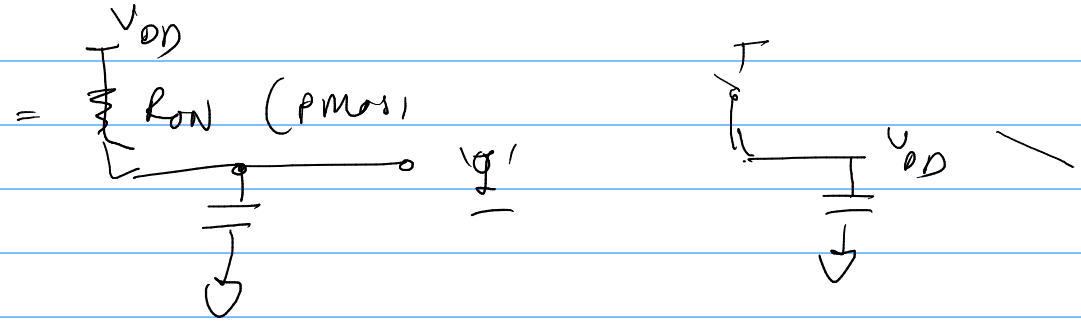
$Y' = [A + B'C']'$ $\qquad B' = \alpha$

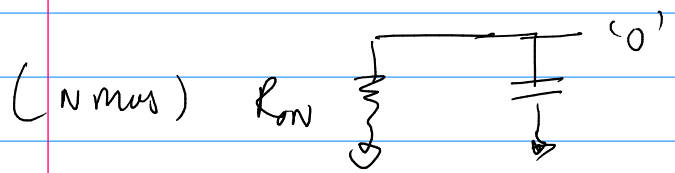
$Y' = [A + \alpha \cdot \beta]'$ $\qquad C' = \beta$




---

# STATIC CMOS Implementation of Logic expressions.



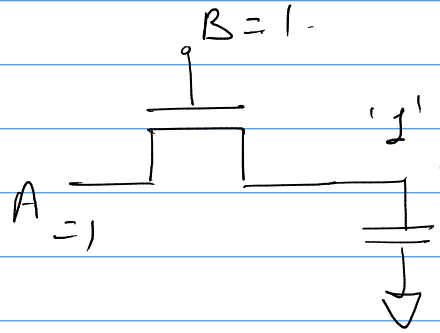




---

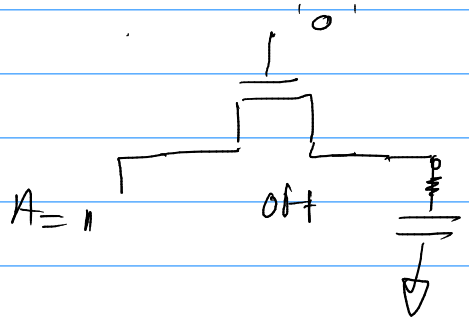
# $Y = (A + BC)'$

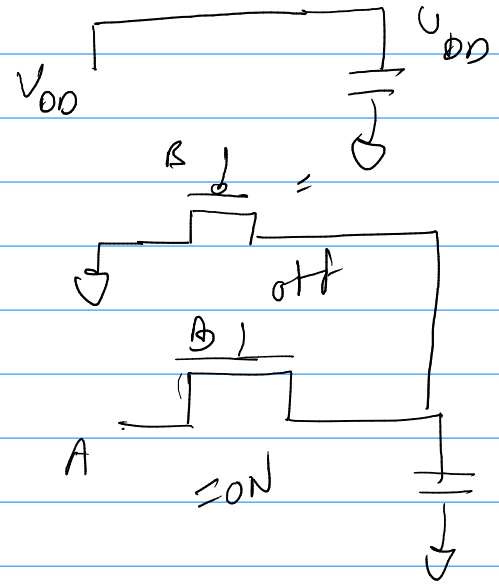
Min. = 2.N

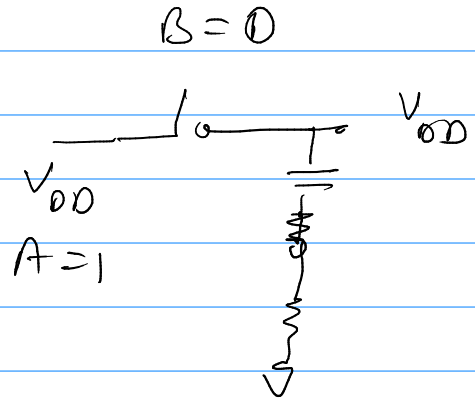
$= (A' + B'C')$




| A | B | O/P. |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |



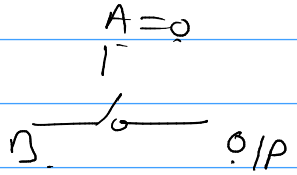

AND 2 transistors

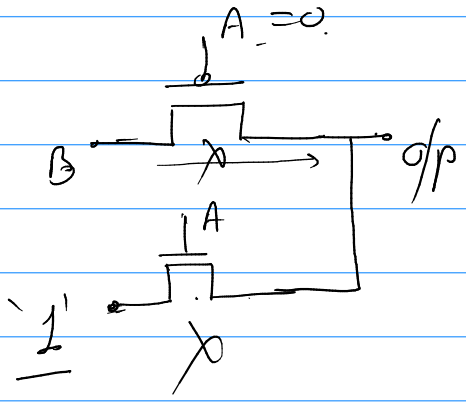
$A + B$

$A + A'B$

$A'B$

When $A = 0$ $\quad$ **O/P = B**




$A'B + A$

$B \quad +0$

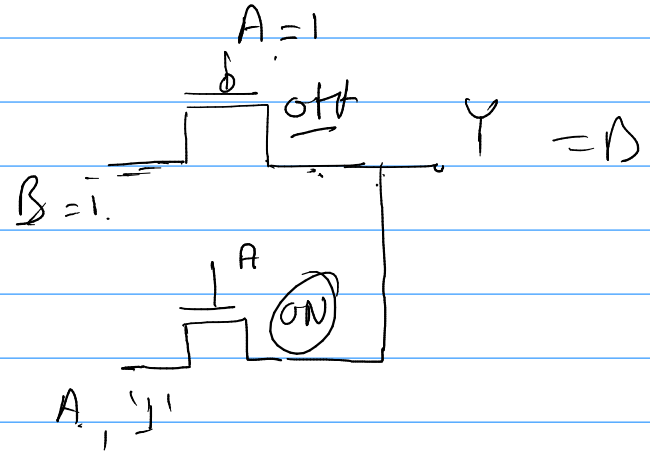
$A = 1$

$A + B \Rightarrow \rightarrow A'B + A = Y$

$1+0=1$

$1+1=1$

$A'B = 2$



$A'B + B'A = XOR$