06/04/2022

Lecture # 4

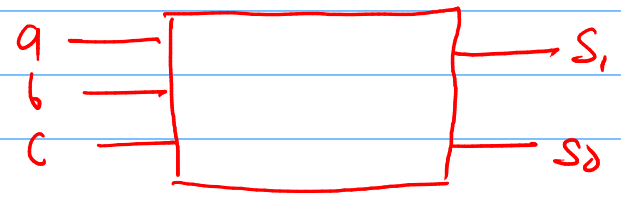
\#

		1	1			
a	1	1	1	1	a_3	a_2 a_1 a_0
b	1	0	1	1	b_3	b_2 b_1 b_0
				0		

a a[3] a[2] a[1] a[0]
   b[3] b[2] b[1] b[0]

.

a	b	c	S_1	S_0
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



$a \oplus b \oplus c$

a	b	c	S_0	
0	0	0	0	
✓ 0	0	1	1	m_1
✓ 0	1	0	1	m_2
0	1	1	0	
✓ 1	0	0	1	m_3
1	0	1	0	
1	1	0	0	
✓ 1	1	1	1	m_4

$S_0 =$

$m_1 + m_2 + m_3 + m_4$

$a'b'c + a'bc' + ab'c' + abc = S_0$

1 1 0 1

0 0 1

a	b	c	S_1	
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	1	m_1
1	0	0	0	
1	0	1	1	m_2
1	1	0	1	m_3
1	1	1	1	m_4

$a'bc + ab'c + abc' + abc = S_1$

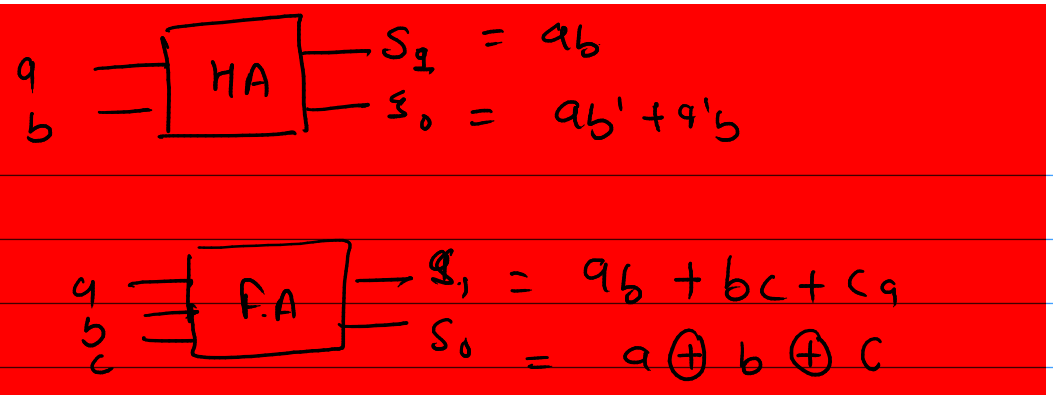
$bc(a' + a) + ab'c + abc'$

$bc + ab'c + abc'$

$= c[b + ab'] + abc'$ ($a + b$)

$= cb + ca + abc' = cb + a[c + bc]$

$= \boxed{cb + ac + ab}$



A $q_3\ q_2\ q_1\ q_0$

B $b_3\ b_2\ b_1\ b_0$ =

$q \oplus b$ — 0

$a \ominus b$ — 1

= 1 0 1 1 =

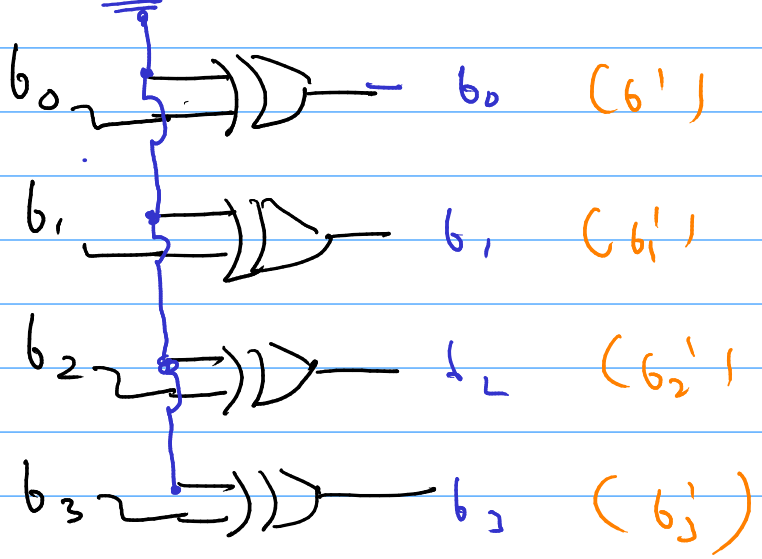
0 1 0 0 = is

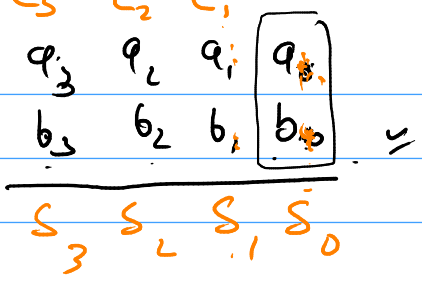
X Y Z

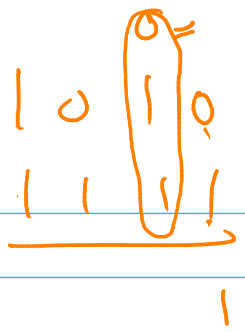
if $Y = 0 \Rightarrow Z = X$. $Z = XY' + YX'$

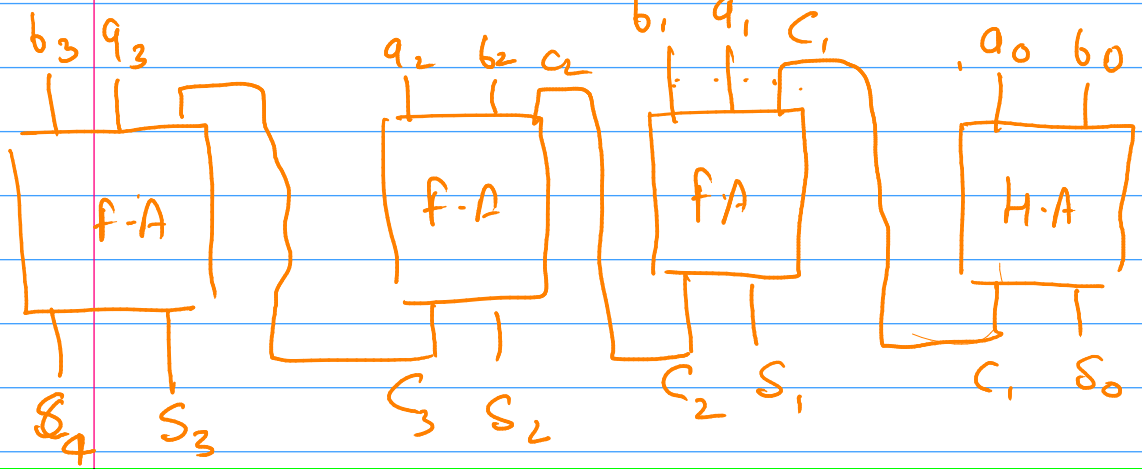
$Y = 1 \Rightarrow Z = X'$

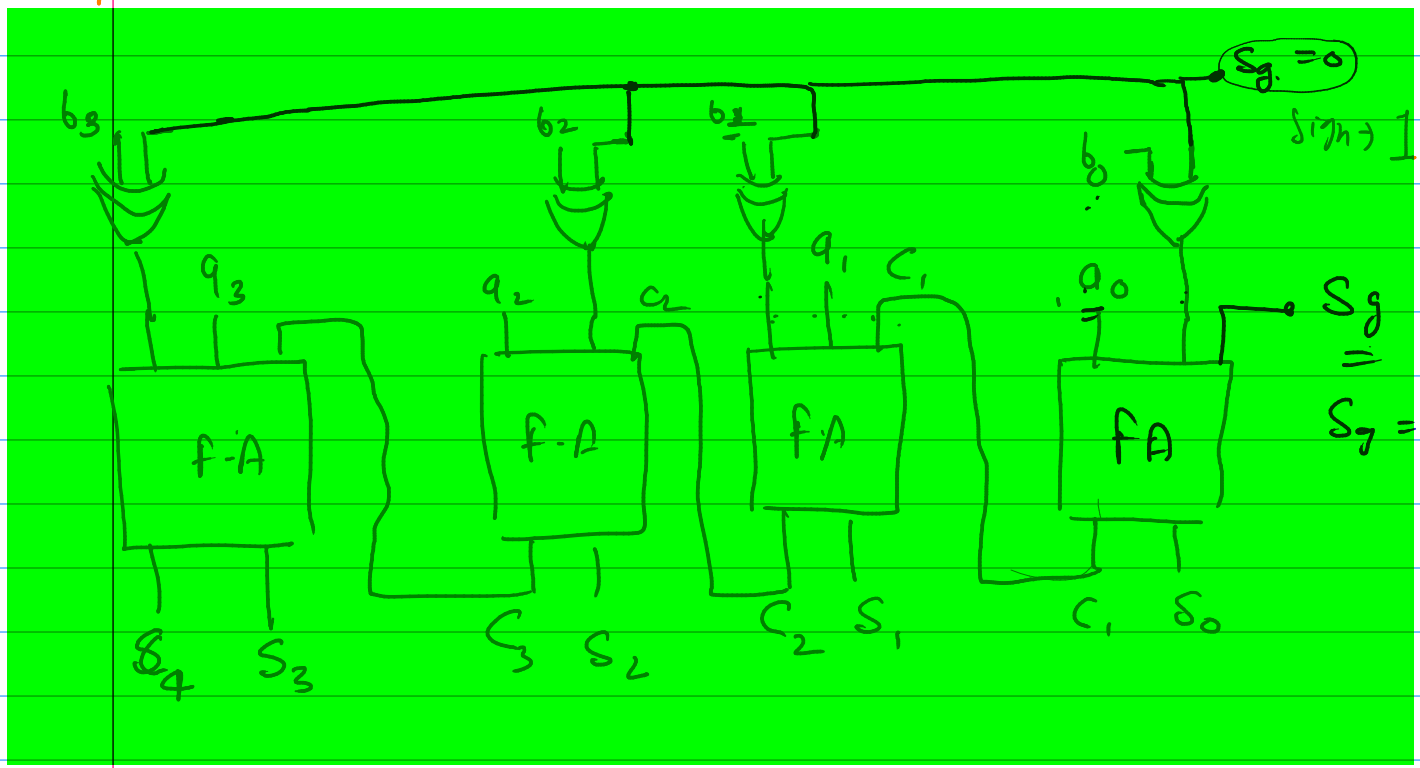
Sign (6) = 1 →











$q_3 \quad q_2 \quad q_1 \quad q_0$

$b_3' \quad b_2' \quad b_1' \quad b_0'$ → 2's.

$+ \ 1$

2^n

$n \Rightarrow$ _ _ _ _ _

n bits

[q]

$\Rightarrow$ q, a', 1, 0] 4

a b

1.	a	a'	ab'	a'b'	a + b	a + b'
0.	b	b'	a'b	ab	a' + b	a' + b'

$a \oplus b$, $a \odot b$

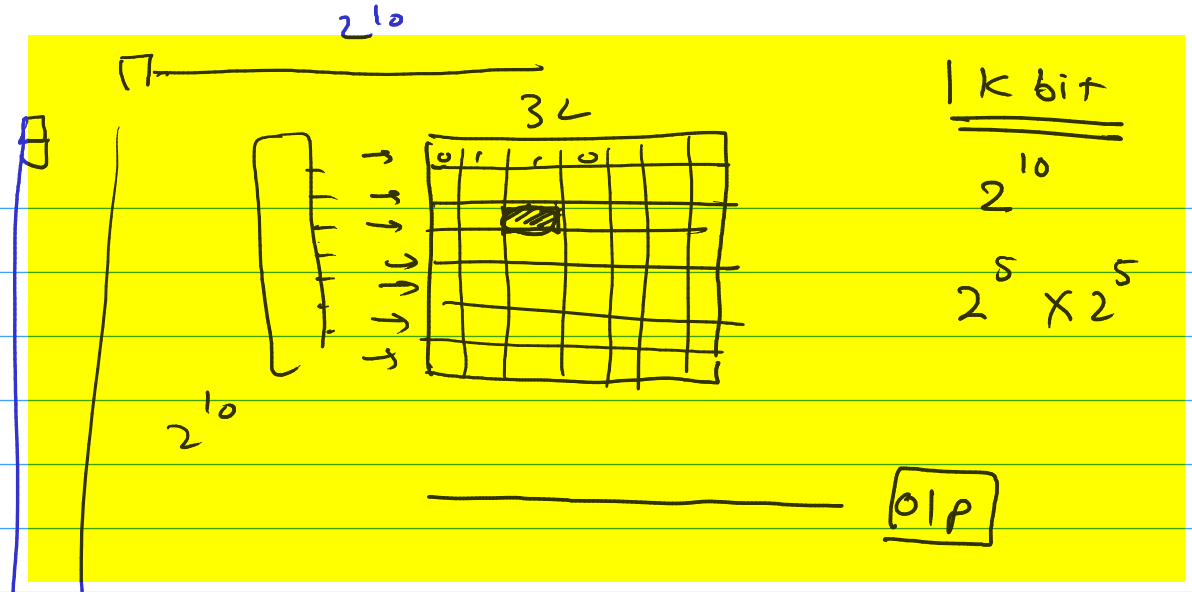
→

a b

=	0 0	=
	0 1	≥
	1 0	=
	1 1	=

2^n

2



#

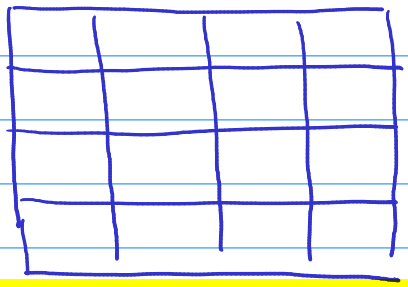
q_4
q_3
q_2
q_1
q_0

$\equiv$ 00 000 = 32
00 001 =
00 010 =

$q_1\ q_0$

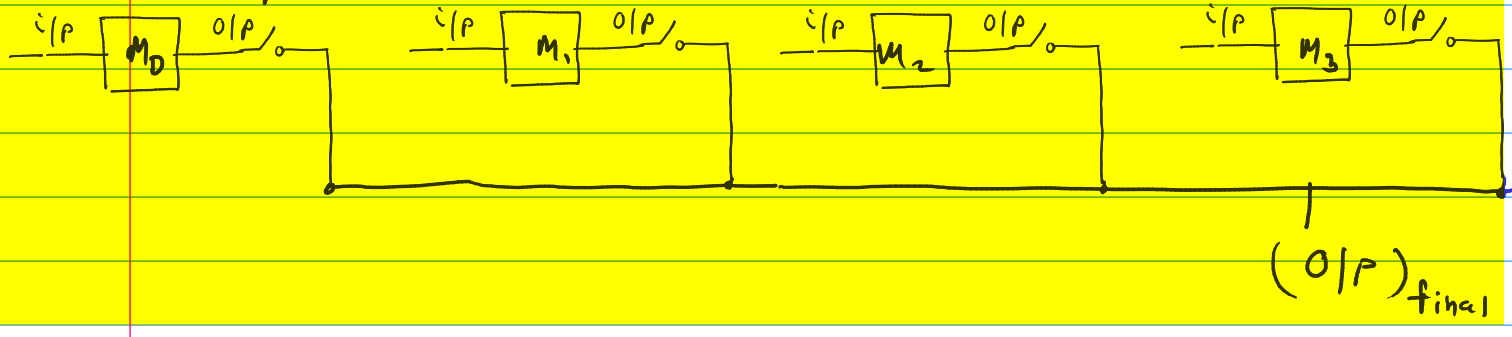
$q_1 q_0$ = = 1 $\Rightarrow$ $q_1' q_0' = 1$

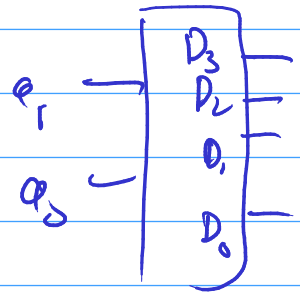
0 1
1 0
1 1



$= D_0$ $= D_1$ $= D_2$ $= D_3$

$q_1' q_0' =$ $q_1' q_0 =$ $q_1 q_0' =$ $q_1 q_0 =$



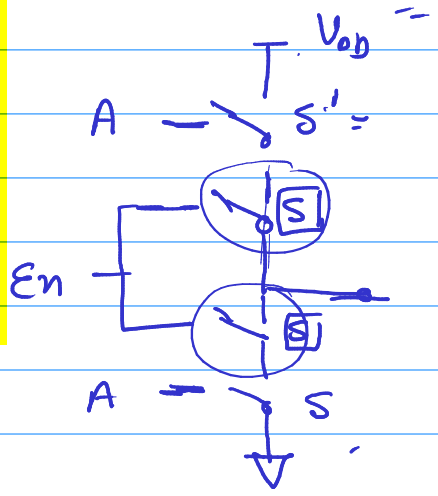


q_1	q_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

$D_0 = q_1' q_0'$ $\qquad$ $q_1' q_0 = D_1$

Tri State Buffer / inverter

A	En	O/P
A	1	A'
X	0	Z

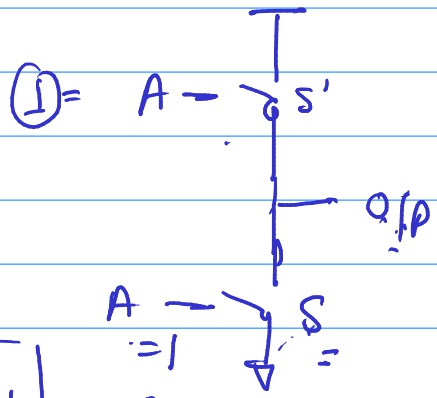


Control

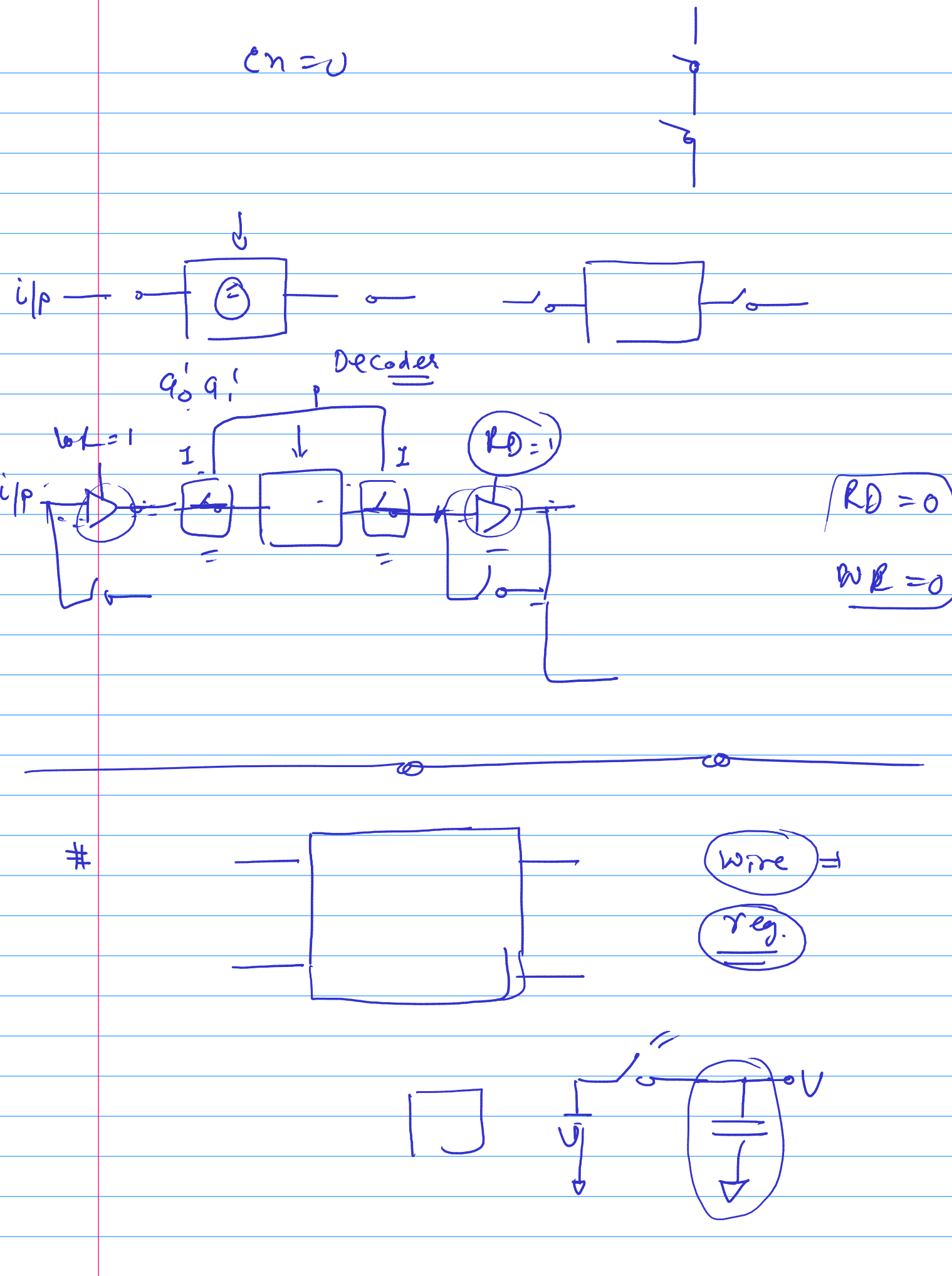
S ⇒ i/p = 1 : ON $\qquad$ i/p = 0 : OFF

Control

S' i/p = 0 : ON $\qquad$ i/p = 1 : OFF



En = 1 , O/P = A'


Cn = 0
i/p
Decoder
$q_0' q_1'$
WL = 1
1
1
RD = 1
i/p
RD = 0
WR = 0
#
wire
reg.
V
V

Module (a , b)

wire a

assign a = ~b } alw.

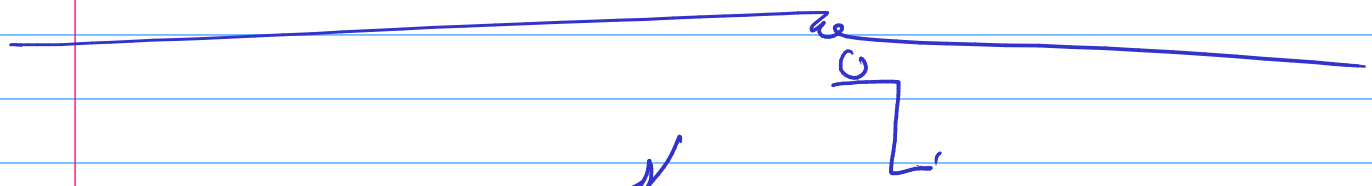
in a , c -

#50ns a = b and c ;

1- - - - - -

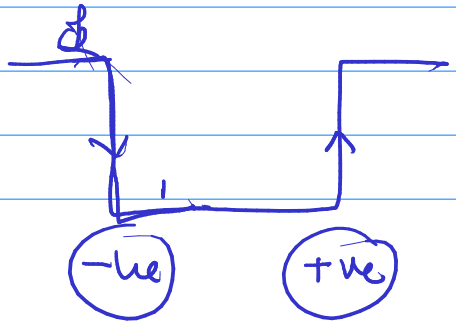
0= 50ns a

alw



always @(b -a)

a = b or c ;



End

always @(posedge clk)

q = b or c