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Active Silicon Chiplet-Based Interposer for Exascale High Performance Computing

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ABSTRACT

With the era of massive multi-core architecture targeting cloud computing for exascale high performance computing (HPC) and big data applications, large scale multi-core are made possible thanks to advanced 3D integration technologies. This paper presents an innovative concept of active silicon interposer with stacked chiplets, with the objective of maintaining overall power consumption budget, increasing chip to chip bandwidth, and preserving full system cost by smart system partitioning.

HIGH PERFORMANCE COMPUTING CHALLENGES

Endless requirements of higher performances, given by Flops/s, while maintaining reasonable power efficiency (pJ/bit), lead to profound technology revolution in high performance computing (HPC) applications (Fig.1) [1]. The progress of computer technology was traditionally fueled by the Moore's law : the running frequency were doubling every technology node while reducing the voltage, therefore maintaining a nearly constant energy density. Then, with more advanced technology nodes, the energy density increased dramatically with the number of devices, both due to leakage and active power. One of the most critical constraint comes from the increase of energy per unit of surface. Also, data traffic is growing drastically, due to the amount of information required to get accurate application but also to the huge number of connected things or people producing and exploiting data. This represents another source of energy wasting for moving data from the production to the storage and then to the processing. The so-called memory wall is reached. Finally, cost of designing and manufacturing the complex and large compute die is critical.

Mono-core then multi-core devices, improved thanks to specialization architecture, were successfully and sequentially introduced in super computers. But data deluge (and associated memory requirement) and cost constraints forced system architects to introduce innovation outside the classical Moore's law box. Heterogeneous integration, symbolized by the chiplet, era is initiated.

CHIPLET AND ACTIVE SILICON INTERPOSER MOTIVATION

The concept of chiplet, in opposition to silicon on chip (SoC) devices, is to partition a large and complex die into several smaller chiplets with rather simpler functions. Then, assembly technologies smartly recompose a functional system. Motivation for chiplet are cost, modularity and heterogeneity. One key interest is that the selection on CMOS technology is not anymore driven by the compute requirements, but each chiplet can use the most optimized technology depending on its specification. Consequently, a multi chiplets / foundries system can be considered.

Classical solutions used - organic interposer, advanced packaging and passive silicon interposer - still suffer from a lake of die-to-die high bandwidth interconnect (Fig.2). Compared to advanced packaging technologies, a silicon interposer provides finer pitches between chiplets leading to higher bandwidth. Also, memory such as high-bandwidth memory (HBM) can also be stacked on the same interposer, leading to close interaction compute to storage. This paper introduces the active silicon interposer which is a natural evolution of passive silicon interposer to overcome limitations regarding chiplet connectivity (scalability), and integrate scalable function (heterogeneity) (Fig.3). As far as technology is concerned, the active silicon interposer takes the full benefit of the passive interposer by using very similar technologies. In terms of architecture, contrarily to passive interposer with system level communication restricted to chip-to-chip side-by-side communication, active interposers offer the possibility of extended communication capability. In addition, active interposers may also integrate system IOs as a specialization of the interposer for system level communication, and primarily with the memory.

Active interposers may also advantageously integrate power management features. The objective is to deliver the power as close as possible to computing chiplets. This allows reducing voltage drops and converter reaction time, and increases energy efficiency.

INTACT, THE CEA PROOF-OF-CONCEPT

CEA unveiled an active silicon interposer proof-of-concept, so-called INTACT (Fig.4) [2-3-4]. Six identical chiplets using 28nm FDSOI technology are face-to-face stacked on a silicon interposer made of 65nm CMOS. The circuit offers a total of 96 cores with scalable cache coherent architecture. Each chiplet is 22mm², the interposer is 200mm². 25 000 copper pillar interconnects at a pitch of 20µm were used to connect the chiplets to the interposer (Fig.5). The interposer is thinned down 100µm for the fabrication of TSV-Middle of 10µm in diameter. 14 000 TSV and solder balls are used to connect the ball-grid array (BGA) to the front side of the interposer.

INTACT uses a flexible system communications fully distributed in the 6 chiplets and in the active interposer using Network-on-Chip (NoC) routers and different kinds of energy-efficient 3D-Plugs. Dense inter-layer communication is achieved. Also, switched capacitor voltage regulators (SCVR) for on-chip power management offer a wide voltage range (0.6 V – 1.2 V). The interposer embeds a memory-IO controller and PHY for socket communication.

Finally, this circuit delivers 220 GOPS peak. The hierarchical system interconnect provides 0.6 ns/mm inter-chiplet latency using asynchronous signaling, and a 0.59 pJ/bit synchronous 3D-Plug energy efficiency with 3 Tb/s/mm2 bandwidth density (Fig 6.).

TOWARDS EVEN MORE EFFICIENT

A 40 to 60µm pitch solder-based interconnect, so called copper pillar, is widely used for die to die interconnect. The usage of an active

silicon interposer could benefit of a finer pitch if available. CEA teams achieved a 20µm pitch with INTACT proof-of-concept, but shrinking again seems not economically viable: new material and processes would be required, and the underfill mandatory to fill the vertical gap between the dies has reached limits (whatever capillary or pre-applied underfill). Also, chiplet to chiplet x and y gaps need to be as small as possible to reduce the interposer size. Finally, the reliability of solder based interconnect have always been a critical challenge, exacerbated when shrinking. Combining knowledge of die sawing, cleaning, and flip-chip with the wafer-to-wafer direct hybrid bonding expertise allows CEA-Leti to develop a 10µm pitch underfill-less die to die interconnect (Fig. 7), with a short-term objective to reach 5µm pitch [5-6]. High reliability has been proven. Removing the underfill between chiplet and the interposer also offers better thermal and mechanical management. Finally, the pertinence of this new technology is definitively proven thanks to various pre-bonding test processes, allowing a known-good-die strategy for both the interposer and the chiplets.

SUMMARY AND CONCLUSIONS

It is widely admitted that heterogeneous integration using various chiplets is mandatory to reach exascale HPC. Among plethora of technological solutions, the CEA active silicon interposer INTACT offers higher bandwidth at a better energy efficiency. Inter-dies and intra-dies interconnects are proven and mature. With on going promising die-to-die interconnect such as direct hybrid bonding, the chiplet-based active silicon interposer is definitively a key technology for future high efficiency systems for high performance computing.

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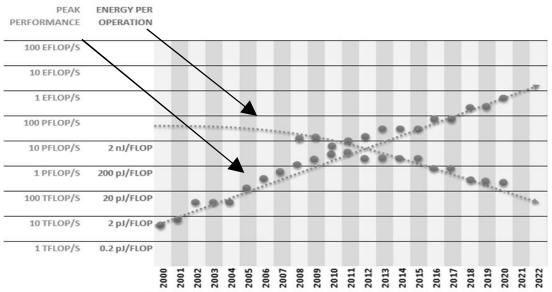

FIGURE 1. Evolution of the computing performance (x10 every 4 years) and energy per operation (:4 every 2 years) of the 500 most powerful computers in the world (www.top500.org)

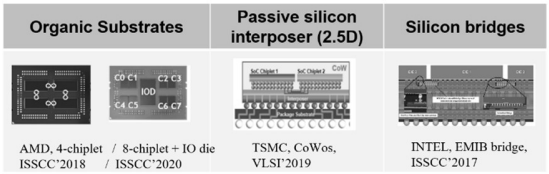

FIGURE 2. Some of the existing heterogeneous technologies using chiplets.

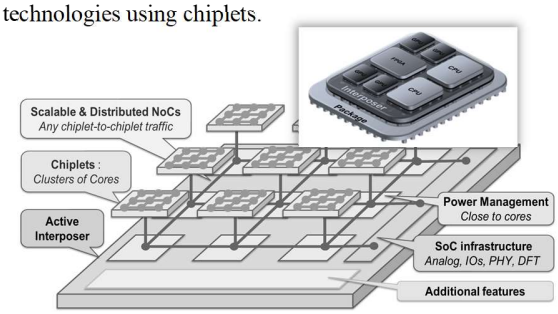

FIGURE 3. Concept of chiplet-based active silicon interposer. The interposer embeds i. Distributed & flexible interconnects; ii. Integrated Voltage Regulators; iii. Memory Controller & System IO's and iv. SOC Infrastructure, DFT

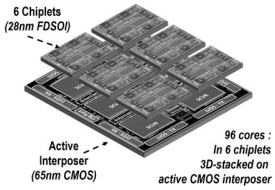

FIGURE 4. INTACT active silicon interposer.

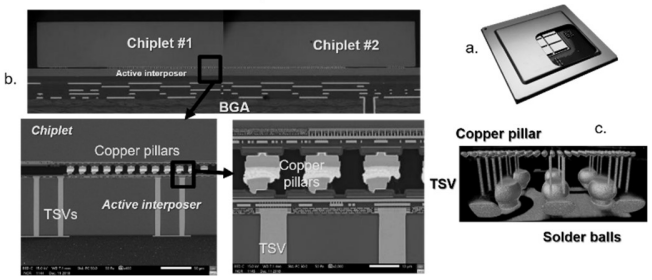

FIGURE 5. INTACT proof-of-concept : a. A prototype with opened lid to observe the structure b. Cross section after assembly c. X-ray tomography of the interposer with visible TSV, copper pillars and solder balls.

FIGURE 6. Main characteristics of INTACT proof-of-concept.

Technology	INTACT
Interposer	65nm CMOS
Chiplet	28nm FDSOI
Inter-die interconnect	Copper pillar pitch 20µm
Intra-die interconnect	TSV-Middle pitch 40µm
Voltage swing	1,2V
Data rate	1,21Gb/s/pin
Power efficiency	0,59pJ/bit
Bandwdith density	3.0Tb/s/mm²

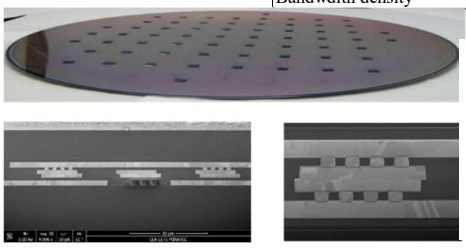

FIGURE 7. Die-to-Interposer interconnect using direct hybrid bonding. A 10µm pitch has been achieved.