(1) For both caches, the instruction cache miss rate is 0.5% and penalty is 50 cycles. For the data cache, miss rate is 2%. but the penalties are different. In a write

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(1)

Instruction miss penalty = 50
Data read = 1 clock
Data write = 2 clock
Data miss = 100 (write through
Data miss = 100 or 200 (write Back)
miss rate for instruction 0.5%
miss rate for data = 2%
Dirty blocks = 30%
25% loads
10% store.

CPI execution = $0.25 * 1 + 0.10 * 2$
$0.65 * 1$

$= 0.25 + 0.2 + 0.65 = 1$

→ write through =
$0.005 * 50 + 0.02 * (0.25 * 50$
$+ 0.10 * 50)$
$= 0.6$
CPI = $1.1 + 0.6 = 1.7$

Write Back

$= 0.005 * 50 +$
$0.02 * (0.25 * (0.5 * 100 + 0.5 * 200) +$
$0.10 (0.5 * 100 + 0.5 * 200))$

$= 0.005 * 50 +$
$0.02 * (0.25 (150) + 0.10 (150)$
$= 0.005 * 50 +$
$* 0.02 (0.35 (150))$
$= 0.25 + 1.05$
$= 1.30$

$CPI = 1.1 + 1.30 = 2.60$

. With write-through the CPI is lower by about 35%

(8)

Main memory = 2^{24} words

Block = 128

cache block size = 64 words

(a) Blocks = $2^{24} / 2^{6} = 2^{18}$

(b) tag = 18 bits

word = 6 bits.

(6) 2 of 5 instruction is data read
1 in 5 instruction is a data write
for cpi of 2, 0.5 instruction accers
per cycle.
20% are data read
10% are data right.

The instruction band with is thus
(0.0050 miss / instruction) *
64 (bytes / miss)) * 0.5 (instruction/cycle
= 0.16 bytes / cycle.

The data read bandwidth =
0.02 (miss/accers) · (0.2 reads/
cycles)
+ 0.1 write cycl * 64 (bytes / miss)

= 0.384 byels / cycle

Total read band with = 0.16 + 0.384
= 0.544
bytes / cycle

Totall write band with = 0.1 * 4 bytes
= 0.4

5

No. of bits used for Block offset.

$= \log 8000 = 8.98 \approx 9$

No. of sets in the cache.

$= \frac{2000K}{8K \times 4} = 62.5$

4

miss rate :- 0.1

Block size = 4 words = 16 bytes

Frequency = 10^9

write fr = 0.25×10^9

40% blocks modify

Fraction of read hits = 0.75 + 0.90

= 0.675

read miss = $0.75 \times 0.10 = 0.075$

write hits = $0.25 \times 0.90 = 0.225$

write miss = $0.25 \times 0.10 = 0.025$

Write through cache:

$0.675 * 0 +$
$0.075 * 2 +$
$0.225 * 1 +$
$0.025 * 3$
$= 0.45$

total Band width used $= 0.45 \times 10^9$

∴ fraction of Bandwidth use
$= \frac{\text{total used}}{\text{available}} = \frac{0.45 \times 10^9}{10^9} = 0.45$

Write Back cache:

$0.675 * 0 +$
$0.075 * (0.6 * 2 + 0.4 * 4) +$
$0.225 * (0) +$
$0.025 * (0.6 * 2 + 0.4 * 4)$
$= 0.21 + 0.07$
$= 0.28$

∴ Total Band width use $= 0.28 \times 10^9$

Fraction $= \frac{0.28 \times 10^9}{10^9} = 0.28$

5

5.1

If the cache is 4-way set associative, then the number of sets is not 4. Rather, the number of sets is the number of rows in the cache divided by 4. Since this cache has 256 rows (2MB/8kB), there are 64 sets. The answer is the $\log_2(64) = 6$ index bits

5.2

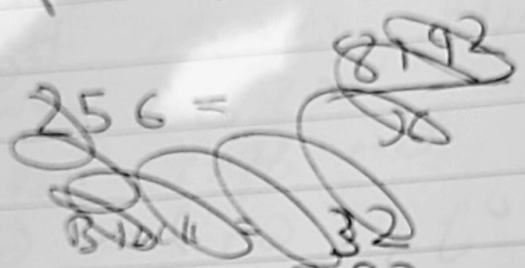
observe:- 8KB block → 2^{13} bytes
addressable → $\log_2(2^{13}) = 13$ bits if byte aligned. Assuming that the blocks are word-aligned, then we have offset bits = 13 − 2 = 11 bits

5.3

26 − 6 − 11 = 9 bits.

(2) Block size = 8 bytes
sets = 256

(a) capacity = 8192 Bytes



rows = $\frac{8192}{8}$

rows = 1024

256 sets -

Associativity = $\frac{1024}{256}$ = 4 way