KV2154

Diven two register are X5 and X6.

The best algorithm to swap 2 registers without using a 3rd 15:

XOR X5, X6 XOR X6, X5 XOR X5, X6

3.1)

addi is an I-Type Instruction Hence, it will take up read, two registers will read, and one register is written

oo Energy Spent

= 1 mem + 2x register read + register write = 140 pJ + 2x70 pJ + 60 pJ

= 340 pJ

=480 PJ

3.2

Id is a R-type instruction

Hence energy spent is similar to itype

plus another 140 pJ

30 Energy spent

=140 pJ + 2x70 pJ + 60 pJ + 140 pJ

30

beg will take up i-mem and 2 register

= 140 pJ + 2×70pJ

= 280 pJ

4 Della Comment

4.1

Data forwarding alone does not suffice as by the time the first ALU instruction already completes the second step, the Second ALU Instruction is already there in first ALU step. Thus, Its too late.

Hence, NOP between 2 Instructions as well as the forwarding between Second ALU step and decade step is required.

(01)

if(g 7 h) g = g + 1 e = g + 1 g = g + 1

BIT X5, X5, CON 926: X5, X5, I (ON: Addi, X6, X6, -1

if (g <= h)
g = (g,0);

h=0;

BEE X5, X6, CON CON: LD X5, O



4+ (3+4+3) X5 + 3= 57 clock goles

Number of instructions executed =

CPI = 57/17 = 3.35

For a 5 Stage pipeline = 5+(17-1) = 21

°. CPI = 21/17 = 1.23



						B			
XOR	51,52,53	IF	ID	EX	MEM	WB		1	
9991	50,53,-6					WEW			
1~	s3, 16(s7)			TF	EO	£×	WEN WE	3	
Sw	54,20(SI)				IF	IO	EXMEM	~B	
or	t2,50,51	2			*	IF	ID EX	WEV	wo
						To	56h c	y CH	2 - 5
									1

At Stage 5, XOR is in write back stage.

At Stage 5, addi is in manary Stage.

At Stage 5, Iwis in execute (ALV) Stage

At Stage 5, Sw is in de code Stage

At Stage 5, Or is in feth Stage

Hence, only SI is Whilten in Stage

18 XII , 8(XI3) 18 XII , 8(XI3) 18 XII , 8(XI3) 2061 XI3, XI2, XII

7.0

Data hazards and resolutions:-

-DEX to 1st RAW hazard occurs when value of X13 is accessed by 1d instruction when it is still in use by

ex Stage of or Instruction. It can be

GONS HIN PRIOSA

Vulve of XII is accessed by 2nd 1d instruction. It can be resolved with 2 MOPS

-) MEM to 1st and MEM to 2nd occurs
when add instruction tries to access
XII and XIO respectively. It can
be resolved with 2 NOPS

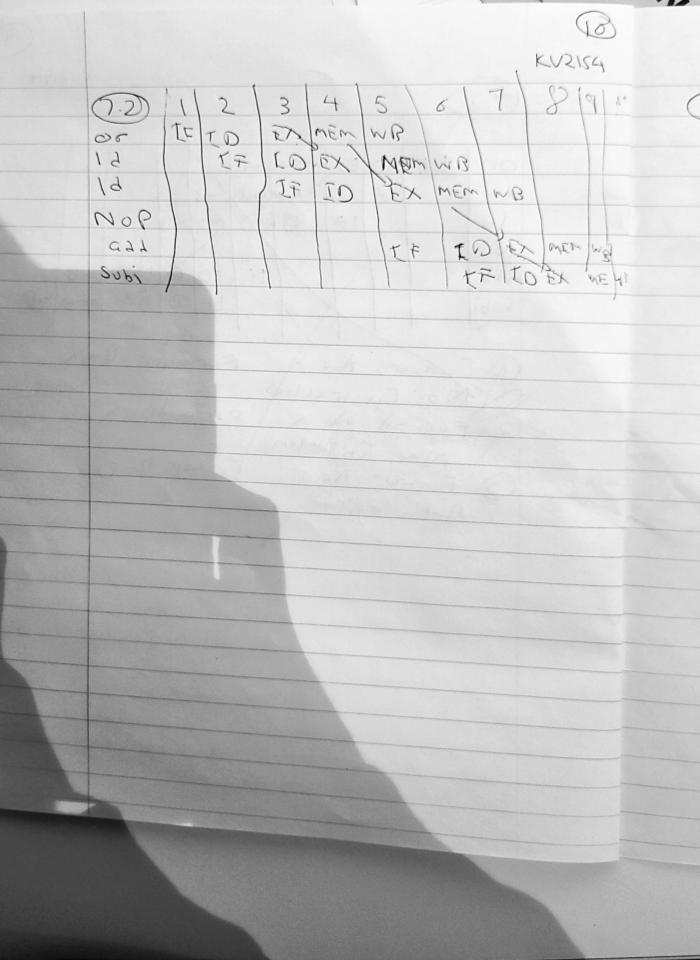
DEX to 1st RAW harzard OCCUTS

When Value of XIZ is accessed by

Subi instruction while it is still in use

by Ex of and instruction.

KU2154 OR X13 X12 , X11 N 08 NOP 19 ×11 8 (X13) NOP add XIZ XIO,XII NOP Subi X13/X12,16



Instruction / Program: -It will de crease. The new Instruction MILL COMPRES CIPS IN ON FURTHER which could has originally taken ? Instruction

It has no effect.

It will complete 3 add in Same Instruction. So no chang in the (PT

Comprexity: -

It will increase. Higher comprehity of credicted is required to english one or more open and.