Paper Name: Computer Organisation & Architecture

Module – 1: [4L] Basic organization of the stored program computer and operation sequence for execution of a program. Role of operating systems and compiler/assembler. Fetch, decode and execute cycle, Concept of operator, operand, registers and storage, Instruction format. Instruction sets and addressing modes. [3L] Commonly used number systems. Fixed and floating point representation of numbers. [1L]

Module – 2: [4L] Overflow and underflow. Design of adders - ripple carry and carry look ahead principles. [1L] Design of ALU. [1L] Fixed point multiplication -Booth's algorithm. [1L] Fixed point division - Restoring and non-restoring algorithms. Floating point - IEEE 754 standard. [1L]

Module – 3: [10L] Memory unit design with special emphasis on implementation of CPU memory interfacing. [2L] Memory organization, static and dynamic memory, memory hierarchy, associative memory. [2L] Cache memory, Virtual memory. Data path design for read/write access. [2L] Hierarchical memory technology: Inclusion, Coherence and locality properties; Cache memory organizations, Techniques for reducing cache misses; Virtual memory organization, mapping and management techniques, memory replacement policies. (4L)

Module – 4: [6L] Design of control unit - hardwired and micro programmed control. [1L] Introduction to instruction pipelining. [2L] Introduction to RISC architectures. RISC vs CISC architectures. [1L] I/O operations - Concept of handshaking, Polled I/O, interrupt and DMA. [2L]

Module – 5: [8L] Introduction: Review of basic computer architecture (Revisited), Quantitative techniques in computer design, measuring and reporting performance. (2L) Pipelining: Basic concepts, instruction and arithmetic pipeline, data hazards, control hazards and structural hazards, techniques for handling hazards. Exception handling. Pipeline optimization techniques; Compiler techniques for improving performance. (6L)

Module – 6: [3L] Instruction-level parallelism: basic concepts, techniques for increasing ILP, superscalar, superpipelined and VLIW processor architectures. Array and vector processors. (3L)

Module – 7: [5L] Multiprocessor architecture: taxonomy of parallel architectures; Centralized shared-memory architecture: synchronization, memory consistency, interconnection networks. Distributed shared-memory architecture. Cluster computers. (3L) Non von Neumann architectures: data flow computers, reduction computer architectures, systolic architectures. (2L)

Text books:

1. Computer System Architecture, by M. Morris Mano

2. Computer Organisation & Architecture, by W.Stallings.Pearson

3. Computer Organisation, by Hamacher V. Carl

4. Advanced Computer Architecture, Kai Hwang