HW2

Oğuzhan Kürşat Karayılan
150140011

a.

First canonical form = a’b’cd + a’bc’d’ + a’bcd’ + a’bcd + abc’d’ + abcd’
Second canonical form =
(a+b+c+d)(a+b+c+d’)(a+b+c’+d)(a+b’+c+d’)(a’+b+c+d)(a’+b+c+d’)(a’+b+c’+d)(a’+b+c’+d’)(a’+b’+c+d’)(a’+b’+c’+d’)

b.

abc’d’ + abcd’ → abd’(c’+c) → abd’
a’bcd + a’bcd’ → a’bc(d’ + d) → a’bc
a’bc’d’ + abc’d’ → bc’d’(a’+a) → bc’d’
a’b’cd + a’bcd → a’cd(b’+b) → a’cd

from abd’ and a’bc we can get consensus term of bcd’ since we have a and a’
bcd’ and bc’d’ → bd’
bd’ + abd’ → bd’
Finally we come up with a’bc + a’cd + bd’
bd’ and a’cd have consensus term of a’bc according to d and d’ term. So it can be eliminated.
Minimized expression is bd’ + a’cd

C

Note: I could not find one input NAND gate. Please think Inverters as one input NAND gate.