Understanding the Concept

A CMOS frequency divider is a simple yet powerful digital circuit that takes a high-frequency clock signal and produces an output clock at half the frequency. It works using a D Flip-Flop , where the inverted output ($\overline{Q}$) is feed back to the input (D). Each rising edge of the clock toggles the output state -- meaning Q switches between 0 and 1 with every clock pulse. This makes the output period twice as long as the input period, effectively dividing the frequency by two.

The design is implemented using CMOS technology, which combines NMOS and PMOS transistors to achieve low power consumption and high-speed operation. In this project, the 65 nm CMOS process is used to ensure small transistor dimensions and high performance.

In short: the divider uses one flip-flop, and by connecting $\overline{Q}$ -> D, the circuit toggles on each clock edge -- dividing the input frequency by 2.

Implementation Steps in Cadence

1. **Open Cadence Virtuoso** and create a new cell for the divider design.
2. **Choose logic style:** use a TSPC or static CMOS D Flip-Flop for high-speed operation.
3. **Draw the schematic:**
    a. Build a D Flip-Flop using CMOS transistors (NMOS and PMOS).
    b. Connect $\overline{Q}$ back to D.
    c. Add input (Clock), output (Q), and power supply pins (VDD and GND).
4. **Set transistor sizes:**
    a. Use minimum length (L = 65 nm).
    b. Start with Wn ≈ 1 µm and Wp ≈ 2 µm, then adjust for better performance.
5. **Create the testbench:**
    a. Add a high frequency clock source.
    b. Connect the divider circuit and observe the output Q.
    c. Run transient simulation.
6. **Measure results:**
    a. Verify that the output frequency is half of the input.

b. Calculate the Figure of Merit (FoM = f_max / Power).

Circuit design of CMOS (DFF)