Kareem Ashraf

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Objective:

Junior Electronics Engineer focused on Digital IC Design. Experienced in Verilog & RTL design with hands-on projects including RISC-V architecture, UART-IP, and PWM cores. Eager to apply skills in fast-placed VLSI design environments.

Education:

- B.Sc. in Electronics and Communications Engineering Cairo University
- Expected Graduation: Feb 2028.
- Three terms lasts for Graduation Project (Spring 2027)
- CGPA: 3.44 / 4.00

Projects:

✅ *Single-Cycle RISC-V RV32I* (FPGA)

- Designed and implemented a complete single-cycle RISC-V processor using Verilog.
- Verified using custom testbenches and uploaded to FPGA.
- Loaded with ***FIBONACCI*** program for verification.
- GitHub Repo: https://github.com/kareem05-ash/RISC_32I

✅ *UART IP Core* (TX/RX + FIFOs + Baud Generator)

- Designed a fully configurable and reusable UART IP with TX, RX, baud rate generator, and 2 buffering FIFOs for (TX, RX) with parameters DEPTH, WIDTH, and others.
- Developed RTL, testbenches, and simulation scripts.
- Verified functionality using waveform analysis using **QuestaSim**, self-checking TBs for each module, and a self-checking TB for top module (with real-world scenarios and corner cases)
- Uploaded to an FPGA board using **Vivado.**
- GitHub Repo: https://github.com/kareem05-ash/UART_IP

✅ *PWM / Timer Core with WB Interface* (Hackathon)

- Co-designed a PWM generator with timer logic and WB Interface integration.
- Verified functionality using waveform analysis using **QuestaSim**, self-checking TBs for each module, and a self-checking TB for top module (with real-world scenarios and corner cases)
- Elaborated Design, Synthesis, and Implementation using **Vivado.**
- GitHub Repo: https://github.com/kareem05-ash/PWM_Timer

Technical Skills:

- **HDLs:** Verilog, SystemVerilog, VHDL.
- **Programing:** C++, Python.
- **Verification:** SV Testbenches, Simulation (**QuestaSim**), Functional Coverage.
- **Tools:** Vivado, QuestaSim, ModelSim, Git & GitHub.
- **Others:** FPGA Implementation, Git Workflow.

Certifications & Courses:

- Digital IC Design Workshop – RTL & FPGA Track. [IEEE CUSB] (done)
  Contents:
  1. Verilog RTL Coding (Combinational/Sequential Logic, FSMs & Memories)
  2. Advanced Testbench Development (Self-checking, Tasks/Functions)
  3. FPGA Design Flow (Xilinx Vivado: Synthesis, STA& Linting)
  4. ASIC Flow Basics (Synthesis& Clock Domain Crossing)
  5. Low-Power Design Techniques

  Final Project: **RISC-V RV32I Single-Cycle Processor**

- Digital Verififcation Workshop. [IEEE ASUSB] (present)
  Contents:
  1. Self-checking testbenches using SystemVerilog
  2. Building UVM agent for verification environment
- PCB Design Using Altium Workshop. [IEEE CUSB] (done)
  Contents:
  1. Schematic building using **Altium.**
  2. PCB final layout, PnR, and Gerber files

  Final Project: A full PCB system that includes:

  1. ESP-07 MCU module, Power regulation using L7805CV
  2. Input modules (LDR sensor & switches), Output modules (Buzzer & LED driver)
  3. Serial communication interface
- Python Youtube for El-Zero Web School (present)
- Git (Version Control) Youtube for El-Zero Web School (done)
  1. Watched 20 videos to master project version control using cmder
  2. Build all project repos on GitHub using Git from git init up to final git push origin main
  3. Use SSH key for protection
- CLI Youtube for El-Zero Web School (done)
  1. Watched 10 videos to get familiar with command line instructions

Soft Skills:

- Microsoft Office: Word, Excell, PowerPoint, Outlock
- Documentation: Document all projects on GitHub (README.md, project_report.pfd)
- Leadership: Team Leader for most of my project teams
- Teamwork
- Time Management
- Problem Solving

Languages:

- English (Advanced)
- German (Intermediate)
- Arabic (Native)