

**University of Maryland, College Park
Department of Electrical and Computer
Engineering**



**A. JAMES CLARK
SCHOOL OF ENGINEERING**

**ENEE 416
Integrated Circuit Fabrication Laboratory
Lab Report**

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Introduction

In the ENEE416 Integrated Circuit Fabrication Laboratory, students engaged in a comprehensive, hands-on exploration of the IC manufacturing process, using 4-inch p-type silicon wafers to simulate real-world fabrication techniques. Throughout the semester, they were introduced to a sequence of essential steps in IC fabrication, including photolithography, etching, and doping. These foundational techniques are integral to the creation of precise and functional CMOS and NMOS transistors, which are the core components of modern integrated circuits.

The lab guided students through each stage, beginning with field oxide growth, which forms an insulating layer that defines active areas on the wafer. Through photolithography, students learned to apply photoresist coatings, carefully align masks, and use ultraviolet light to define intricate patterns for etching and doping. The use of dehydration baking, photoresist spinning, and contact alignment tools was essential to achieve accurate layer structures. Following photolithography, students proceeded with material deposition, such as polysilicon for gate formation and aluminum for conductive layers, with etching steps in between to selectively remove material. Using tools like spinners, hotplates, and contact aligners, students practiced applying, developing, and precisely etching photoresist layers to shape the wafer surface.

Each lab culminated in an inspection phase, where students used microscopes to verify the alignment and accuracy of patterned layers, examining surface morphology and confirming that fabricated structures met design requirements. Measurements of thicknesses and careful observation of surface patterns allowed students to evaluate the success of their fabrication efforts and to understand how even the smallest errors or misalignments could impact device performance. Through this meticulous process, students not only gained technical skills in IC manufacturing but also developed an appreciation for the precision, creativity, and troubleshooting required in semiconductor fabrication. This experience highlighted the real-world challenges and limitations of IC production, preparing students to tackle the complexities of creating miniaturized electronic components in professional settings.

Experimental Details

Lab 1: Photoresist Application and Mask Alignment (Mask 1: Active Layer)

Dehydration (Hard) Bake

The process began with dehydration baking, where the 4-inch p-type silicon wafer was pre-baked at 120°C for approximately 10 minutes to remove any residual moisture, ensuring a clean surface for further processing.

HMDS Application

Once the wafer had cooled on a heat sink, a half-pipette of Hexamethyldisilazane (HMDS) was applied. This adhesion promoter was spun at 4000 rpm for 40 seconds to create a uniform layer that would help the photoresist adhere more effectively.

Photoresist Application

The photoresist used was Shipley 1813, which was applied similarly to the HMDS with a slightly larger amount and spun at 4000 rpm for 45 seconds. This ensured even coverage of the wafer surface. The wafer was then soft-baked at 95°C for 1 minute to improve the adhesion of the photoresist and prevent any unwanted movement during exposure.

Mask Alignment & Exposure

Using a contact aligner, the wafer was carefully aligned to the active layer mask, ensuring that alignment markers were precisely matched. The active area was defined using a dark-field mask. The wafer was exposed to 365 nm UV light for 6-7 seconds, allowing the UV light to transfer the mask pattern onto the photoresist.

Development

After exposure, the wafer was developed in Shipley CD-26 for approximately 40 seconds with gentle agitation to dissolve the exposed photoresist. This was followed by rinsing in deionized (DI) water and drying with nitrogen. The developed patterns were examined under a microscope, with images taken for documentation.

Lab 2: Oxide Etching

Etching Process

The wafer was submerged in a 6:1 Buffered Hydrofluoric Acid (BHF) solution until the exposed oxide layer was removed, indicated by the wafer surface becoming hydrophobic. This process took around 7.5 minutes, effectively etching away the exposed oxide in the active areas.

Resist Stripping

Following etching, the photoresist was removed in Microchem Remover PG with two batches (3 minutes each), followed by rinses in isopropyl alcohol (IPA) and DI water. Profilometer measurements showed the final oxide thicknesses post-etching at around $1.375\mu\text{m}$.

Lab 3: Reapplication of Photoresist and Mask Alignment

Process Repetition

The wafer was dehydrated and re-coated with HMDS and Shipley 1813 photoresist in a similar sequence to Lab 1, spinning at 4000 rpm. The wafer was soft-baked again at 95°C . Following this, the wafer was aligned on the contact aligner, and the same active layer mask was used for alignment. Exposure and development were carried out similarly, followed by a hard bake to improve pattern durability.

Lab 4: Polysilicon Etching (Mask 2: Polysilicon & Gate Oxide Layer)

Polysilicon and Gate Oxide Preparation

The wafer was dehydrated and treated with HMDS as in previous labs, followed by Shipley 1813 application and soft baking.

Polysilicon Etching

Following the application and alignment of the polysilicon mask, UV exposure and development were performed to define the polysilicon gate structure. The wafer was submerged in an $\text{HNO}_3:\text{H}_2\text{O}:HF$ solution for approximately 1 minute, over-etching slightly to ensure complete removal of the polysilicon in the exposed areas. Profilometer measurements confirmed successful etching with a final thickness of $\sim 19\text{ k}\text{\AA}$.

Resist Stripping

The photoresist was stripped using Remover PG, and the wafer was rinsed in IPA and DI water. Profilometer measurements after this indicated successful fabrication with a remaining thickness of $\sim 6.03\text{ k}\text{\AA}$.

Lab 5: Spin-On Dopant Application (Source-Drain n+ Deposition)

Doping Process

After a thorough clean using H₂SO₄:H₂O₂, the wafer was dipped briefly in BOE to remove any native oxide. Following a dehydration bake at 120°C for 10 minutes, Filmtronics Phosphosilicate Glass (PSG) dopant was applied using a spinner at 4000 rpm for 40 seconds to create a uniform dopant layer.

Diffusion and Removal

The wafer was subsequently processed in an oven at 190°C by lab staff for pre-diffusion, followed by PSG layer removal in BHF. These steps created the n+ regions necessary for defining the MOSFET source and drain.

Lab 6: Creating Via Holes (Mask 3: Contact Layer)

Preparation and Alignment

Starting with a dehydration bake, HMDS and Shipley 1813 photoresist were applied as before. The contact mask was carefully aligned to ensure correct via hole placement. UV exposure and development followed to open the via holes in the photoresist layer.

BOE Etching

The wafer was etched in BHF for about 4 minutes, creating the contact layer openings. Final profilometer measurements showed successful pattern development, with the wafer dried and stripped of photoresist for imaging and analysis.

Lab 7: Contact Layer Formation

Wafer Preparation:

The contact layer was formed where I prepared the wafer with dehydration baking on a hotplate at 120°C for 10 minutes to remove any moisture. HMDS was applied and spun for 40 seconds. Shipley 1813 photoresist was then applied and spun at 4000 rpm for 40 seconds, followed by a soft bake at 100°C for 1 minute to set the photoresist layer.

Mask Alignment and Exposure:

I aligned the wafer using a contact aligner, carefully positioning the contact mask to define the contact pads accurately. The wafer was exposed to UV light at 365 nm for 6 seconds. After exposure, it was developed using Shipley CD-26 for 40 seconds, rinsed with DI water, and dried with nitrogen. Under the microscope, check the verniers to confirm that the layer was well-aligned with the source/drain regions and the polysilicon gate.

Etching and Measurements:

The intermediate oxide layer was etched using a 6:1 BHF solution for 4 minutes, with a slight over-etch. Following this, the wafer was rinsed with DI water and dried with nitrogen.

Photoresist Removal and Inspection:

The photoresist was removed using Microchem Remover PG, rinsed with IPA and DI water, and dried with nitrogen. A final inspection with the microscope confirmed that the contact holes were clearly visible and accurately positioned. These procedures were essential for creating the contact points that connect various regions in the IC, ensuring proper electrical pathways for device functionality.

Lab 8: Metal Layer Formation

Wafer Preparation:

The metal layer was formed where the wafer was initially prepared with an 8000 Å layer of aluminum, applied by the lab staff, to create a conductive surface for final metal connections. I then performed dehydration baking at 120°C for 10 minutes, applied HMDS, and spun it for 40 seconds. Shipley 1813 photoresist was applied and spun at 4000 rpm for another 40 seconds, followed by a soft bake at 100°C for ~1 minute to solidify the photoresist layer.

Mask Alignment and Exposure:

The metal mask was aligned over the wafer using the contact aligner, with careful attention to the metal pattern's alignment over the contact pads. The wafer was exposed to UV light at 365 nm for 6 seconds, transferring the pattern. The wafer was then developed in Shipley CD-26 for 35-40 seconds, rinsed in DI water, and dried with nitrogen. I used the microscope to check alignment accuracy by viewing the verniers at the left, center, and right positions. A hard bake at 120°C for 10 minutes was performed to stabilize the pattern before etching.

Etching and Measurements:

The aluminum layer was etched using Aluminum Etchant Type A, a solution of phosphoric acid, nitric acid, acetic acid, and water, for approximately 1 minute and 10 seconds, with an additional 10-second over-etch to ensure ~95% aluminum removal. The wafer was rinsed thoroughly with DI water and dried with nitrogen.

Photoresist Removal and Final Inspection:

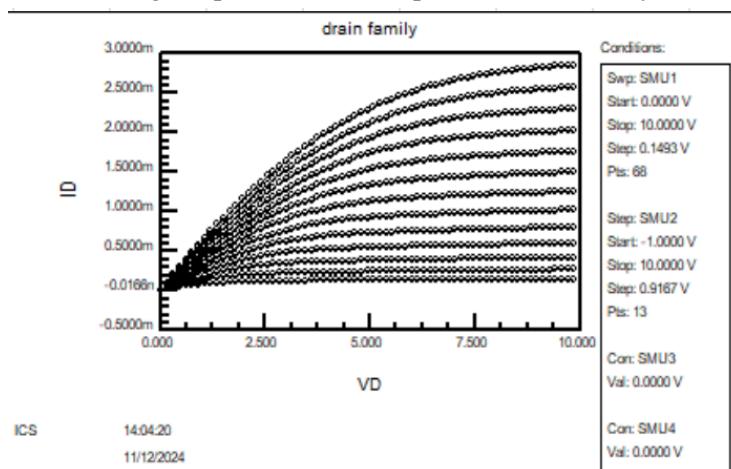
Finally, the photoresist was removed using Microchem Remover PG, followed by an IPA and DI water rinse. The metal layer, which enables electrical connections within the IC, will be essential for functional connections between the source, drain, and gate regions during testing.

Testing Phase

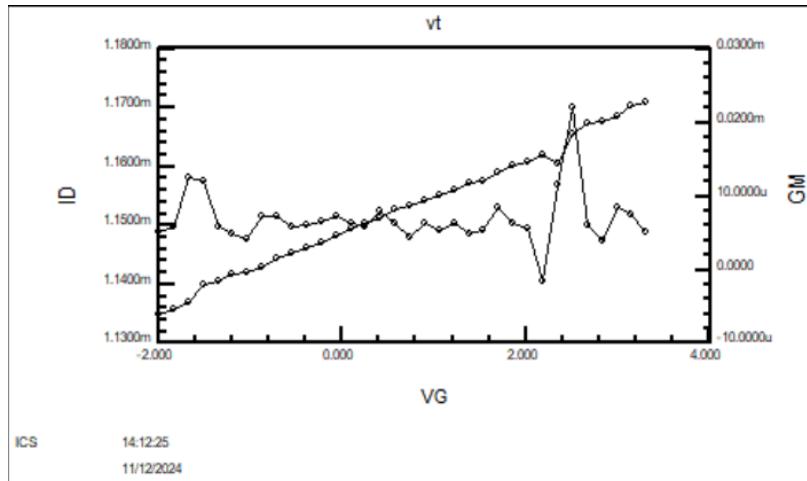
The testing phase of the IC fabrication process evaluated the functional performance of key components, ensuring the integrity and accuracy of the fabrication steps. This stage focused on analyzing MOSFET characteristics, including threshold voltage (VT_V_T_{VT}), transconductance (g_m_g_m_{gm}), and channel length modulation (λ), as well as parameters like contact resistance, line resistance, and diode behavior. The MOSFET measurements demonstrated the device's switching and amplification capabilities, with Drain Family and Gate Family curves highlighting its behavior in the triode and saturation regions. The contact resistance measurements verified the quality of electrical connections, emphasizing the importance of minimizing resistive losses in IC designs. Similarly, the diffusion and polysilicon line resistance tests provided insight into the material properties and their impact on circuit performance. Diode testing confirmed forward turn-on voltage and series resistance, validating the overall functionality of the device. These results underscored the significance of precise fabrication techniques and material selection in achieving reliable IC performance and highlighted the sensitivity of these devices to process variations.

MOSFETs:

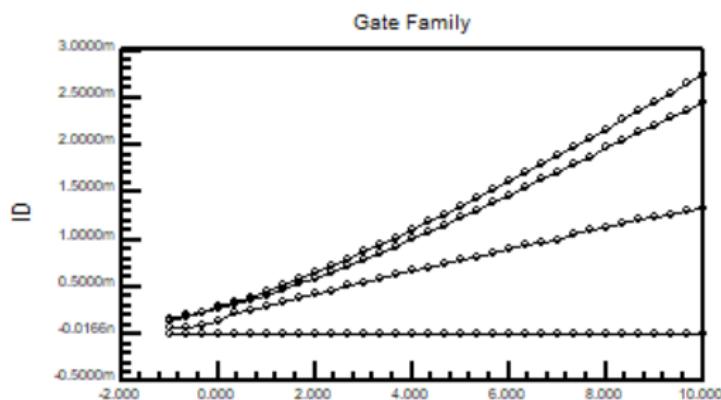
The testing of MOSFET devices was a critical part of the integrated circuit fabrication process, aimed at understanding the electrical behavior and performance of these components. The analysis focused on key parameters such as threshold voltage (VT_V_T_{VT}), transconductance (g_m_g_m_{gm}), and channel length modulation (λ). These metrics were derived from characteristic curves, including the Drain Family, Threshold Voltage, and Gate Family plots. By evaluating these aspects, the testing phase provided a comprehensive view of the MOSFET's functionality in both analog and digital applications, offering insights into the device's switching, amplification, and operational efficiency.



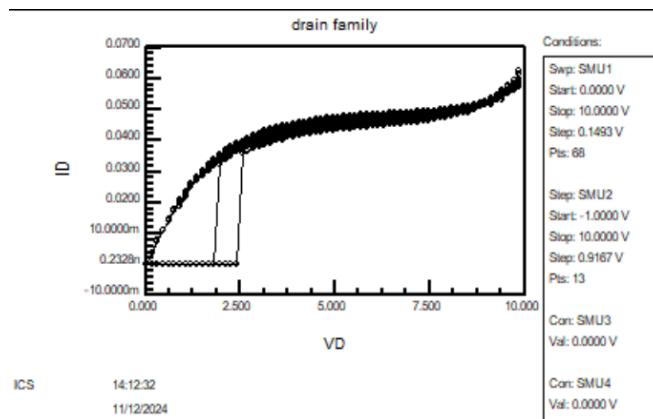
The **Drain Family** curve illustrates the variation of drain current (ID) as a function of drain voltage (VD) for multiple gate voltages (VGS). This graph highlights the two primary regions of MOSFET operation: the triode region, where ID increases linearly with VD, and the saturation region, where ID stabilizes due to the pinch-off effect. The slope in the saturation region is a key parameter for determining the channel length modulation (λ) and output resistance (r_0). Observing the transition between these regions provides critical information about the MOSFET's ability to handle varying voltage levels and its overall performance in switching applications.



The **Threshold Voltage** plot evaluates the point at which the MOSFET transitions from the off-state to conduction. This is represented by the exponential rise in ID as VGS crosses the threshold voltage (VT). Additionally, the plot overlays the transconductance (gm), which is the rate of change of ID with respect to VGS . The maximum gm value identifies the optimal operating point for analog amplification, indicating the device's responsiveness and efficiency. This measurement is particularly critical in high-frequency circuits, where precise control over gm can significantly impact performance.



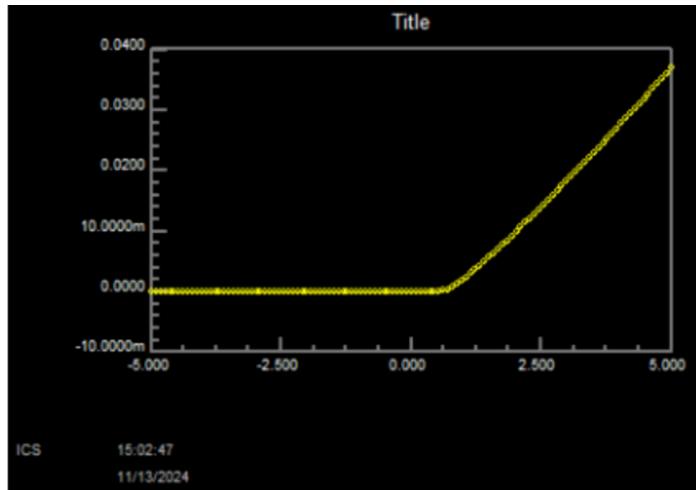
The **Gate Family** curve examines the relationship between ID and VGS for different VD values, showcasing the MOSFET's behavior as it transitions from subthreshold to strong inversion. As VD increases, the device enters the saturation region more rapidly due to the pinch-off effect. Negative ID observed in the subthreshold region reflects the effects of substrate doping or leakage current, providing additional insight into the MOSFET's material properties and structural characteristics. This analysis offers a holistic understanding of the MOSFET's operational versatility and its suitability for various IC applications.



The **Drain Family** curve for the MOSFET indicates a failure caused by a short circuit, evident from the significant current (ID) flowing at low drain voltage (VD) without transitioning through the expected triode and saturation regions. In a properly functioning MOSFET, ID would initially rise linearly with VD in the triode region before stabilizing in the saturation region due to the pinch-off effect. The immediate and abnormal rise in current suggests a direct connection between the source and drain, bypassing gate control. This issue is likely due to fabrication defects, such as over-etching, misaligned layers, or residual conductive material during the contact or metal layer processes. The short circuit compromises the MOSFET's ability to function as a switch or amplifier. Further analysis of the wafer under a microscope and resistance measurements across the terminals are needed to identify and rectify the cause of the short.

Diodes:

The diode testing phase focused on evaluating its forward bias characteristics and operational parameters to ensure proper functionality and performance. The forward bias region of the diode was analyzed to determine the turn-on voltage, which is the point where the diode transitions from a non-conductive to a conductive state. This critical parameter plays a significant role in defining the diode's suitability for various applications, such as rectifiers, switches, and voltage regulation circuits.



The current-voltage (I-V) curve obtained during testing demonstrated the diode's behavior under forward bias. The turn-on voltage was identified as the point where a significant increase in current occurred, indicating the onset of conduction. This transition highlights the diode's efficiency in conducting current once the applied voltage exceeds the built-in potential barrier. Beyond this region, the diode displayed a linear increase in current with voltage, governed by its internal resistance.

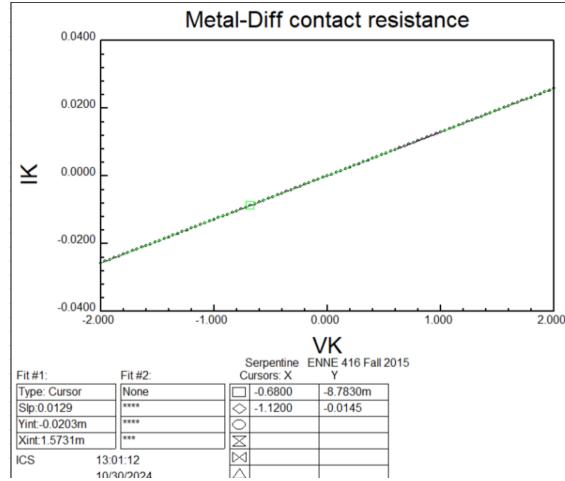
The series resistance of the diode was calculated by analyzing the slope of the I-V curve in the linear region of the forward bias. This resistance, a combination of the internal diode structure and contact resistance, affects the diode's efficiency and power dissipation. A low series resistance is essential for minimizing voltage drops and ensuring maximum current flow, particularly in high-power or high-frequency applications.

These testing results validated the successful fabrication of the diode, with the observed turn-on voltage and series resistance aligning with theoretical expectations. The data provided insights into the diode's operational efficiency and potential limitations, underscoring the importance of precise fabrication techniques and material quality in achieving optimal device performance.

Die Location	Average Resistance (k-ohms)
Right	2256
Bottom	2136
Left	2172
Top	2213
Middle	2229

Serpentine resistors:

The serpentine structure was used to measure the contact resistance for metal-diffusion interfaces. The I-V plot indicates a linear relationship between the current (I_K) and voltage (V_K), confirming stable and predictable contact behavior. The slope of the line, measured as 0.0129, was used to calculate the total resistance of the contact chain. Dividing this value by the number of contact points in the chain provides the average resistance per contact, a critical metric for ensuring minimal voltage drops and efficient current flow.

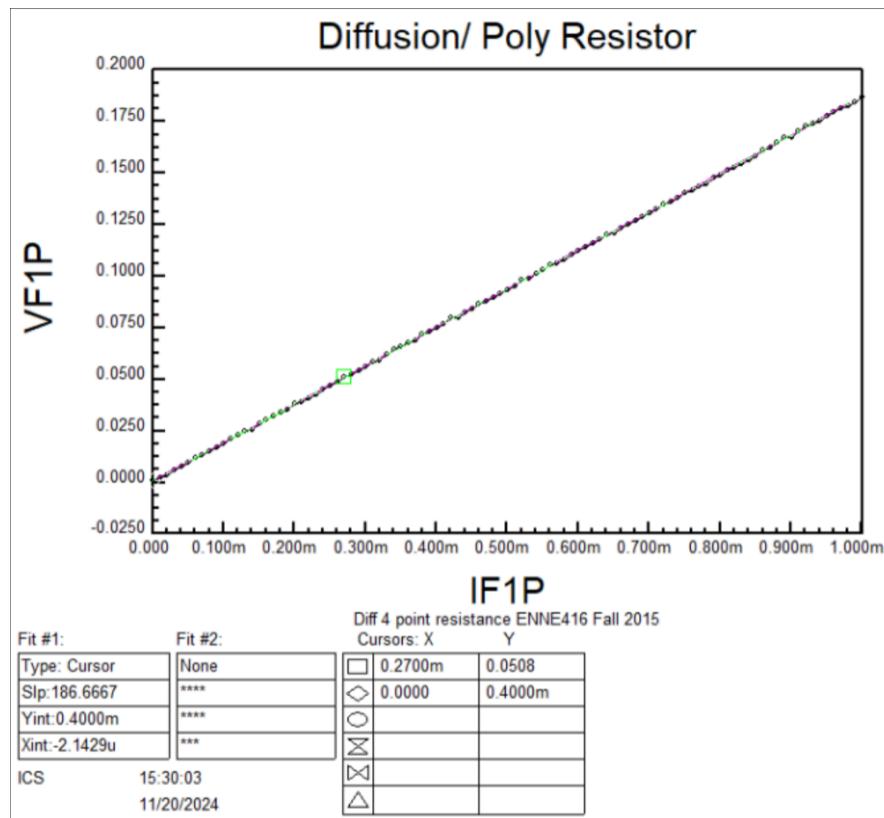


The consistent linearity of the graph suggests good material quality and fabrication accuracy, with low-resistance connections between the metal and diffusion layers. This performance is essential in ICs, as high contact resistance could lead to power losses, slower circuit response times, and increased heat generation. The data confirms that the metal-diffusion contacts were fabricated successfully, with resistance values aligning with expectations for high-performance circuits. Further analysis or comparisons with other interface types, such as metal-poly, can provide additional insights into overall contact performance.

Die Location	Diffusion Chain Resistance
Right	75.1
Bottom	73.6
Left	74.2
Top	74.7
Middle	74.2

4 Point Resistor Testing:

The four-point probing method was used to measure the resistance of the diffusion and polysilicon resistors. The I-V plot demonstrates a linear relationship between the voltage (VF1P) and current (IF1P), confirming consistent resistive behavior across the tested structure. The slope of the line, calculated as 186.6667, represents the total resistance of the resistor. Using the known geometry of the resistor, the sheet resistance can be calculated by dividing the total resistance by the number of squares in the structure.



This linearity indicates uniform resistive properties, with minimal variability due to fabrication imperfections. The diffusion resistor typically exhibits lower sheet resistance due to its material properties, making it suitable for applications requiring lower resistance and higher current flow. In contrast, polysilicon resistors, while having higher resistance, are often used in circuits requiring controlled resistance values for specific functionalities. The results confirm the successful fabrication of the resistors, aligning with theoretical expectations and validating the four-point probing method's effectiveness in measuring intrinsic resistance accurately.

Discussion

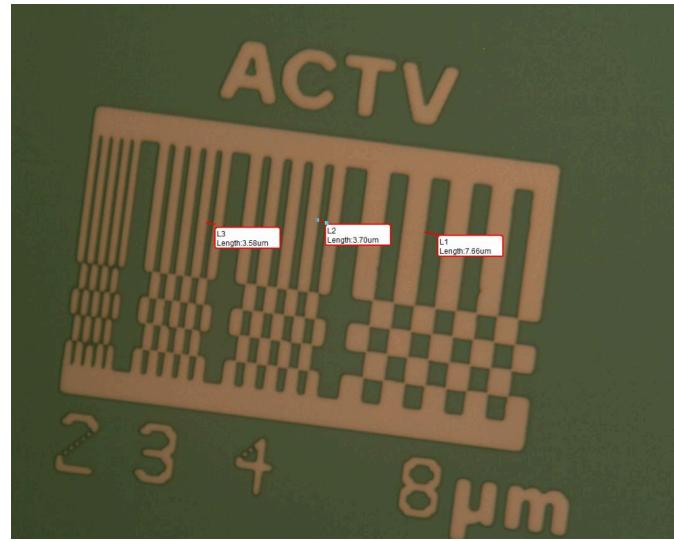


Figure 1: In this image we are looking at the active layer measuring from the reference pattern we obtained three measurements. The lengths of L1, L2, L3 are shown in the image above with respective lengths of $7.66\mu\text{m}$, $3.70\mu\text{m}$, and $3.58\mu\text{m}$.

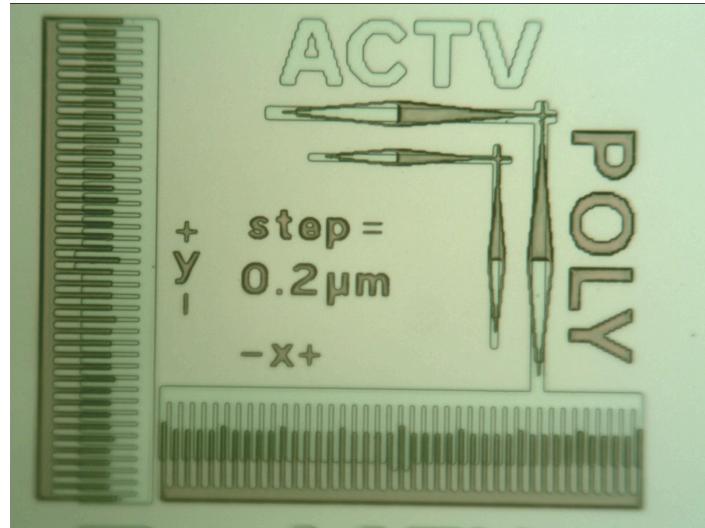


Figure 2: Post-development images showing the alignment of the first two masks, poly and active respectively. Regions are well aligned indicating successful alignment.

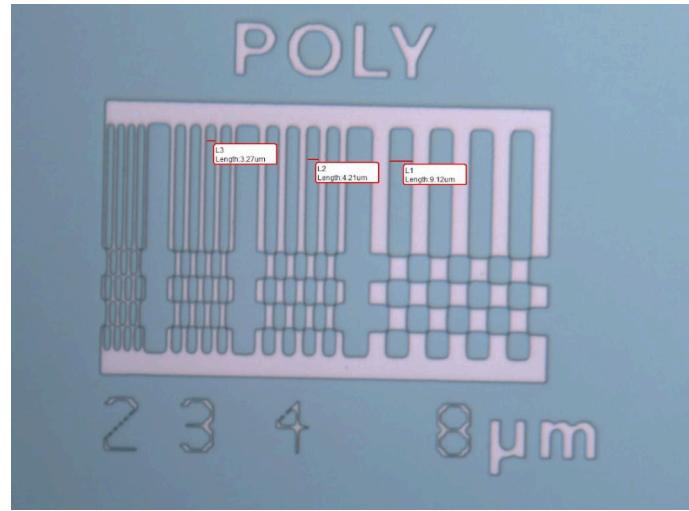


Figure 3: In this image we are looking at the poly mask layer measuring from the reference pattern we obtained three measurements. The lengths of L1, L2, L3 are shown in the image above with respective lengths of 9.12 μ m, 4.21 μ m, and 3.27 μ m.

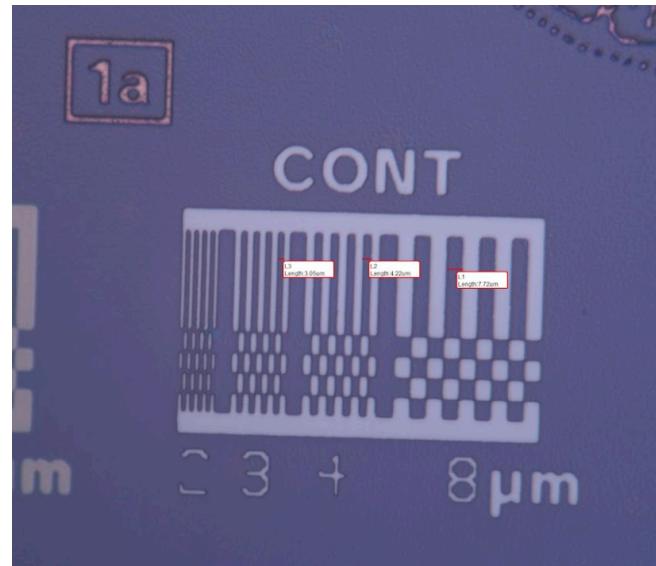


Figure 4: In this image we are looking at the contact mask layer measuring from the reference pattern we obtained three measurements. The lengths of L1, L2, L3 are shown in the image above with respective lengths of 7.72 μ m, 4.22 μ m, and 3.05 μ m.

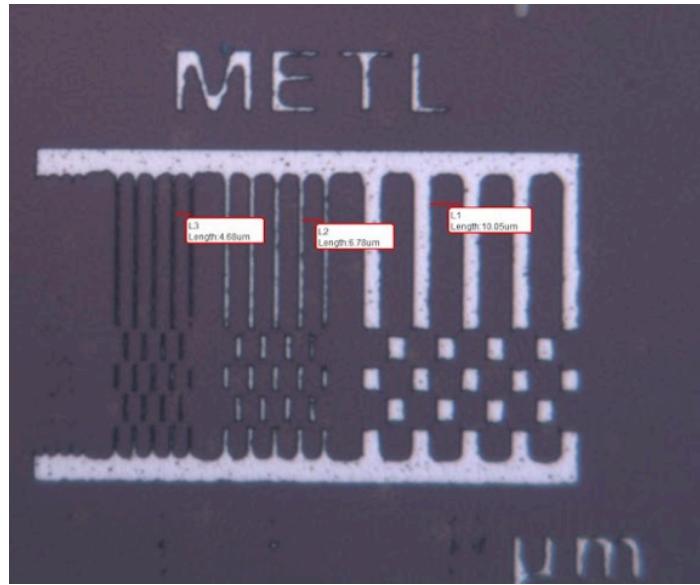


Figure 5: In this image we are looking at the metal layer measuring from the reference pattern we obtained three measurements. The lengths of L1, L2, L3 are shown in the image above with respective lengths of $10.05\mu\text{m}$, $6.78\mu\text{m}$, and $4.68\mu\text{m}$. The measurement to scale is 23.38 for all measurements.

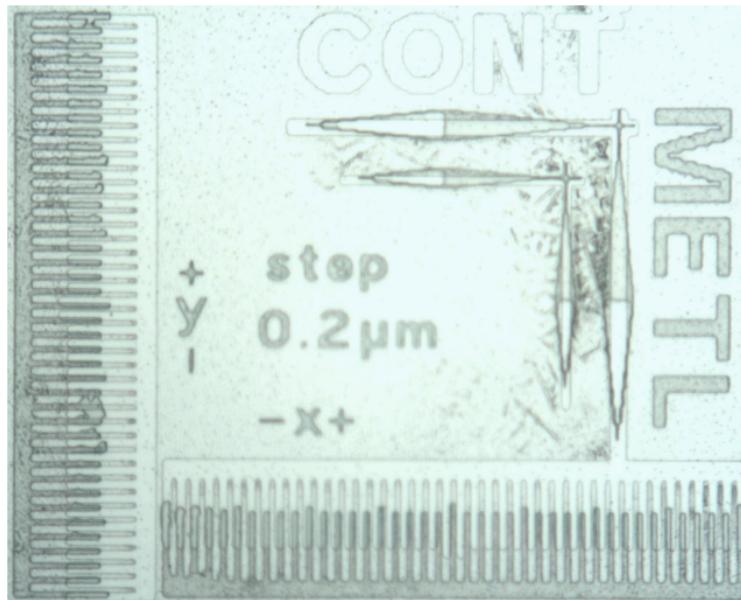


Figure 6: Post-development images showing the alignment markers and test structures for the contact (CONT) and metal (METL) layers. The markers, labeled with directions (+Y, -X), and spacing step of $0.2 \mu\text{m}$, aid in precise alignment of subsequent layers during the photolithography process. Regions are well aligned indicating successful alignment.

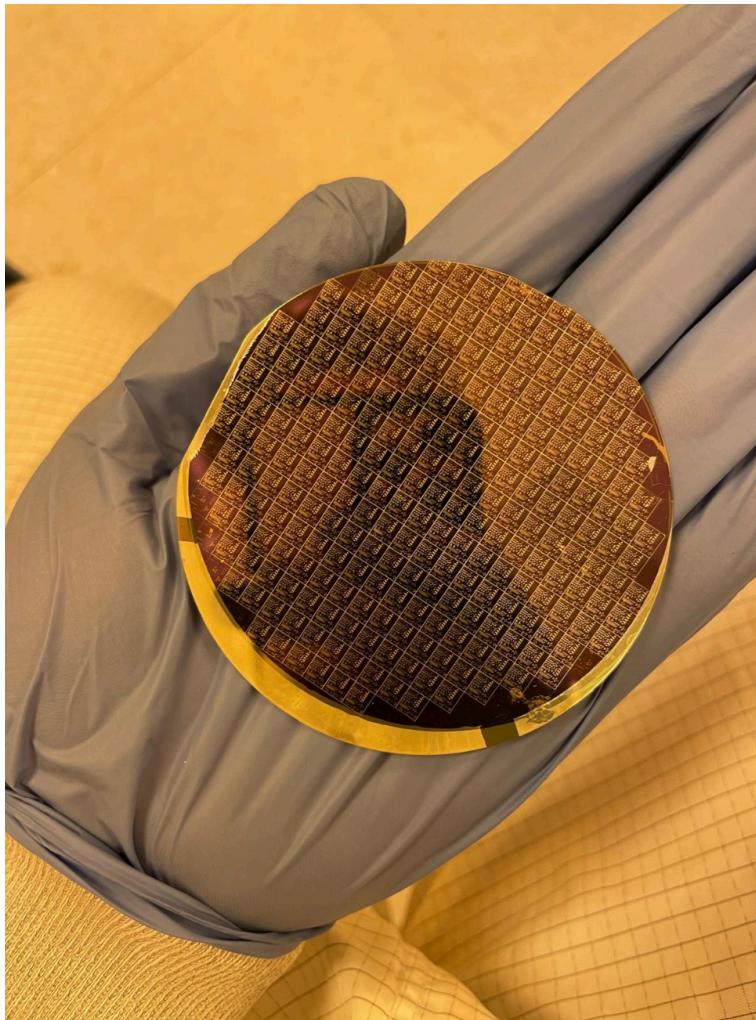


Figure 7: Completed silicon wafer after all fabrication steps. The wafer displays a grid of integrated circuits, each representing an individual device fabricated during the process. The array of small, uniform squares demonstrates the accuracy achieved through photolithography, etching, and doping. The outer edge features alignment markers, aiding in mask alignment during each layer's processing. This image highlights the successful creation of complex circuitry on a micro-scale, showcasing the precision and careful handling required in IC fabrication.

Conclusion

The ENEE416 labs provided valuable hands-on experience in the fundamental steps of IC fabrication, emphasizing the practical challenges and nuances of CMOS technology. Through sequential experiments, we created essential structures like active layers, polysilicon gates, and contact layers, using techniques such as photolithography, etching, and doping. Each fabrication step required precision, and even small deviations, such as slight misalignments or thickness variations, highlighted the sensitivity of IC manufacturing processes to environmental and procedural variables.

The measurements taken after each step confirmed the accuracy of our process in most areas, with profilometer readings and microscope imaging indicating successful pattern transfer and etching. Any deviations observed, such as minor differences in oxide thickness after etching, underscored the importance of control in material application and exposure times. These deviations, although minor, offer insights into factors like the uniformity of photoresist coatings and etchant behavior, which are critical to maintaining consistency in larger-scale fabrication.

Overall, the lab exercises deepened our understanding of IC fabrication's complexity and the precision needed to achieve reliable results. By working through each step and overcoming challenges inherent in photolithography and etching, we gained an appreciation for the meticulous nature of this field and the continuous improvements required for modern CMOS technology.

References

- R.C. Jaeger, *Introduction to Microelectronic Fabrication*, 2nd ed., vol. 5, Prentice Hall, Upper Saddle River, NJ, 2002.
- A. Modafe, G. Becker, and M.L., *ENEE 416 Lab 1 Directions*, University of Maryland, Revised August 17.
- A. Modafe, G. Becker, and M.L., *ENEE 416 Lab 2 and 3 Directions*, University of Maryland, Revised August 17.
- A. Modafe, G. Becker, and M.L., *ENEE 416 Lab 4 and 5 Directions*, University of Maryland, Revised August 17.
- A. Modafe, G. Becker, and M.L., *ENEE 416 Lab 6 Directions*, University of Maryland, Revised August 17.
- A. Modafe, G. Becker, and M.L., *ENEE 416 Lab 7 Directions*, University of Maryland, Revised August 17.
- A. Modafe, G. Becker, and M.L., *ENEE 416 Lab 8 Directions*, University of Maryland, Revised August 17.
- S. Wolf and R.N. Tauber, *Silicon Processing for the VLSI Era*, 2nd ed., vol. 1, Lattice Press, 1986.
- Shipley Company LLC, *Photoresist Data Sheets*.