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Subject : Advanced Computer Architecture
Assignment Title :Advanced Computer Architecture Assignment
Submission Date : 27/01/2022

q1.

1. PC : Program counter it has the size of 12 bits and it has the next inst address
2. AR : Address register it has the size of 12 bits and it has the address for memory
3. DR : Data register it has the size of 16 bits and it has the memory operand
4. AC : Accumulator it has the size of 16 bits and it has the holds data of processor register
5. IR : Instruction register it has the size of 16 bits and it has the instruction code
6. TR : Temporary register it has the size of 16 bits and it has the temporary data
7. INR : Input buffer register it has the size of 8 bits and it has the input ASCII data
8. OUTR : Output buffer register it has the size of 8 bits and it has the output ASCII data
9. SCR : Sequence counter register it has the size of 4 bits
10. E, R : Single bit flip-flops interrupt, flag/utility

q2.

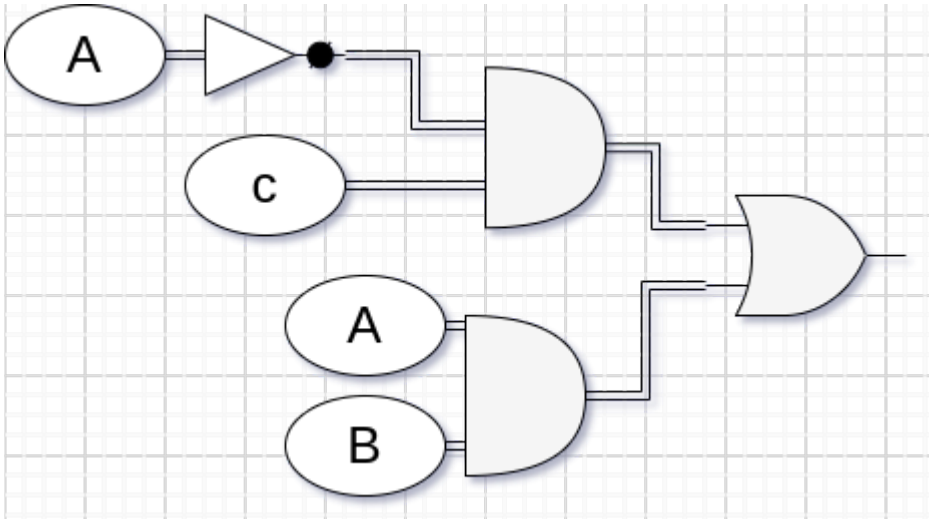
1.

$\bar{a}\,\bar{b}\,c+\bar{a}\,bc+ab\,\bar{c}+abc$

2.

1. $\bar{a}\,\bar{b}\,c+\bar{a}\,bc+ab\,\bar{c}+abc$
2. rule (ab+ac = ab+c) $\bar{A}\,C(\bar{B}+B)+AB\,\bar{C}+ABC$
3. rule $\bar{A}+A=1$ $\bar{A}\,C\,1+AB\,\bar{C}+ABC$
4. rule a1 = a $class\,\bar{A}\,C+AB\,\bar{C}+ABC$
5. rule (ab+ac = ab+c) $\bar{A}\,C+AB(\bar{C}+C)$
6. rule $\bar{A}+A=1$ $\bar{A}\,C+A\,B\,1$
7. rule a1 = a $\bar{A}\,C+c\,A\,B$

3.



q3.

what is DMA?

Direct memory access (DMA) is a data transfer mode that transfers data between I/O and memory and all of this happenes without getting the processor involved and there are 2 methods to get data transferd 1. interrupt driven I/O programmed I/O.

Why?

It is used for transferring data because it does not involve the processor which means it can do the data transfer faster and it has more effectiveness when transferring large block of data.

Advantages

1. getting more speed from reading and writing tasks because the processor is not getting involved in the task.
2. reduces the overhead of the processor when the DMA is implemented.

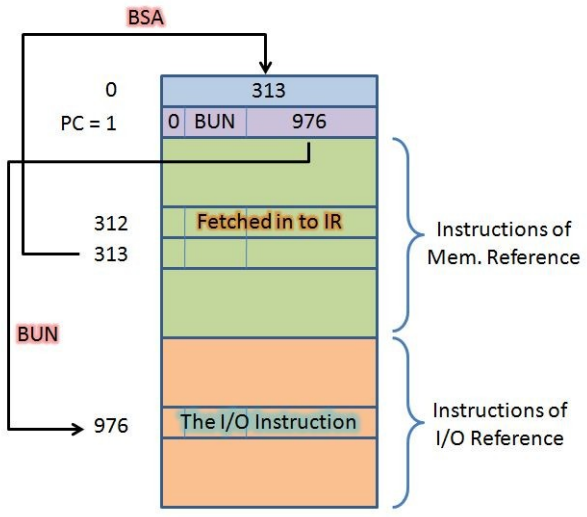
disadvantages

1. The DMA controller is a hardware component which means it will add to the cost.
2. Using DMA controller can make the problem of Cache coherence occur.

q4.

Interrupt Cycle:

Interrupt Cycle is cycle that is very similar to the instruction cycle, as a start it checks the states of the IEN to check wather it should proceed or not, if it the value of IEN is true it means that we can proceed to the next step which is to save the content in PC in memory add [0] by using BSA instruction then it does a BUN instruction to memory [1] which takes the address that has the instructions to begin a new cycle of instructions now when the instructions are over we go to the memory [1] where we saved where we were before the interruption started and continue what we were doing.



During the interruption cycle.

q5.

A) 0010 1011 right

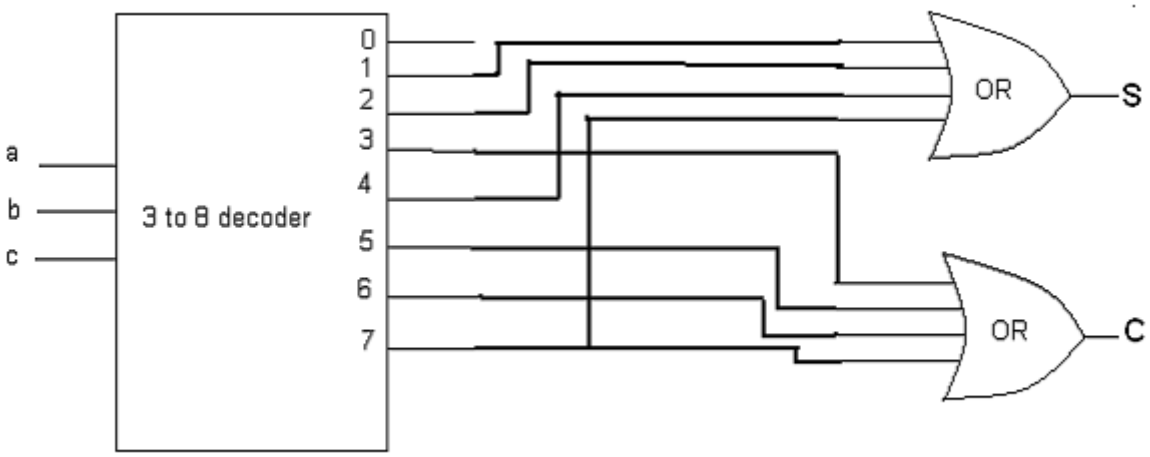
B) 1010 1100 left

q6.

S = ab’c’ + a’b’c + a’bc’ + abc = Σ(1,2,4,7)

C = ab + ac + bc = ab(c + c’) + ac (b + b’) + bc (a + a’) = abc + abc’ + abc + ab’c + abc + a’bc

= abc +a’bc +ab’c+abc’= Σ (3, 5, 6, 7)

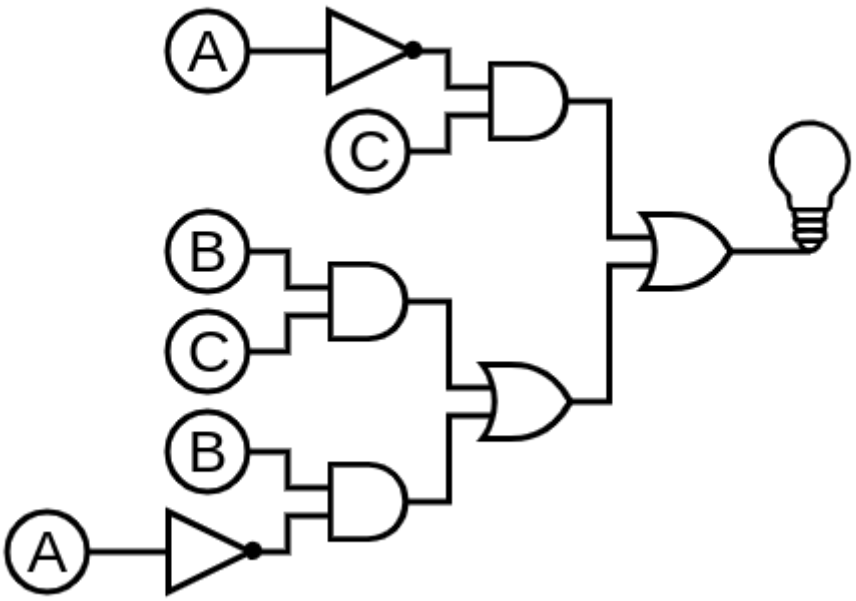


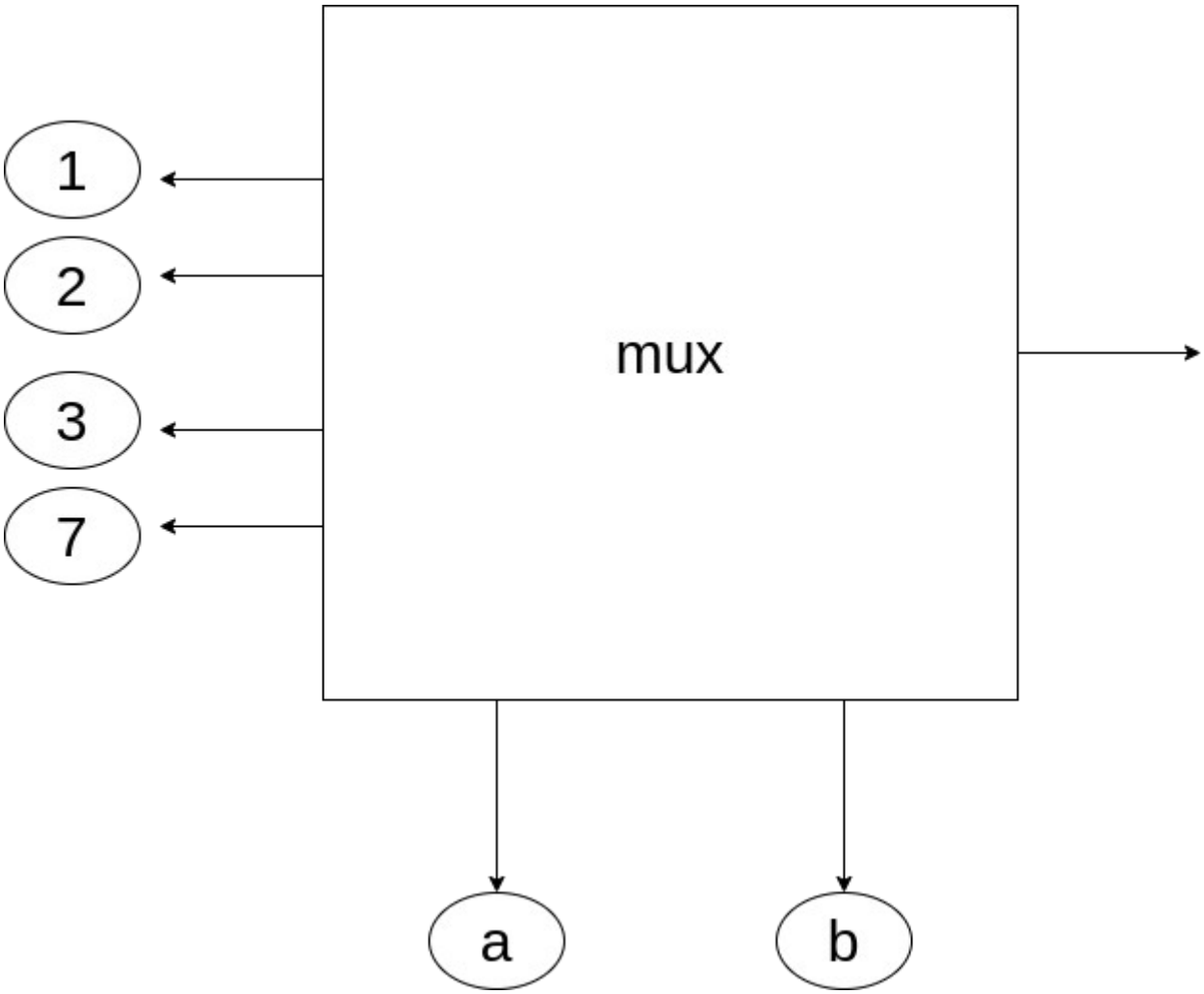
q7.

the main equation from the truth table would be $\bar{a}\bar{b}c+\bar{a}b\bar{c}+\bar{a}bc+ab\bar{c}$

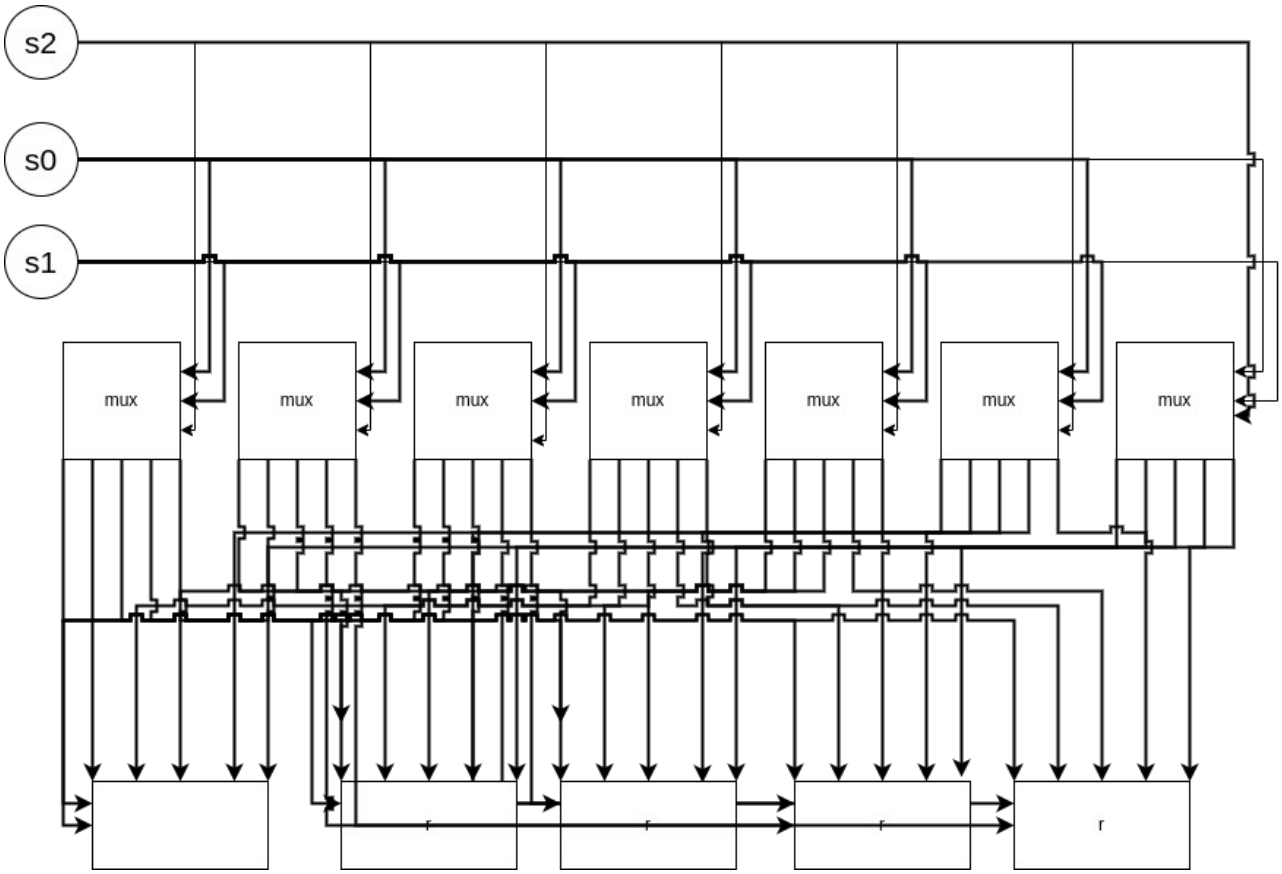
after simplification $\bar{A}C+BC+B\bar{A}$

s0	s1	in
0	0	1
0	1	2
1	0	3
1	1	7


A
C
B
C
B
A


1
2
3
7
mux
a
b

q8.



q9.

1. $ABCD_{16}=1010101111001101_2$

   A B C D
   1010 1011 1100 1101

   001 010 101 111 001 101
   1 2 5 7 1 5

   $1010101111001101_2=125715_8$

q10.

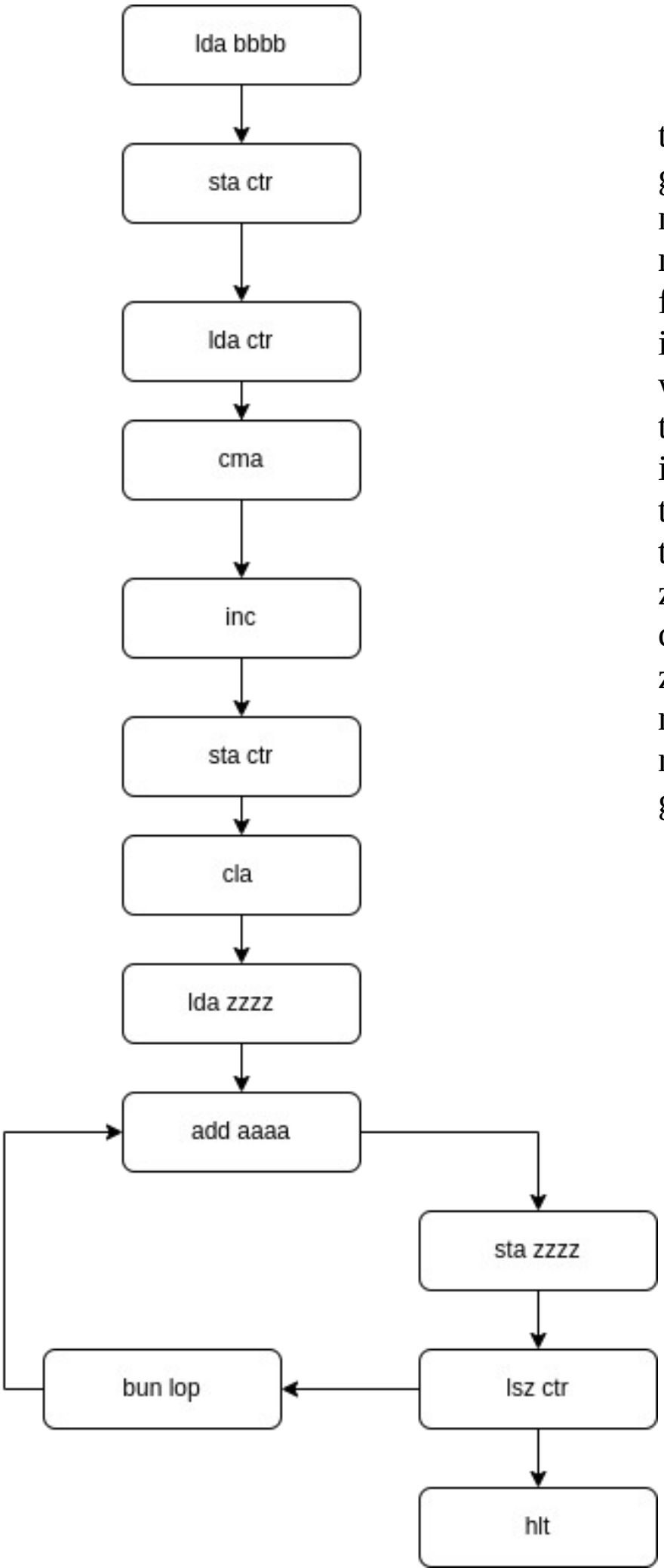
77	0100 1101

90	0101 1010
sum	1010 0111
-77	111 0011
-90	110 0110
sum	1 0101 1001
2’s comp	10100111

q11.

```
ORG 200 //Start address 200
    LDA BBBB // Load multiplier
    STA CTR // Store count
    LDA CTR // Load count to ac
    CMA // 1 complements the count
    INC // increment the count
    STA CTR // Store count
CLA
LOP,   LDA ZZZZ // Load value Z to AC
     ADD AAAA
     STA ZZZZ // Store Z in memory
     ISZ CTR // Increment count and if 0 skip
     BUN LOP //Repeat
     HLT //hult (stop)

CTR, DEC 0 //Count
AAAA HEX 10 //Multiplicand
ZZZZ HEX 0 //Results
BBBB HEX 50 //Multiplier
```



the code works by grabing the second number and making a duplicat from it and placing it as counter then we clear and enter the loop,
in the loop it load the number z add it to a then stores it in z and check the counter if it reachd zero to skip if not it repates, when it reaches zero it goess to hult (stop)

q12.

1. What is RISC Architectures?

   It a reduces instruction set computer that needs a lot of instructions to achieve low level operations because it uses simple commands for each clock cycle.

   What is CISC Architectures?

   it is Complex Instruction Set Computer that takes more time to execute instruction because they are made of more complex assembly language level plus the processor comes with more complex instructions that are made of huge collection of simple to complex instructions.

2. RISC Characteristics

   1- Pipeline architecture
   2- it has low number of instructions and its limited plus its decreased
   3- "Load" like instructions have the right of the entry to the memory
   4- less Addressing modes
   5- Instruction is uniform and its format can be simplified

   CISC Characteristics
   1- CISC might need more time to finish executing the code as compared with an only clock cycle.
   2- CISC It has a high level language and it was built for more simple compilations plus complex data structure.
   3- it requires less registers usually from 5 to 20 and it has more addersing nodes.
   4- For writing an application, less instruction is required
   5- for coding it need extremely small ram because code length is very short
   6- Since it is faster to design the hardware than the software, the instructions are highlighted on hardware while designing.
   7- Instructions are larger as compared with a single word.
   8- It gives simple programming within assembly language.

   Advantages RISC
   1- The performance of this processor is good because of the easy & limited no. of the instruction set.

   2- it is cheaper to build because it uses several transistors
   3- due to its simplicity the processor grants the instruction to utilize open space on a microprocessor.

   4- comparing to other processes It is very simple due to this; it is capable of finishing the task within a single clock cycle.

   Advantages CISC
   1- power usage is regulates the speed of the clock and voltage and it is created by the processor by creating procedure.

   2- a small effort is required from the processor to change the program from high level language to machine language.

   3- A single instruction can be executed by using different low-level tasks

4- It doesn’t use much memory due to a short length of code.

5- CISC utilizes less instruction set to execute the same instruction as the RISC.

6- The instruction can be stored within RAM on every CISC

3. Disadvantages RICS

1- Because the next instructions may rely on thhttps://downsub.com/e earlier instruction for their implementation inside a cycle, the performance of this processor may differ depending on the executed code.
2- Compilers and programmers regularly employ the complicated instruction.
3- These processors require highly fast memory to keep track of many instructions that demand a large amount of cache memory to respond to commands in a short amount of time.

Disadvantages CISC
1- The CISC's existing guidelines are 20 percent inside a program event.
2- When compared to RISC computers, CISC processors execute every instruction cycle on every program relatively slowly.
3- When compared to RISC, this processor uses a higher number of transistors.
4- The CISC's pipeline execution will make it tough to utilize.
Because of the slow clock, the machine's performance suffers.

Q13.

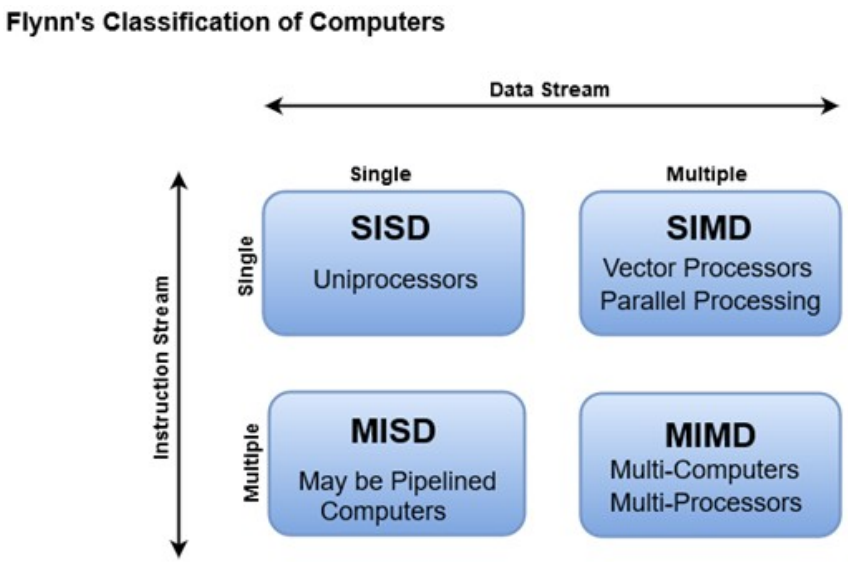
M.J. Flynn planned a classification for the organization of a knowledge processing system|ADP system|ADPS|system} by the quantity of directions and data things that area unit manipulated at the same time.

The sequence of directions scan from memory constitutes Associate in Nursing instruction stream.

The operations performed on the info within the processor represent a knowledge stream.

Flynn's classification divides computers into

1-(SISD)Single instruction stream, single data stream
2-(SIMD) Single instruction stream, multiple data stream
3-(MISD) Multiple instruction stream, single data stream
4-(MIMD) Multiple instruction stream, multiple data stream



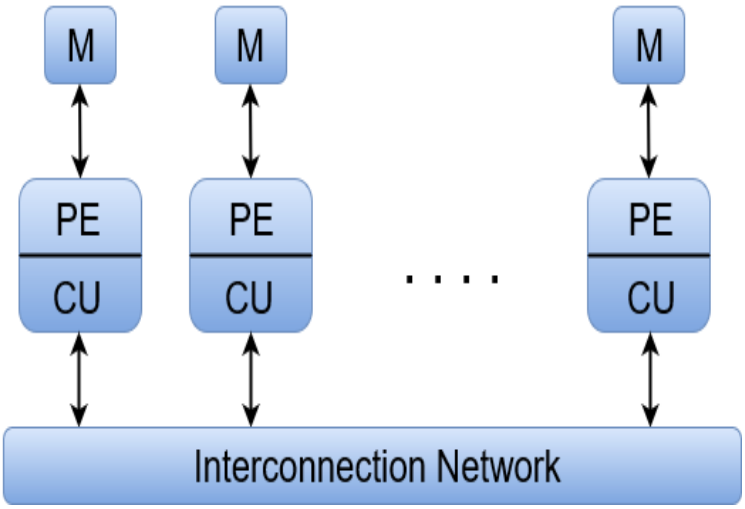
1. MIMD stands for Multiple Instruction and Multiple Data Stream.
   In this organization, all processors during a parallel pc will execute totally different directions and care for varied information at constant time.
2. Advantages

   If a tangle can be broken into isolated portions that don't need to interact much between them, parallel acceleration can be achieved. The precise definition of "much" is determined on how quickly distinct nodes interact.

   You'll be able to successfully higher I/O information measures on activities that need summarizing information (e.g., "identify the K greatest values/mean/distribution of values of the entries during this gigantic pile of data").
   /
   Each CPU will have a large amount of physical memory, as well as its own cache.

   They're arguably easier to build all you need is a high-speed network and a handful of CPU nodes in a single rack.

   In MIMD, every processor encompasses a separate program Associate in Nursingd an instruction stream is generated from every program.
   M = Memory Module
   PE = Processing Element
   CU = Control Unit **MIMD:**



3. SISD
   SISD stands for 'Single Instruction and Single information Stream'. It represents the organization of one laptop containing a bearing unit, a processor unit, and a memory unit.

   Instructions ar dead consecutive, and also the system might or might not have internal multiprocessing capabilities.

   Most standard computers have SISD design just like the ancient Von-Neumann computers.

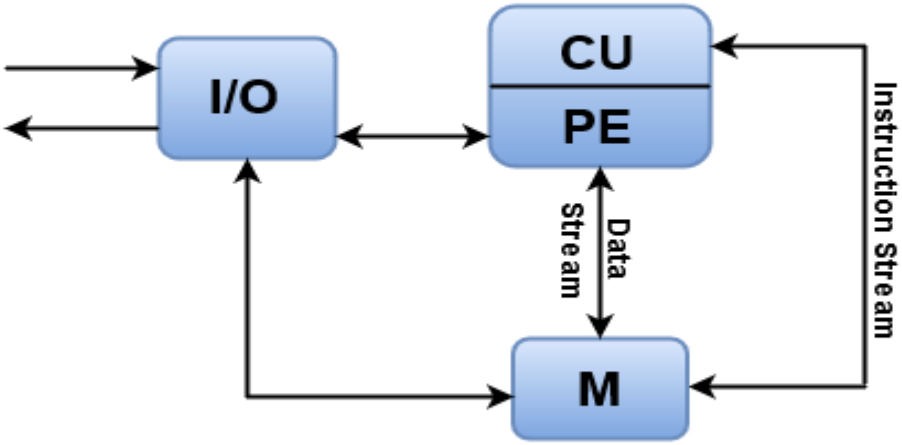
Parallel process, during this case, is also achieved
Explanation:

Instructions ar decoded by the management Unit so the management Unit sends the directions to the process units for execution.

Data Stream flows between the processors and memory bi-directionally.

SISD:

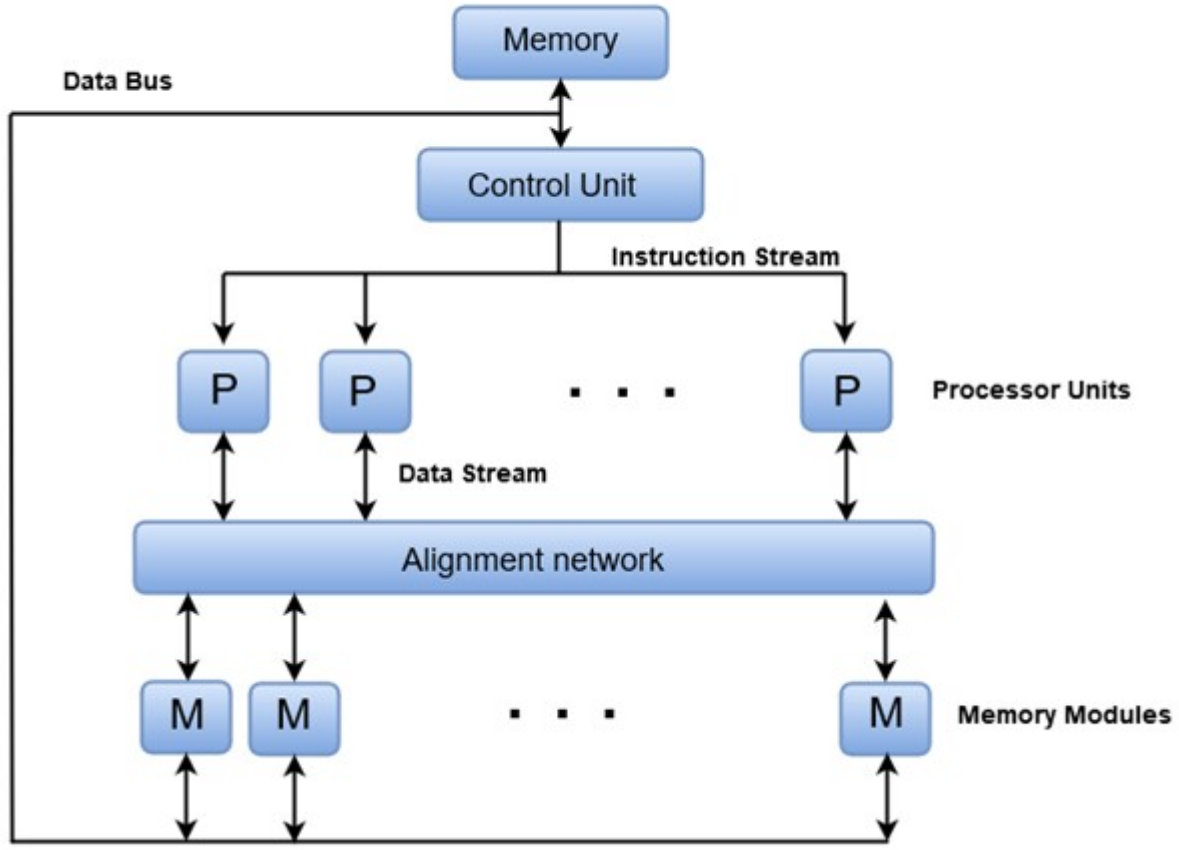
CU = Control Unit
PE = Processing Element
M = Memory



4. SIMD
SIMD stands for 'Single Instruction and Multiple information Stream'. It represents a company that has several process units below the management of a standard management unit.

All processors receive identical instruction from the management unit however care for totally different things of information.
The shared memory unit should contain multiple modules so it will communicate with all the processors at the same time.
Explanation:
SIMD is principally dedicated to array process machines. However, vector processors may be seen as a section of this cluster.

SIMD:



5.

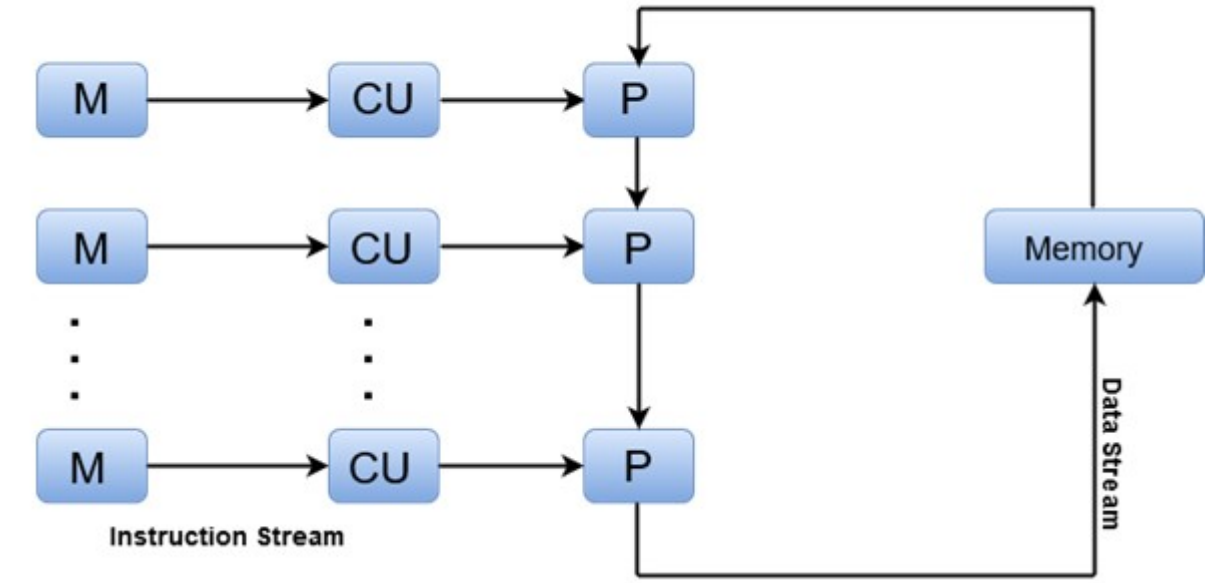
MISD
MISD stands for 'Multiple Instruction and Single information stream'.

MISD structure is barely of theoretical interest since no sensible system has been made victimisation this organization.

In MISD, multiple process units care for one single-data stream. every process unit operates on the info severally via separate instruction stream.
M = Memory Modules
CU = Control Unit

P = Processor Units

MISD:



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