FAIRCHILD SEMICONDUCTOR®

January 2009

FSEM311, FSEM311Z
Green Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanche Rugged Sense FET
- Precision Fixed Operating Frequency
- Internal Start-up Circuit
- Pulse-by-Pulse Current Limiting
- Over Voltage Protection (OVP)
- Over Load Protection (OLP)
- Internal Thermal Shutdown Function (TSD)
- Auto-Restart Mode
- Under Voltage Lockout (UVLO)
- Low Operating Current (3mA)
- Adjustable Peak Current Limit
- Built-in Soft Start

Applications

- SMPS for STB, DVD & DVCD Player
- SMPS for Auxiliary Power

Description

The FSEM311 family of integrated Pulse Width Modulator (PWM) and Sense FET are specifically designed for high performance offline Switch Mode Power Supplies (SMPS) with minimal external components. All Ex series devices are integrated high voltage power switching regulators which combine an avalanche rugged Sense FET with a current mode PWM control block. The integrated PWM controller features include: Under Voltage Lock Out (UVLO) protection, Leading Edge Blanking (LEB), an optimized gate turn-on/turn-off driver, Thermal Shut Down (TSD) protection and temperature compensated precision current sources for loop compensation and fault protection circuitry. When start up the FSEM311 offers good soft start performance. When compared to a discrete MOSFET and controller or RCC switching converter solution, the FSEM311 family devices reduce total component count, design size, weight while increasing efficiency, productivity, and system reliability. Both devices provide a basic platform that is well suited for the design of cost-effective flyback converters.

Related Resources

- *AN-4137, AN-4141, AN-4147, AN-4150 (Flyback)*

Ordering Information

Part Number	Oper. Temp.	Top Mark	Eco Status	PKG	Packing Method	BV_{DSS}	Maximum Output Power Table(1)			
							Current Limit	$R_{DS(ON)}$,MAX	230V_{AC} ± 15%(2) Open Frame(3)	85 ~ 265V_{AC} Open Frame(3)
FSEM311	-25 ~ 85°C	EM311	RoHS	8-DIP	Rail	650V	0.58A	19 Ω	13W	8W
FSEM311Z	-25 ~ 85°C	EM311Z	RoHS	8-DIP	Rail	700V	0.58A	19 Ω	13W	8W

For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Notes:
1. The junction temperature can limit the maximum output power.
2. 230V_{AC} or 100/115V_{AC} with doubler. The maximum power with CCM operation.
3. Maximum practical continuous power in an open-frame design at 50°C ambient.

Application Diagram

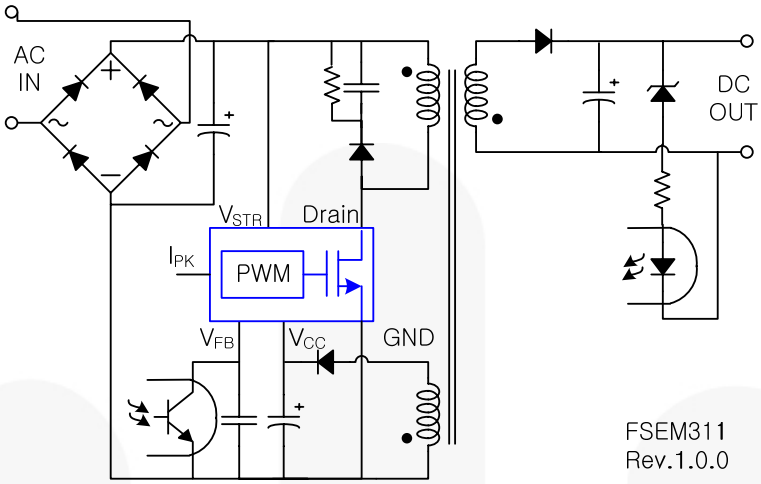

Figure 1. Typical Application

Internal Block Diagram

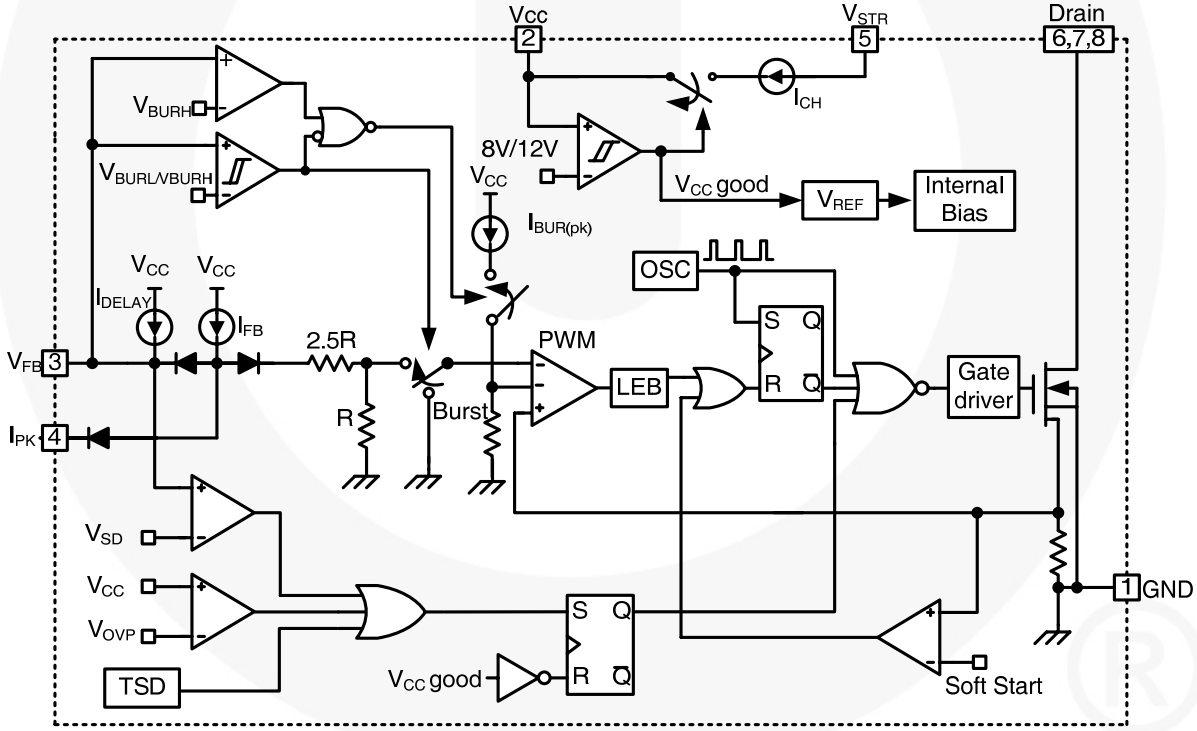

Figure 2. Internal Block Diagram

Marking Information

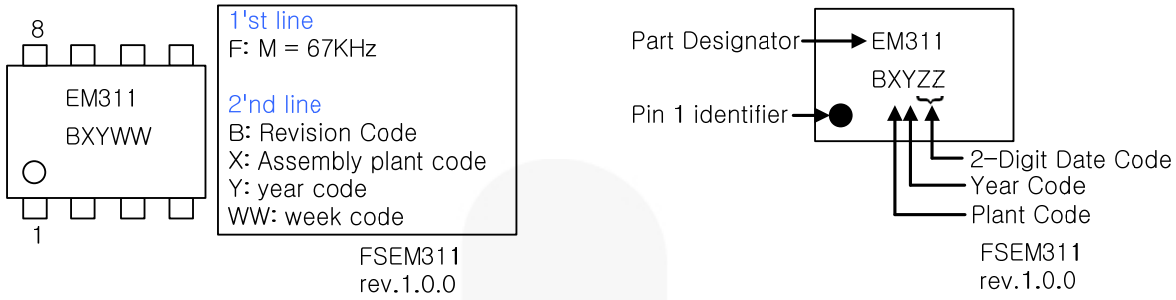

Figure 3. Top Mark

Pin Configuration

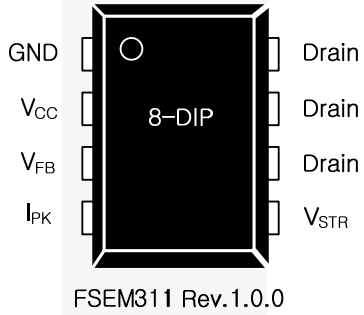

Figure 4. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	GND	**Ground.** Sense FET source terminal on primary side and internal control ground.
2	V_{CC}	**Positive supply voltage input.** Although connected to an auxiliary transformer winding, current is supplied from pin 5 (V_{STR}) via an internal switch during start-up (see Internal Block Diagram Section). It is not until V_{CC} reaches the UVLO upper threshold (12V) that the internal start-up switch opens and device power is supplied via the auxiliary transformer winding.
3	V_{FB}	**Feedback Voltage**. is the non-inverting input to the PWM comparator. It has a 0.9mA current source connected internally while a capacitor and opto-coupler are typically connected externally. There is a time delay while charging external capacitor C_{FB} from 3V to 6V using an internal 5μA current source. This time delay prevents false triggering under transient conditions but still allows the protection mechanism to operate under true overload conditions.
4	I_{PK}	**Peak Current Limit**. Adjusts the peak current limit of the Sense FET. The feedback 0.9mA current source is diverted to the parallel combination of an internal 2.8kΩ resistor and any external resistor to GND on this pin to determine the peak current limit.
5	V_{STR}	**Start up.** Is connected to the rectified AC line voltage source. At start-up the internal switch supplies internal bias and charges an external storage capacitor placed between the Vcc pin and ground. Once the Vcc reaches 12V, the internal switch is opened.
6, 7, 8	Drain	**Drain**. Are designed to connect directly to the primary lead of the transformer and are capable of switching a maximum of 650V. Minimizing the length of the trace connecting these pins to the transformer will decrease leakage inductance.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A = 25°C, unless otherwise specified.

Symbol	Parameter		Min.	Max.	Unit
V_{STR}	V_{STR} Pin Voltage		650		V
V_{DS}	Drain Pin Voltage	FSEM311	650		V
		FSEM311Z	700		
V_{CC}	Supply Voltage			20	V
V_{FB}	Feedback Voltage Range		-0.3	Internally clamped voltage(4)	V
I_{DM}	Drain Current Pulsed(5)			1.5	A
E_{AS}	Single Pulsed Avalanche Energy(6)			10	mJ
P_D	Total Power Dissipation			1.5	W
T_J	Recommended Operating Junction Temperature		-25	Internally limited	°C
T_A	Operating Ambient Temperature		-25	85	°C
T_{STG}	Storage Temperature		-55	150	°C
ESD(7)	Human Body Model, JESD 22-A114A		2		KV
	Charged Device Model, JESD 22-C101C		2		
Θ_{JA}(8) (9)	Junction-to-Ambient Thermal Resistance		80.01		°C/W
Θ_{JC}(8) (10)	Junction-to-Case Thermal Resistance		18.85		
Θ_{JT}(8) (11)	Junction-to-Top Thermal Resistance		33.70		

Notes:

4. V_{FB} is clamped by internal clamping diode(8V, I_{CLAMP_MAX} < 100μA). After shut down before V_{CC} reaching V_{STOP}, V_{SD} < V_{FB} < V_{CC}
5. Repetitive rating: Pulse width limited by maximum junction temperature.
6. L=51mH, starting T_J=25°C.
7. Meet JEDEC Standards JESD 22-A114A and JESD 22-C101C.
8. All items are tested with the standards JESD 51-2 and JESD 51-10 (DIP Package).
9. Free-standing, with no heat-sink, under natural convection.
10. Infinite cooling condition - refer to the SEMI G30-88.
11. Measured on the PKG top surface.

Electrical Characteristics

T_A = 25°C unless otherwise specified

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Units
Sense FET Section							
BV_{DSS}	Drain Source Breakdown Voltage	FSEM311	V_{CC} = 0V, I_D = 100μA	650			V
		FSEM311Z		700			
I_{DSS}	Zero Gate Voltage Drain Current		V_{DS} = 650V, V_{GS} = 0V			50	μA
			V_{DS} = 650V, V_{GS} = 0V, T_C = 125°C			200	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[12]		V_{GS} = 10V, V_{GS} = 0V, T_C = 125°C		14.0	19.0	Ω
C_{SS}	Input Capacitance		V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		162		pF
C_{OSS}	Output Capacitance		V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		18		pF
C_{RSS}	Reverse Transfer Capacitance		V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		3.8		pF
$t_{d(ON)}$	Turn-On Delay Time		V_{DD} = 350V, I_D = 25mA		9.5		nS
t_r	Rise Time		V_{DD} = 350V, I_D = 25mA		19		nS
$t_{d(off)}$	Turn-Off Delay Time		V_{DD} = 350V, I_D = 25mA		33.0		nS
t_f	Fall Time		V_{DD} = 350V, I_D = 25mA		42		nS
Control Section							
f_{OSC}	Switching Frequency		V_{DS} = 650V, V_{GS} = 0V	61	67	73	KHz
Δf_{OSC}	Switching Frequency Variation[13]		-25°C < T_J < 85°C		±5	±10	%
D_{MAX}	Maximum Duty Cycle		V_{FB} = 4V	71	77	83	%
D_{MIN}	Minimum Duty Cycle		V_{FB} = 0V	0	0	0	%
V_{START}	UVLO Threshold Voltage			11	12	13	V
V_{STOP}			After turn on	7	8	9	V
I_{FB}	Feedback Source Current		V_{FB} = 0V	700	900	1100	μA
$t_{S/S}$	Internal Soft Start Time		V_{FB} = 4V	10	15	20	ms
Burst Mode Section							
V_{BURH}	Burst-Mode High Threshold Voltage			0.4	0.5	0.6	V
V_{BURL}	Burst-Mode Low Threshold Voltage			0.25	0.35	0.45	
Protection Section							
I_{LIM}	Peak Current Limit		T_J = 25°C, di/dt = 90mA/μsec	0.51	0.58	0.65	A
t_{CLD}	Current Limit Delay Time[13]			200			ns
V_{SD}	Shutdown Feedback Voltage			5.5	6.0	6.5	V
I_{DELAY}	Shutdown Delay Current		V_{FB} = 4V	3.5	5.0	6.5	μA
t_{LEB}	Leading-Edge Blanking Time[13]			200			ns
V_{OVP}	Over Voltage Protection			18	19	-	V
TSD	Thermal Shutdown Temperature[13]			125	140	155	°C
Total Device Section							
I_{OP}	Operating Supply Current (Control Part Only)		V_{CC} = 14V	1	3	5	mA
I_{CH}	Start-up Charging Current		V_{CC} = 0V	0.70	0.85	1.00	mA
V_{STR}	Minimum V_{STR} Supply Voltage		V_{CC} = 0V	35	-	-`	V

Notes:

12. Pulse test: Pulse width=300ms, duty=2%
13. Though guaranteed, it is not 100% tested in the mass production.

Typical Performance Characteristics

These characteristic graphs are normalized at T_A= 25°C

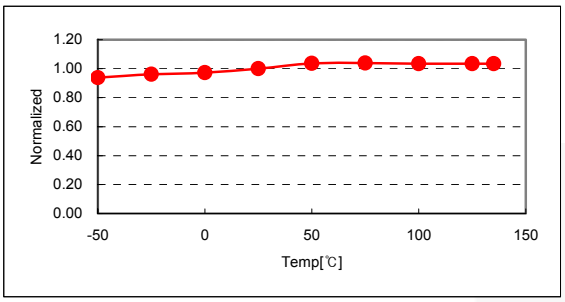

Figure 5. Operating Frequency (F_{OSC}) vs. T_A

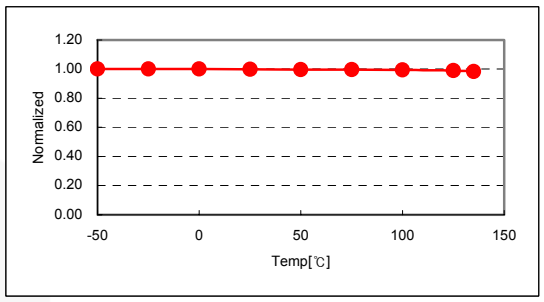

Figure 6. Maximum Duty Cycle (D_{MAX}) vs. T_A

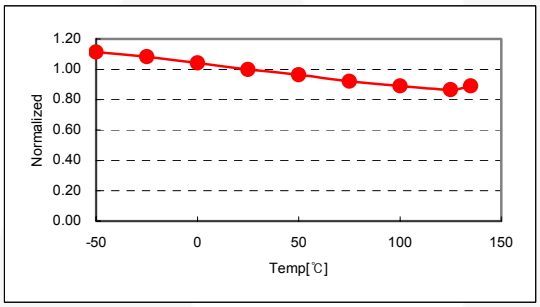

Figure 7. Operating Supply Current(I_{OP}) vs. T_A

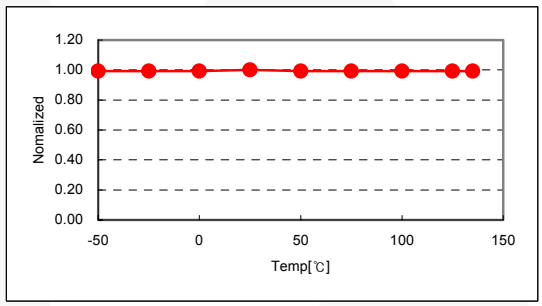

Figure 8. Start Threshold Voltage (V_{START}) vs. T_A

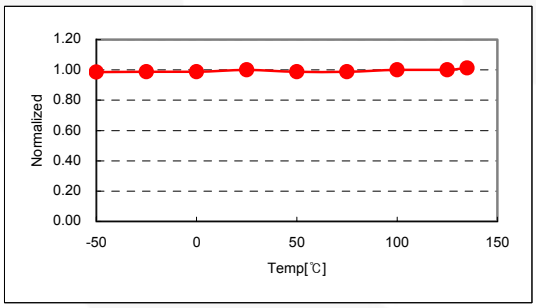

Figure 9. Stop Threshold Voltage (V_{STOP}) vs. T_A

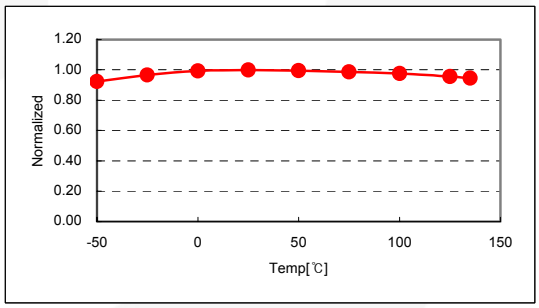

Figure 10. Feedback Source Current (I_{FB}) vs. T_A

Typical Performance Characteristics (continued)

These characteristic graphs are normalized at T_A= 25°C

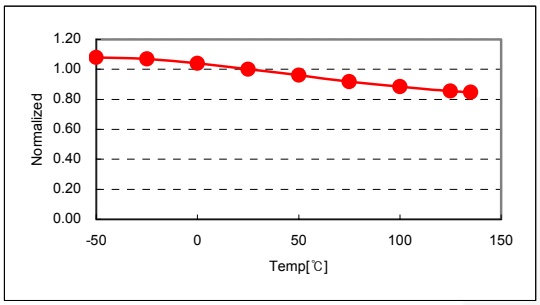

Figure 11. Start Up Charging Current (I_{CH}) vs. T_A

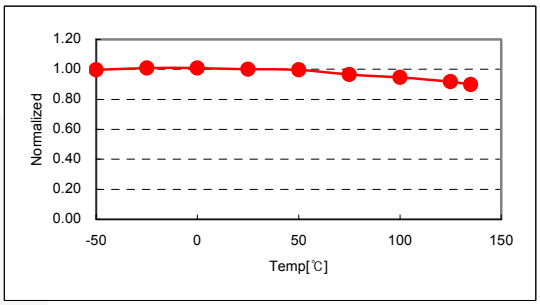

Figure 12. Peak Current Limit (I_{LIM}) vs. T_A

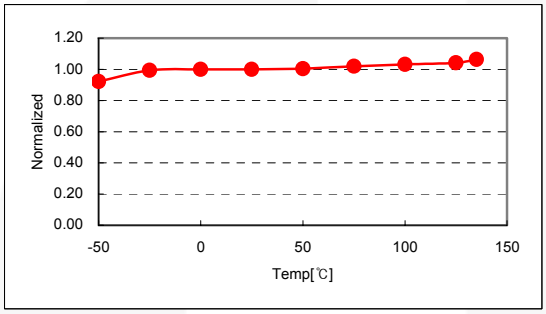

Figure 13. Operating Supply Current(I_{OP}) vs. T_A

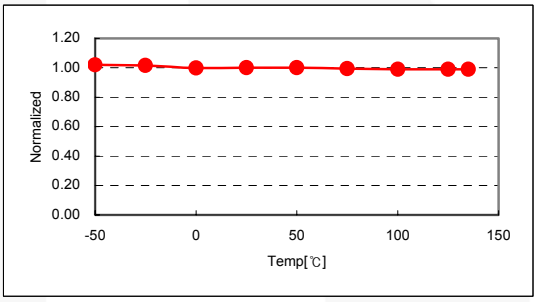

Figure 14. Start Threshold Voltage (V_{START}) vs. T_A

Functional Description

1. Start-up: In early generations of Fairchild Power Switches (FPS™) the V_{STR} pin had an external resistor to the DC input voltage line. In this generation the startup resistor is replaced by an internal high voltage current source and a switch that shuts off when 15ms goes by after the supply voltage, V_{CC}, gets above 12V. The source turns back on if V_{CC} drops below 8V.

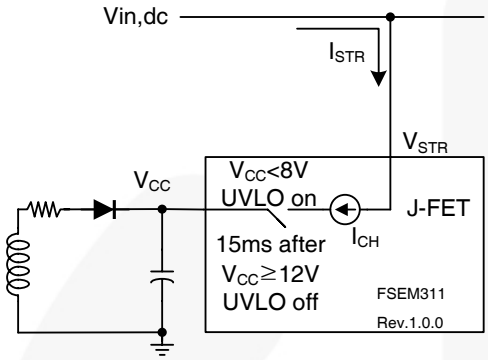

Figure 15. Start up Circuit

2. Feedback Control: The FSEM311 employs current mode control, as shown in Figure 16. An opto-coupler (such as the H11A817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{SENSE} resistor plus an offset voltage makes it possible to control the switching duty cycle. When the KA431 reference pin voltage exceeds the internal reference voltage of 2.5V, the opto-coupler LED current increases, the feedback voltage V_{FB} is pulled down and it reduces the duty cycle. This event typically happens when the input voltage is increased or the output load is decreased.

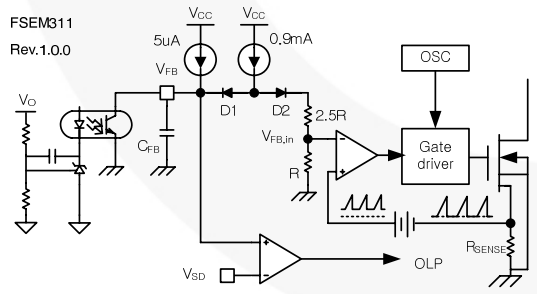

Figure 16. Pulse-Width-Modulation (PWM) Circuit

3. Leading Edge Blanking (LEB) : At the instant the internal Sense FET is turned on, the primary side capacitance and secondary side rectifier diode reverse recovery typically cause a high current spike through the Sense FET. Excessive voltage across the R_{SENSE} resistor leads to incorrect feedback operation in the current mode PWM control. To counter this effect, the FPS employs a leading edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (t_{LEB}) after the Sense FET is turned on.

4. Protection Circuits: The FPS has several protective functions such as over load protection (OLP), over voltage protection (OVP), under voltage lock out (UVLO) and thermal shutdown (TSD). Because these protection circuits are fully integrated inside the IC without external components, the reliability is improved without increasing cost. Once a fault condition occurs, switching is terminated and the Sense FET remains off. This causes V_{CC} to fall. When V_{CC} reaches the UVLO stop voltage V_{STOP} (8V), the protection is reset and the internal high voltage current source charges the V_{CC} capacitor via the V_{STR} pin. When V_{CC} reaches the UVLO start voltage V_{START} (12V), the FPS resumes its normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power Sense FET until the fault condition is eliminated.

4.1 Over Load Protection (OLP): Overload is defined as the load current exceeding a pre-set level due to an unexpected event. In this situation, the protection circuit should be activated in order to protect the SMPS. However, even when the SMPS is operating normally, the over load protection (OLP) circuit can be activated during the load transition. In order to avoid this undesired operation, the OLP circuit is designed to be activated after a specified time to determine whether it is a transient situation or an overload situation. In conjunction with the I_{PK} current limit pin (if used) the current mode feedback path would limit the current in the Sense FET when the maximum PWM duty cycle is attained. If the output consumes more than this maximum power, the output voltage (V_O) decreases below its rating voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 3V, the feedback input diode is blocked and the 5μA current source (I_{DELAY}) starts to charge C_{FB} slowly up to Vcc. In this condition, V_{FB} increases until it reaches 6V, when the switching operation is terminated as shown in Figure 17. The shutdown delay time is the time required to charge C_{FB} from 3V to 6V with 5μA current source.

4.2 Thermal Shutdown (TSD): The Sense FET and the control IC are integrated, making it easier for the control IC to detect the temperature of the Sense FET. When the temperature exceeds approximately 140°C, thermal shutdown is activated.

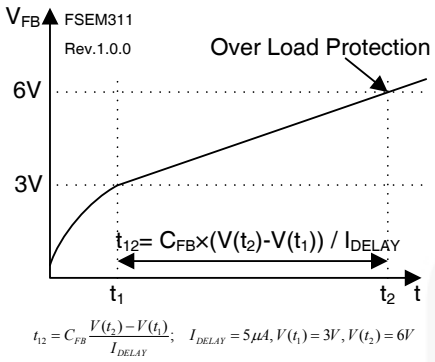

Figure 17. Over Load Protection (OLP)

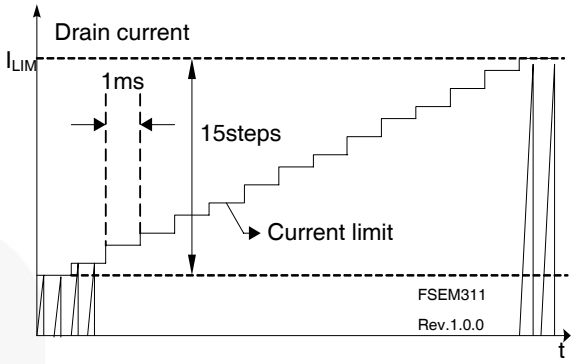

Figure 18. Pulse-Width-Modulation (PWM) Circuit

4.3 Over Voltage Protection (OVP): In the event of a malfunction in the secondary side feedback circuit, or an open feedback loop caused by a soldering defect, the current through the opto-coupler transistor becomes almost zero (refer to Figure 16). Then, V_{FB} climbs up in a similar manner to the over load situation, forcing the preset maximum current to be supplied to the SMPS until the over load protection is activated. Because excess energy is provided to the output, the output voltage may exceed the rated voltage before the over load protection is activated, resulting in the breakdown of the devices in the secondary side. In order to prevent this situation, an over voltage protection (OVP) circuit is employed. In general, Vcc is proportional to the output voltage and the FPS uses V_{CC} instead of directly monitoring the output voltage. If V_{CC} exceeds 19V, OVP circuit is activated resulting in termination of the switching operation. In order to avoid undesired activation of OVP during normal operation, V_{CC} should be properly designed to be below 19V.

5. Soft Start: The FPS has an internal soft start circuit that slowly increases the feedback voltage together with the Sense FET current after it starts up. The typical soft start time is 15msec, as shown in Figure 18, where progressive increments of the Sense FET current are allowed during the start-up phase. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. It also helps to prevent transformer saturation and reduce the stress on the secondary diode.

6. Burst Operation: In order to minimize power dissipation in standby mode, the FPS enters burst mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 19, the device automatically enters burst mode when the feedback voltage drops below V_{BURH}. Switching still continues but the current limit is set to a fixed limit internally to minimize flux density in the transformer. The fixed current limit is larger than that defined by V_{FB} = V_{BURH} and therefore, V_{FB} is driven down further. Switching continues until the feedback voltage drops below V_{BURL}. At this point switching stops and the output voltages start to drop at a rate dependent on the standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH}, switching resumes. The feedback voltage then falls and the process repeats. Burst mode operation alternately enables and disables switching of the Sense FET and reduces switching loss in Standby mode.

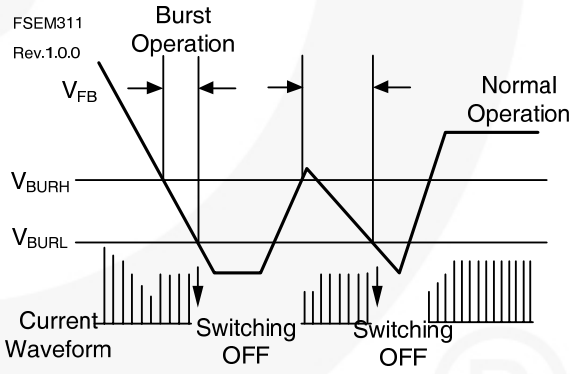

Figure 19. Burst Operation

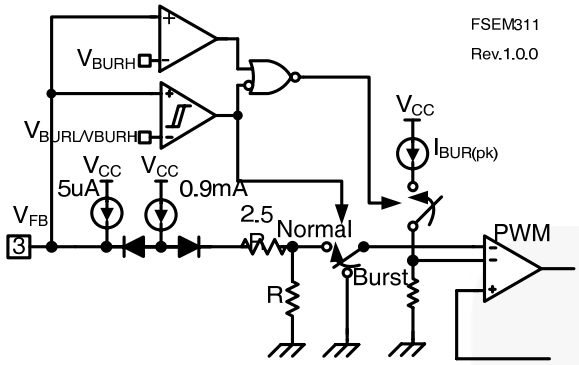

Figure 20. Burst Operation Function

7. Adjusting Peak Current Limit: As shown in Figure 21, a combined 2.8kΩ internal resistance is connected to the non-inverting lead on the PWM comparator. An external resistance of Rx on the current limit pin forms a parallel resistance with the 2.8kΩ when the internal diodes are biased by the main current source of 900μA

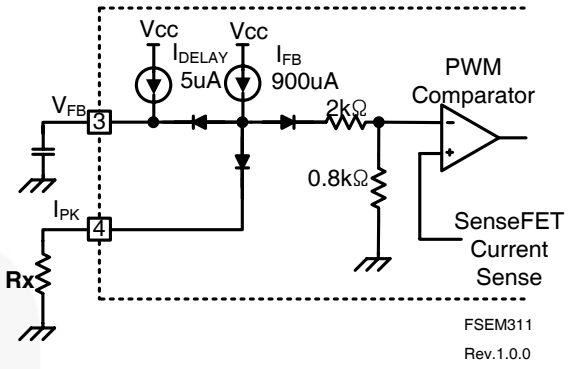

Figure 21. Peak Current Limit Adjustment

For example, FSEM311 has a typical Sense FET peak current limit (I_{LIM}) of 0.58A. I_{LIM} can be adjusted to 0.4A by inserting Rx between the I_{PK} pin and the ground. The value of the Rx can be estimated by the following equations:

$$0.58A : 0.4A = 2.8k\Omega : Xk\Omega \quad (1)$$

$$X = Rx \parallel 2.8k\Omega \quad (2)$$

(X represents the resistance of the parallel network)

Applications Information

1. About Audible Noise

Switching mode power converters have electronic and magnetic components, which generate audible noises when the operating frequency is in the range of 20~20,000 Hz. Even though they operate above 20 kHz, they can make noise depending on the load condition. Designers can employ several methods to reduce these noises. Here are three of these methods:

Glue or Varnish

The most common method involves using glue or varnish to tighten magnetic components. The motion of core, bobbin and coil and the chattering or magnetostriction of core can cause the transformer to produce audible noise. The use of rigid glue and varnish helps reducing the transformer noise. But, it also can crack the core. This is because sudden changes in the ambient temperature cause the core and the glue to expand or shrink in a different ratio according to the temperature.

Ceramic Capacitor

Using a film capacitor instead of a ceramic capacitor as a snubber capacitor is another noise reduction solution. Some dielectric materials show a piezoelectric effect depending on the electric field intensity. Hence, a snubber capacitor becomes one of the most significant sources of audible noise. It is considerable to use a zener clamp circuit instead of an RCD snubber for higher efficiency as well as lower audible noise.

Adjusting Sound Frequency

Moving the fundamental frequency of noise out of 2~4 kHz range is the third method. Generally, humans are more sensitive to noise in the range of 2~4 kHz. When the fundamental frequency of noise is located in this range, one perceives the noise as louder although the noise intensity level is identical. Refer to Figure 22.Equal Loudness Curves.

When FPS acts in Burst mode and the Burst operation is suspected to be a source of noise, this method may be helpful. If the frequency of Burst mode operation lies in the range of 2~4 kHz, adjusting feedback loop can shift the Burst operation frequency. In order to reduce the Burst operation frequency, increase a feedback gain capacitor (CF), opto-coupler supply resistor (RD) and feedback capacitor (CB) and decrease a feedback gain resistor (RF) as shown in Figure 23.Typical Feedback Network of FPS.

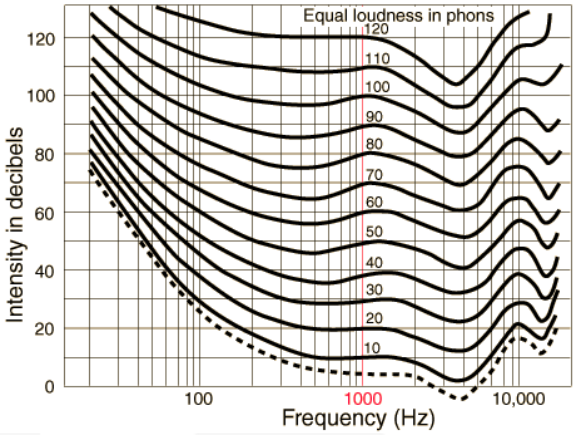

Figure 22. Equal Loudness Curves

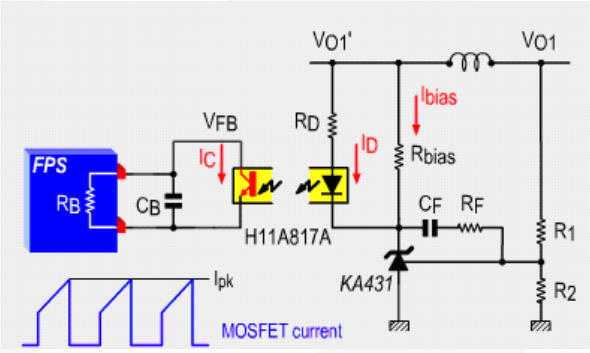

Figure 23. Typical Feedback Circuit

2. Other Reference Materials

AN-4134: Design Guidelines for Off-line Forward Converters Using Fairchild Power Switch (FPS™)

AN-4137: Design Guidelines for Off-line Flyback Converters Using Fairchild Power Switch (FPS)

AN-4140: Transformer Design Consideration for Off-line Flyback Converters using Fairchild Power Switch (FPS™)

AN-4141: Troubleshooting and Design Tips for Fairchild Power Switch (FPS™) Flyback Applications

AN-4147: Design Guidelines for RCD Snubber of Flyback

AN-4148: Audible Noise Reduction Techniques for FPS Applications

Physical Dimensions

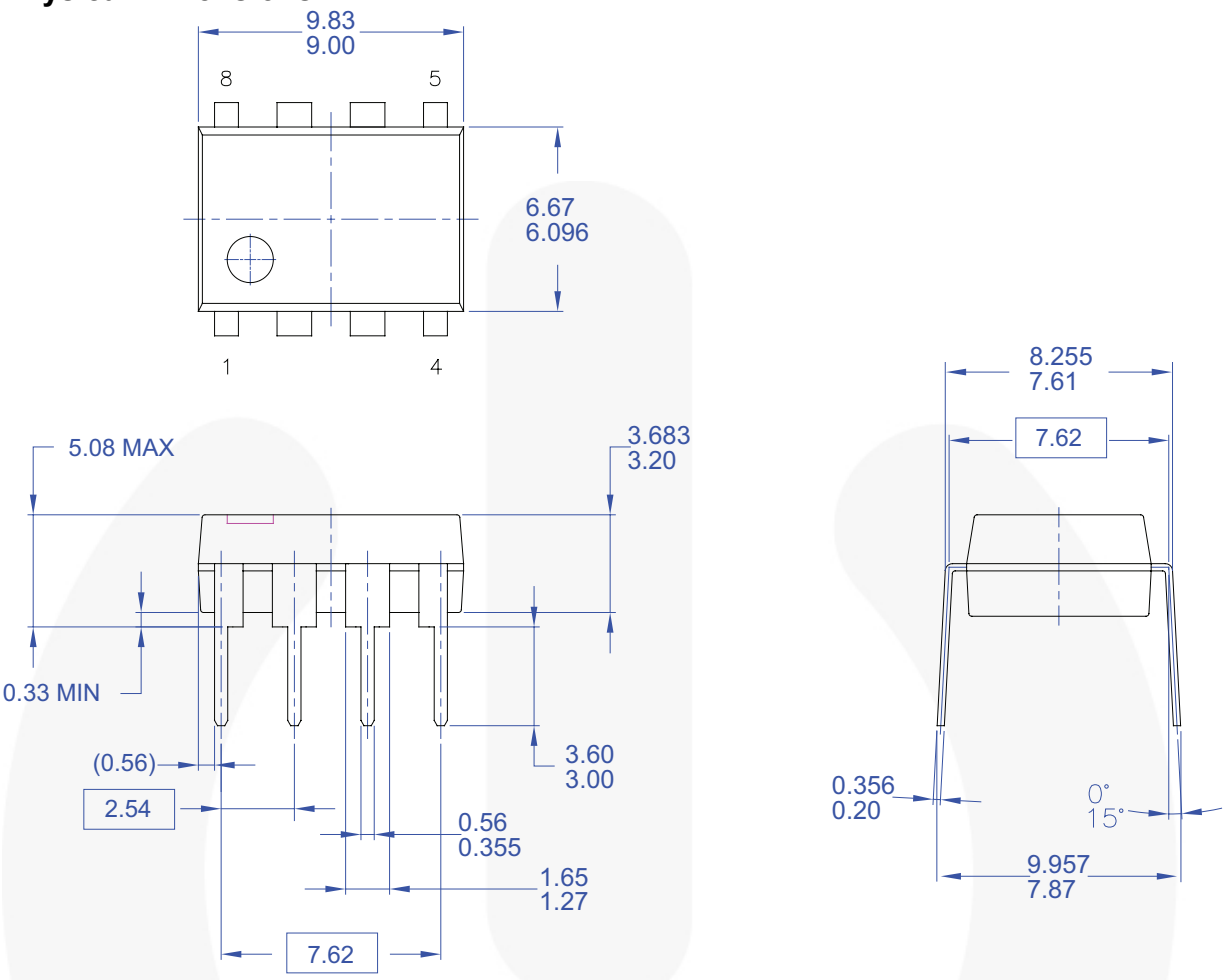

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Figure 24. 8-Lead, Dual In-Line Package(DIP)

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