Laboratory 5: MOSFETs and BJTs, DC Characteristics

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***Abstract*—This investigation focuses on the electrical characteristics of MOSFETs and BJTs, addressing the effects of temperature and gate/base voltage on their performance. The experiments involved curve tracing, transconductance calculations, and small-signal modeling, as well as temperature manipulation through heating and cooling. The results show that temperature influences the threshold voltage and carrier mobility in MOSFETs and the base-emitter voltage in BJTs, which subsequently affect their electrical characteristics. Data was extrapolated by way of MATLAB.**

***Index Terms*—MOSFET, BJT, temperature, electrical characteristics, curve tracer, transconductance, small-signal model, Elvis-II+, MATLAB**

I. Introduction

The performance of semiconductor devices, such as MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) and BJTs (Bipolar Junction Transistors), is greatly influenced by various factors, including temperature and applied voltage. Understanding these dependencies is crucial for designing and optimizing electronic circuits. This investigation presents a series of laboratory experiments that investigate the temperature dependence and gate/base voltage impact on the electrical characteristics of firstly MOSFETs and then BJTs.

II. Methodology and Analysis

A. MOSFET i-v Characteristics Using a Curve Tracer

Within this part of the investigation, we take under examination one of the NMOS Transistors on the CD 4007 IC. And so, we constructed the circuit seen in figure 1; with the pin configuration of CD 4007 IC such that the NMOS is being utilized. Once we constructed the circuit, we commenced to connect the drain terminal to the function generator, connect the wiper of a 10-kW potentiometer to the gate terminal operating with 5 V across its main terminals, and connect the source terminal to ground as shown in the figure. We then set the function generator feature to generate a triangular waveform over a 0 V to 10 V signal range.

Using varying gate voltages, we performed analysis of the component over a sweep from 0V to 10 V. It is noted that when we set the gate voltage to 2 V, which is the threshold voltage value according to the manufacturing manual of the CD 4007 IC device, we also measured a threshold value of 2.3172 as seen in figure 2. Further, the oscilloscope plot of this run of the configuration can be found in appendix A. This value matches the expected value from the aforementioned manual,

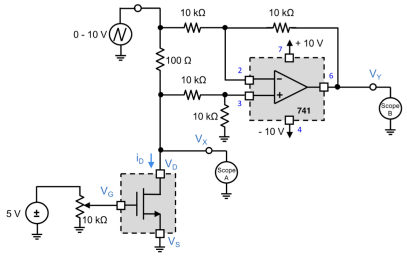

Fig. 1. Curve-Trace Set-Up for Measuring the NMOS Transistor I-V Characteristic

with slight variation which we assume is due to electric noise [1]. It is noted that an LTSpice simulation was conducted in order to examine the theoretical behaviour, which matches our results. LTSpice plots can be found in appendix B.

Fig. 2. Threshold Voltage Reading

Then, by running a series of tests with varying gate voltages of 0, 2.82, 3.3, 3.8, 4.3 and 4.8 Volts; we were able to arrive at the I-V characteristic of the transistor when exposed to different gate voltages. As seen in figure 3, when the gate voltage applied to the transistor is 0 V, the drain current remains close to 0, with some minimal noise. We also see the drain current increase proportionally to the gate voltage which follows from theory as a positive gate voltage in an NMOS transistor forms an n-type channel, enabling current flow between the source and drain. This current flow induced by the voltage applied is then proportional to that voltage being applied. It is noted that the capabilities of the ELVIS-II does not allow to capture plots to complete the highest two readings.

We then chose a midpoint within the active region of the transistors using the runs of the 2.82 V, 3.3 V and 3.8 V. Then, by way of MATLAB, we calculated the slope of the given plots and extrapolated the points to extend a straight line to the x intercept. The derivation can be seen in figure 4. Using these x axis intercepts, we can arrive at the effective early voltage of the transistor at each gate voltage level. Then,

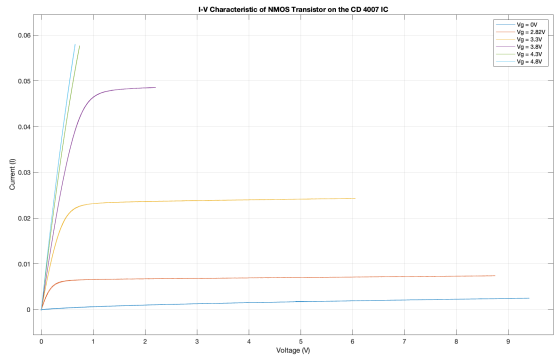

Fig. 3. I-V Characteristic of NMOS Transistor on CD 4007 IC, Across Varying Gate Voltages

by calculating the average of these values, we can arrive at an estimate for the effective early voltage of the transistor, which is the measure of the output impedance of a MOSFET when it is operating in the saturation region [1]. As seen from the plot, we arrive at intercepts at -18.889 V, -62.375 V and -109.596 V, leading to an effective early voltage of 63.62 V.

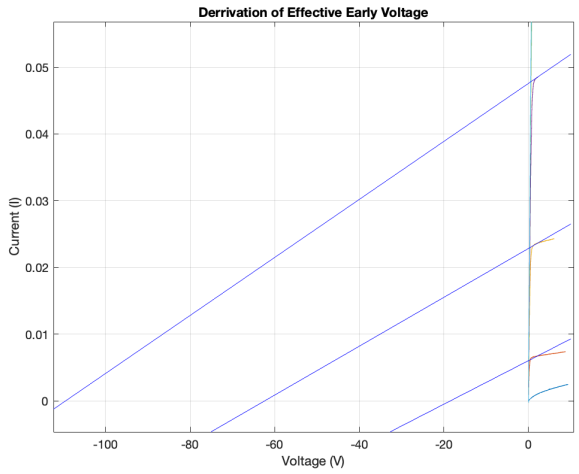

Fig. 4. Derivation of Effective Early Voltage

Within the next test of the laboratory, we were tasked with computing the transconductance of the device under examination according to the formula in figure 5. To do this, we set the drain voltage to 5 V, then measured the gate voltage and drain current using our setup at two different gate voltages; 3 V and 3.1 V. It is noted that the input signal was modified to a DC variable voltage source. For the gate voltages of 3.0928 V and 2.8863 V, we measured a drain current of 0.03925 A and 0.02391 A respectively. This allowed us to arrive at 74.286 mS as the transconductance of our device, which further follows from general theory. Further, we composed the small signal model of our MOSFET under examination for low frequency operation as seen in figure 6. Within this model, Vgs is the gate voltage at that specific instance of the run, gm is the transconductance calculated earlier, and r0 can be extracted by multiplying the reciprocal of the effective early voltage by the reciprocal of the drain current [1]. The formula for which can be found in appendix B.

$$g_m = \frac{\Delta i_D}{\Delta v_{GS}}$$

Fig. 5. Trans-conductance Formula

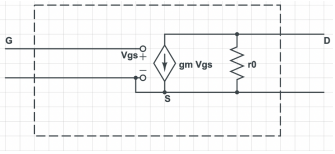

Fig. 6. Small Signal Model of MOSFET for Low Frequency Operation

B. MOSFET Temperature Effects

By using the same setup as the preceding part, we ran the same triangular wave across our setup, however, with each instance of the run, a heat gun or freeze spray was used to cool or heat the transistor, to obtain results across varying temperatures. As seen from figure 7, the plot of the varying temperature heavily effects the performance of the device under examination. At different temperatures, we see the curves shifting. As temperatures increase the curve shifts to the right and conversely, as the temperature decreases, the threshold voltage increases, and the iD-vDS curves shift to the left. Further, the lower the temperature, the higher the curve is shifted upwards within the plot. This follows from theory as when temperature changes, the threshold voltage and carrier mobility in the channel are impacted, shifting the iD-vDS curves. When temperature increases, the threshold voltage decreases, and the curves shift right/downwards; when temperature decreases, the threshold voltage increases, and the curves shift left/upwards.

It is gathered then by theory that as temperature increases, the number of charge carriers in the semiconductor material (intrinsic carrier concentration) also increases. This causes the internal electric potential difference (built-in potential) within the pn junctions to decrease. Consequently, the gate voltage needed for the MOSFET to turn on (threshold voltage) also decreases. And on the other hand, when the temperature is reduced, the number of charge carriers in the semiconductor are reduced, which causes the internal potential to increase and in turn results in a higher threshold voltage [1]. To minimize temperature-related changes in MOSFET behavior, we can choose temperature-stable components, select MOSFETs with lower temperature sensitivity, or implement temperature control mechanisms like heatsinks and cooling fans for stable temperatures.

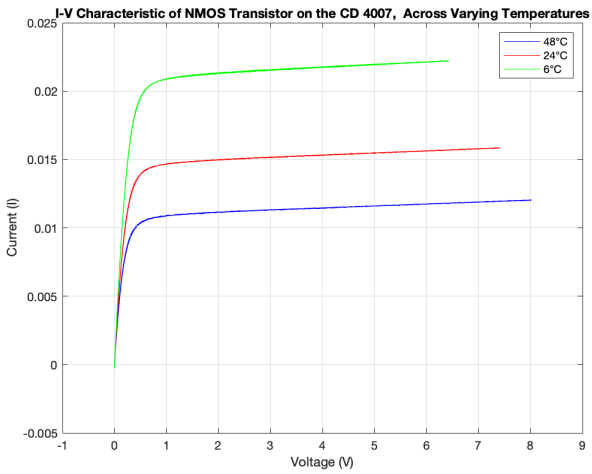

Fig. 7. Temperature Effects on NMOS Transistor

C. BJT i-v Characteristics Using a Curve Tracer

In this part of your laboratory we investigated the iC-vCE characteristics of the 2N2222A npn transistor. Using the same curve-tracer circuit setup we have been using, we placed the BJT into the test port to arrive at the circuit in figure 8. We then set the base voltage using the 10-kW potentiometer so that it is 0 V, and ran the same triangular wave discussed in the preceding part. We repeated this for variable base voltage values ranging from 0 mV to 750 mV in order to examine the device under testing, the BJT. This resulted in 15 different I-V characteristics, each for a different base voltage. As these results vary in magnitude, we have opted to display the results using two plots for visibility, figure 9 and 10. As seen from the figure the drain current of the device increases as we increase the gate voltage. In this case also we can observe through the plots that the base-emitter junction voltage is around 0.65, the point at which nearly all of the plots start to spike as the device turns on. It is noted that an LTSpice simulation was conducted in order to examine the theoretical behaviour, which matches our results. LTSpice plots can be found in appendix B.

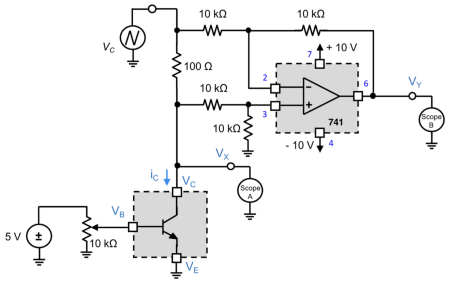

Fig. 8. Curve-Trace Set-Up for Measuring the BJT I-V Characteristic

We then commenced to derive the effective early voltage of the device. To do this, we followed a similar set of steps as part 1 of the laboratory. By calculating the slope of each plateau and extrapolating a line till the x intercept of each respective

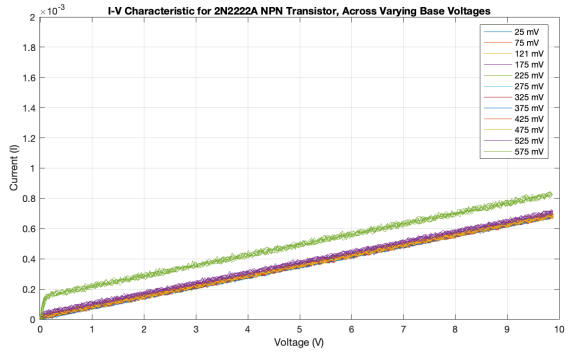

Fig. 9. I-V Characteristic of BJT, Across Varying Gate Voltages, 1

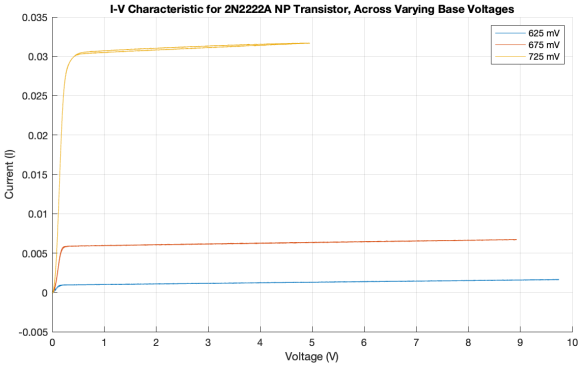

Fig. 10. I-V Characteristic of BJT, Across Varying Gate Voltages, 2

plot. This derivation can be found in figure 11. Then, using these x intercepts, we calculated an average which signifies an estimated effective early voltage. This value we arrived at is an average of the highest 13 readings, this is to avoid difficult readings or readings that represent the unactive region. We have come to find that the estimated effective early voltage of the 2N2222A npn transistor is 14.457 V.

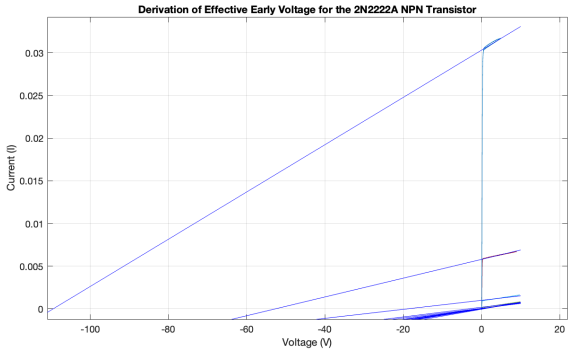

Fig. 11. Effective Early Voltage Derivation, BJT

Now, in order to arrive at the transconductance of the device, we must repeat a similar procedure to what we did in part 1 of the laboratory. This is done by setting the base voltage to 650 mV and the collector voltage to 5 V. This required that the

triangular signal source be replaced with a DC programmable source. Once completed, we measured the base voltage and collector current. We then repeated this for a base voltage of 700 mV in order to collect two sets of readings to use for our calculation of the transconductance. Using the formula in figure 12, we arrived at a transconductance of 193.91 mS. Further, by way of theory, we were able to arrive at the equivalent small-signal model of the BJT for low-frequency operation as seen in figure 13.

$$g_m = \frac{\Delta i_C}{\Delta v_{BE}}$$

Fig. 12. Trans-conductance Formula, BJT

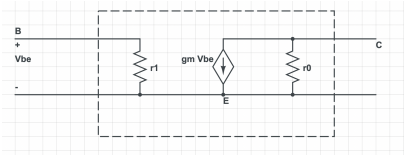

Fig. 13. Small Signal Model of BJT for Low Frequency Operation (Hybrid-Pi Model)

D. BJT Temperature Effects

We then commenced to complete temperature analysis upon the 2N2222A npn transistor. In a similar fashion to that of part 2, we heated and cooled the transistor in order to arrive at I-V characteristic plots of varying temperature. And so, we reconnected the triangular wave in order to arrive at the plots in figure 14. As seen from the plot; as temperature varies, it impacts the BJT's base-emitter voltage, which in turn affects the iC-vCE characteristics. With increasing temperature, the base-emitter voltage usually decreases due to a rise in intrinsic carrier concentration, leading to upward-shifting iC-vCE curves. On the other hand, decreasing temperature results in an increased base-emitter voltage, causing the iC-vCE curves to shift downward.

III. Conclusion

This investigation provided valuable insights into the effects of temperature and gate/base voltage on the electrical characteristics of MOSFETs and BJTs. It was observed that temperature changes significantly impact the performance of both of these devices. For MOSFETs, increasing temperature led to a decrease in threshold voltage, while for BJTs, it led to a decrease in base-emitter voltage. These effects were attributed to the temperature-dependent intrinsic carrier concentration in the semiconductor material. By understanding these dependencies, designers can better select appropriate components, optimize circuit performance, and implement temperature control mechanisms to ensure stable operation in various applications. This ensures familiarization of digital circuits under varying performance conditions and serves as a solid understanding of how these mechanisms work.

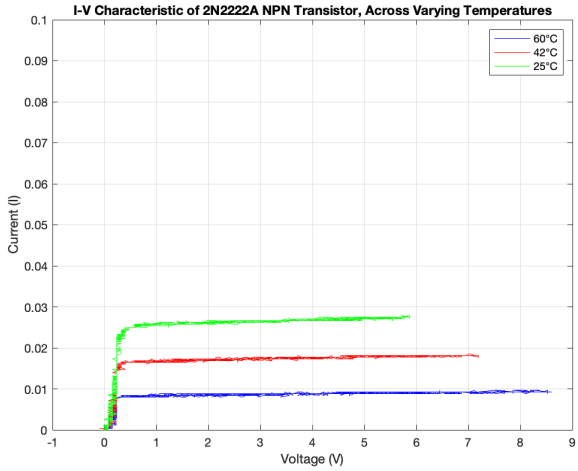

Fig. 14. Temperature Effects on BJT Device

IV. References

[1] A. S. Sedra and K. C. Smith, Microelectronic Circuits, 8th ed. Oxford University Press, 2019.

Appendix A:

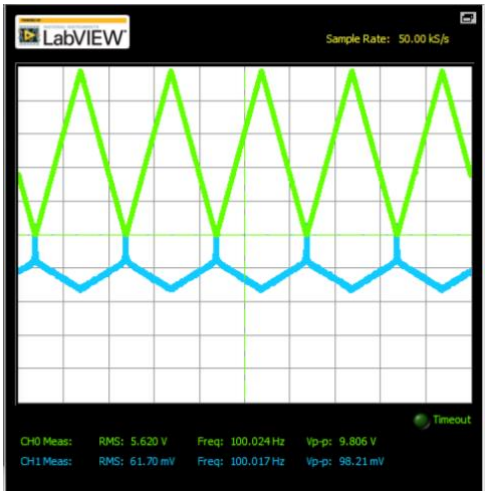

Figure 1 – Threshold Voltage on NMOS

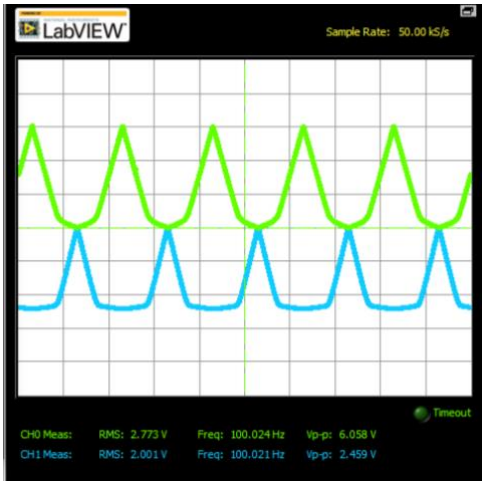

Figure 2 – 3.3 V Gate Voltage on NMOS

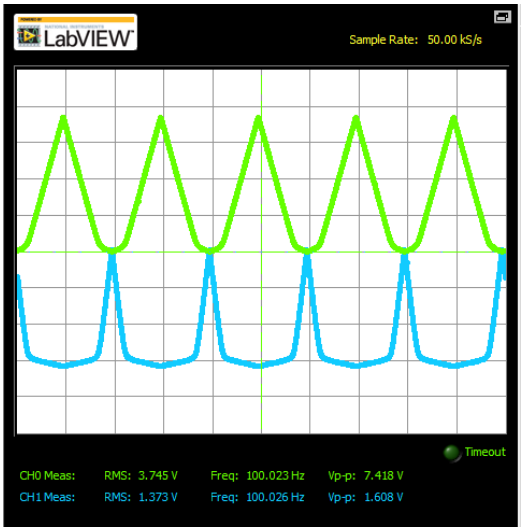

Figure 3 – Base Voltage of 700mV on BJT

Appendix B:

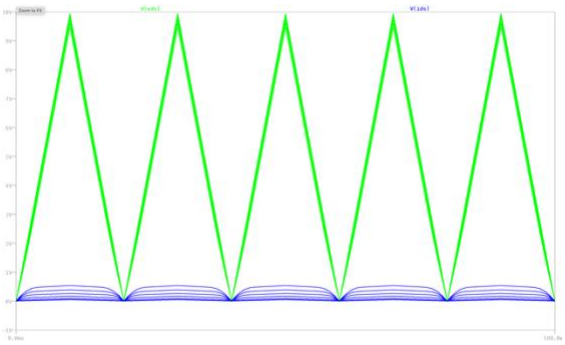

Figure 1 – MOSFET Scope Plot, LTSpice

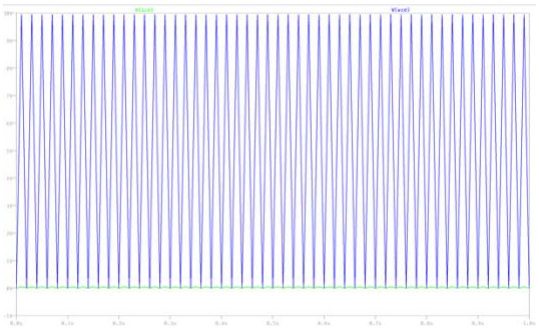

Figure 2 – BJT Scope Plot, LTSpice

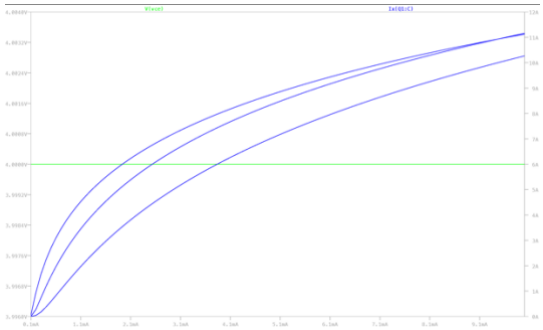

Figure 3 – BJT i-v Characteristic for Varying Temperature, LTSpice

$$\frac{1}{r_O} = \left[\frac{\partial i_D}{\partial v_{DS}}\right]_{v_{GS}\ \text{constant}} \approx \lambda I_D = \frac{I_D}{V_A}$$

Figure 4 – r0 Formula from Sedra and Smith