Zagazig University
Faculty of Engineering
Second term -3rd year
Computer & Sys. Dept.

Extended Bipolar RAM Design Using DM 7489

1- Objective:

1.1 Quick introduction to Proteus.

- basic window and elements
- method to select required components and right connection

1.2 Explain how to generate large dynamic memory from DM7489 using Proteus simulator.

1.3 Design the simulated circuit in test-board.

2- Requirements:

- **S/W Requirements:**

  2.1 Proteus 6 or higher

  2.2 Windows O.S.

- **H/W Requirements:**

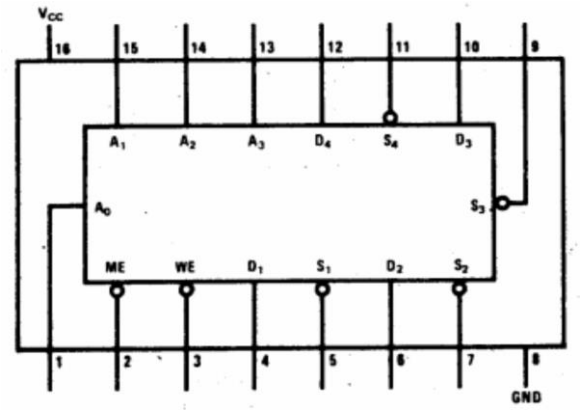
Device or component	**Description**
DM 7489	16X4 bits RAM
7 seg-BCD	7 segments BCD display
Thumb-switch	Switch with 4 bits outputs
Logic state (0,1) – voltage source	Two level voltage source (5,0) v.
7404	inverter
74139	2X4 decoder

3- Introduction

DM7489 is a dynamic bipolar random access memory that is fully decoded 64-bits. It is organized as 16X4-bit words. The memory is addressed by applying a binary number to the four address inputs. After addressing information may be either written into or read from memory which is controlled by memory enable and write enable control bits. To write, both memory enable and write enable inputs must be in the logical "0" state. Information applied to the four write inputs will then be written into the address location. To read information from the memory, the memory enable inputs must be in the logical "0" state and the write enable input must be in the logical "1" state. Information will be read as the complement of what was written in the memory. When the memory enable input is in the logical "1" state, the outputs will go to the logical "1" state that means the memory chip is not used in read or write.

It can be used to design large dynamic memory chips. To design any memory chip, first step is to simulate the behavior using Proteus simulator. Second step is to test read and write operation. Finally is to generate the circuit in test board.

Connection Diagram



Truth Table

Memory Enable	Write Enable	Operation	Outputs
0	0	Write	Logical "1" state
0	1	Read	Complement of stored data
1	X	Hold	Logical "1" state

Basic Proteus Concepts:

• Work area window
Act as test-board in real: Show the space in the program in which the selected components can be connected together.

• Tools window
Include selected components, power supplies and devices to measure outputs.

• Components window
Include all components the Proteus Simulator are provided

4- Procedure:

1- Run the Proteus simulation program and select the following components from components window as in figure 1:

- 7489
- 7404
- 74139
- 7 seg-BCD
- Thumbswitch
- Logic state

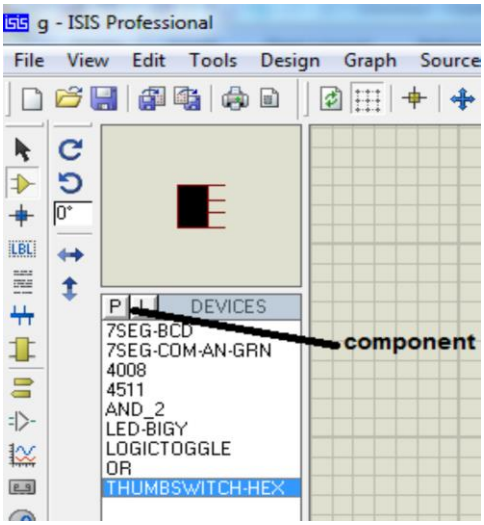


Figure (1)

2- Connect all components together in work area window as shown in figure 2

3- Set the inputs of 7489 chip as in figure 2 to simulate read/write operation

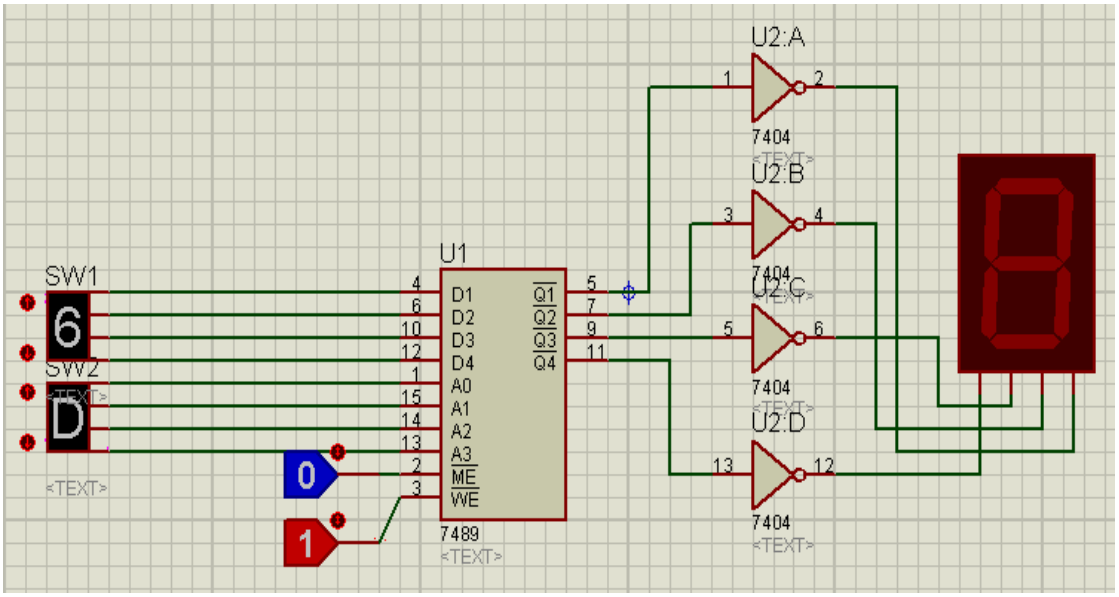


Figure (2)

4- Press in run or F6 and then record the output.
5- Try to insert address and data on the specified bits on chip and change the logical states of memory enable and write enable then, record the output.

Task

Related to Computer Organization Course:

Answer the following questions:

1. What are the functions of the ME and WE inputs' bits?
2. Draw the schematic diagram as you learn in computer organization course to show memory organization (internal structure). In your diagram show the function of the ME and WE bits.

Simulate and implement Dynamic RAM with the following characteristics:

- total size of 64-bits.
- Word size of 8 -bits.
- Active low → write control signal and, active high → read signal in the same control line.

Hints

- Task should be performed in a groups where each group contains five students as a maximum
- Each group should preform one report, one simulated program and one mini-project.
- For all groups, each member will be examined individually so, you must understand the task.