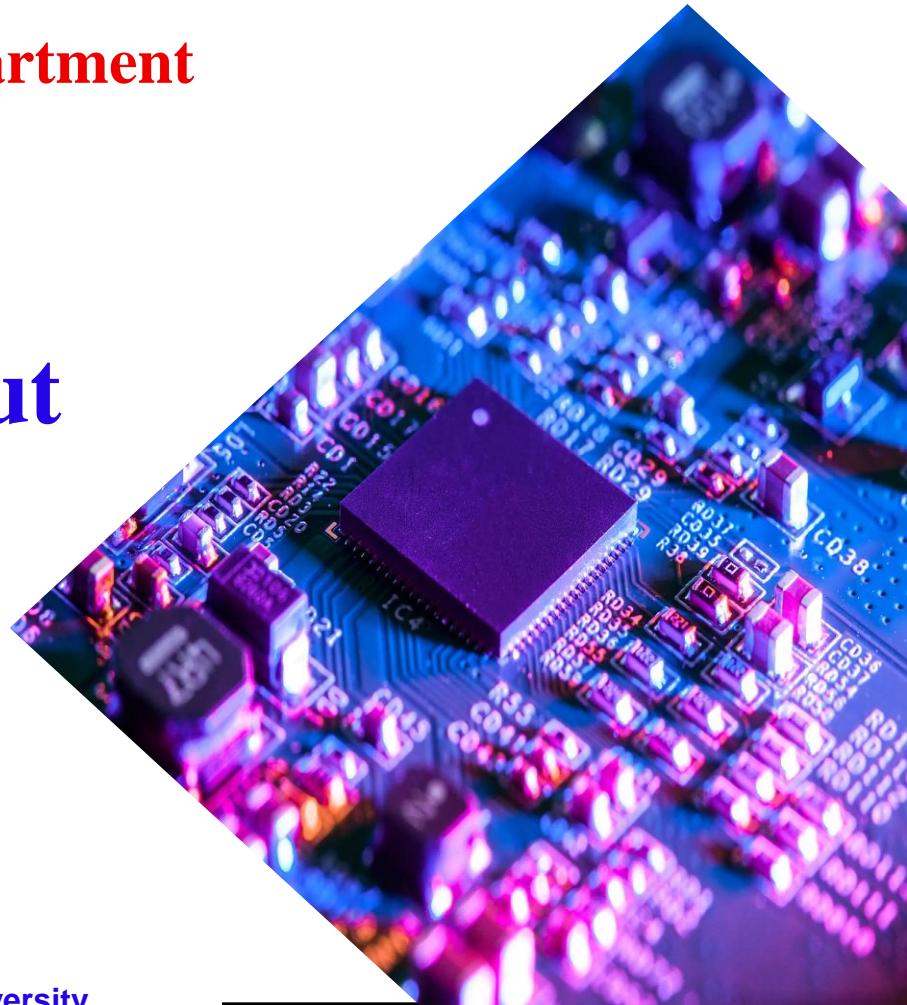


Electronics and communication department

LAB 02: CMOS Lay-Out



Outline



MOS-CROSS SECTION



DRC



COMS INVERTER LAY-OUT



LAY-OUT STEPS



CMOS METAL LAYER



Report



METAL LAYER PARASETICS



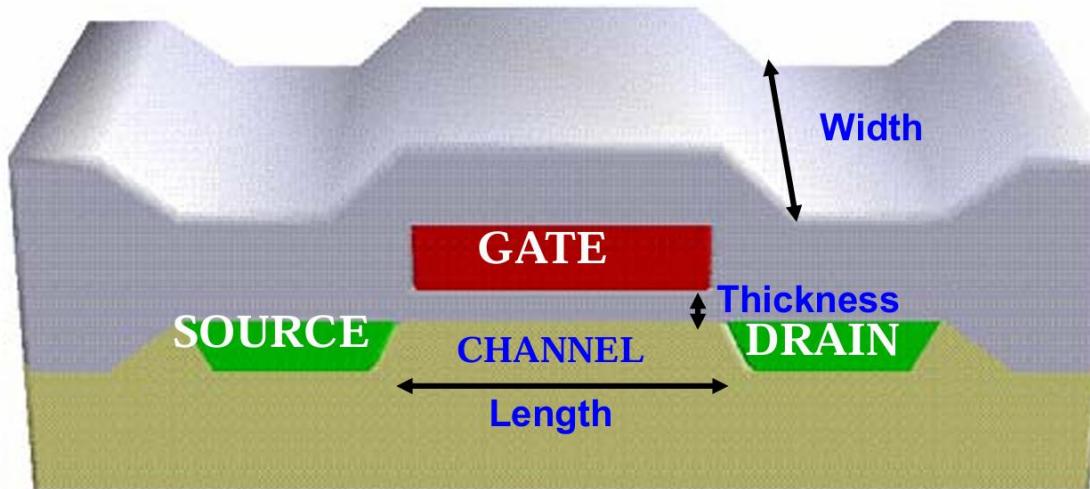
DESIGN FLOW CHART



Lamda Rules

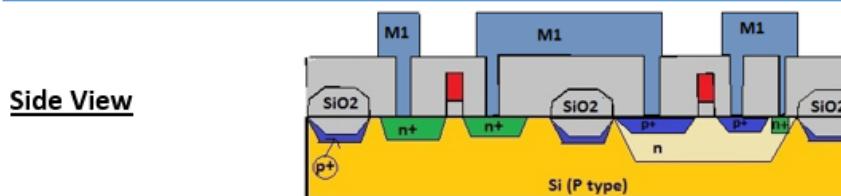
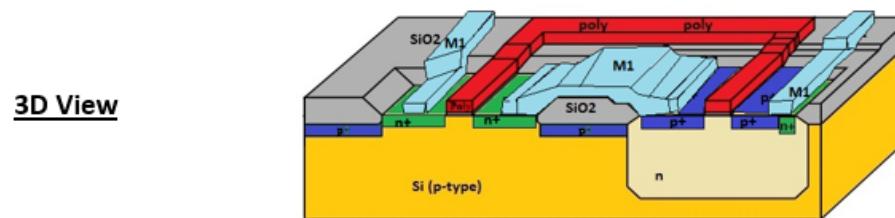
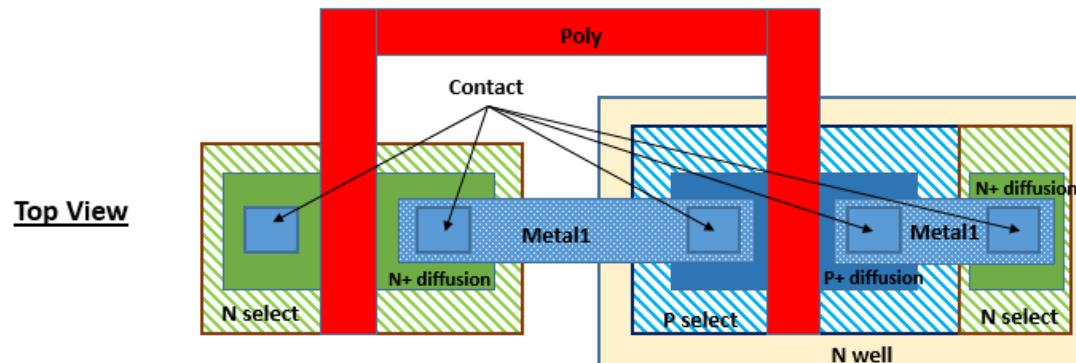
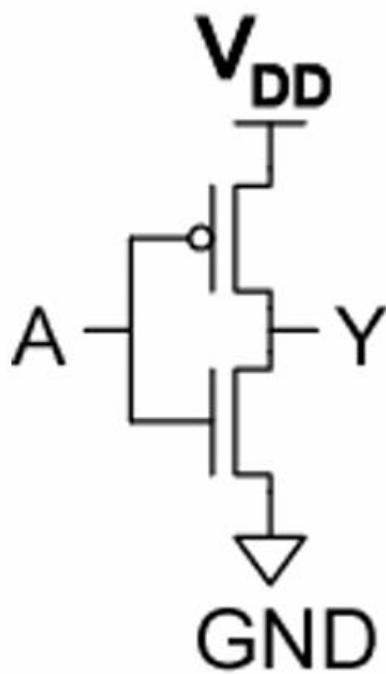


MOS Cross-Section

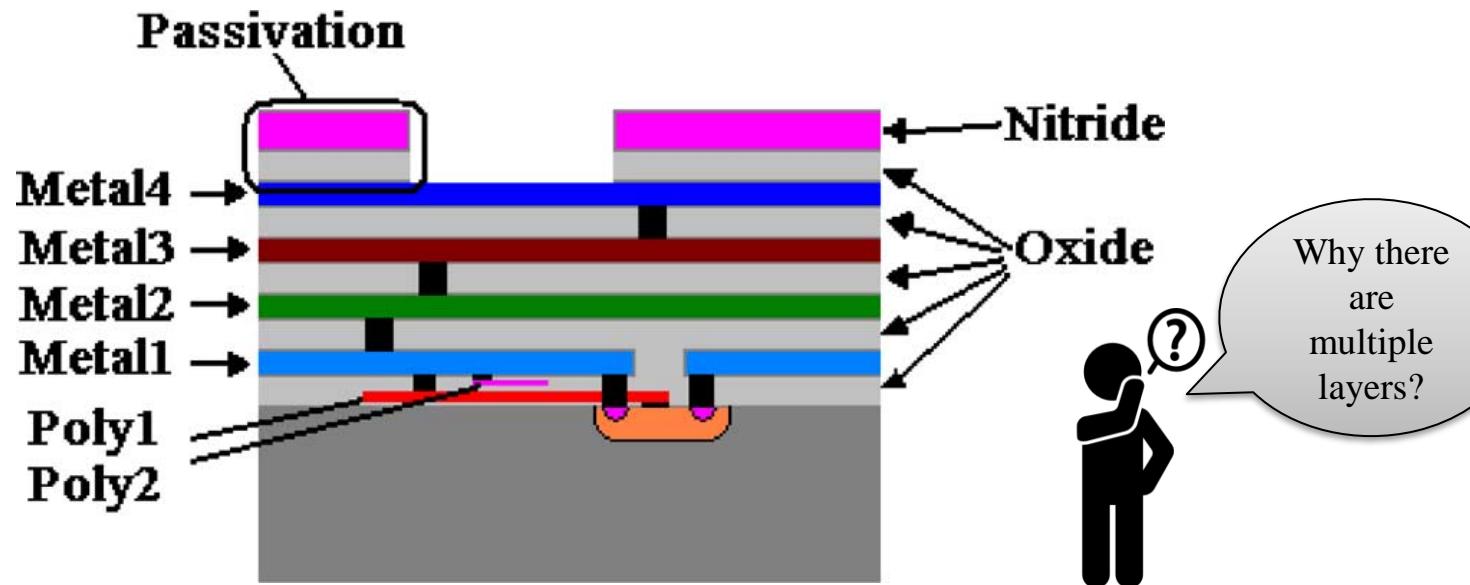


- ❑ The layout refers to the vertical view of a CMOS wafer, illustrating the arrangement of transistors, interconnects, and other components on the chip.
- ❑ The layout is crucial for ensuring proper electrical performance, minimizing parasitic capacitance and resistance, and optimizing area efficiency on silicon wafers.

CMOS Inverter



Metal layers



- The metal layer in CMOS technology serves as the primary interconnect network, facilitating electrical connections between transistors and other circuit components.
- Typically made of aluminum or copper, these metals are chosen for their excellent conductivity

Metal layer parasitic capacitance

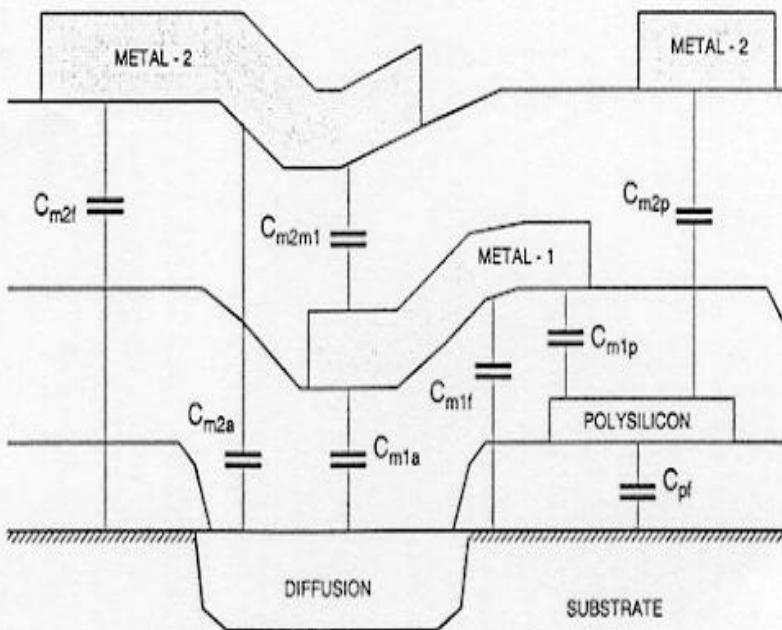
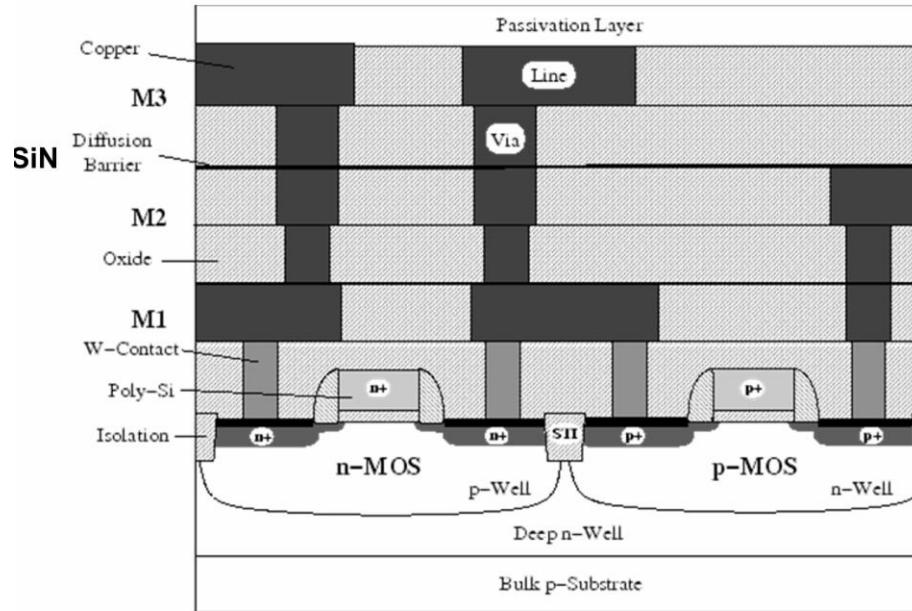


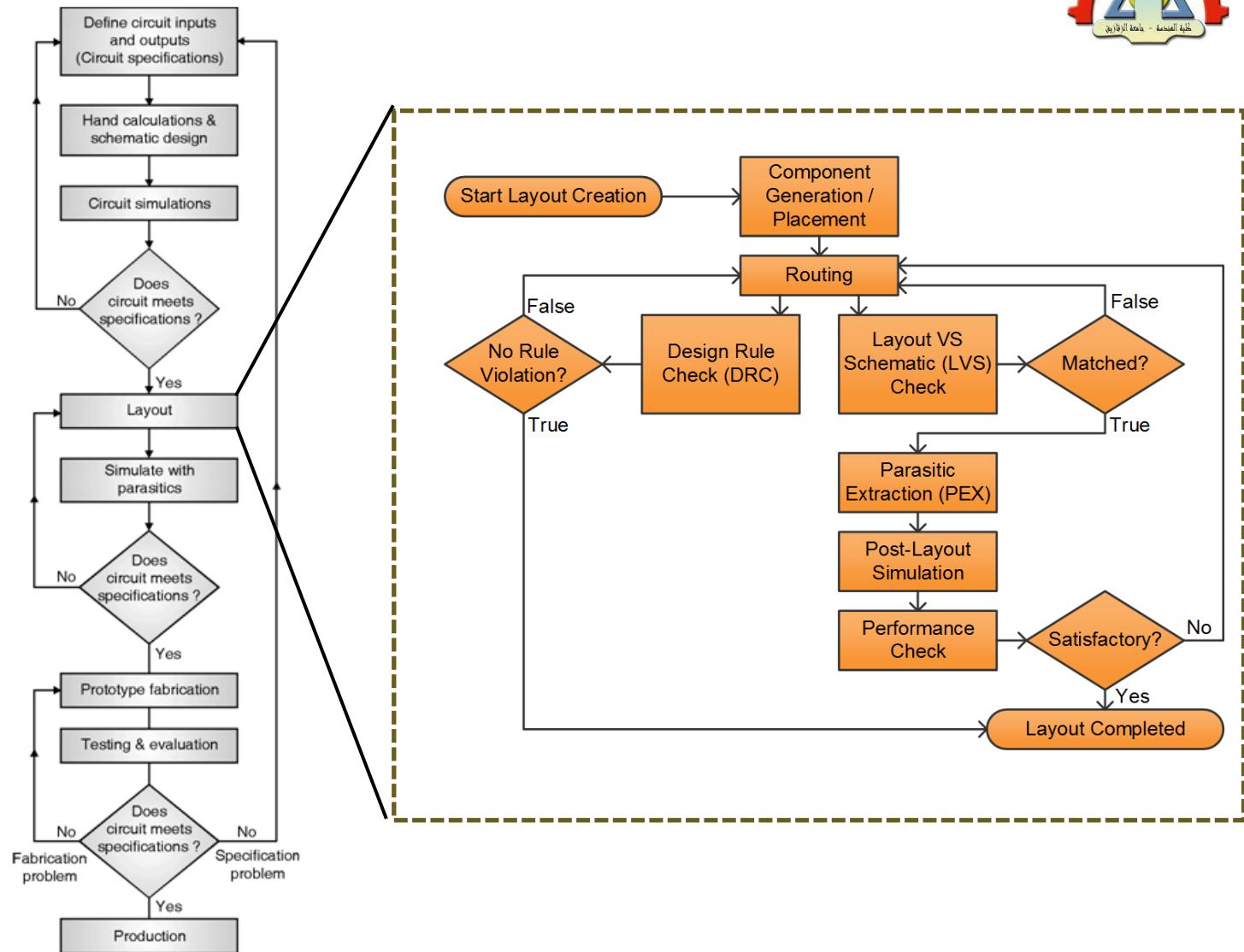
	Plate Cap. aF/ μm^2			Fringe Cap. aF/ μm		
	min	typ	max	min	typ	max
Poly1 to subs. (FOX)	53	58	63	85	88	92
Metal1 to poly1	35	38	43	84	88	93
Metal1 to substrate	21	23	26	75	79	82
Metal1 to diffusion	35	38	43	84	88	93
Metal2 to poly1	16	18	20	83	87	91
Metal2 to substrate	13	14	15	78	81	85
Metal2 to diffusion	16	18	20	83	87	91
Metal2 to metall1	31	35	38	95	100	104

Via



- Vias provide vertical electrical connections between different metal layers, allowing signals and power to be routed throughout the chip efficiently.
- They enable transitions between metal layers, facilitating complex circuit designs that require interconnections across multiple levels.

Design flow chart

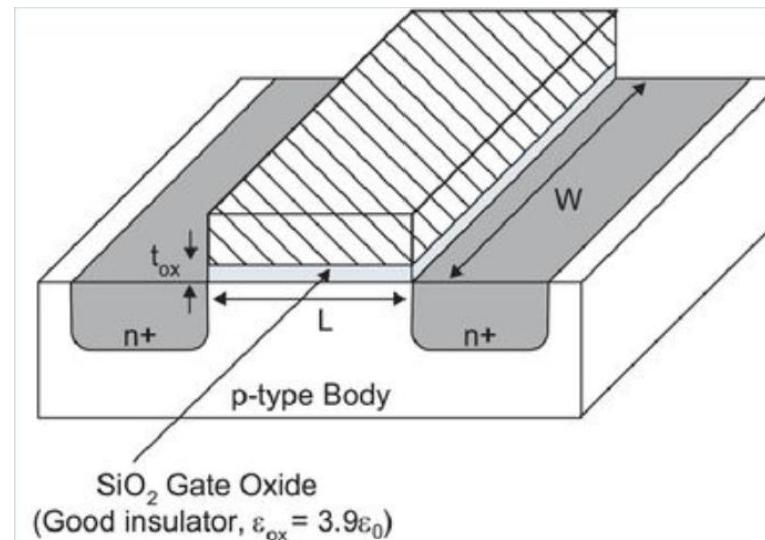


Lamda Rule

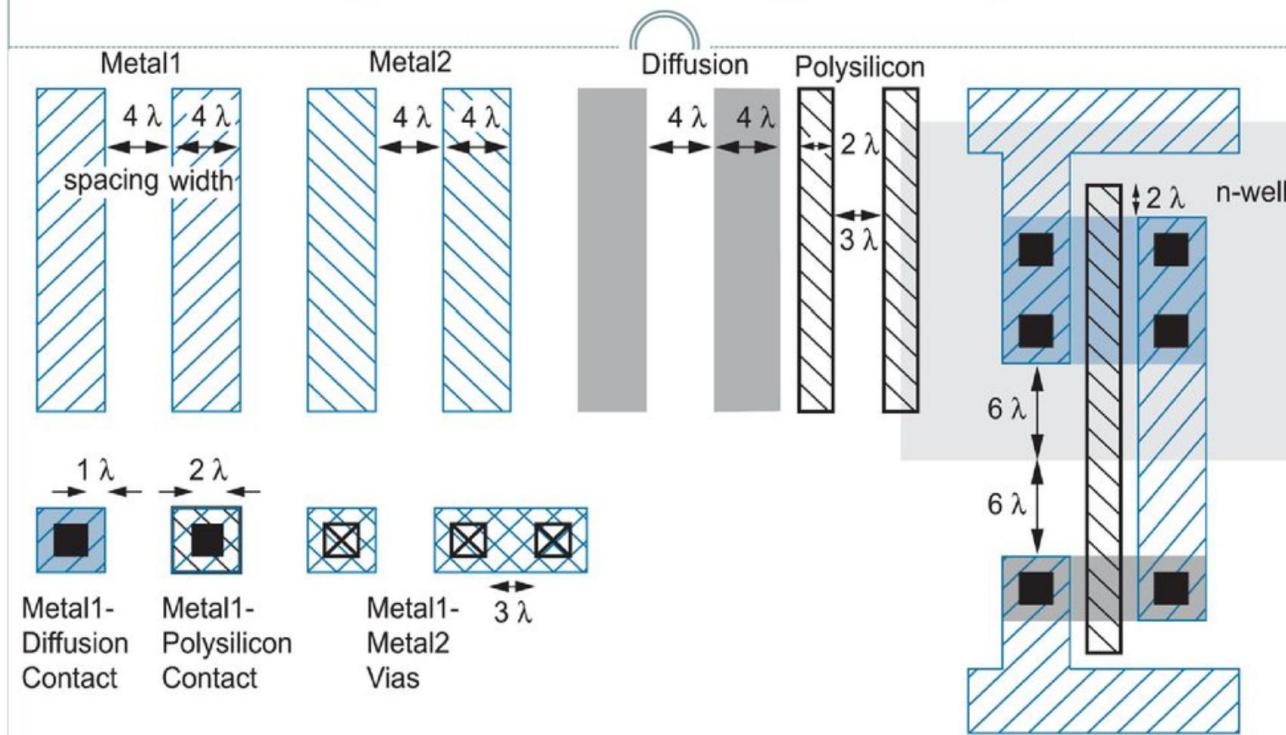
Feature Size:-

the minimum distance between the source and drain on a MOS transistor

$$\text{feature size} = 2 * \lambda$$

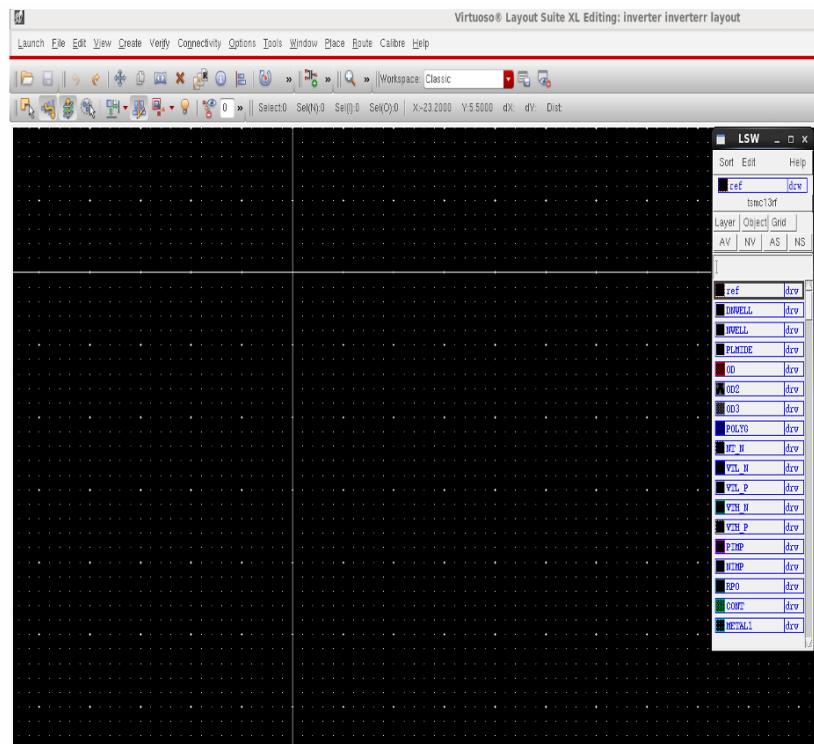


Design rules and gate layout



Lay-out in cadence

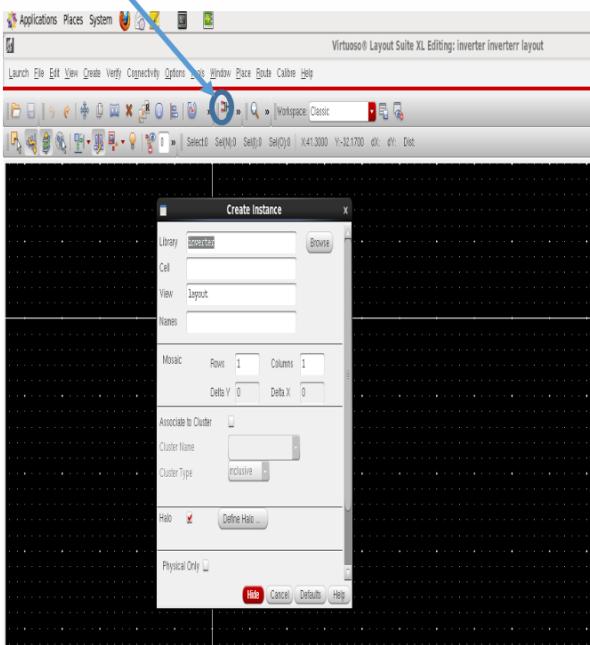
- 1- from schematic window click on launch--->layout XL
- 2- choose create new lay-out and automatic configuration and click ok
- 3- lay-out and layer selection window will pop up as shown



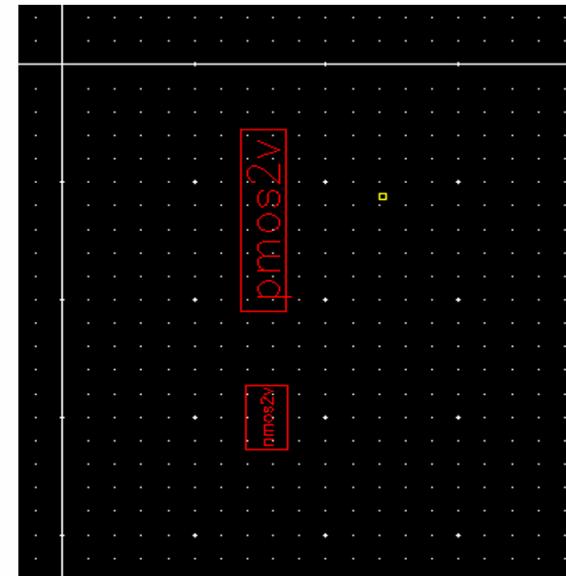
Lay-out in cadence

Creating n-mos and p-mos layout

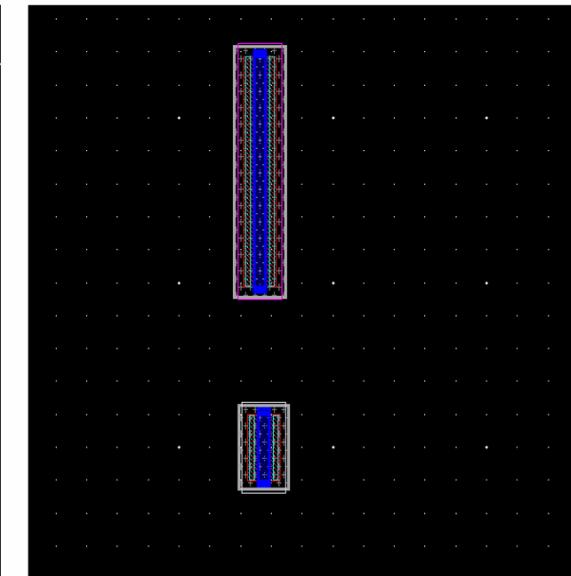
1- click here to choose component



2- choose nmos2v and pmos2v and place it after sizing



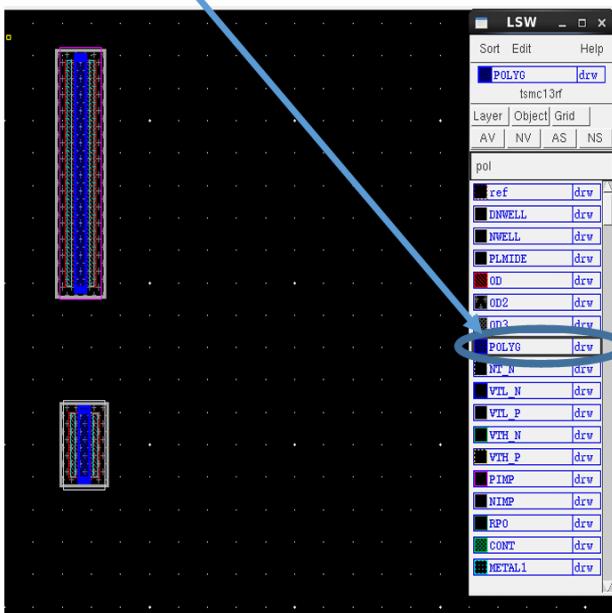
2- press shift+f to show details



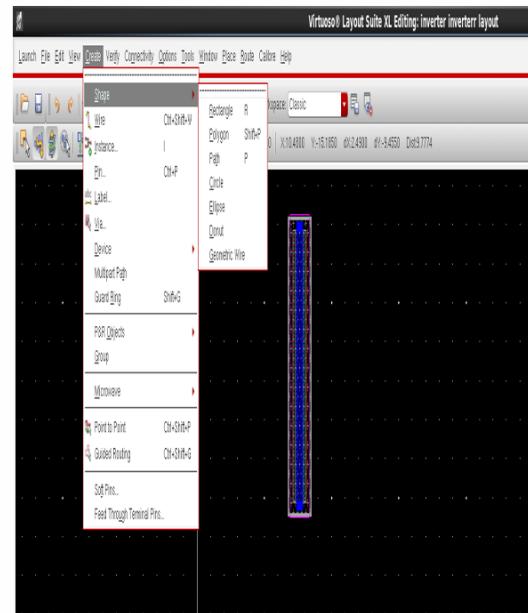
Lay-out in cadence

Connecting gate

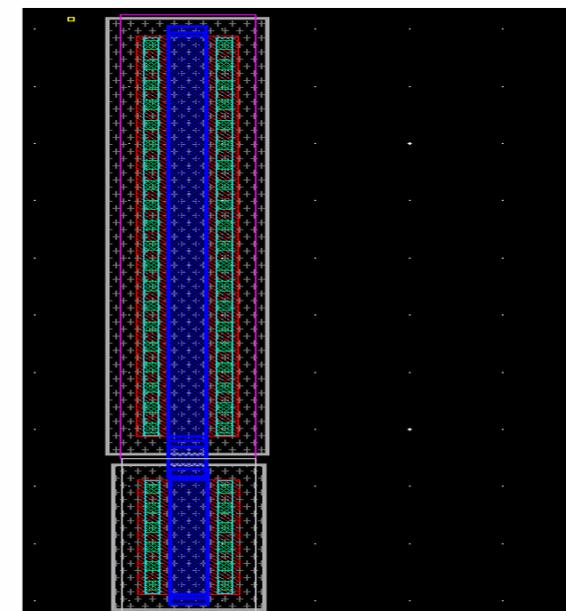
1- from layer selection window choose poly silicon to connect gates



2- choose create--> shape ---> rectangular to draw poly layer



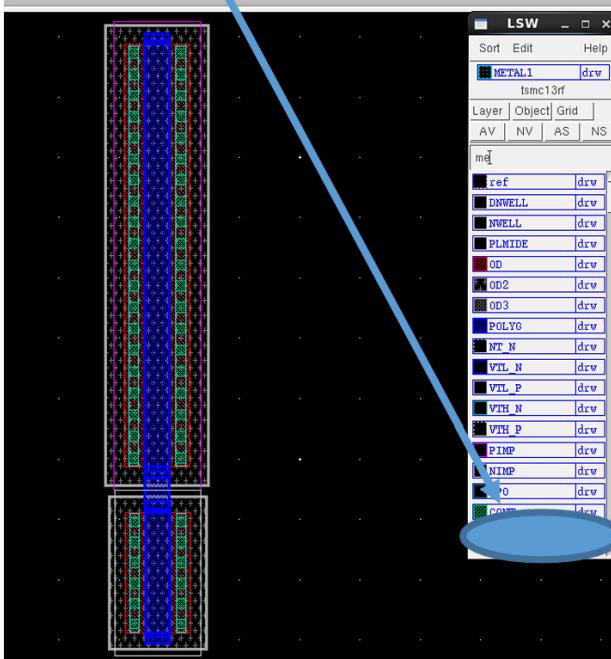
2- draw poly layer to connect gates as shown



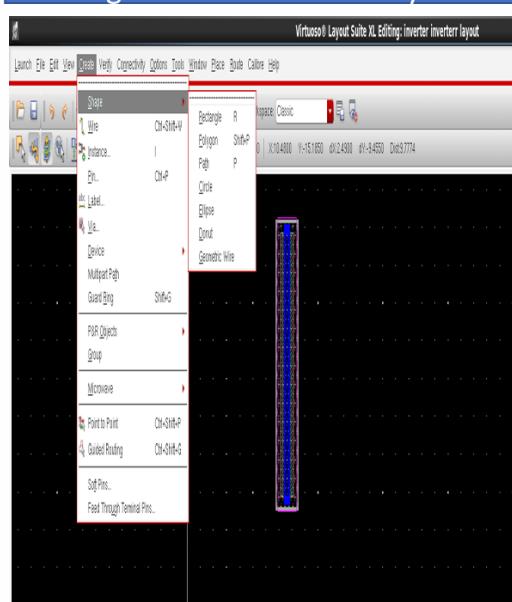
Lay-out in cadence

Connecting drains

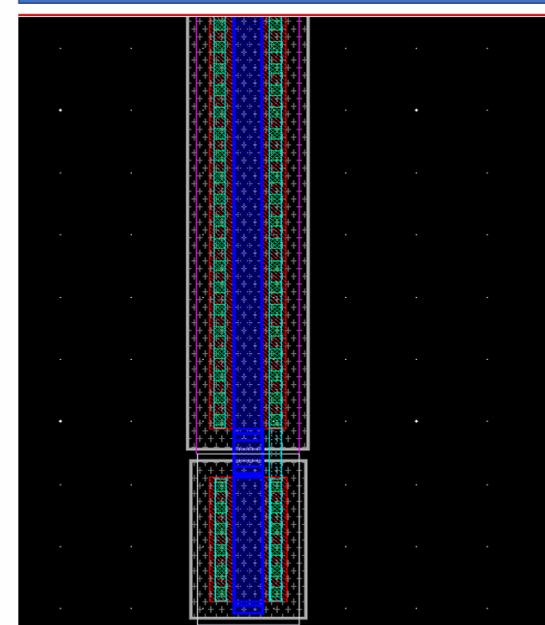
1- from layer selection window choose poly silicon to connect drains



2- choose create--> shape ---> rectangular to draw metal layer



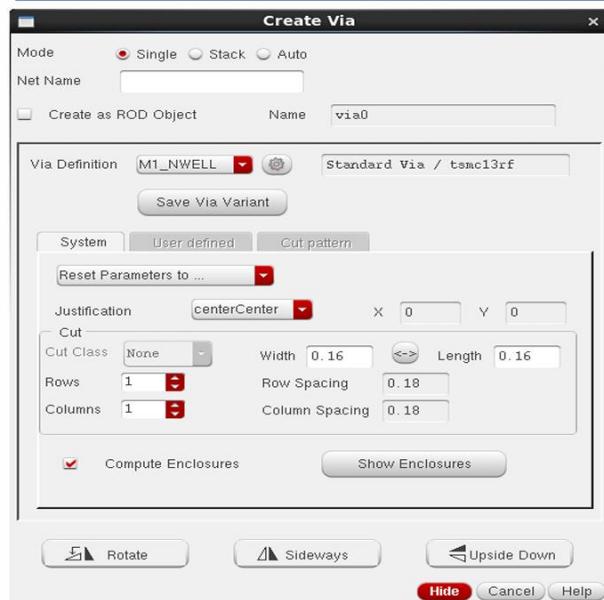
2- draw metal layer to connect drains as shown



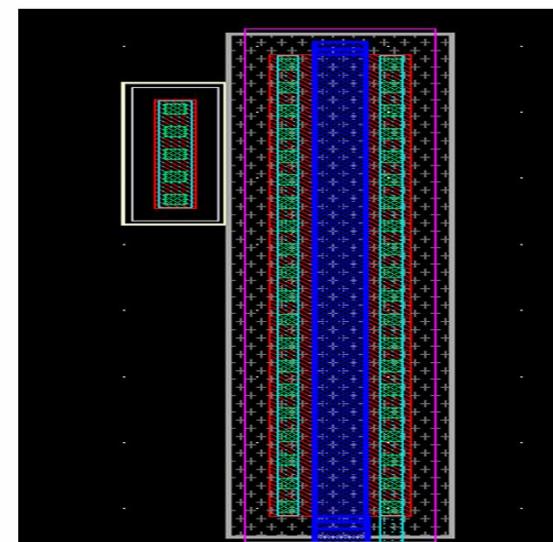
Lay-out in cadence

Connecting bulk of P-MOS

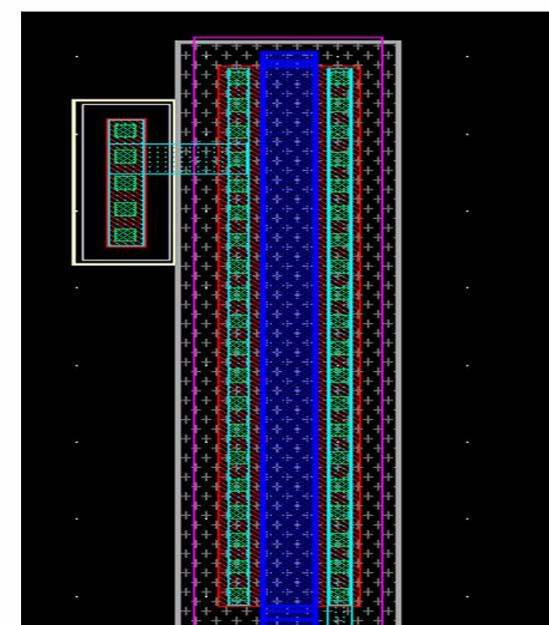
1- click on create---> via and set via definition to M1-NWELL and set rows to 3



2- place M1-NWELL close to p-mosfet



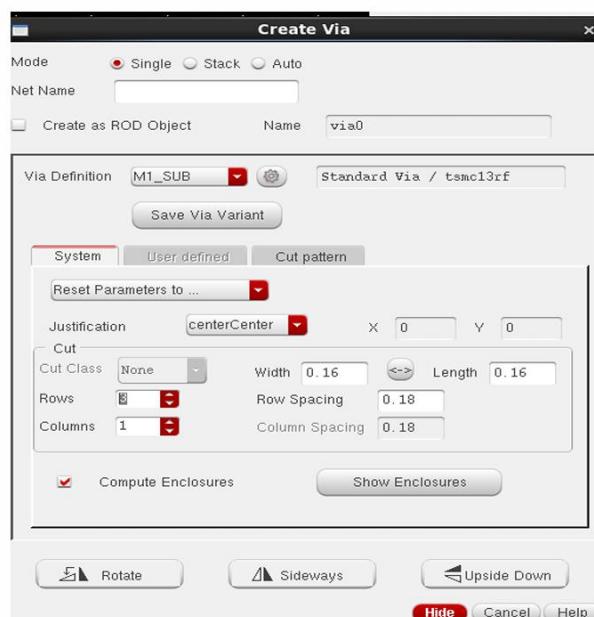
2- connect M1-NEWELL to source of p-mosfet



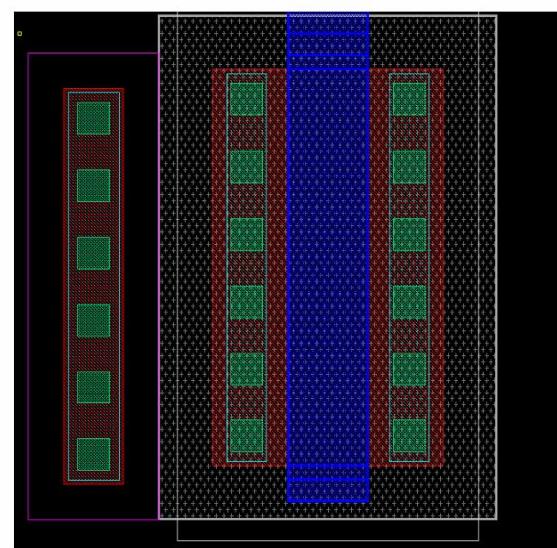
Lay-out in cadence

Connecting bulk of N-MOS

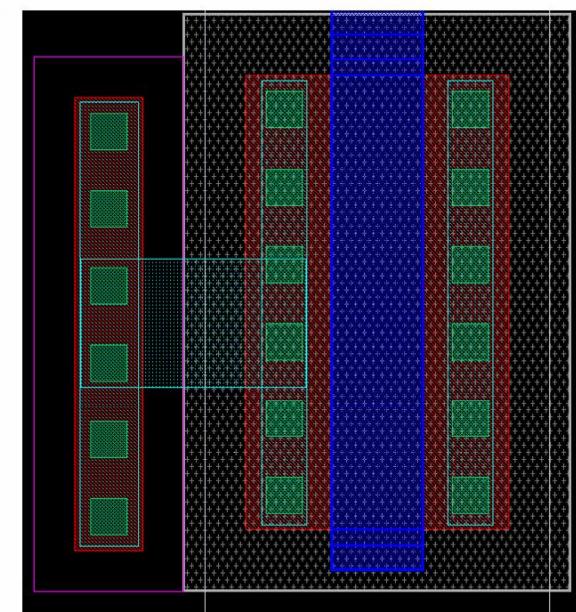
1- click on create---> via and set via definition to M1-Sub and set rows to 6



2- place M1-SUB close to N-mosfet



2- connect M1-SUB to source of N-mosfet



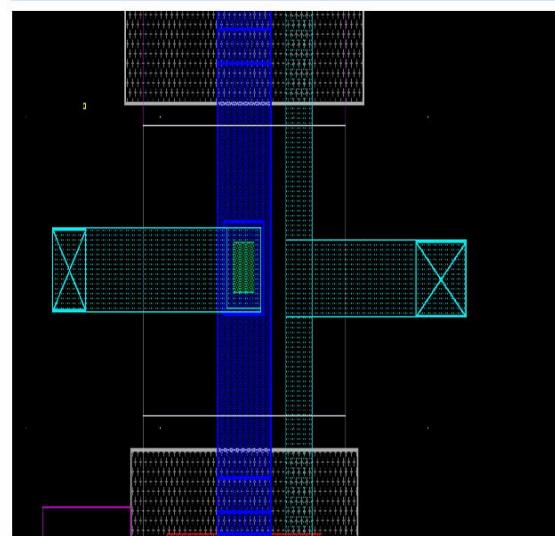
Lay-out in cadence

Connecting pins

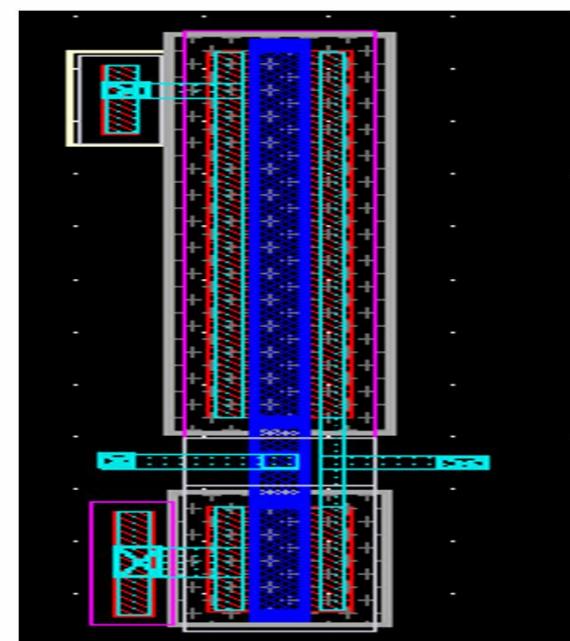
1- from layer selection window choose M1 pin



2- draw M1 pin at input/output pin as interface



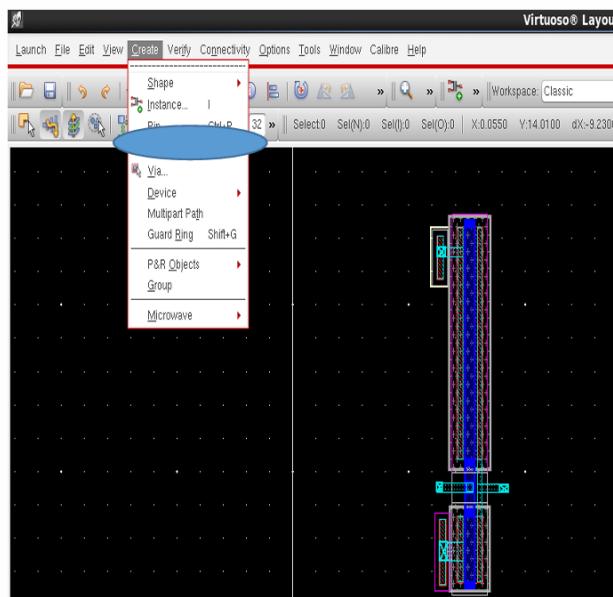
2- draw M1 pin at VDD/GND pin as interface



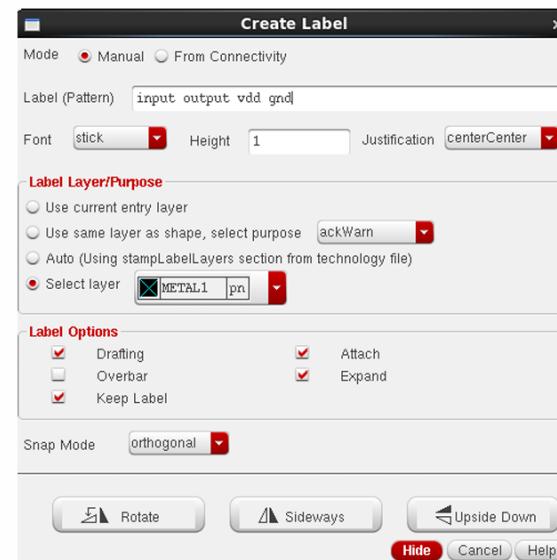
Lay-out in cadence

Connecting label

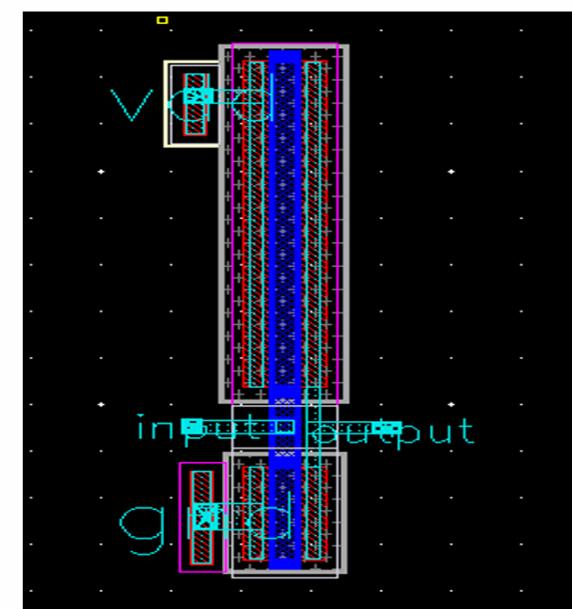
1- from create choose label



2- enter the name of input / output / VDD / GND pins



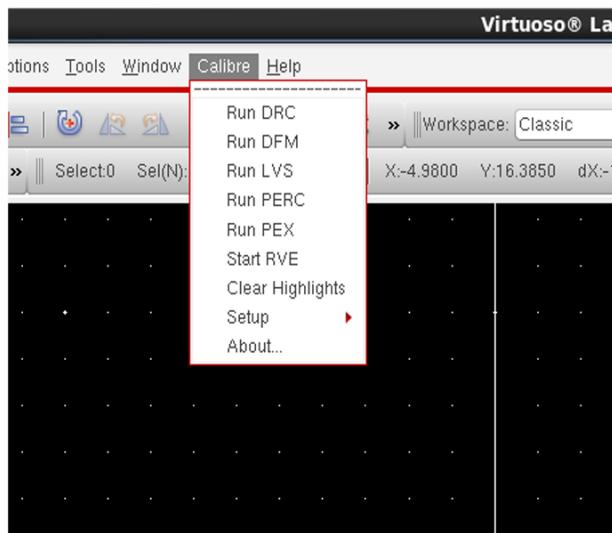
3- place the name on corresponding pin



Lay-out in cadence

DRC

1- from caliber choose Run DRC



2- enter rule path file as shown

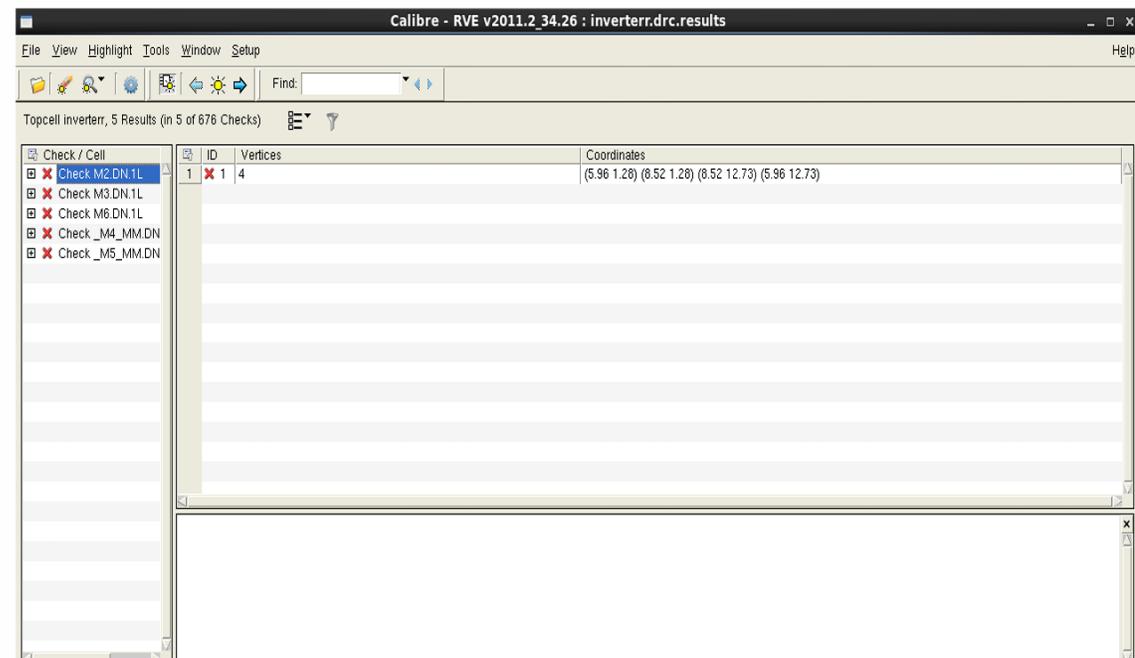


Lay-out in cadence

DRC

3- Click on RUN DRC

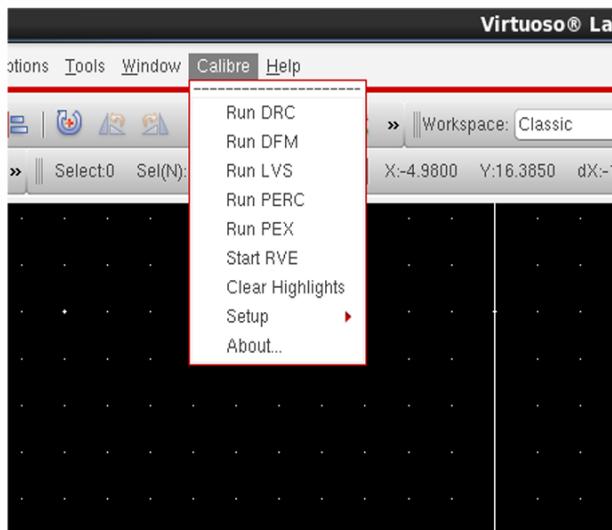
- 1- RVE window will pop up which tell you the DRC errors in the drawn lay out
- 2- all density errors can be ignored as it used in full-chip analysis
- 3- any other error should be resolved



Lay-out in cadence

LVS

1- from caliber choose Run LVS



2- enter rule path file as shown

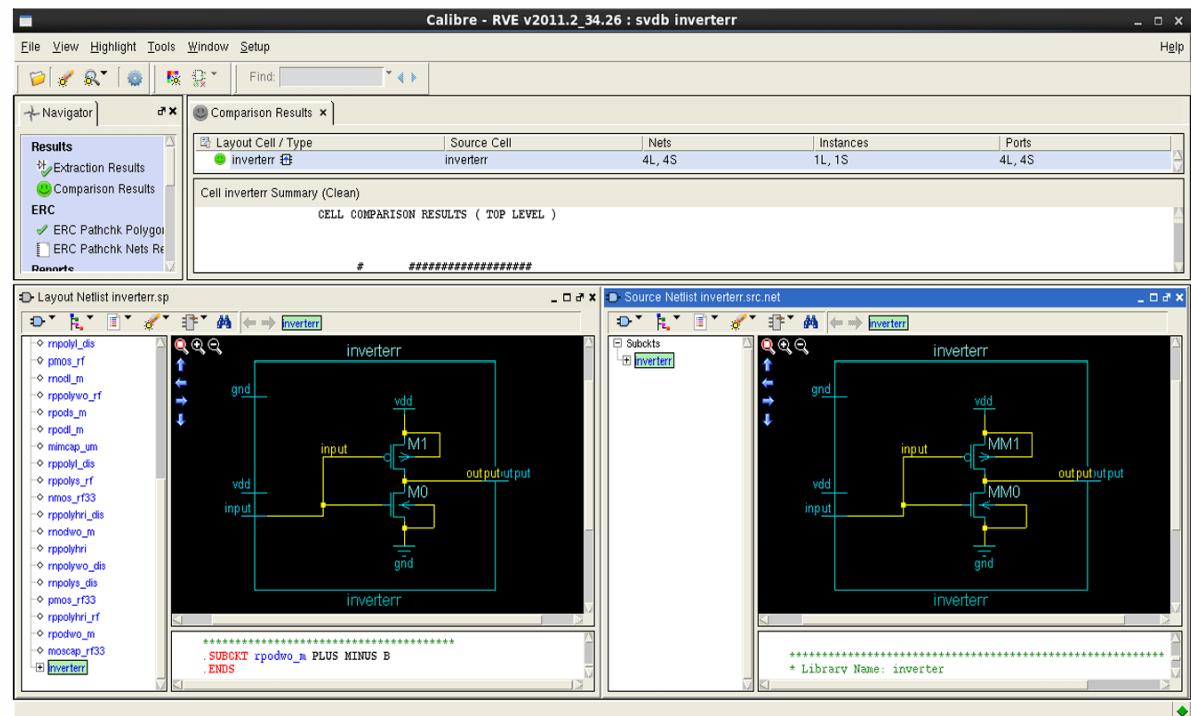


Lay-out in cadence

LVS

3- Click on RUN LVS

Pop – up window will tell you if schematic match lay-out or not as shown in figure





REPORT

- Students are required to write a lab report addressing two key tasks: First, discuss the effect of technology shrink on parasitic capacitance in circuits, highlighting how reducing feature sizes impacts capacitance values and overall circuit performance. Second, simulate a NAND logic gate using appropriate software tools and provide a detailed layout of the gate, including all relevant dimensions and connections. Make sure to analyze the results and discuss any implications related to the design and functionality of the NAND gate.

Thank You