Spartan6 - DSP48A1 Project

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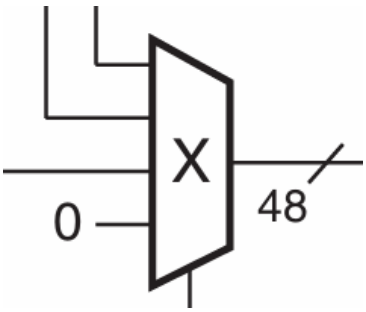
RTL code:

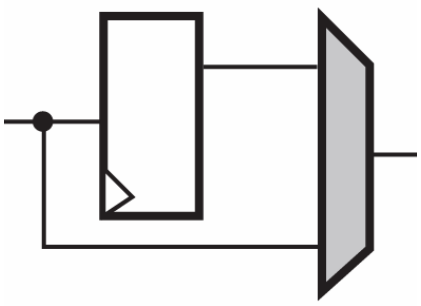
Mux4x1 code:

```
module mux4x1 #(parameter WIDTH = 16)(
    input [WIDTH-1:0]IN0,IN1,IN2,IN3,
    input [1:0]SEL,
    output reg [WIDTH-1:0] out
);
always @(*) begin
    case (SEL)
        2'b00: out <= IN0;
        2'b01: out <= IN1;
        2'b10: out <= IN2;
        2'b11: out <= IN3;
    endcase
end
endmodule
```



Mux following Register code:

```
module reg_mux#(parameter WIDTH = 16, parameter RSTTYPE = "SYNC")(
    input CLK, RST, EN, SEL,
    input [WIDTH-1:0] D,
    output [WIDTH-1:0] out
);
reg [WIDTH-1:0] out_reg;

    generate
        if (RSTTYPE == "ASYNC") begin
            always @(posedge CLK or posedge RST) begin
                if (RST) begin
                    out_reg <= 48'b0;     // Asynchronous reset
                end else if (EN) begin
                    out_reg <= D;
                end
            end
        end
        else if(RSTTYPE=="SYNC") begin
            always @(posedge CLK) begin
                if (RST) begin
                    out_reg <= 48'b0;     // Synchronous reset
                end else if (EN) begin
                    out_reg <= D;
                end
            end
        end
    endgenerate

assign out=(SEL)?out_reg:D;

endmodule
```



Instantiation code (main code):

```
module Spartan6_DSP48A1(A,B,D,C,CLK,CARRYIN,OPMODE,BCIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,
                        CEA,CEB,CEC,CEM,CEP,CED,CECARRYIN,CEOPMODE,PCIN,BCOUT,PCOUT,P,M,CARRYOUT,CARRYOUTF);

//PARAMETERS
parameter A0REG = 1'b0;
parameter A1REG = 1'b1;
parameter B0REG = 1'b0;
parameter B1REG = 1'b1;
parameter CREG = 1'b1;
parameter DREG = 1'b1;
parameter MREG = 1'b1;
parameter PREG = 1'b1;
parameter CARRYINREG = 1'b1;
parameter CARRYOUTREG = 1'b1;
parameter OPMODEREG = 1'b1;
parameter CARRYINSEL = "OPMODE5";
parameter B_INPUT = "DIRECT";
parameter RSTTYPE = "SYNC";
//Data Ports
input [17:0]A;
input [17:0]B;
input [17:0]BCIN;
input [47:0]C;
input [17:0]D;
input CARRYIN;
output [35:0]M;
output [47:0]P;
output CARRYOUT;
output CARRYOUTF;
//Control Input Ports
input CLK;
input [7:0]OPMODE;
```

```
//Clock Enable Input Ports
input CEA,CEB,CEC,CECARRYIN,CED,CEM,CEOPMODE,CEP;
//Reset Input Ports
input RSTA,RSTB,RSTC,RSTCARRYIN,RSTD,RSTM,RSTOPMODE,RSTP;
//Cascade Ports
input [47:0]PCIN;
output [17:0]BCOUT;
output[47:0]PCOUT;

//Wires
wire [17:0]D_WIRE ;
wire [17:0]B0_WIRE ;
wire [17:0]B1_WIRE ;
wire [17:0]B_IN_WIRE;
wire [17:0]D_B0_MUX_WIRE;
wire [17:0]A0_WIRE ;
wire [17:0]A1_WIRE ;
wire [47:0]C_WIRE ;
wire [35:0]A1xB1_OUT_WIRE ;
wire [35:0]M_WIRE ;
wire CARRYIN_WIRE;
wire CARRYOUT_WIRE;
wire CY1_WIRE;
wire CY0_WIRE;
wire [47:0]X_Z_MUX;
wire [47:0]P_WIRE ;
wire [47:0]X_WIRE ;
wire [47:0]D_A_B_CONCAT_WIRE; //D[11:0],A[17:0],B[17:0]
wire [47:0]Z_WIRE ;
wire [17:0]D_B0_PRE_ADD_SUB_WIRE ;
wire [7:0]OPMODE_WIRE;
```

```
reg_mux #(.WIDTH(18),.RSTTYPE(RSTTYPE)) D_REG (.CLK(CLK),.RST(RSTD),.EN(CED),.SEL(DREG),.D(D),.out(D_WIRE));
reg_mux #(.WIDTH(18),.RSTTYPE(RSTTYPE)) B0_REG (.CLK(CLK),.RST(RSTB),.EN(CEB),.SEL(B0REG),.D(B_IN_WIRE),.out(B0_WIRE));
reg_mux #(.WIDTH(18),.RSTTYPE(RSTTYPE)) A0_REG (.CLK(CLK),.RST(RSTA),.EN(CEA),.SEL(A0REG),.D(A),.out(A0_WIRE));
reg_mux #(.WIDTH(48),.RSTTYPE(RSTTYPE)) C_REG (.CLK(CLK),.RST(RSTC),.EN(CEC),.SEL(CREG),.D(C),.out(C_WIRE));

reg_mux #(.WIDTH(18),.RSTTYPE(RSTTYPE)) B1_REG (.CLK(CLK),.RST(RSTB),.EN(CEB),.SEL(B1REG),.D(D_B0_MUX_WIRE),.out(B1_WIRE));
reg_mux #(.WIDTH(18),.RSTTYPE(RSTTYPE)) A1_REG (.CLK(CLK),.RST(RSTA),.EN(CEA),.SEL(A1REG),.D(A0_WIRE),.out(A1_WIRE));
reg_mux #(.WIDTH(36),.RSTTYPE(RSTTYPE)) M_REG (.CLK(CLK),.RST(RSTM),.EN(CEM),.SEL(MREG),.D(A1xB1_OUT_WIRE),.out(M_WIRE));

reg_mux #(.WIDTH(1),.RSTTYPE(RSTTYPE)) CY1 (.CLK(CLK),.RST(RSTCARRYIN),.EN(CECARRYIN),.SEL(CARRYINREG),.D(CARRYIN_WIRE),.out(CY1_WIRE));
reg_mux #(.WIDTH(1),.RSTTYPE(RSTTYPE)) CY0 (.CLK(CLK),.RST(RSTCARRYIN),.EN(CECARRYIN),.SEL(CARRYOUTREG),.D(CARRYOUT_WIRE),.out(CY0_WIRE));

reg_mux #(.WIDTH(8),.RSTTYPE(RSTTYPE)) OPMODE_REG (.CLK(CLK),.RST(RSTOPMODE),.EN(CEOPMODE),.SEL(OPMODEREG),.D(OPMODE),.out(OPMODE_WIRE));

reg_mux #(.WIDTH(48),.RSTTYPE(RSTTYPE)) P_REG (.CLK(CLK),.RST(RSTP),.EN(CEP),.SEL(PREG),.D(X_Z_MUX),.out(P_WIRE));

mux4x1 #(.WIDTH(48)) X_MUX (.IN0(48'h000000000000),.IN1({12'h000,M_WIRE}),.IN2(P_WIRE),.IN3(D_A_B_CONCAT_WIRE),.SEL(OPMODE_WIRE[1:0]),.out(X_WIRE));
mux4x1 #(.WIDTH(48)) Z_MUX (.IN0(48'h000000000000),.IN1(PCIN),.IN2(P_WIRE),.IN3(C_WIRE),.SEL(OPMODE_WIRE[3:2]),.out(Z_WIRE));


assign B_IN_WIRE = (B_INPUT == "CASCADE") ? BCIN : (B_INPUT == "DIRECT") ? B : 0;
assign D_B0_PRE_ADD_SUB_WIRE = (OPMODE_WIRE[6]) ? (D_WIRE - B0_WIRE) : (D_WIRE + B0_WIRE);
assign D_B0_MUX_WIRE = (OPMODE_WIRE[4]) ? D_B0_PRE_ADD_SUB_WIRE : B0_WIRE;
assign A1xB1_OUT_WIRE = A1_WIRE * B1_WIRE ;
assign D_A_B_CONCAT_WIRE = {D_WIRE[11:0],A1_WIRE,B1_WIRE};
assign M_WIRE = M;
assign BCOUT = B1_WIRE;
assign CARRYIN_WIRE = (CARRYINSEL == "CARRYIN") ? CARRYIN : (CARRYINSEL == "OPMODE5") ? OPMODE_WIRE[5] : 0;
assign {CARRYOUT_WIRE,X_Z_MUX} = (OPMODE_WIRE[7]) ? (Z_WIRE - (X_WIRE + CY1_WIRE)) : (Z_WIRE + (X_WIRE + CY1_WIRE));
assign P = P_WIRE;
assign PCOUT = P_WIRE;
assign CARRYOUT = CY0_WIRE;
assign CARRYOUTF = CY0_WIRE;

endmodule
```

Testbench code:

```
//Testing
initial begin
    RSTA=1'b1;
    RSTB=1'b1;
    RSTC=1'b1;
    RSTCARRYIN=1'b1;
    RSTD=1'b1;
    RSTM=1'b1;
    RSTOPMODE=1'b1;
    RSTP=1'b1;
    A=18'h0;
    D=18'h0;
    C=18'h0;
    B=18'h0;
    OPMODE=8'h0;
    CARRYIN=1'b0;
    BCIN=18'h0;
    CEA=1'b0;
    CEB=1'b0;
    CEM=1'b0;
    CEP=1'b0;
    CEC=1'b0;
    CED=1'b0;
    CECARRYIN=1'b0;
    CEOPMODE=1'b0;
    PCIN=18'h0;
    repeat(50) @(negedge CLK);
```

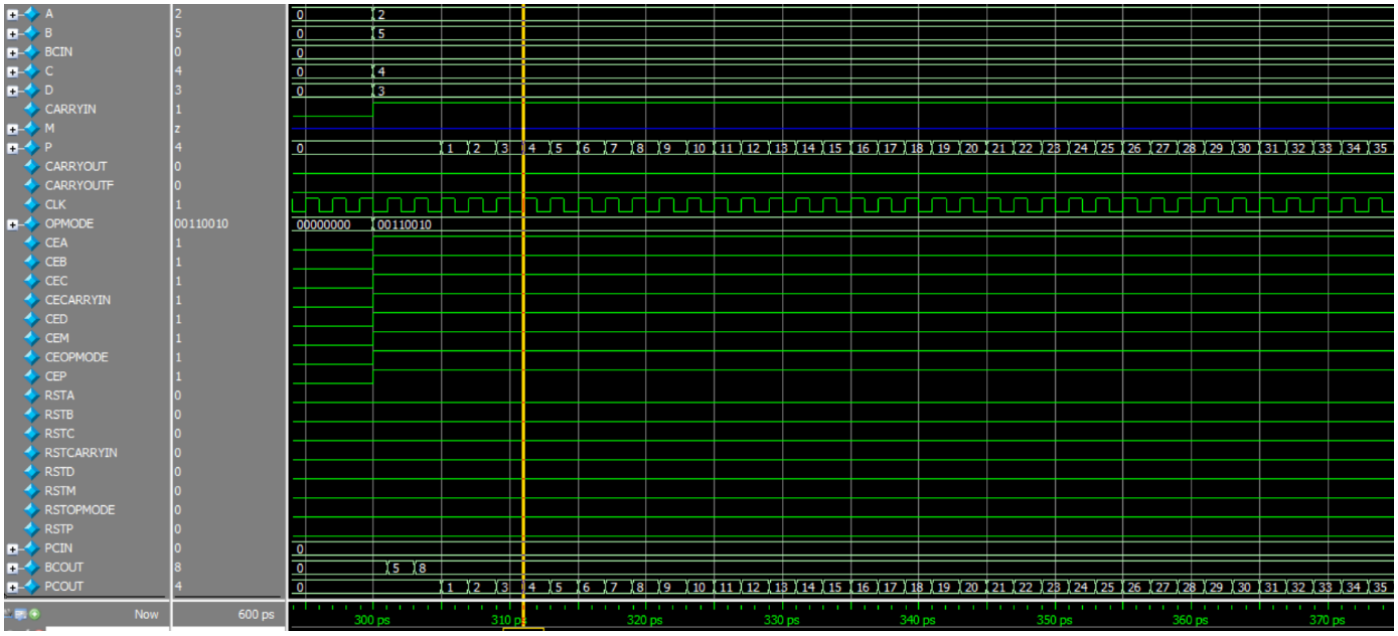
```
    RSTA=1'b0;
    RSTB=1'b0;
    RSTC=1'b0;
    RSTCARRYIN=1'b0;
    RSTD=1'b0;
    RSTM=1'b0;
    RSTOPMODE=1'b0;
    RSTP=1'b0;
    repeat(50) @(negedge CLK);

    A=18'h2;
    D=18'h3;
    C=18'h4;
    B=18'h5;
    OPMODE=8'b00110010;
    CARRYIN=1'b1;
    BCIN=18'h0;
    CEA=1'b1;
    CEB=1'b1;
    CEM=1'b1;
    CEP=1'b1;
    CEC=1'b1;
    CED=1'b1;
    CECARRYIN=1'b1;
    CEOPMODE=1'b1;
    PCIN=18'h0;
    repeat(100) @(negedge CLK);
```

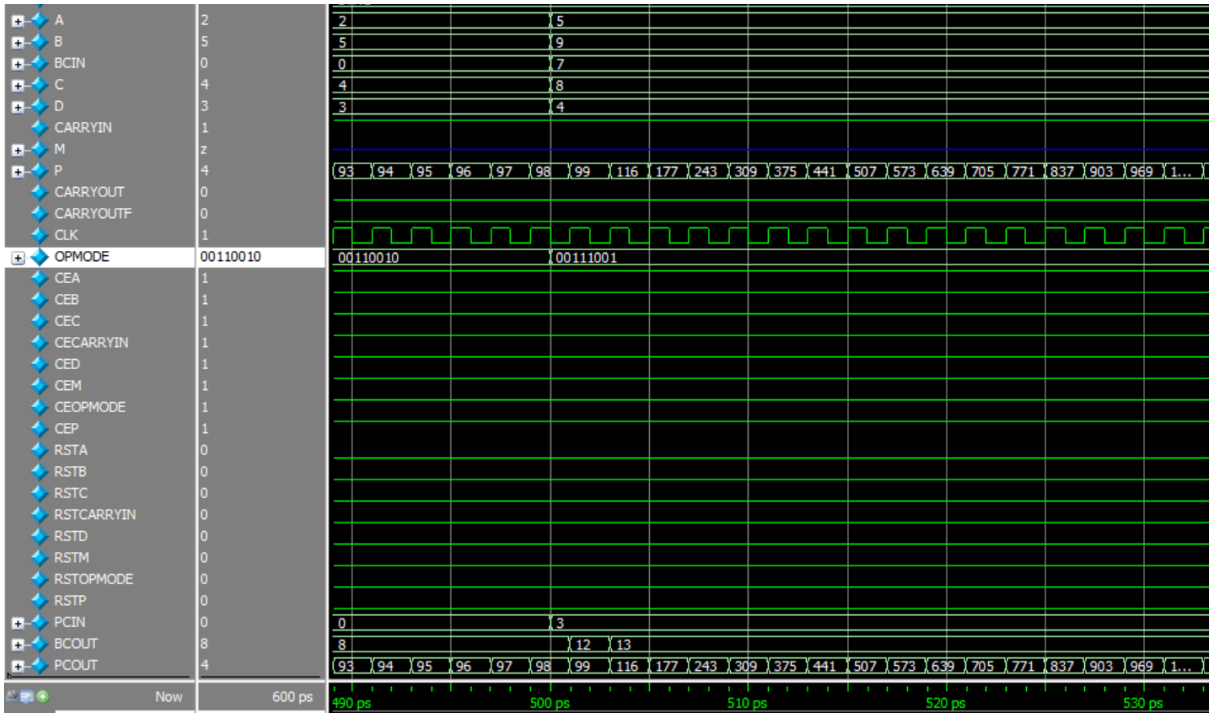
```
    A=18'h5;
    D=18'h4;
    C=18'h8;
    B=18'h9;
    OPMODE=8'b0011100
    CARRYIN=1'b1;
    BCIN=18'h7;
    CEA=1'b1;
    CEB=1'b1;
    CEM=1'b1;
    CEP=1'b1;
    CEC=1'b1;
    CED=1'b1;
    CECARRYIN=1'b1;
    CEOPMODE=1'b1;
    PCIN=18'h3;

#100
$stop;
end
endmodule
```

Do file:

```
vlib work
vlog project1.v MUX4x1.v REG_MUX.v project1tb.v
vsim -voptargs="+acc" Spartan6_DSP48A1_tb
add wave *
run -all
```

QuestaSim Snippets:



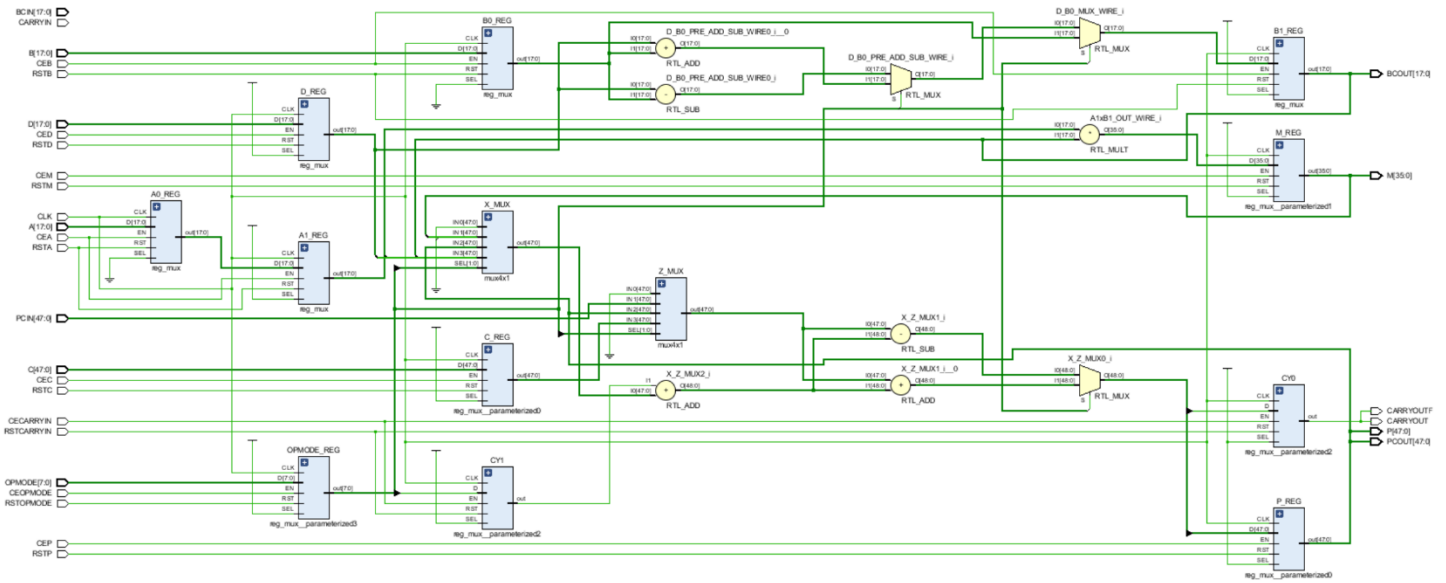


Constraint File:

```
## Clock signal
set_property -dict { PACKAGE_PIN W5   IOSTANDARD LVCMOS33 } [get_ports CLK]
create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports CLK]
```

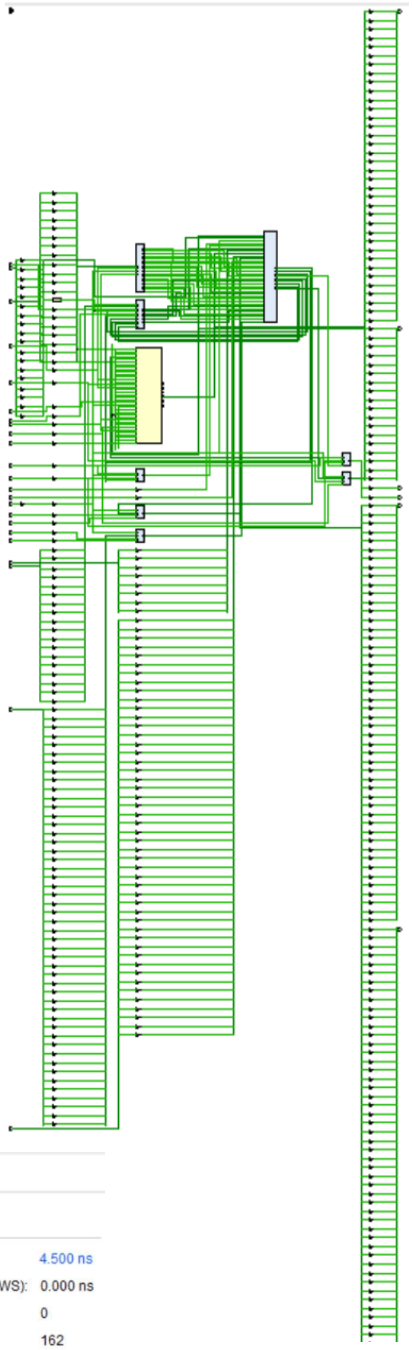
Elaboration:

- Elaborated Design (20 warnings, 17 infos)
  - General Messages (20 warnings, 17 infos)
    - [Synth 8-6157] synthesizing module 'Spartan6_DSP48A1' [project1.v:4] (6 more like this)
    - [Synth 8-6155] done synthesizing module 'reg_mux' (1#1) [REG_MUX.v:1] (6 more like this)
    - [Synth 8-3848] Net M in module/entity Spartan6_DSP48A1 does not have driver. [project1.v:29]
    - [Synth 8-3331] design Spartan6_DSP48A1 has unconnected port CARRYIN (18 more like this)
    - [Project 1-570] Preparing netlist for logic optimization
    - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
    - [Project 1-111] Unisim Transformation Summary:
      No Unisim elements were transformed.



Synthesis:

- Synthesis (58 warnings, 50 infos)
  - [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a200t'
  - [Synth 8-6157] synthesizing module 'Spartan6_DSP48A1' [project1.v:4] (6 more like this)
  - [Synth 8-6155] done synthesizing module 'reg_mux' (1#1) [REG_MUX.v:1] (6 more like this)
  - [Synth 8-3848] Net M in module/entity Spartan6_DSP48A1 does not have driver. [project1.v:29]
  - [Synth 8-3331] design Spartan6_DSP48A1 has unconnected port CARRYIN (37 more like this)
  - [Device 21-403] Loading part xc7a200tffg1156-3
  - [Project 1-236] Implementation specific constraints were found while reading constraint file [F:/Digital Diploma/work/Constraints_basys3_project1.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/Spartan6_DSP48A1_propImpl.xdc].
    Resolution: To avoid this warning, move constraints listed in ['Undefined'] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
  - [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [project1.v:89] (1 more like this)
  - [Synth 8-3886] merging instance 'A0_REG/out_reg_reg[0]' (FDRE) to 'A1_REG/out_reg_reg[0]' (17 more like this)
  - [Synth 8-3332] Sequential element (B0_REG/out_reg_reg[17]) is unused and will be removed from module Spartan6_DSP48A1. (17 more like this)
  - [Synth 8-5842] Cannot pack DSP OPMODE registers because of constant '1' value. Packing the registers will cause simulation mismatch at initial cycle [project1.v:91]
  - [Project 1-571] Translating synthesized netlist
  - [Netlist 29-17] Analyzing 207 Unisim elements for replacement
  - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
  - [Project 1-570] Preparing netlist for logic optimization (1 more like this)
  - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
  - [Project 1-111] Unisim Transformation Summary:
    No Unisim elements were transformed. (1 more like this)
  - [Common 17-83] Releasing license: Synthesis
  - [Constraints 18-5210] No constraint will be written out.
  - [Common 17-1381] The checkpoint 'F:/Digital Diploma/work/Spartan6_DSP48A1/Spartan6_DSP48A1.runs/synth_1/Spartan6_DSP48A1.dcp' has been generated.
  - [runtcl-4] Executing : report_utilization -file Spartan6_DSP48A1_utilization_synth.rpt -pb Spartan6_DSP48A1_utilization_synth.pb
  - [Common 17-206] Exiting Vivado at Wed Jul 31 20:44:54 2024...
- Synthesized Design (6 infos)
  - General Messages (6 infos)
    - [Netlist 29-17] Analyzing 207 Unisim elements for replacement
    - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
    - [Project 1-479] Netlist was created with Vivado 2018.2
    - [Project 1-570] Preparing netlist for logic optimization
    - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
    - [Project 1-111] Unisim Transformation Summary:
      No Unisim elements were transformed.



Name	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
Spartan6_DSP48A1	182	160	1	327	1
A1_REG (reg_mux)	0	18	0	0	0
B1_REG (reg_mux_0)	0	18	0	0	0
C_REG (reg_mux__pa...	0	48	0	0	0
CY0 (reg_mux__para...	0	1	0	0	0
CY1 (reg_mux__para...	1	1	0	0	0
D_REG (reg_mux_2)	0	18	0	0	0
OPMODE_REG (reg_...	180	8	0	0	0
P_REG (reg_mux__pa...	0	48	0	0	0

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.172 ns	Worst Hold Slack (WHS):	0.182 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	87	Total Number of Endpoints:	87	Total Number of Endpoints:	162

All user specified timing constraints are met.

Implementation:

- Implementation (1 warning, 92 infos)
  - Design Initialization (11 infos)
    - [Netlist 29-17] Analyzing 207 Unisim elements for replacement
    - [Netlist 29-28] Unisim Transformation completed in 1 CPU seconds
    - [Project 1-479] Netlist was created with Vivado 2018.2
    - [Device 21-403] Loading part xc7a200tffg1156-3
    - [Project 1-570] Preparing netlist for logic optimization
    - [Timing 38-478] Restoring timing data from binary archive.
    - [Timing 38-479] Binary timing data restore complete.
    - [Project 1-856] Restoring constraints from binary archive.
    - [Project 1-853] Binary constraint restore complete.
    - [Project 1-111] Unisim Transformation Summary:
      No Unisim elements were transformed.
    - [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646
  - Opt Design (24 infos)
    - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a200t'
    - [Project 1-461] DRC finished with 0 Errors
    - [Project 1-462] Please refer to the DRC report (report_drc) for more information.
    - [Timing 38-35] Done setting XDC timing constraints.
    - [Opt 31-49] Retargeted 0 cell(s).
    - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s). (1 more like this)
    - [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)
    - [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.
    - [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
    - [Common 17-83] Releasing license: Implementation
    - [Timing 38-480] Writing timing data to binary archive.
    - [Common 17-1381] The checkpoint 'F:/Digital Diploma/work/Spartan6_DSP48A1/Spartan6_DSP48A1.runs/impl_1/Spartan6_DSP48A1_opt.dcp' has been generated.
    - [runtcl-4] Executing : report_drc -file Spartan6_DSP48A1_drc_opted.rpt -pb Spartan6_DSP48A1_drc_opted.pb -rpx Spartan6_DSP48A1_drc_opted.rpx
    - [IP_Flow 19-234] Refreshing IP repositories
    - [IP_Flow 19-1704] No user IP repositories specified
    - [IP_Flow 19-2313] Loaded Vivado IP repository 'D:/vi/Vivado/2018.2/data/ip'.
    - [DRC 23-27] Running DRC with 2 threads (1 more like this)
    - [Coretcl 2-168] The results of DRC are in file Spartan6_DSP48A1_drc_opted.rpt.
  - Place Design (23 infos)
    - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a200t'
    - [DRC 23-27] Running DRC with 2 threads (1 more like this)
    - [Vivado_Tcl 4-198] DRC finished with 0 Errors (1 more like this)
    - [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information. (1 more like this)
    - [Place 30-611] Multithreading enabled for place_design using a maximum of 2 CPUs
    - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
    - [Timing 38-35] Done setting XDC timing constraints. (2 more like this)
    - [Physopt 32-65] No nets found for high-fanout optimization.
    - [Physopt 32-232] Optimized 0 net. Created 0 new instance.
    - [Physopt 32-775] End 1 Pass. Optimized 0 net or cell. Created 0 new cell, deleted 0 existing cell and moved 0 existing cell
    - [Place 46-31] BUFG insertion identified 0 candidate nets, 0 success, 0 skipped for placement/routing, 0 skipped for timing, 0 skipped for netlist change reason.
    - [Place 30-746] Post Placement Timing Summary WNS=3.990. For the most accurate timing information please run report_timing.
    - [Common 17-83] Releasing license: Implementation
    - [Timing 38-480] Writing timing data to binary archive.
    - [Common 17-1381] The checkpoint 'F:/Digital Diploma/work/Spartan6_DSP48A1/Spartan6_DSP48A1.runs/impl_1/Spartan6_DSP48A1_placed.dcp' has been generated.
    - [runtcl-4] Executing : report_io -file Spartan6_DSP48A1_io_placed.rpt (2 more like this)

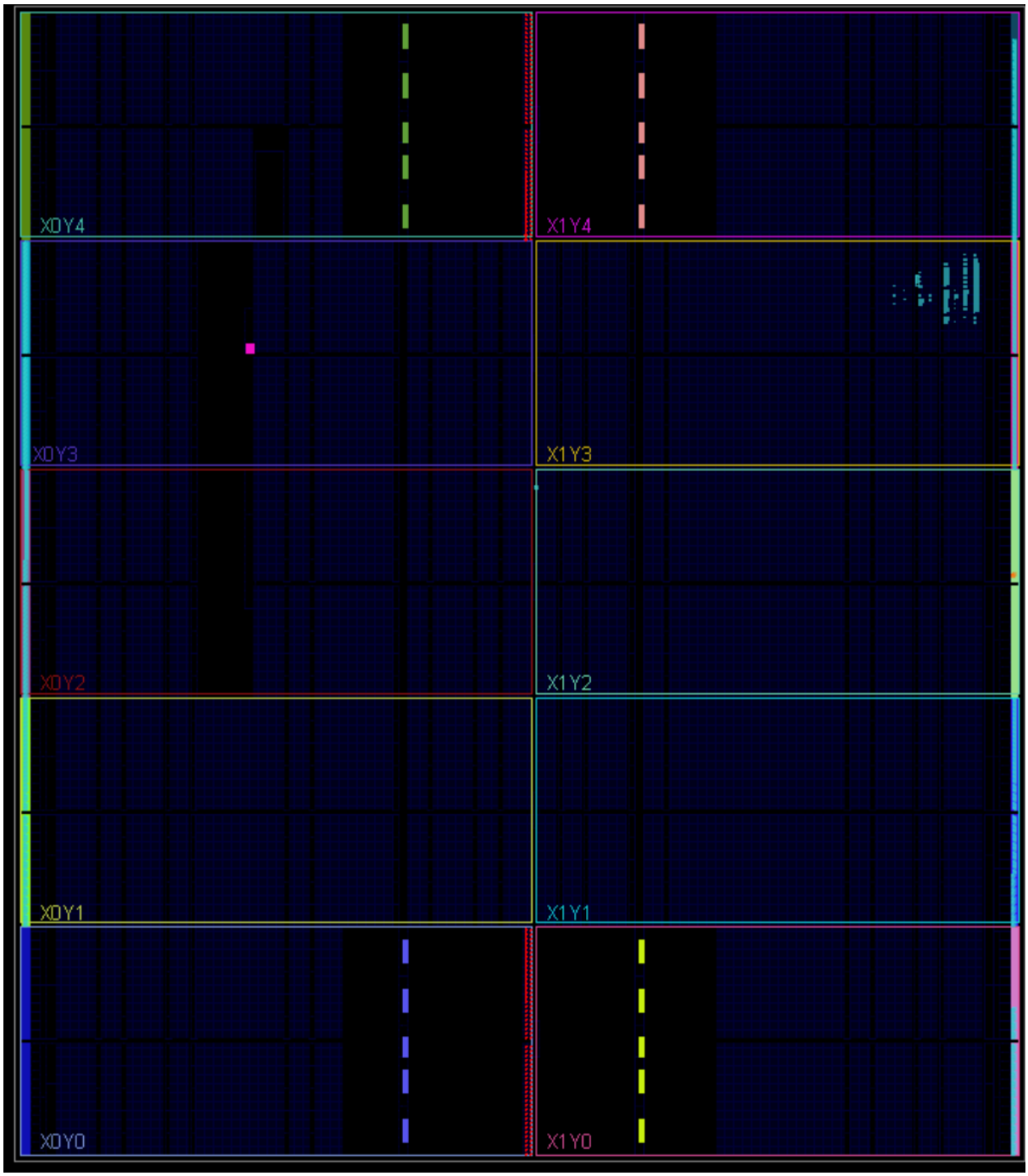
- Route Design (1 warning, 34 infos)
  - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a200t'
  - DRC (1 warning)
    - Pin Planning (1 warning)
      - [DRC CFGBVS-7] CONFIG_VOLTAGE with Config Bank VCCO: The CONFIG_MODE property of current_design specifies a configuration mode (SPIx4) that uses pins in bank 14. I/O standards used in this bank have a voltage requirement of 1.80. However, the CONFIG_VOLTAGE for current_design is set to 3.3. Ensure that your configuration voltage is compatible with the I/O standards in banks used by your configuration mode. Refer to device configuration user guide for more information. Pins used by config mode: V28 (IO_L1P_T0_D00_MOSI_14), V29 (IO_L1N_T0_D01_DIN_14), V26 (IO_L2P_T0_D02_14), V27 (IO_L2N_T0_D03_14), W26 (IO_L3P_T0_DQS_PUDC_B_14), and Y27 (IO_L6P_T0_FCS_B_14)
  - [Vivado_Tcl 4-198] DRC finished with 0 Errors, 1 Warnings
  - [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.
  - [Route 35-254] Multithreading enabled for route_design using a maximum of 2 CPUs
  - [Route 35-416] Intermediate Timing Summary | WNS=3.974 | TNS=0.000 | WHS=-0.105 | THS=-0.105 | (2 more like this)
  - [Route 35-57] Estimated Timing Summary | WNS=3.977 | TNS=0.000 | WHS=0.246 | THS=0.000 |
  - [Route 35-327] The final timing numbers are based on the router estimated timing analysis. For a complete and accurate timing signoff, please run report_timing_summary.
  - [Route 35-16] Router Completed Successfully
  - [Common 17-83] Releasing license: Implementation
  - [Timing 38-480] Writing timing data to binary archive.
  - [Common 17-1381] The checkpoint 'F:/Digital Diploma/work/Spartan6_DSP48A1/Spartan6_DSP48A1.runs/impl_1/Spartan6_DSP48A1_routed.dcp' has been generated.
  - [DRC 23-27] Running DRC with 2 threads (1 more like this)
  - [Coretcl 2-168] The results of DRC are in file Spartan6_DSP48A1_drc_routed.rpt.
  - [runtcl-4] Executing : report_drc -file Spartan6_DSP48A1_drc_routed.rpt -pb Spartan6_DSP48A1_drc_routed.pb -rpx Spartan6_DSP48A1_drc_routed.rpx (7 more like this)
  - [Timing 38-35] Done setting XDC timing constraints. (2 more like this)
  - [DRC 23-133] Running Methodology with 2 threads
  - [Coretcl 2-1520] The results of Report Methodology are in file Spartan6_DSP48A1_methodology_drc_routed.rpt.
  - [Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.
  - [Timing 38-91] UpdateTimingParams: Speed grade: -3, Delay Type: min_max, Timing Stage: Requireds. (1 more like this)
  - [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (1 more like this)
- Implemented Design (9 infos)
  - General Messages (9 infos)
    - [Netlist 29-17] Analyzing 207 Unisim elements for replacement
    - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
    - [Project 1-479] Netlist was created with Vivado 2018.2
    - [Project 1-570] Preparing netlist for logic optimization
    - [Timing 38-478] Restoring timing data from binary archive.
    - [Timing 38-479] Binary timing data restore complete.
    - [Project 1-856] Restoring constraints from binary archive.
    - [Project 1-853] Binary constraint restore complete.
    - [Project 1-111] Unisim Transformation Summary:
      No Unisim elements were transformed.

Name	Slice LUTs (133800)	Slice Registers (267600)	Slice (33450)	LUT as Logic (133800)	LUT Flip Flop Pairs (133800)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
N Spartan6_DSP48A1	181	179	92	181	50	1	327	1
A1_REG (reg_mux)	0	18	8	0	0	0	0	0
B1_REG (reg_mux_0)	0	36	14	0	0	0	0	0
C_REG (reg_mux__pa...	0	48	13	0	0	0	0	0
CY0 (reg_mux__para...	0	2	2	0	0	0	0	0
CY1 (reg_mux__para...	1	1	1	1	1	0	0	0
D_REG (reg_mux_2)	0	18	10	0	0	0	0	0
OPMODE_REG (reg_...	180	8	55	180	0	0	0	0
P_REG (reg_mux__pa...	0	48	12	0	0	0	0	0

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3.979 ns	Worst Hold Slack (WHS):	0.261 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	106	Total Number of Endpoints:	106	Total Number of Endpoints:	181

All user specified timing constraints are met.


X0Y4
X1Y4
X0Y3
X1Y3
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0