SPI Protocol

Final Project

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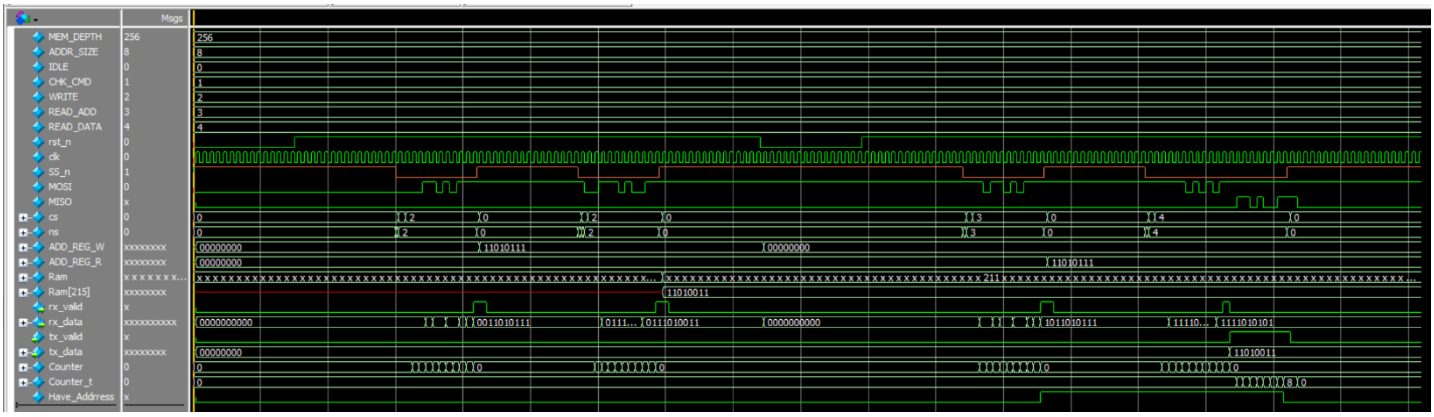
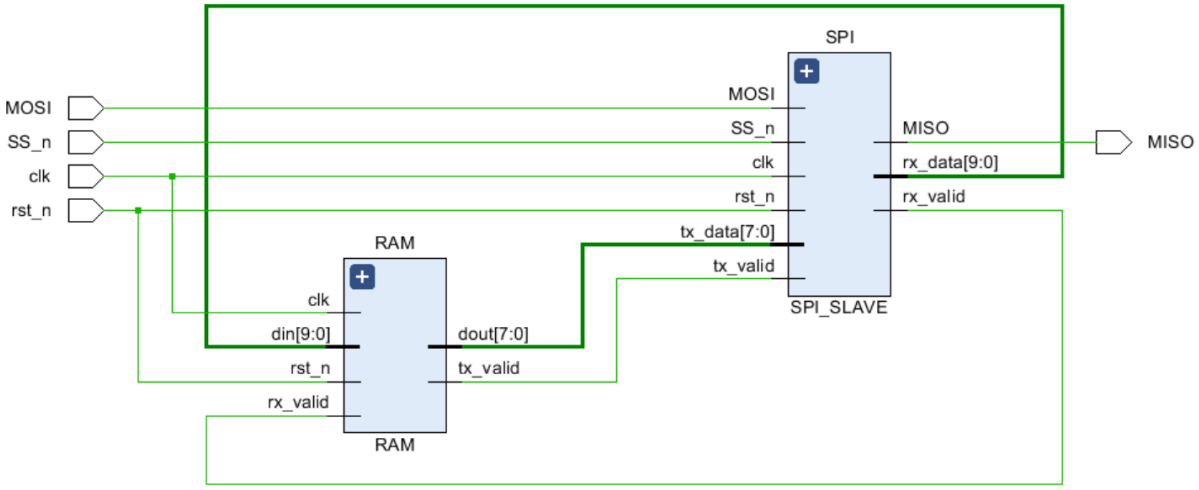
1-Snippets from the waveforms:



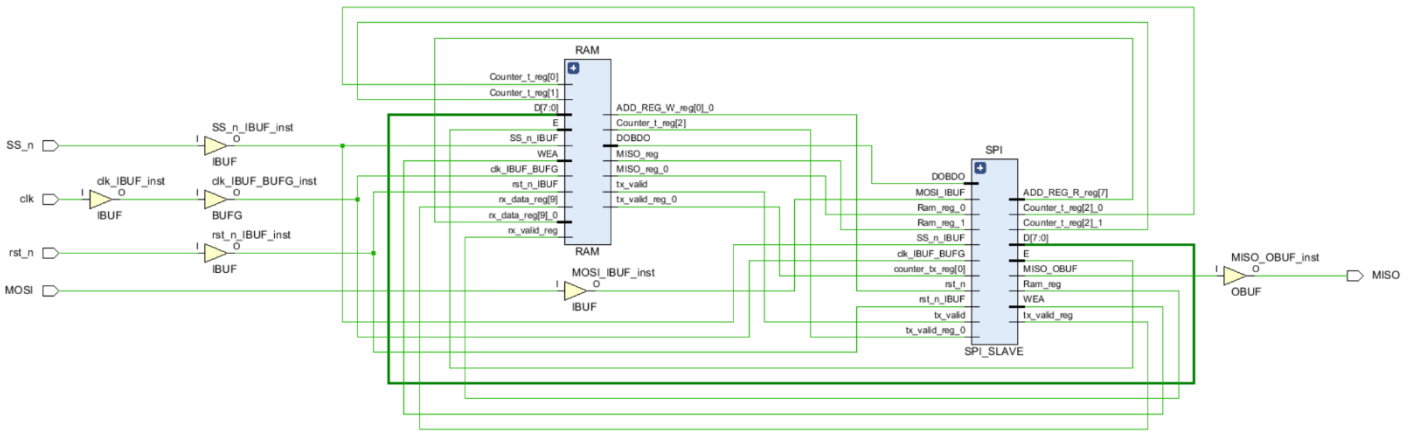
2-Synthesis snippets:

- Sequential:

  Schematic after the elaboration:



  Schematic after the Synthesis:



Encoding used:

```
-----------------------------------------------------------------------------------------------------
                   State |                     New Encoding |                Previous Encoding
-----------------------------------------------------------------------------------------------------
                    IDLE |                              000 |                             000
                 CHK_CMD |                              001 |                             001
                   WRITE |                              010 |                             010
                READ_ADD |                              011 |                             011
               READ_DATA |                              100 |                             100
-----------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'SPI_SLAVE'
-----------------------------------------------------------------------------
```

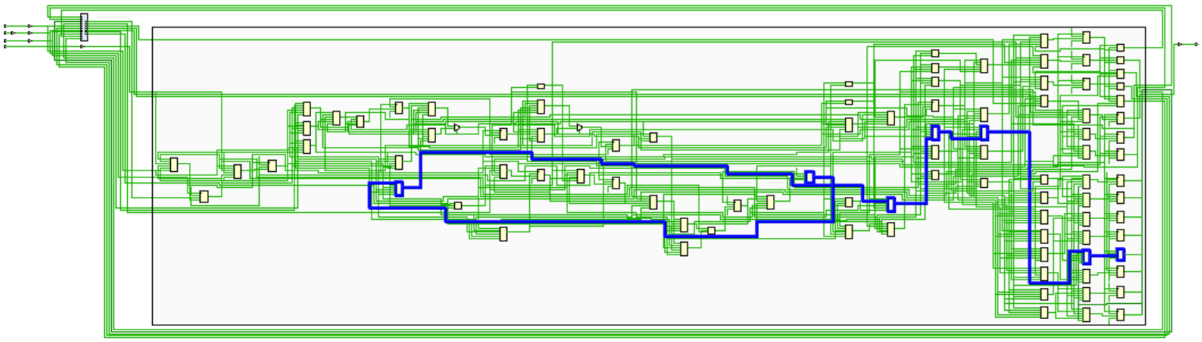
Timing report:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.264 ns	Worst Hold Slack (WHS):	0.142 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	105	Total Number of Endpoints:	105	Total Number of Endpoints:	48

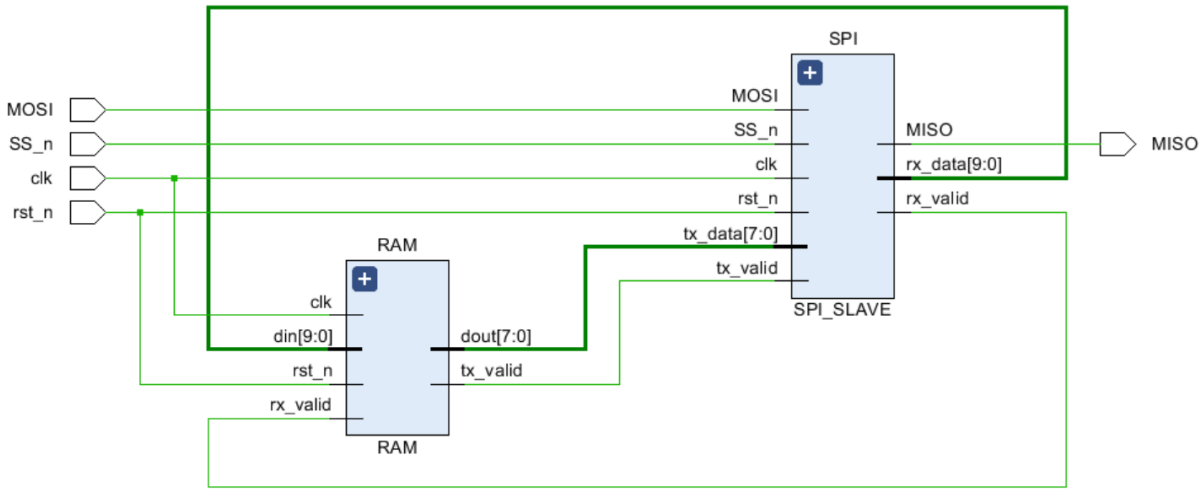
Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock
Path 1	5.264	5	6	20	SPI/FSM_sequential_cs_reg[0]/C	SPI/rx_data_reg[4]/D	4.585	1.247	3.338	10.0	sys_clk_pin	sys_clk_pin
Path 2	5.264	5	6	20	SPI/FSM_sequential_cs_reg[0]/C	SPI/rx_data_reg[5]/D	4.585	1.247	3.338	10.0	sys_clk_pin	sys_clk_pin
Path 3	5.264	5	6	20	SPI/FSM_sequential_cs_reg[0]/C	SPI/rx_data_reg[8]/D	4.585	1.247	3.338	10.0	sys_clk_pin	sys_clk_pin
Path 4	5.264	5	6	20	SPI/FSM_sequential_cs_reg[0]/C	SPI/rx_data_reg[9]/D	4.585	1.247	3.338	10.0	sys_clk_pin	sys_clk_pin
Path 5	5.277	5	6	20	SPI/FSM_sequential_cs_reg[0]/C	SPI/rx_data_reg[0]/D	4.572	1.247	3.325	10.0	sys_clk_pin	sys_clk_pin
Path 6	5.277	5	6	20	SPI/FSM_sequential_cs_reg[0]/C	SPI/rx_data_reg[1]/D	4.572	1.247	3.325	10.0	sys_clk_pin	sys_clk_pin

Snippet of the critical path highlighted:

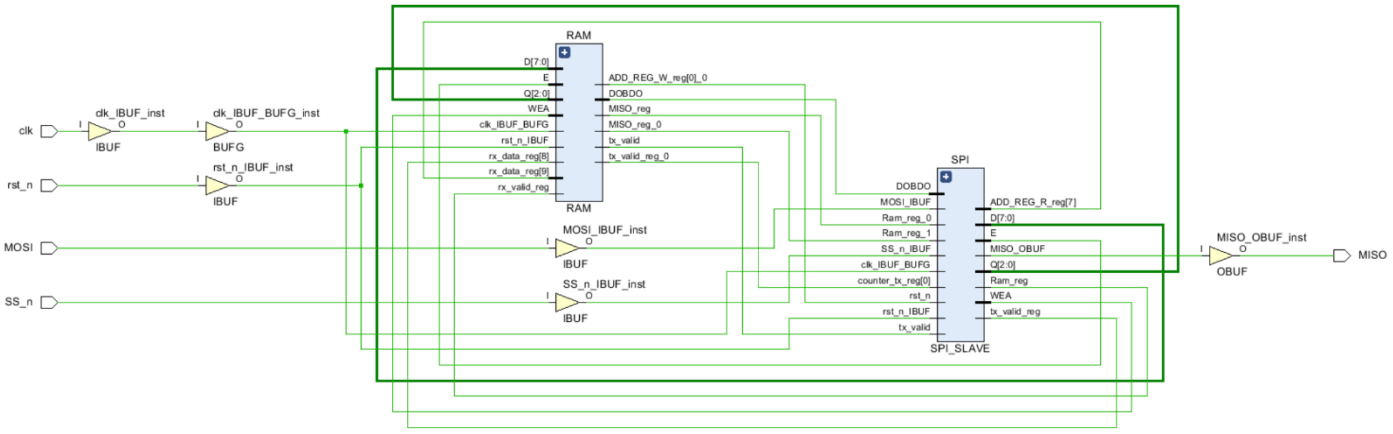


- Gray:

  Schematic after the elaboration:



  Schematic after the Synthesis:



  Encoding used:

```
----------------------------------------------------------------------------------------------------
                   State |                     New Encoding |               Previous Encoding
----------------------------------------------------------------------------------------------------
                    IDLE |                              000 |                              000
                 CHK_CMD |                              001 |                              001
                   WRITE |                              011 |                              011
                READ_ADD |                              010 |                              010
               READ_DATA |                              111 |                              110
----------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'SPI_SLAVE'
----------------------------------------------------------------------------------
```

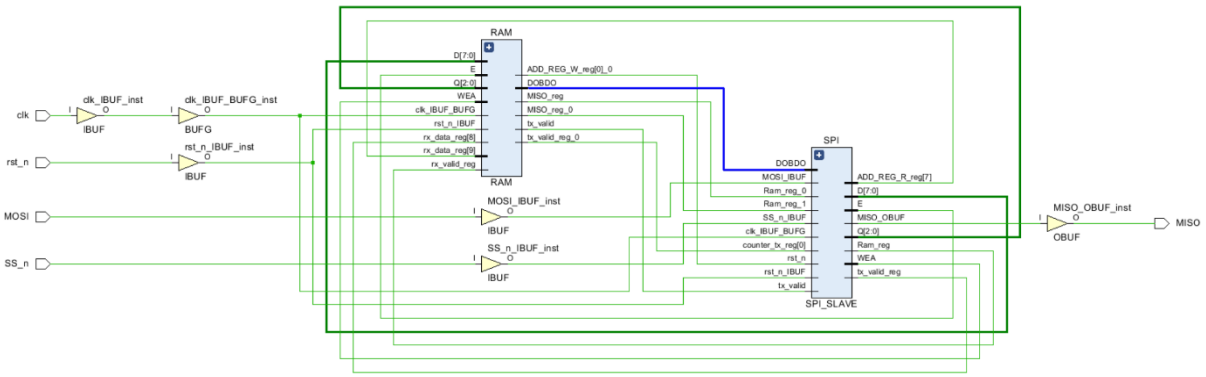
Timing report:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.242 ns	Worst Hold Slack (WHS):	0.142 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	105	Total Number of Endpoints:	105	Total Number of Endpoints:	48

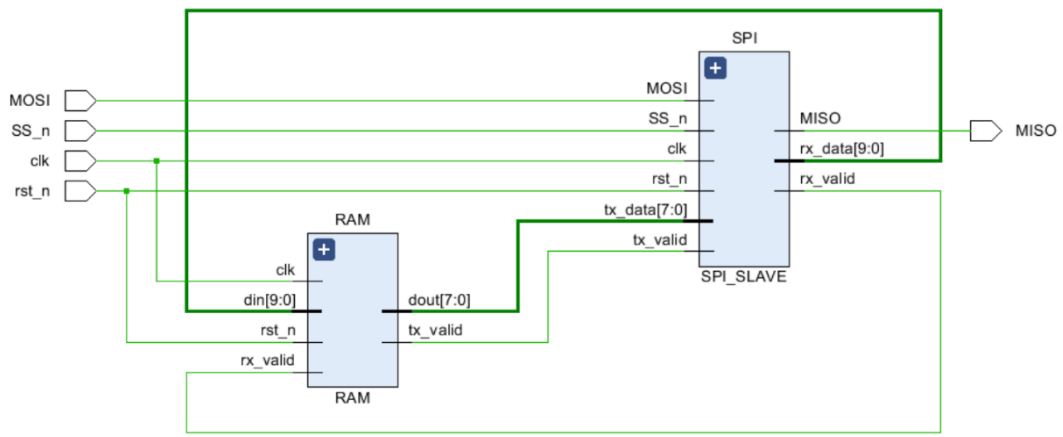
Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock
Path 1	5.242	2	3	1	RAM/Ram_reg/CLKBWRCLK	SPI/MISO_reg/D	4.607	2.696	1.911	10.0	sys_clk_pin	sys_clk_pin
Path 2	6.482	2	3	23	SPI/Counter_reg[3]/C	SPI/Counter_reg[0]/CE	3.136	0.901	2.235	10.0	sys_clk_pin	sys_clk_pin
Path 3	6.482	2	3	23	SPI/Counter_reg[3]/C	SPI/Counter_reg[1]/CE	3.136	0.901	2.235	10.0	sys_clk_pin	sys_clk_pin
Path 4	6.482	2	3	23	SPI/Counter_reg[3]/C	SPI/Counter_reg[2]/CE	3.136	0.901	2.235	10.0	sys_clk_pin	sys_clk_pin
Path 5	6.482	2	3	23	SPI/Counter_reg[3]/C	SPI/Counter_reg[3]/CE	3.136	0.901	2.235	10.0	sys_clk_pin	sys_clk_pin
Path 6	6.964	1	2	6	SPI/rx_data_reg[9]/C	RAM/Ram_reg/WEA[0]	2.324	0.751	1.573	10.0	sys_clk_pin	sys_clk_pin
Path 7	6.964	1	2	6	SPI/rx_data_reg[9]/C	RAM/Ram_reg/WEA[1]	2.324	0.751	1.573	10.0	sys_clk_pin	sys_clk_pin
Path 8	7.023	3	4	19	RAM/tx_valid_reg/C	SPI/Counter_reg[1]/D	2.826	0.999	1.827	10.0	sys_clk_pin	sys_clk_pin
Path 9	7.029	2	3	20	SPI/FSM_gray_cs_reg[1]/C	SPI/rx_data_reg[5]/D	2.820	0.875	1.945	10.0	sys_clk_pin	sys_clk_pin
Path 10	7.029	2	3	20	SPI/FSM_gray_cs_reg[1]/C	SPI/rx_data_reg[7]/D	2.820	0.875	1.945	10.0	sys_clk_pin	sys_clk_pin

Snippet of the critical path highlighted:

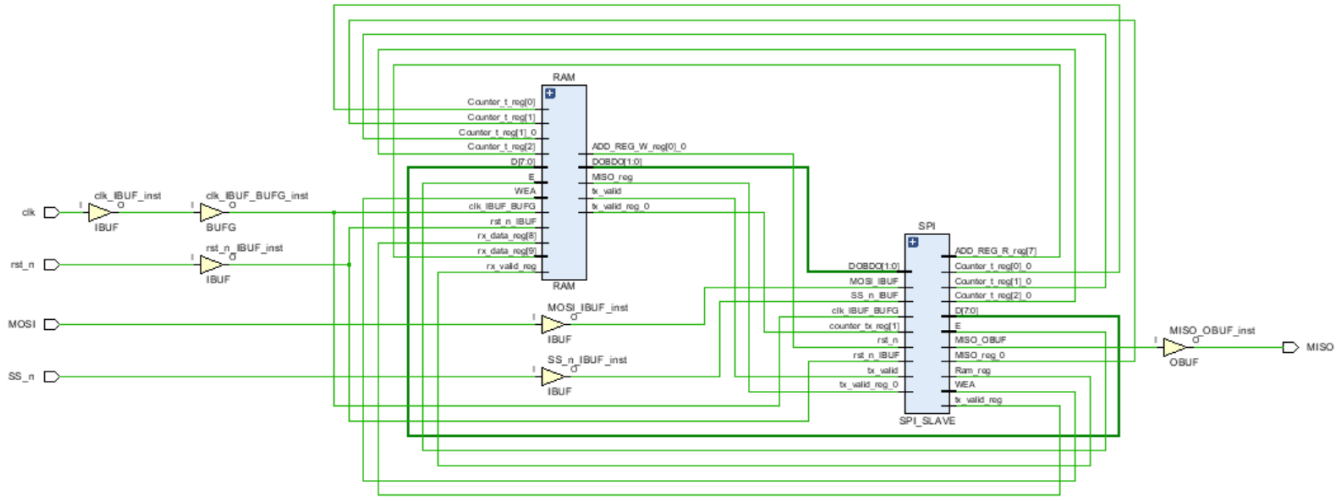


- OneHot:

Schematic after the elaboration:



Schematic after the Synthesis:



Encoding used:

```
    Parameter IDLE bound to: 5'b00001
    Parameter CHK_CMD bound to: 5'b00010
    Parameter WRITE bound to: 5'b00100
    Parameter READ_ADD bound to: 5'b01000
    Parameter READ_DATA bound to: 5'b10000
INFO: [Synth 8-5534] Detected attribute (* fsm_encoding = "one-hot" *)
```

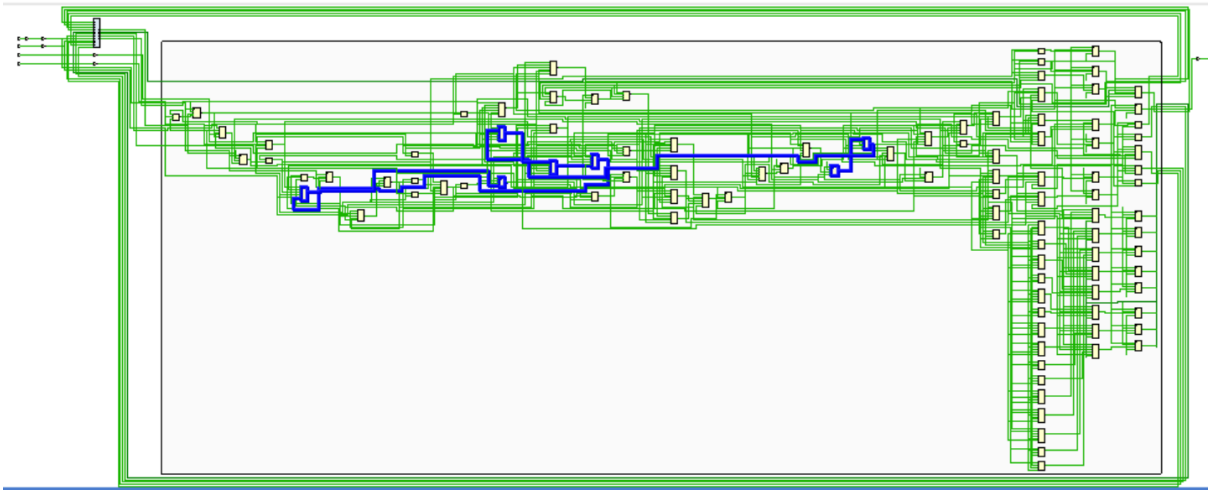
Timing report:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	4.578 ns	Worst Hold Slack (WHS):	0.146 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	111	Total Number of Endpoints:	111	Total Number of Endpoints:	50

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock
Path 1	4.578	5	6	14	SPI/cs_reg[0]/C	SPI/Counter_reg[0]/S	4.809	1.247	3.562	10.0	sys_clk_pin	sys_clk_pin
Path 2	4.578	5	6	14	SPI/cs_reg[0]/C	SPI/Counter_reg[1]/S	4.809	1.247	3.562	10.0	sys_clk_pin	sys_clk_pin
Path 3	4.578	5	6	14	SPI/cs_reg[0]/C	SPI/Counter_reg[2]/S	4.809	1.247	3.562	10.0	sys_clk_pin	sys_clk_pin
Path 4	4.578	5	6	14	SPI/cs_reg[0]/C	SPI/Counter_reg[3]/S	4.809	1.247	3.562	10.0	sys_clk_pin	sys_clk_pin
Path 5	4.872	3	4	1	RAM/Ram_reg/CLKBWRCLK	SPI/MISO_reg/D	4.977	2.826	2.151	10.0	sys_clk_pin	sys_clk_pin
Path 6	5.709	4	5	14	SPI/cs_reg[0]/C	SPI/Counter_reg[0]/CE	3.909	1.123	2.786	10.0	sys_clk_pin	sys_clk_pin
Path 7	5.709	4	5	14	SPI/cs_reg[0]/C	SPI/Counter_reg[1]/CE	3.909	1.123	2.786	10.0	sys_clk_pin	sys_clk_pin
Path 8	5.709	4	5	14	SPI/cs_reg[0]/C	SPI/Counter_reg[2]/CE	3.909	1.123	2.786	10.0	sys_clk_pin	sys_clk_pin
Path 9	5.709	4	5	14	SPI/cs_reg[0]/C	SPI/Counter_reg[3]/CE	3.909	1.123	2.786	10.0	sys_clk_pin	sys_clk_pin
Path 10	6.254	5	6	16	SPI/cs_reg[3]/C	SPI/rx_valid_reg/D	3.595	1.247	2.348	10.0	sys_clk_pin	sys_clk_pin

Snippet of the critical path highlighted:

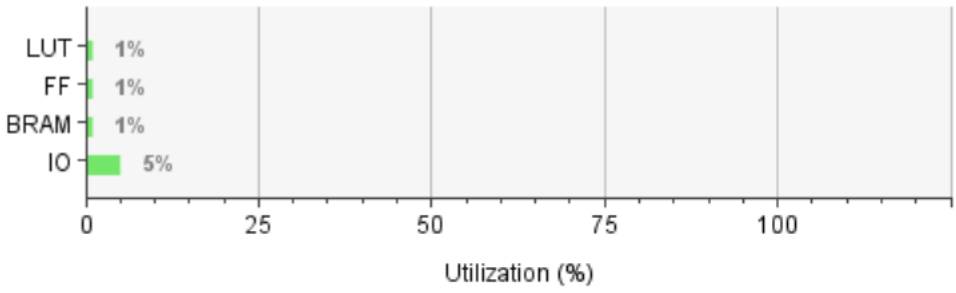


Implementation snippets:

- Sequential:

  Utilization report:

Resource	Utilization	Available	Utilization %
LUT	76	20800	0.37
FF	45	41600	0.11
BRAM	0.50	50	1.00
IO	5	106	4.72

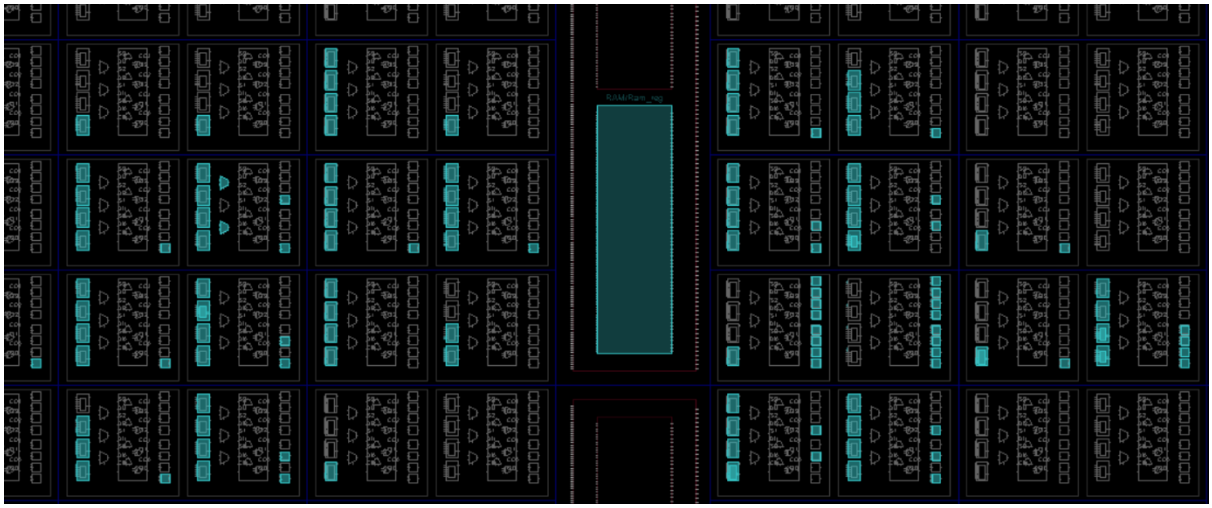


  Timing report:

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.036 ns	Worst Hold Slack (WHS):	0.077 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	106	Total Number of Endpoints:	106	Total Number of Endpoints:	48

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock
Path 1	5.036	3	1	RAM/Ram_reg/CLKBWRCLK	SPI/MISO_reg/D	4.943	2.826	2.117	10.0	sys_clk_pin	sys_clk_pin
Path 2	5.369	5	25	SPI/FSM_sequential_cs_reg[1]/C	SPI/rx_data_reg[9]/D	4.523	1.076	3.447	10.0	sys_clk_pin	sys_clk_pin
Path 3	5.383	5	25	SPI/FSM_sequential_cs_reg[1]/C	SPI/rx_data_reg[2]/D	4.509	1.076	3.433	10.0	sys_clk_pin	sys_clk_pin
Path 4	5.399	5	25	SPI/FSM_sequential_cs_reg[1]/C	SPI/rx_data_reg[4]/D	4.541	1.076	3.465	10.0	sys_clk_pin	sys_clk_pin
Path 5	5.403	5	25	SPI/FSM_sequential_cs_reg[1]/C	SPI/rx_data_reg[8]/D	4.537	1.076	3.461	10.0	sys_clk_pin	sys_clk_pin
Path 6	5.411	5	25	SPI/FSM_sequential_cs_reg[1]/C	SPI/rx_data_reg[6]/D	4.531	1.076	3.455	10.0	sys_clk_pin	sys_clk_pin
Path 7	5.499	5	25	SPI/FSM_sequential_cs_reg[1]/C	SPI/rx_data_reg[3]/D	4.393	1.076	3.317	10.0	sys_clk_pin	sys_clk_pin
Path 8	5.502	5	25	SPI/FSM_sequential_cs_reg[1]/C	SPI/rx_data_reg[5]/D	4.390	1.076	3.314	10.0	sys_clk_pin	sys_clk_pin
Path 9	5.538	5	25	SPI/FSM_sequential_cs_reg[1]/C	SPI/rx_data_reg[7]/D	4.401	1.076	3.325	10.0	sys_clk_pin	sys_clk_pin
Path 10	5.589	5	25	SPI/FSM_sequential_cs_reg[1]/C	SPI/rx_data_reg[1]/D	4.301	1.076	3.225	10.0	sys_clk_pin	sys_clk_pin

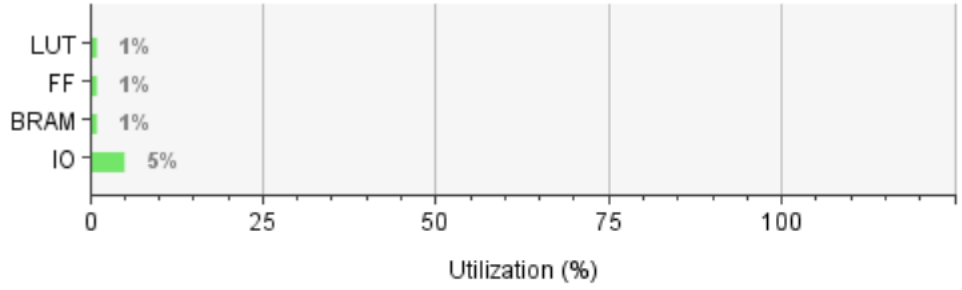
FPGA device:



- Gray:

Utilization report:

Resource	Utilization	Available	Utilization %
LUT	72	20800	0.35
FF	45	41600	0.11
BRAM	0.50	50	1.00
IO	5	106	4.72

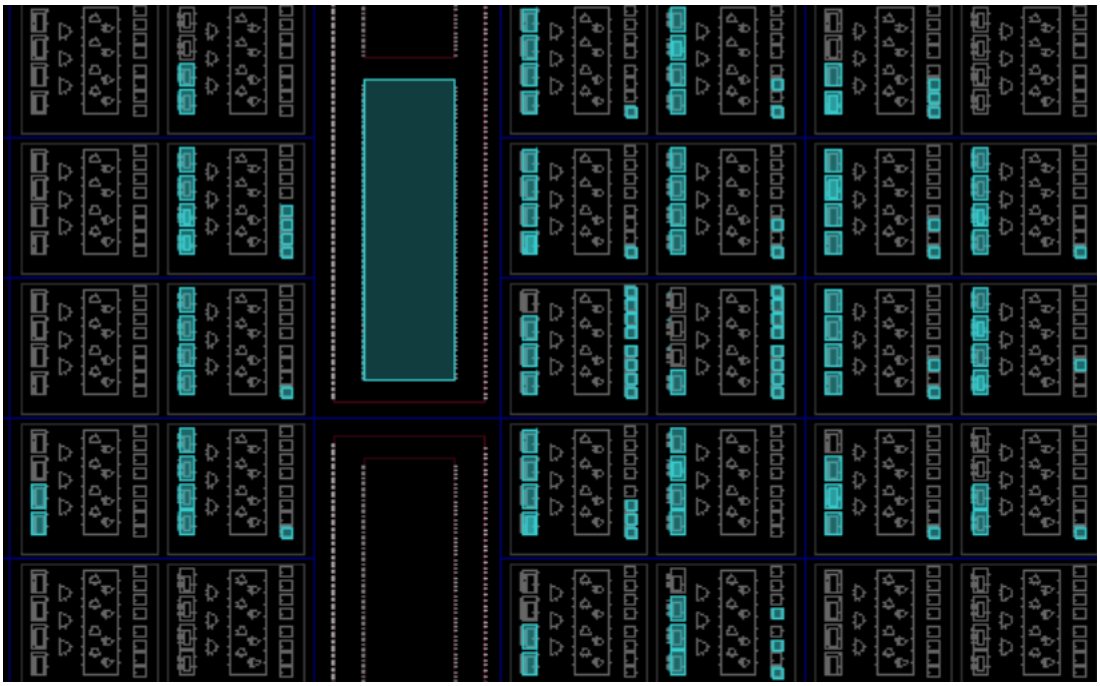


Timing report:

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.189 ns	Worst Hold Slack (WHS):	0.080 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	106	Total Number of Endpoints:	106	Total Number of Endpoints:	48

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock
Path 1	5.189	2	2	1	RAM/Ram_reg/CLKBWRCLK	SPI/MISO_reg/D	4.741	2.702	2.039	10.0	sys_clk_pin	sys_clk_pin
Path 2	5.583	2	3	26	SPI/Counter_reg[0]/C	SPI/Counter_reg[0]/CE	4.177	0.940	3.237	10.0	sys_clk_pin	sys_clk_pin
Path 3	5.627	3	3	26	SPI/Counter_reg[0]/C	SPI/Counter_reg[1]/D	4.311	1.064	3.247	10.0	sys_clk_pin	sys_clk_pin
Path 4	5.634	3	3	26	SPI/Counter_reg[0]/C	SPI/Counter_reg[3]/D	4.308	1.064	3.244	10.0	sys_clk_pin	sys_clk_pin
Path 5	5.642	3	3	26	SPI/Counter_reg[0]/C	SPI/Counter_reg[2]/D	4.337	1.090	3.247	10.0	sys_clk_pin	sys_clk_pin
Path 6	5.875	2	3	26	SPI/Counter_reg[0]/C	SPI/Counter_reg[1]/CE	3.816	0.940	2.876	10.0	sys_clk_pin	sys_clk_pin
Path 7	5.875	2	3	26	SPI/Counter_reg[0]/C	SPI/Counter_reg[2]/CE	3.816	0.940	2.876	10.0	sys_clk_pin	sys_clk_pin
Path 8	5.875	2	3	26	SPI/Counter_reg[0]/C	SPI/Counter_reg[3]/CE	3.816	0.940	2.876	10.0	sys_clk_pin	sys_clk_pin
Path 9	6.083	3	3	26	SPI/Counter_reg[0]/C	SPI/rx_valid_reg/D	3.888	1.064	2.824	10.0	sys_clk_pin	sys_clk_pin
Path 10	6.287	2	2	26	SPI/Counter_reg[0]/C	SPI/rx_data_reg[0]/D	3.604	0.940	2.664	10.0	sys_clk_pin	sys_clk_pin

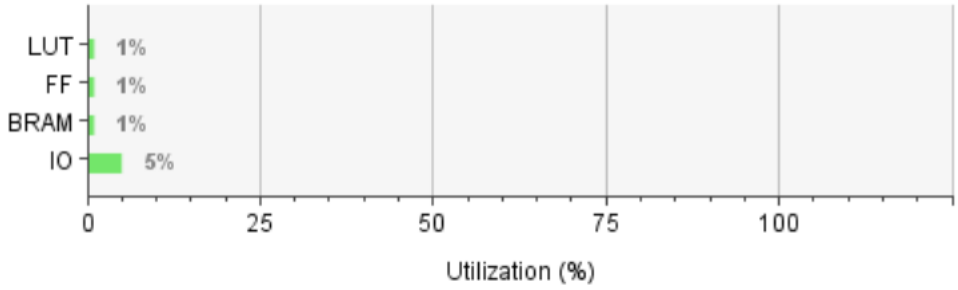
FPGA device:



- OneHot:

  Utilization report:

Resource	Utilization	Available	Utilization %
LUT	72	20800	0.35
FF	47	41600	0.11
BRAM	0.50	50	1.00
IO	5	106	4.72



  Timing report:

Setup

Worst Negative Slack (WNS):	4.536 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	112

Hold

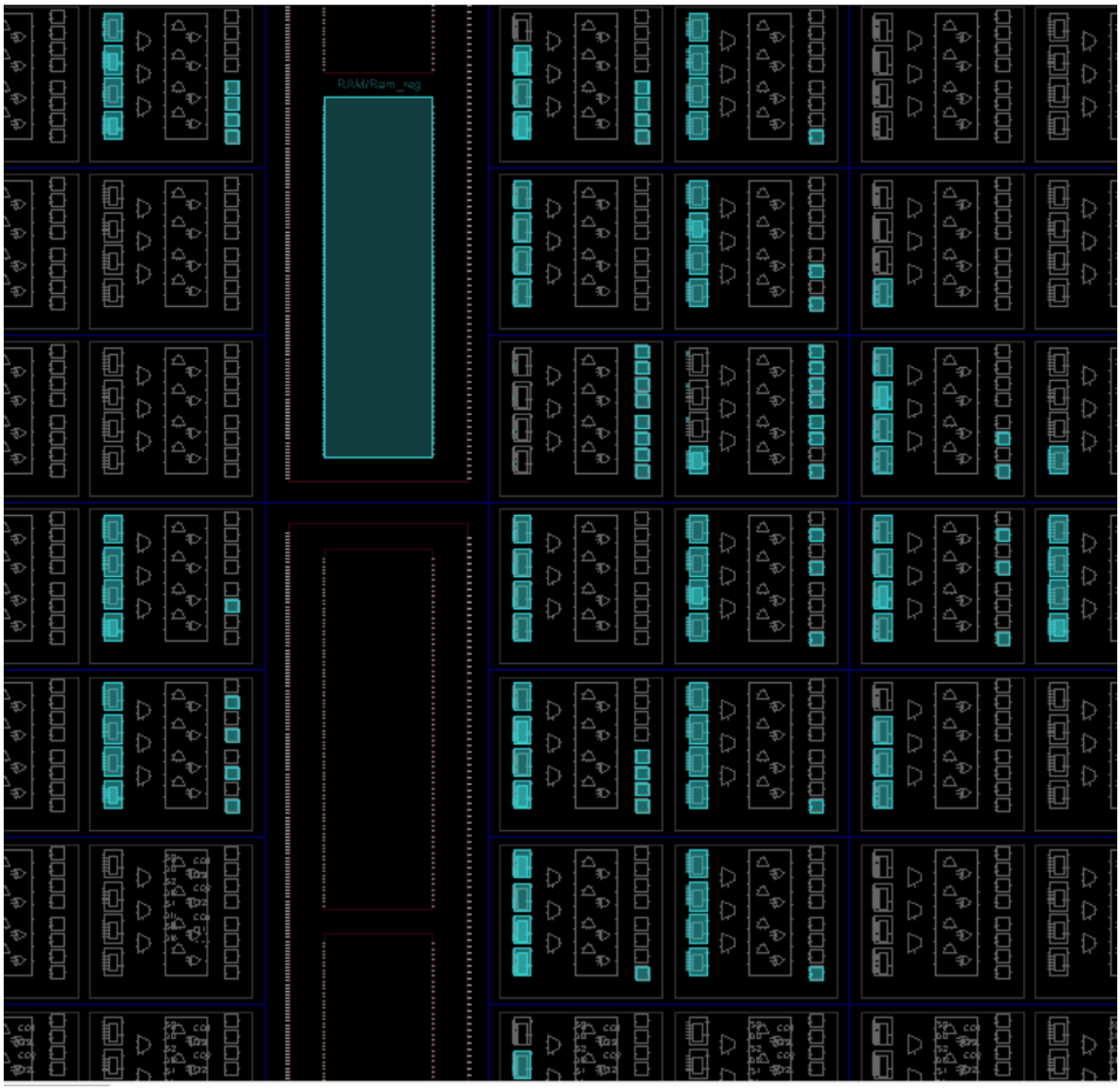
Worst Hold Slack (WHS):	0.067 ns
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	112

Pulse Width

Worst Pulse Width Slack (WPWS):	4.500 ns
Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	50

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock
Path 1	4.536	5	6	14	SPI/cs_reg[0]/C	SPI/Counter_reg[0]/S	4.800	1.306	3.494	10.0	sys_clk_pin	sys_clk_pin
Path 2	4.536	5	6	14	SPI/cs_reg[0]/C	SPI/Counter_reg[1]/S	4.800	1.306	3.494	10.0	sys_clk_pin	sys_clk_pin
Path 3	4.536	5	6	14	SPI/cs_reg[0]/C	SPI/Counter_reg[2]/S	4.800	1.306	3.494	10.0	sys_clk_pin	sys_clk_pin
Path 4	4.536	5	6	14	SPI/cs_reg[0]/C	SPI/Counter_reg[3]/S	4.800	1.306	3.494	10.0	sys_clk_pin	sys_clk_pin
Path 5	4.636	3	3	1	RAM/Ram_reg/CLKBWRCLK	SPI/MISO_reg/D	5.344	2.826	2.518	10.0	sys_clk_pin	sys_clk_pin
Path 6	4.993	4	5	14	SPI/cs_reg[0]/C	SPI/Counter_reg[3]/D	4.614	1.175	3.439	10.0	sys_clk_pin	sys_clk_pin
Path 7	5.634	4	5	14	SPI/cs_reg[0]/C	SPI/Counter_reg[0]/CE	4.058	1.182	2.876	10.0	sys_clk_pin	sys_clk_pin
Path 8	5.634	4	5	14	SPI/cs_reg[0]/C	SPI/Counter_reg[1]/CE	4.058	1.182	2.876	10.0	sys_clk_pin	sys_clk_pin
Path 9	5.634	4	5	14	SPI/cs_reg[0]/C	SPI/Counter_reg[2]/CE	4.058	1.182	2.876	10.0	sys_clk_pin	sys_clk_pin
Path 10	5.634	4	5	14	SPI/cs_reg[0]/C	SPI/Counter_reg[3]/CE	4.058	1.182	2.876	10.0	sys_clk_pin	sys_clk_pin

FPGA device:



We saw that one-hot encoding has the best Timing.

Snippet of the “Messages” tab showing no critical warnings or errors: