# Lab 1 Introduction to Cadence Analog Design Flow


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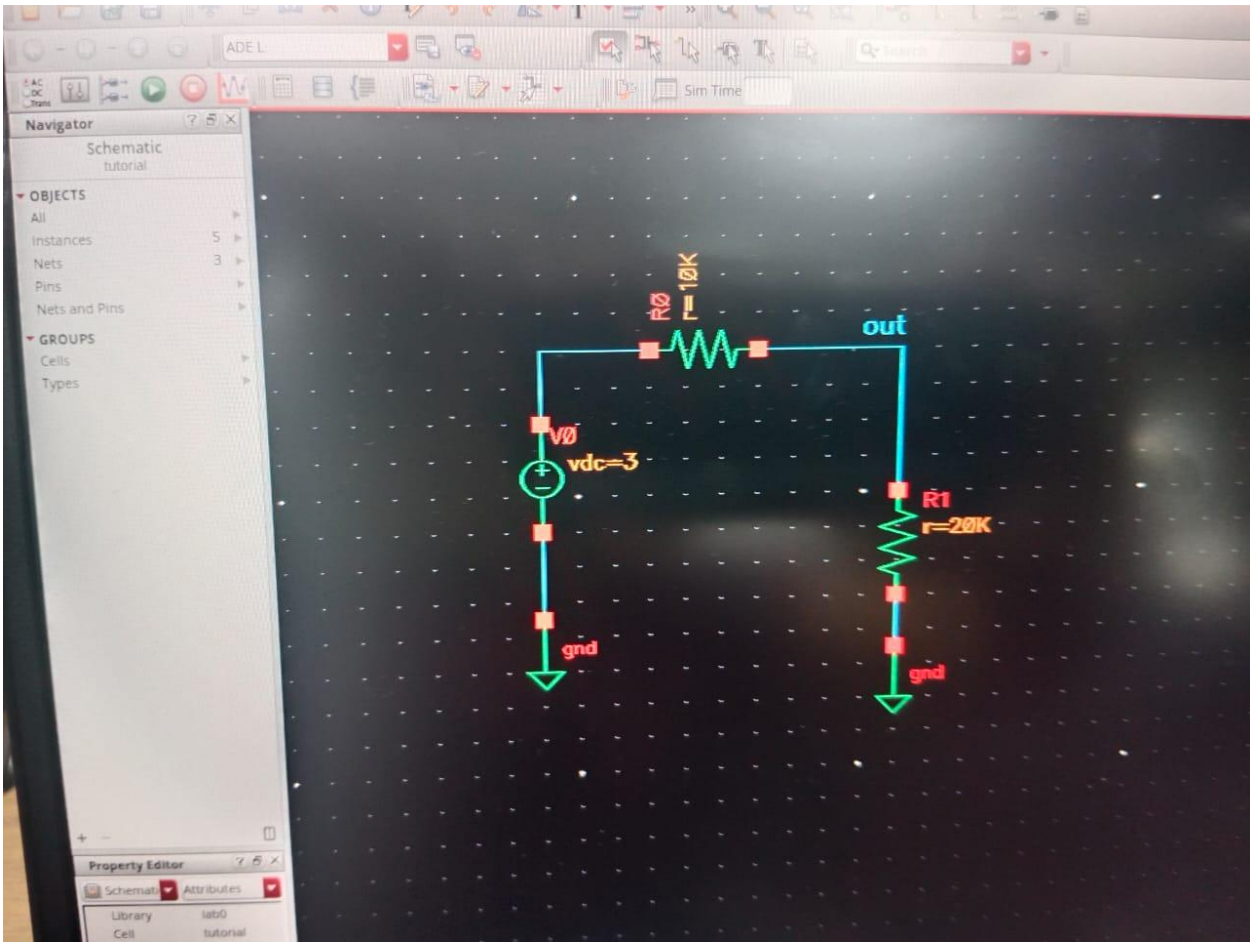
**Analog Design**

**Eng. Mariam Mamdoh**

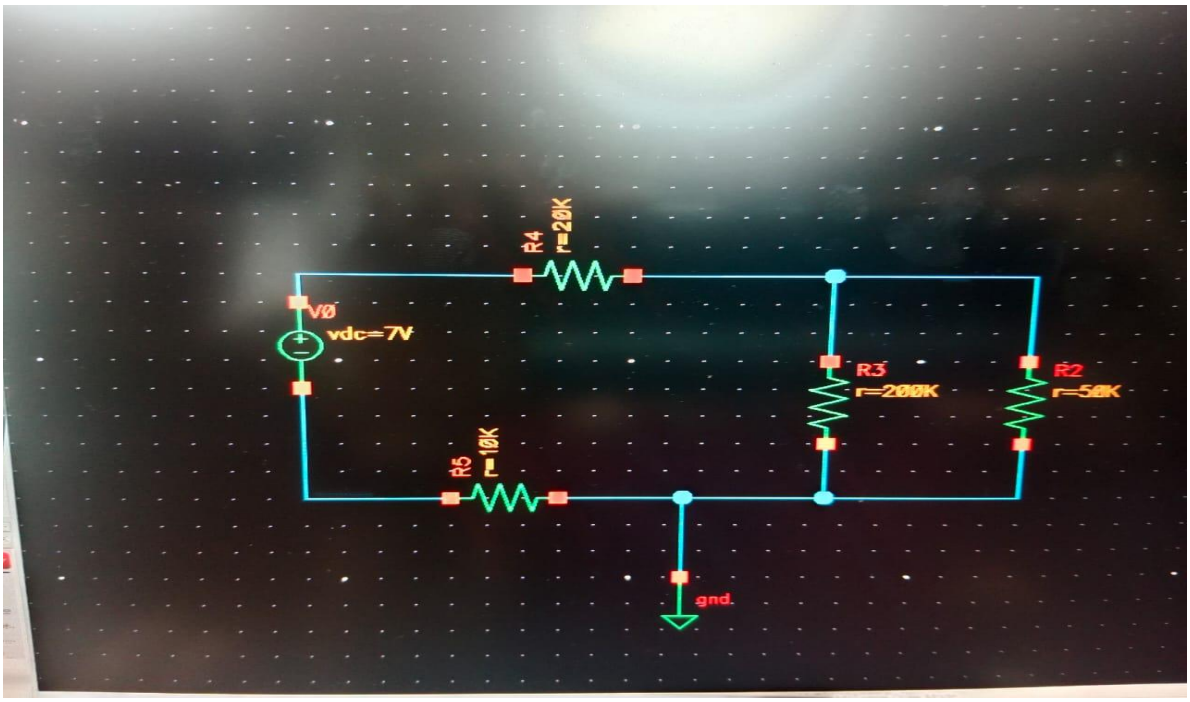
## First Circuit without operating points:



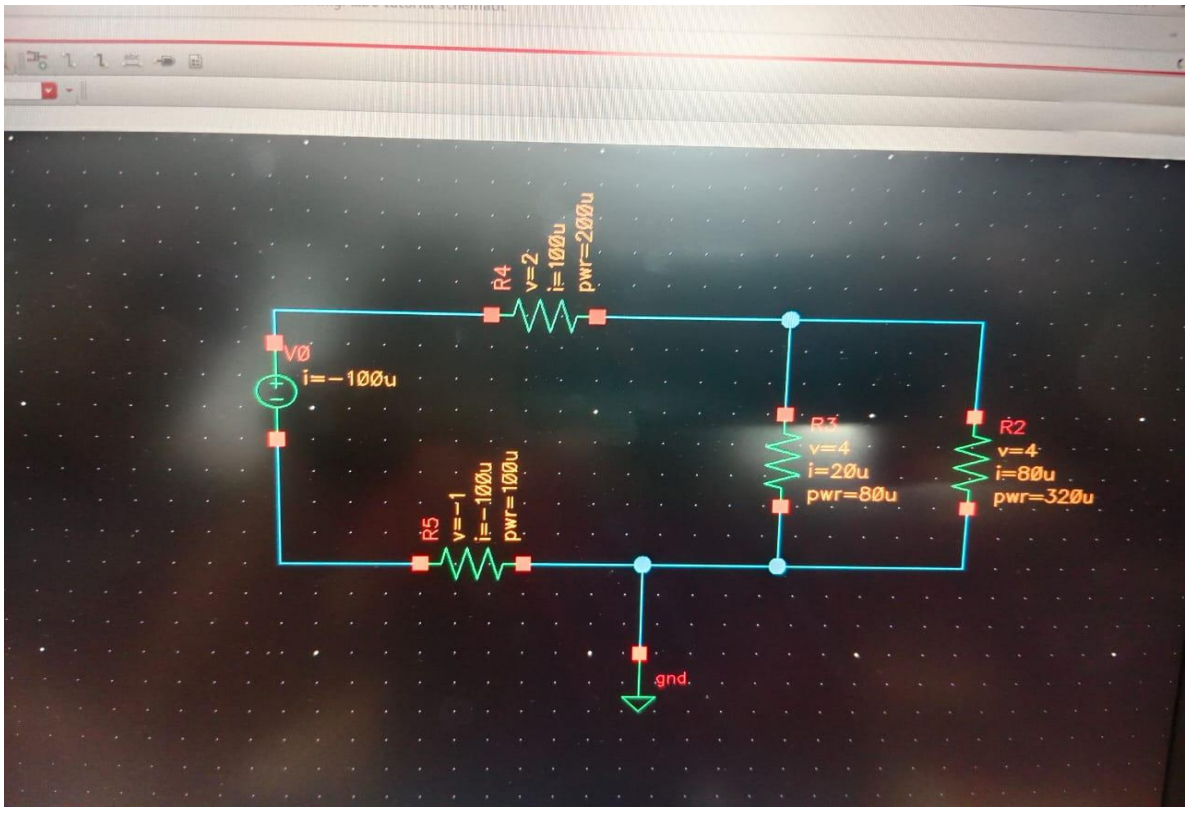
# A- Kirchhoff's Voltage Law (KVL)

**Experiment#1**

**1- schematic**




**2- The Result**



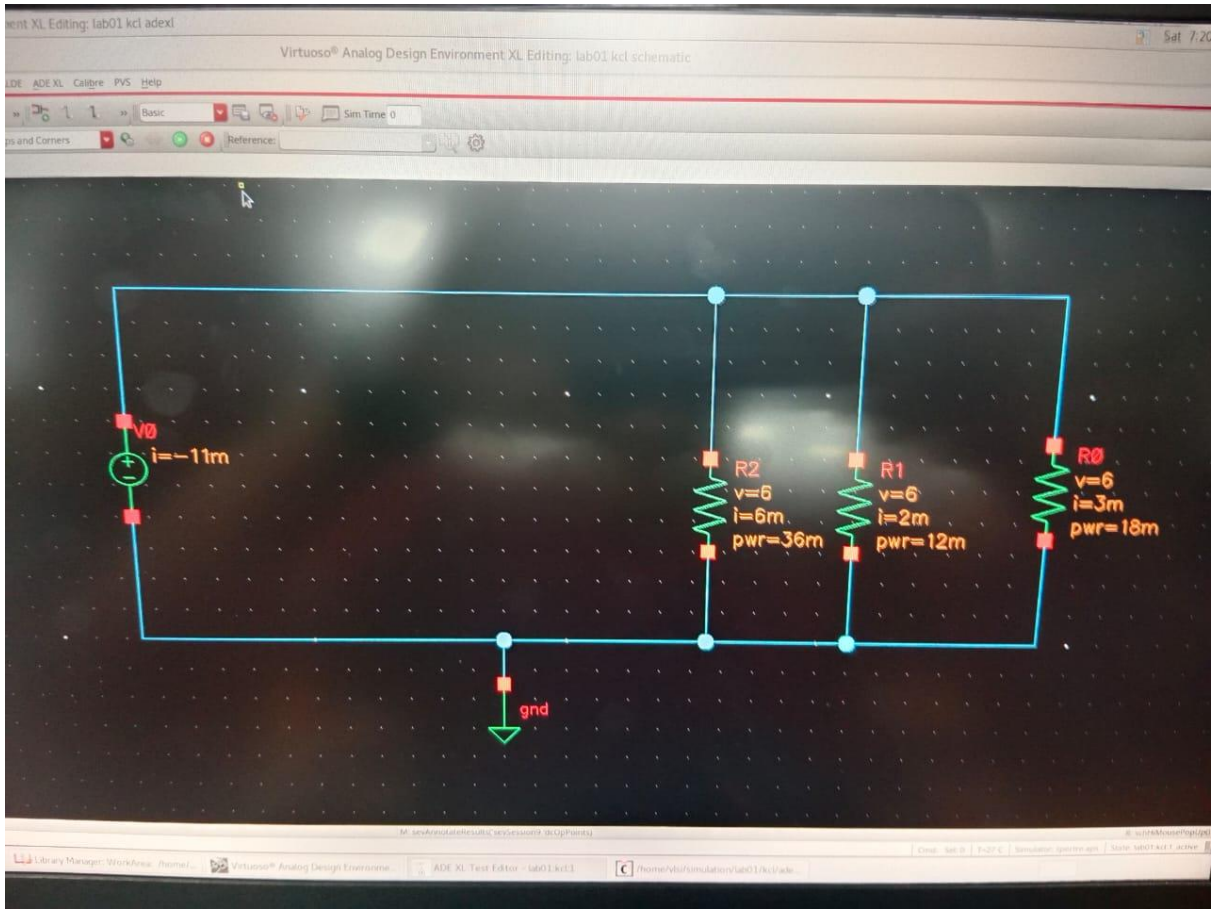
# B-Kirchhoff's Current Law (KCL)

**Experiment#1**

### 1- Schematic

We forgot to take a screenshot of the Schematic but the results are right according to the lab1 documentation.

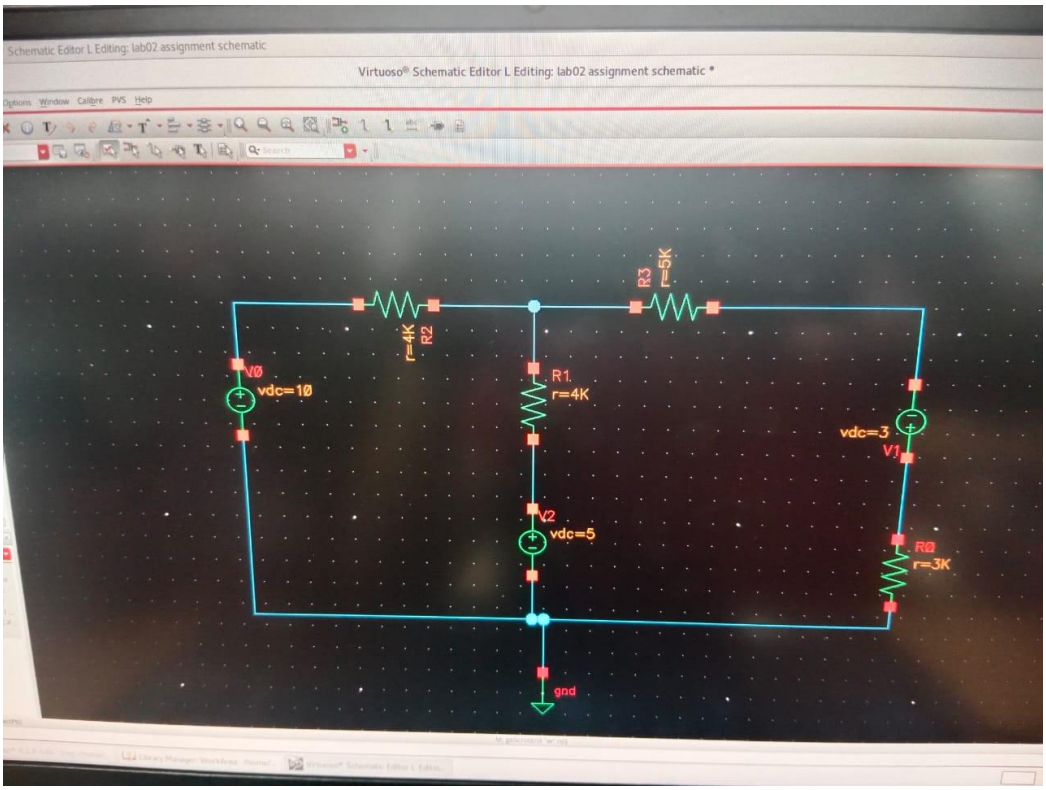
### 2- The Result



# Assignment 1

**Experiment#1**

**1- Schematic**




**2- The Result**