

Lab 1

Introduction to Cadence Analog Design Flow

1. Introduction

This lab is a tutorial on Cadence Virtuoso, which is the simulation tool we will use for the rest of the training. The official program name is Virtuoso, but the common name among users is just Cadence. We will use the name Cadence in this training. The deadline for submitting the lab worksheet is before starting the next lab. You can work on the Cadence tutorial part on your own before or after the lab, but it is a good idea to start before the lab and ask the TA during the lab if you have questions.

2. Cadence Tutorial

2.1. Cadence Setup and Launch

To set up Cadence on your instructional account, navigate to your home directory (you can do this by typing `cd ~`).

Run only once:

After connecting open a terminal and run:

```
~ee105/sp2017/cadence-setup.sh
```

This script will create a folder named `cadence_files` in your home directory, where your designs will be stored. The script will add the Cadence libraries that you'll need in this class to the program setup.

If you'd like to create a folder with a different name, run:

```
~ee105/sp2017/cadence-setup.sh folder_name
```

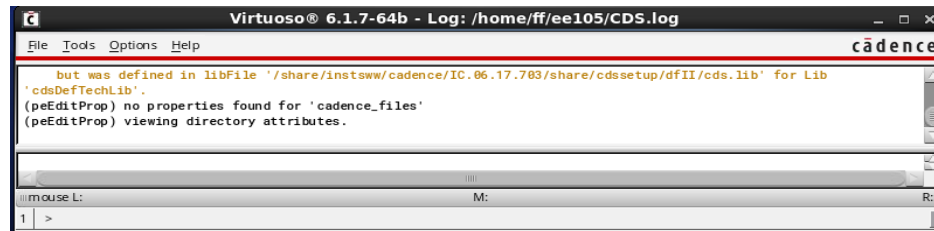
To run the program:

Open a new terminal, navigate to the folder you just made, and run:

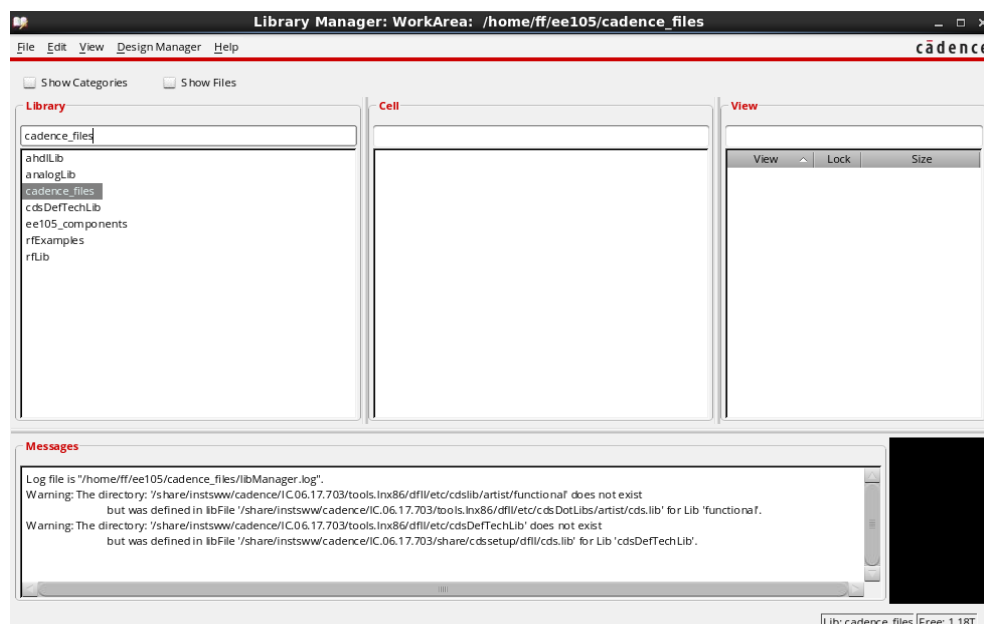
```
source cadence_setup  
virtuoso &
```

2.2. Cadence overview

After **opening Cadence**, you'll see the main window:



Go to Tools->Library Manager, it should open the following window:



The hierarchy in Cadence is:

Library (left side) -> **Cell** (middle) -> **View** (right).

A library contains multiple cells, and each cell contains multiple views.

The libraries that we will use in this class are:

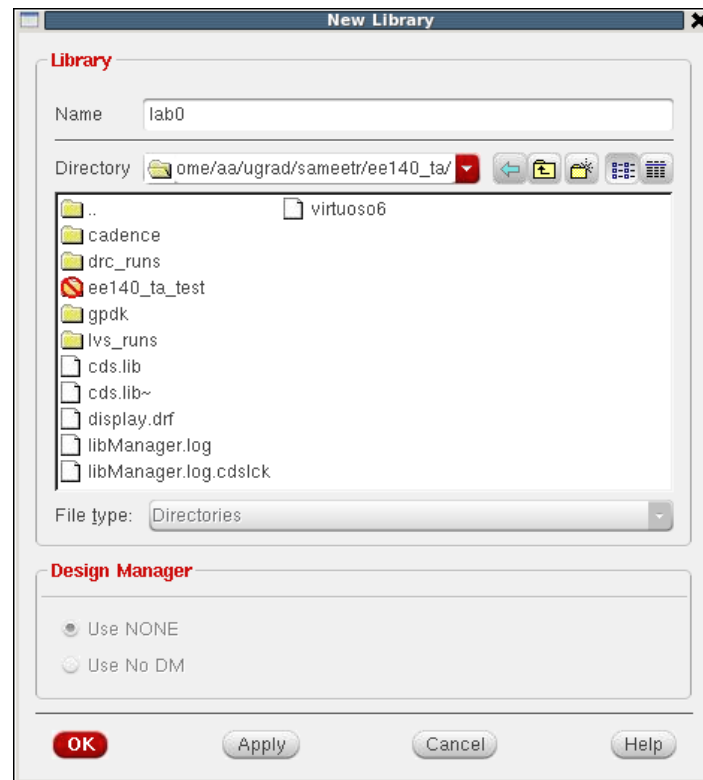
analogLib - the basic analog components (resistors, capacitors, voltage and current sources, etc)

The views that we will use for each cell are:

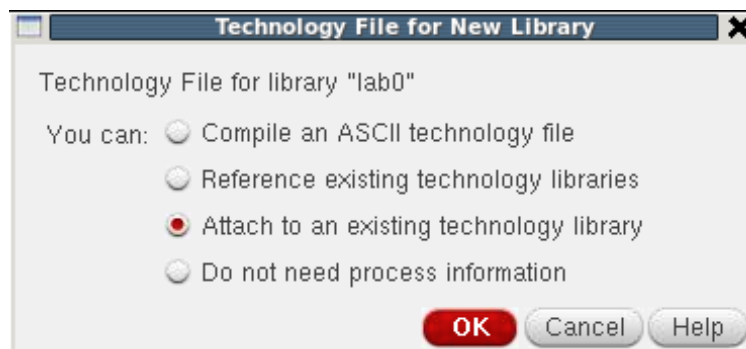
- **schematic** - the actual circuit, the components and interconnections
- **symbol** - the appearance of the cell in another schematic view

Creating a new Library

To **create a new library**, to do this, go to the library manager and click **File→ New→ Library**. A **new window** will pop up. Type “**lab0**” in the name field and press **OK**.



At this point, Cadence will prompt you for something called a Technology File. Select to “**Attach to an existing technology library**” The technology file is collection of information and libraries that define the layers and devices available for a given process technology.



For this class, we will not use any technology file. Therefore, go ahead and choose ‘Do not need process information.’

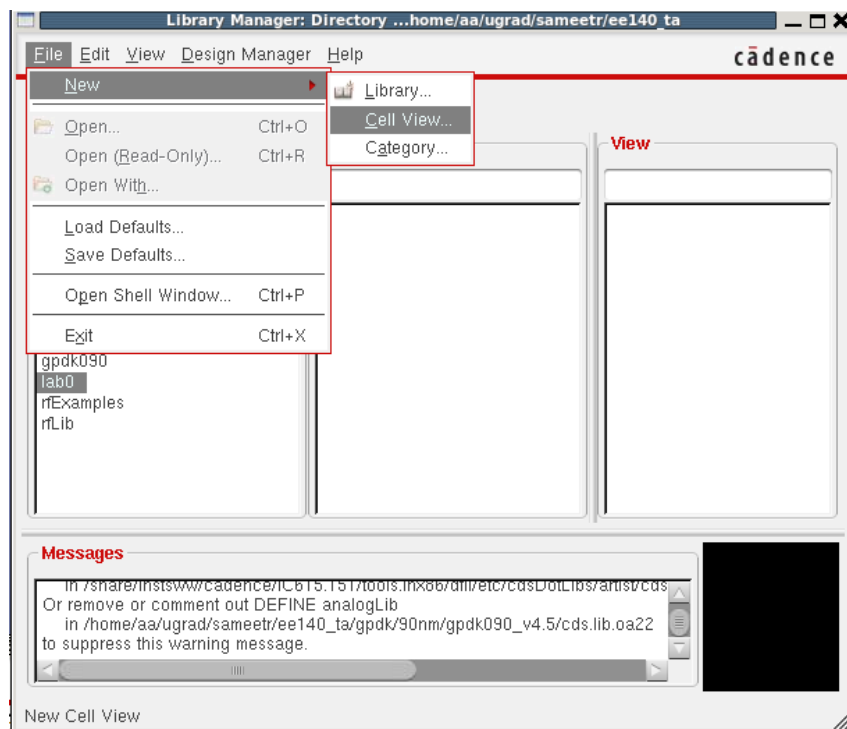
Creating a new schematic

To **create** a **new schematic** design:

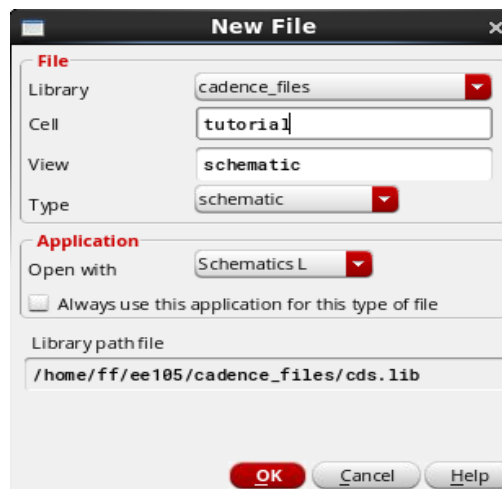
Click on the cadence_files library in the Library Manager

File -> New -> Cell View

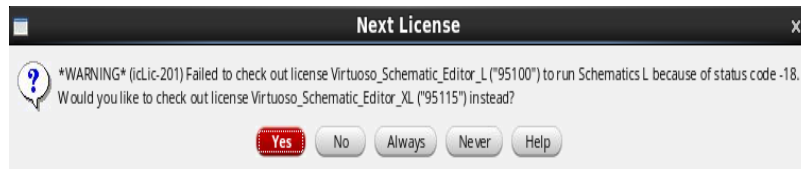
A new window pops up, but it may be at the background:



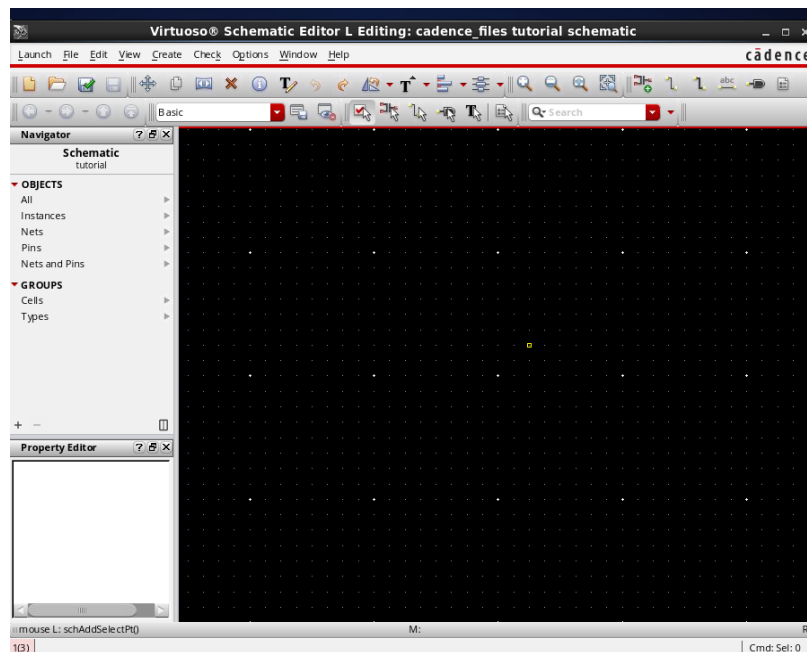
This is a general tip in Cadence - if you expect a window to open and it's not there, check the taskbar.



We will give it a name "**tutorial**", the type should be "**schematic**". Note that you can make cells in any available library by choosing proper one from '**Library**' (if you have permission to edit). Click **OK**. The following window will open:



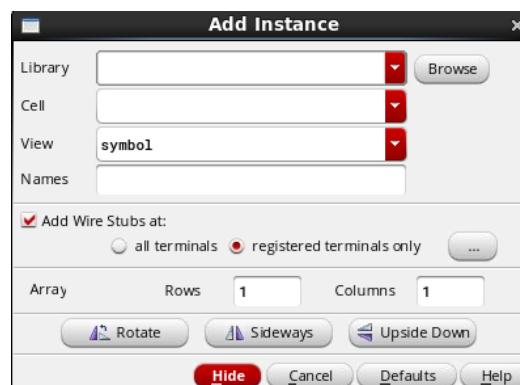
Click "Always" to avoid getting this message later. The **schematic window** will open:



This is the main window where we'll draw our circuit. Generally we won't use the menus, but keyboard shortcuts.

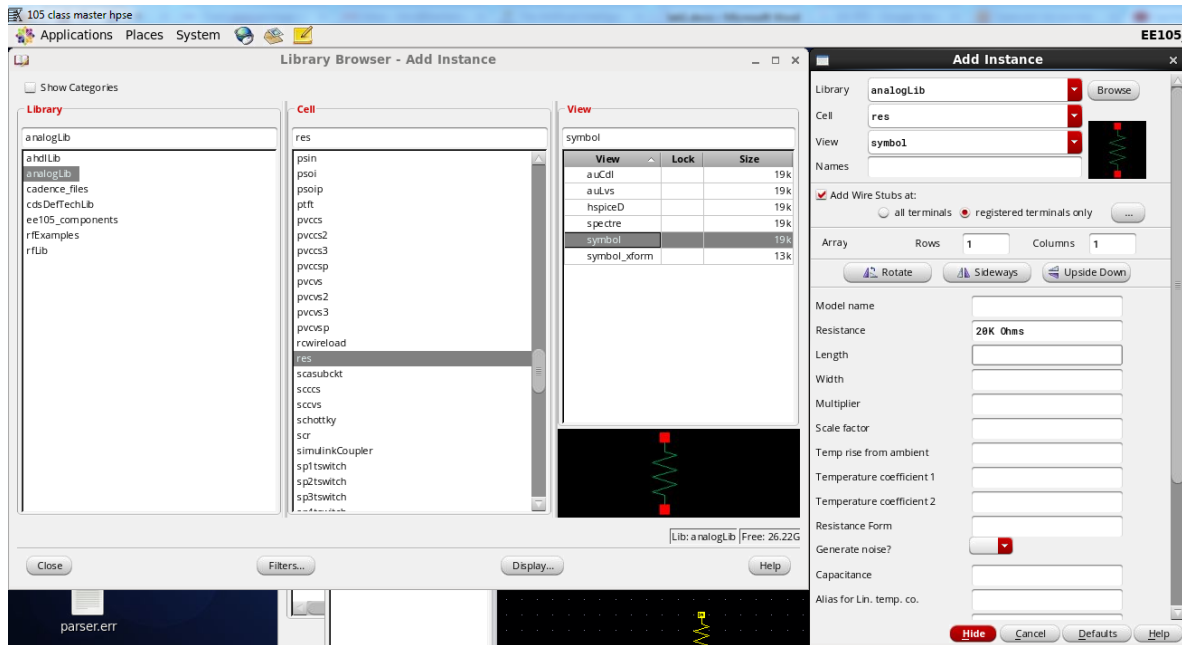
Adding components

To add an element, click "**i**". The following window will appear:



You can type the library, cell and view names, or click Browse:

Select "**analogLib**" library, "**res**" cell and "**symbol**" view. Another window will open:



Here you specify the parameters of the component. A **resistor** has a single **parameter** (resistance), change it to **20kΩ**.

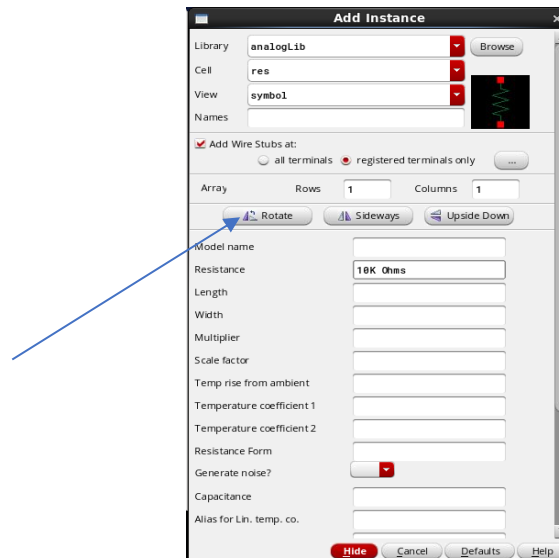
In **Cadence** you **don't** have to **write** the **units** (**Ohms**, **volts**, **etc**). For the **resistance**, type **20k** and hit Tab. The **Ohms** will be **automatically** completed. The useful prefixes in Cadence are single letters: **p** - pico, **n** - nano, **u** - micro, **m** - milli, **k** - kilo, **M** - mega, **G** – giga.

Click on the schematic window to place the resistor.

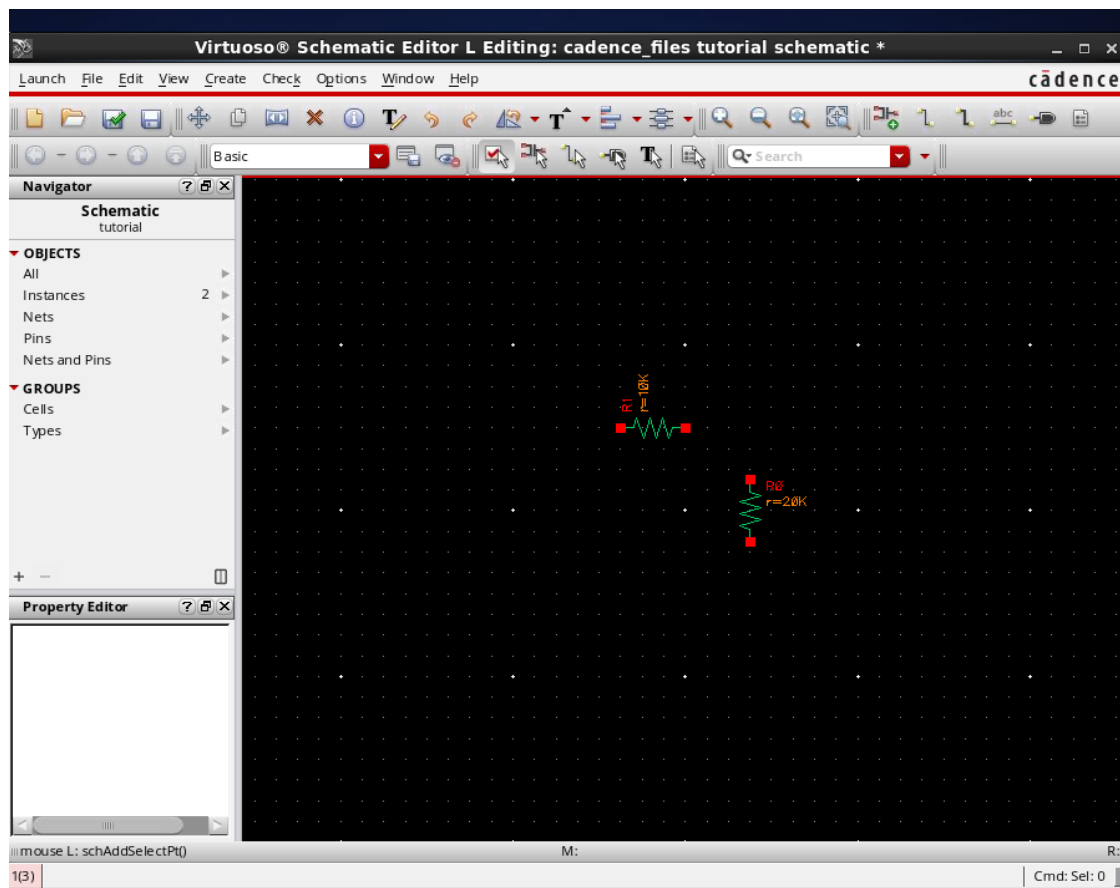
The useful components in the analogLib library are:

res	Resistor
cap	Capacitor
gnd	Ground
vdc/idc DC	DC voltage/current source
vsin/isin	Sinusoidal voltage/current source
vpulse/ipulse	Square-wave voltage/current source

Now add another resistor of **10k Ω** . Click "**Rotate**" to make it **horizontal** and **place** it on the schematic:

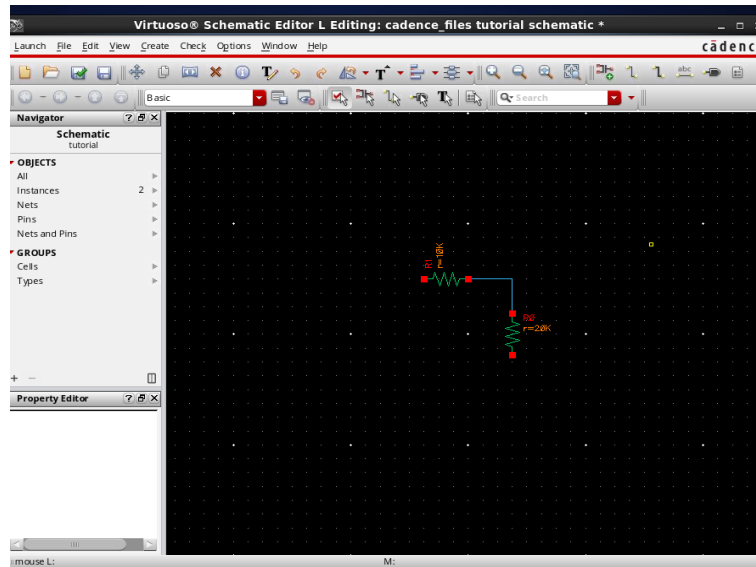


Your **schematic** should look like this:

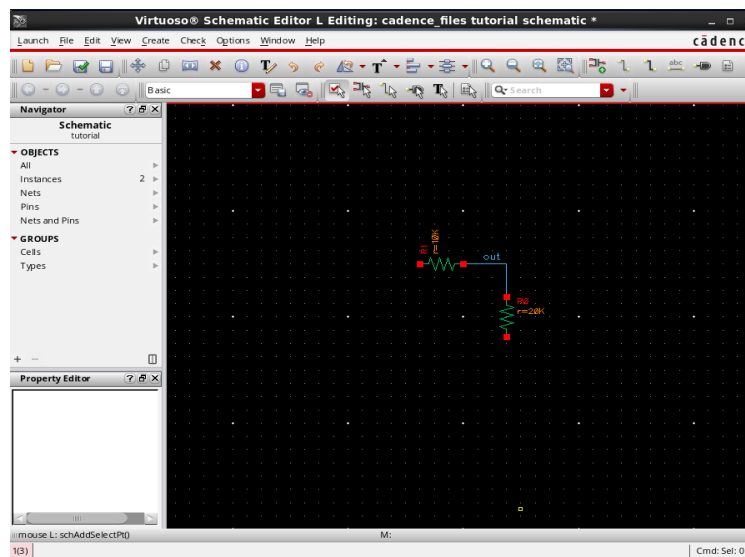


Adding wires and labels

To **connect** the **resistors** with a **wire**, click "**w**". Click on the **first terminal** to **connect**, and then on the **second terminal**. Click **Esc**. Now you have the following **schematic**:



To create a **wire label**, click "**I**" (**lowercase L**). Type out and click on the wire. Click **Esc**. Now you have the following schematic:



Labels can be used to connect nodes. If you want to connect two nodes in your circuit, you can give them the same label, without connecting them with a wire. It is usually useful for large circuits, to reduce the number of wires. Labels are also useful for output expressions, as we will see later.

Other useful shortcuts

- Components - click on the desired component, then click:
 - **c** - copy component
 - **m** - move component (preserves the wire connections)
 - **Shift+M** - move component (without the wire connections)
 - **q** - edit component properties (same window as the add component window)
- **f** - fits the circuit to fit the screen
- **mouse scroll** - zoom in and out
- **z** - selects area to zoom
- **Shift+X** - check and save.

Check that all nodes are connected properly. If you have errors, you have to fix them to simulate the circuit. You can run simulations if you have warnings. Pay attention to the warnings, usually they indicate a problem in your circuit, like unconnected nodes.

3. DC simulation - resistive divider

Add a DC voltage source and grounds to create the resistive divider circuit shown in Figure 1.

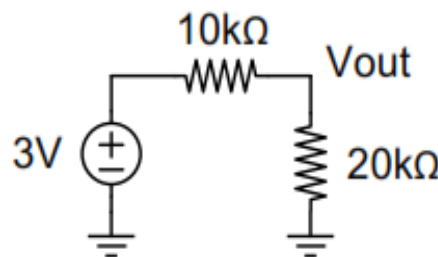
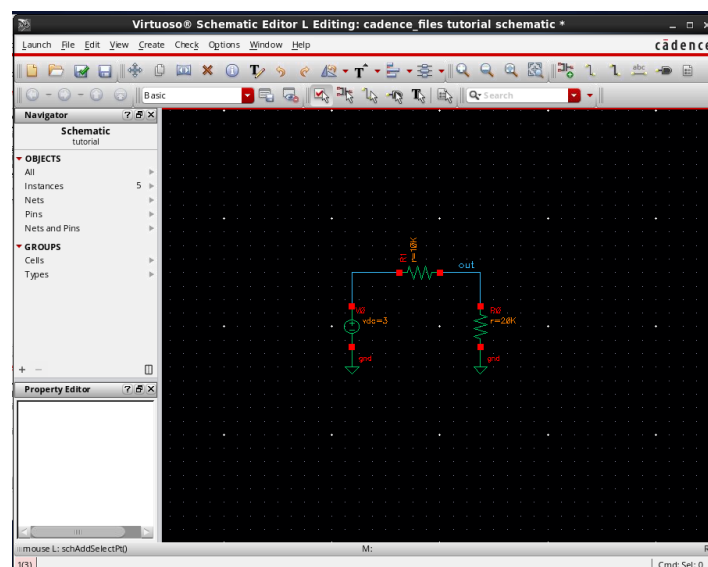


Figure 1: Resistor circuit to build

You should get the following schematic:



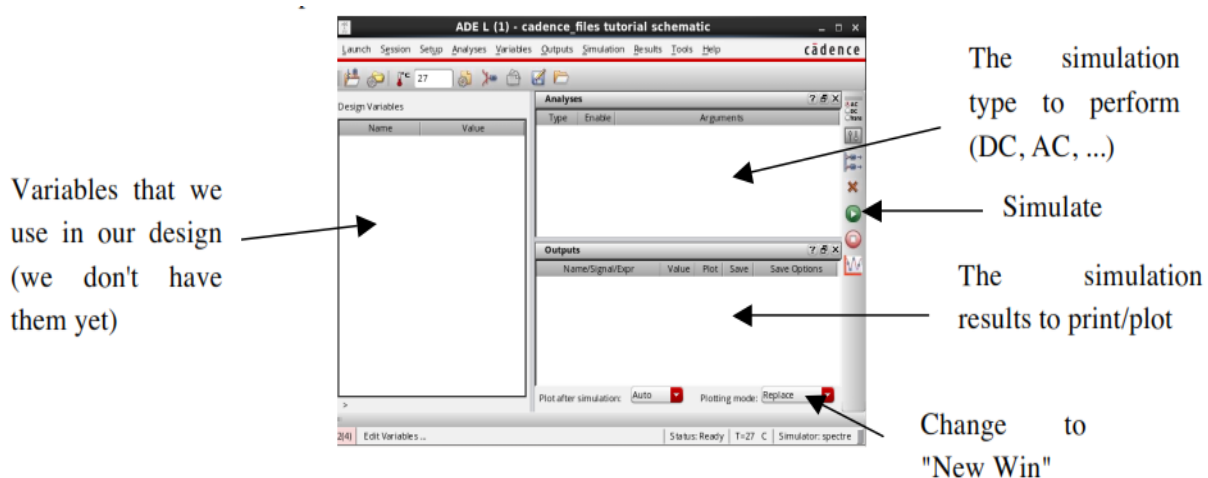
Click **Shift+X** to **check** and **save** your schematic.

To open the **simulation window**, click **Launch -> ADEL**. You will see the following window:



Click "**Always**" to avoid getting this **message later**.

The **ADE** window will **open**:



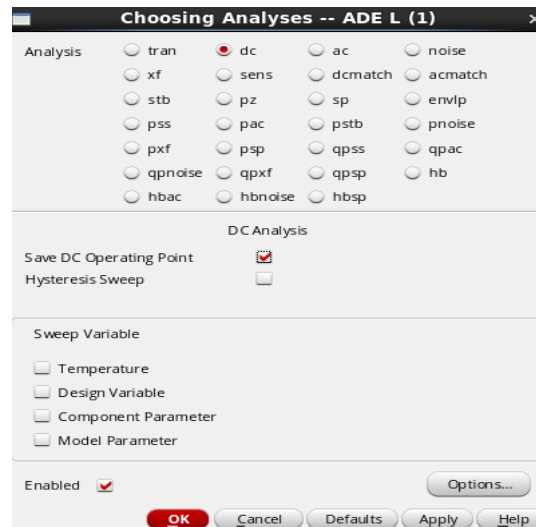
The Analysis box - specifying the simulation type

In the Analysis box: **right click -> Edit**.

Here we select the different simulation types for our schematic. The useful simulations in our class are:

- **dc - DC simulation**. Only **DC sources** are **used**, and the results are DC voltages and DC currents. This is in general a non-linear analysis (unless we only have linear components, like in our case).
- **ac - AC simulation**. This is a **linear phasor analysis** of the circuit. The simulation result is a phasor (magnitude and phase) of the voltages and the currents in our circuit. We can use it to calculate the transfer function from the input to the desired output. Here we define the frequency range to perform the simulation.
- **tran - transient simulation**. This is a **non-linear time-domain simulation**. The simulation results is a time-domain waveform of the voltages and the currents in our circuit.

In this part of the tutorial we will perform a **DC simulation**. Select dc, and check "**Save DC operating point**":



Click **OK**.

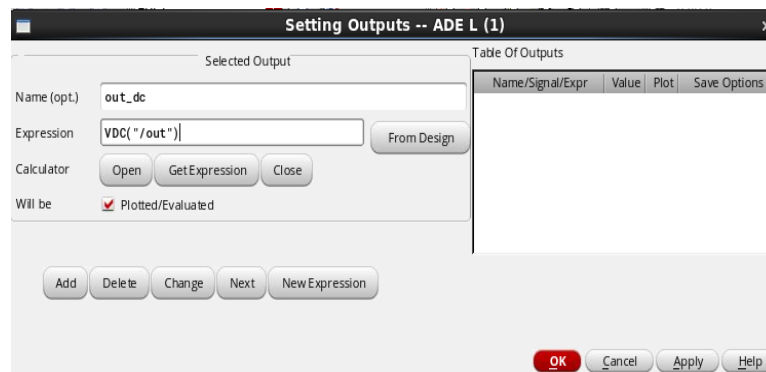
The Outputs box - specifying the simulation outputs

After performing the simulation we should specify the results that we are interested in.

In the Outputs box: **right click -> Edit**.

In the Name section type: **out_dc**

In the Expression section, type: **VDC("/out")**:



Click **OK**.

We created an output expression named "**out_dc**" for the **DC voltage** at the node "**out**".

A very useful tool in Cadence for the output expressions syntax is the calculator. In the main ADE window: **Tools -> Calculator**. At the bottom you have a list of the various functions that

can be performed on the simulation results. If you are not sure about the command syntax, the Calculator is a very useful place to start.

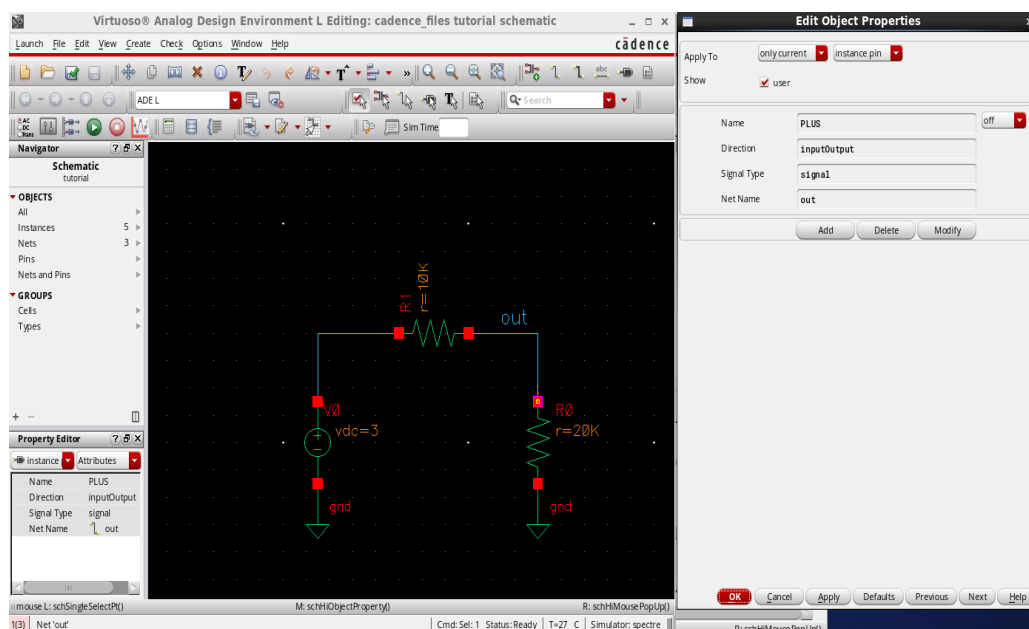
The syntax for the output expressions is:

VDC/IDC DC	voltage/current (dc analysis)
VF/IF	AC voltage/current (ac analysis)
VT/IT	Transient voltage/current (tran analysis)

For **voltage outputs**, the syntax is **VDC** ("/node_name"). For **current output**, the syntax is **IDC** ("/component_name/terminal name").

In our circuit to see the terminal name of the **20k** resistor connected to "**out**", click on it (the **red square**) and **press q**.

You will see the following window:

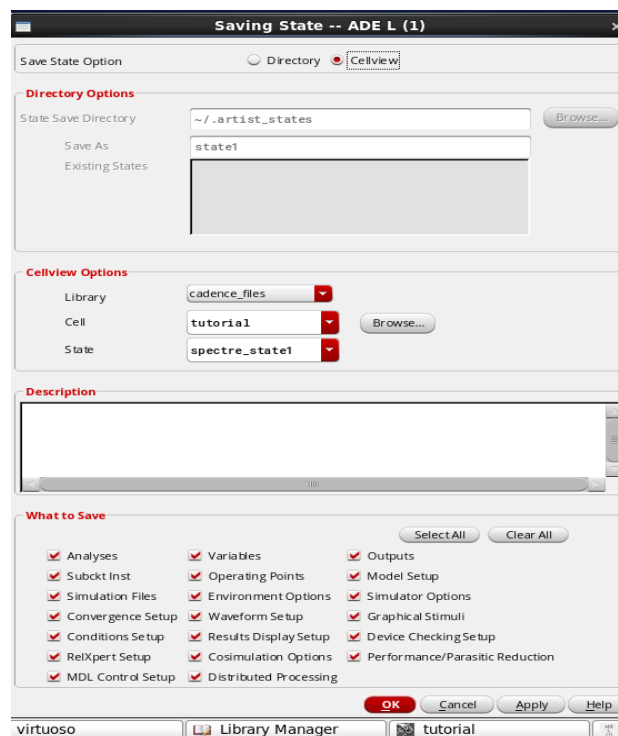


So the component name is **R0** and the terminal name is **PLUS**. For the **output DC current** through this node add the following output expression: **IDC** ("/R0/PLUS"):



Another option is to click on **idc** in the **Calculator**, and then **click on the resistor terminal**.

To **save your simulation setup: Session -> Save State**. At the top change to "**Cellview**":



Click **OK**. It will a view named "**spectre_state1**" in the "**tutorial**" cell.

Click the "**play**" button to perform the **simulation**. You should see the **simulated DC voltage** and **current** at the Value column. **Add the screenshot of the ADE window with the simulated result to your lab worksheet**.

A- Kirchhoff's Voltage Law (KVL)

1. Introduction:

” The algebraic sum of all voltages in a loop must equal zero”

The algebraic mean accounts for signs (polarities) as well as magnitudes. A loop means any path traced from one point in a circuit around to other points in that circuit, and finally back to the initial point.

2. Experiment:

- 1- Connections are made as shown in Fig.1
- 2- Measure voltages, and currents across the resistors R1, R2, and R4.

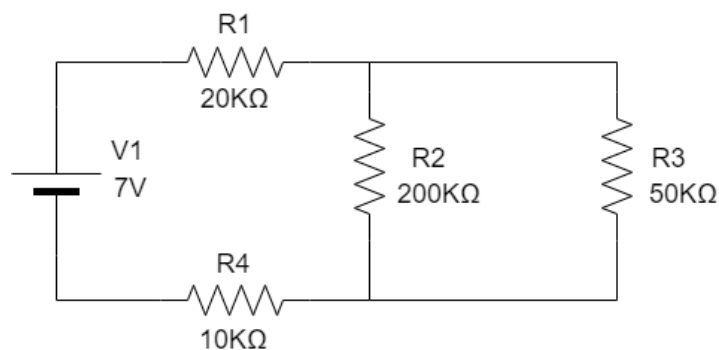
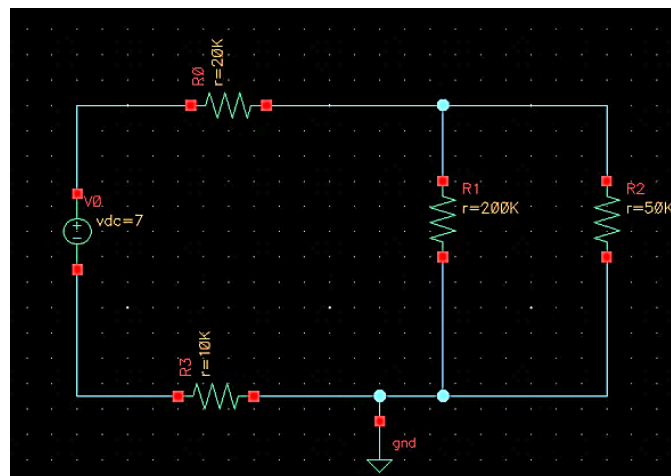


Figure 1: KCL configuration

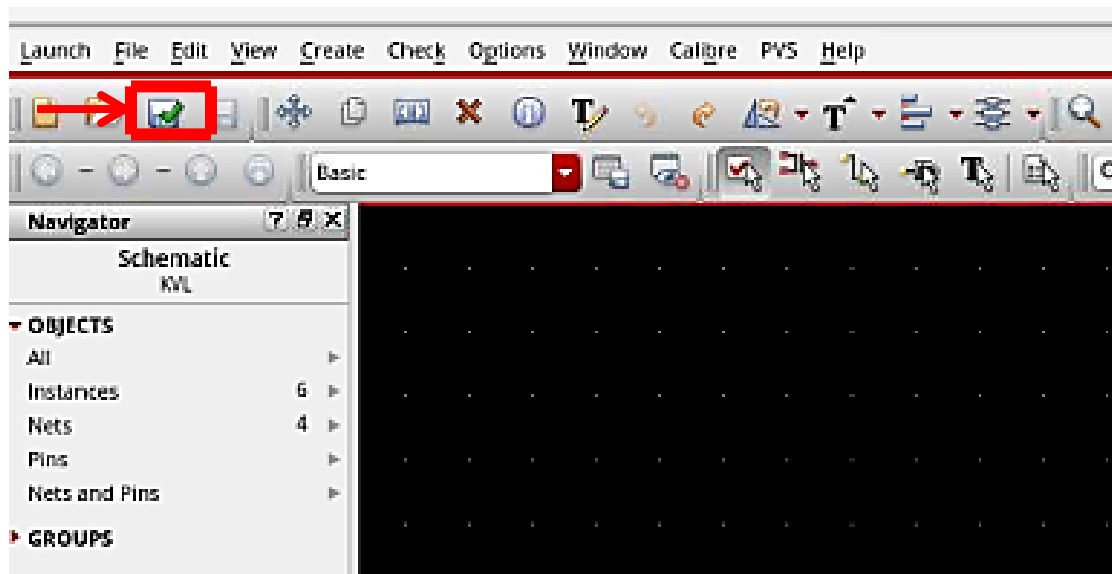
	R1	R2	R4	Total
Volts				
Amps				
Ohms	20 KΩ	200 KΩ	10 Ω	

3. Simulation procedures:

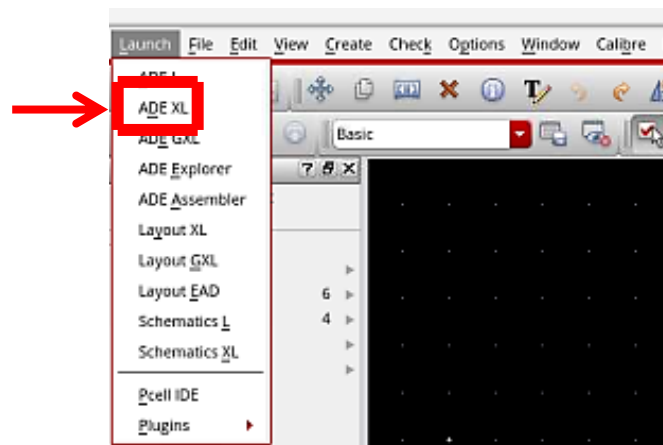
➤ Draw schematic:



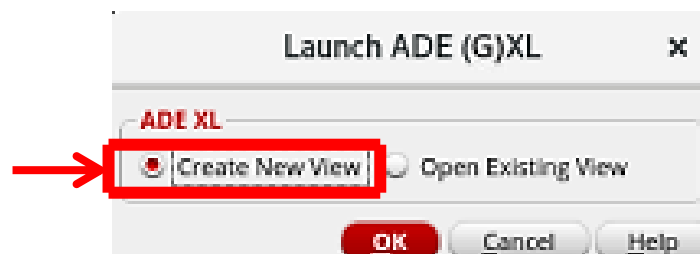
➤ Check and save



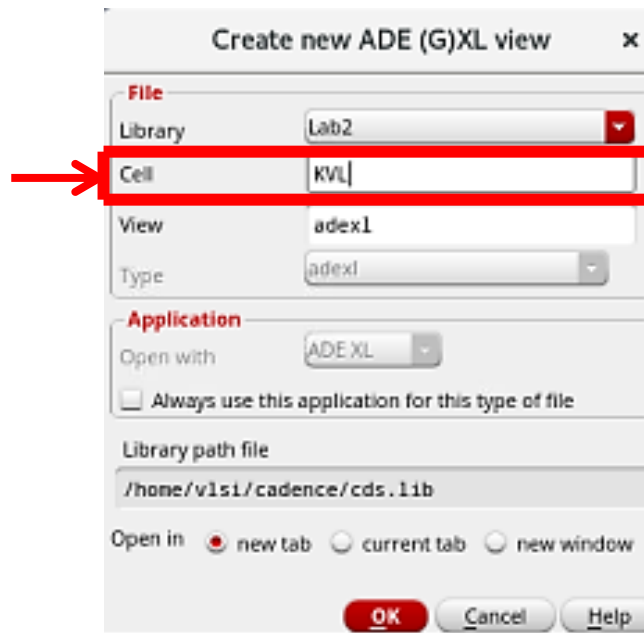
➤ Lunch => ADE XL



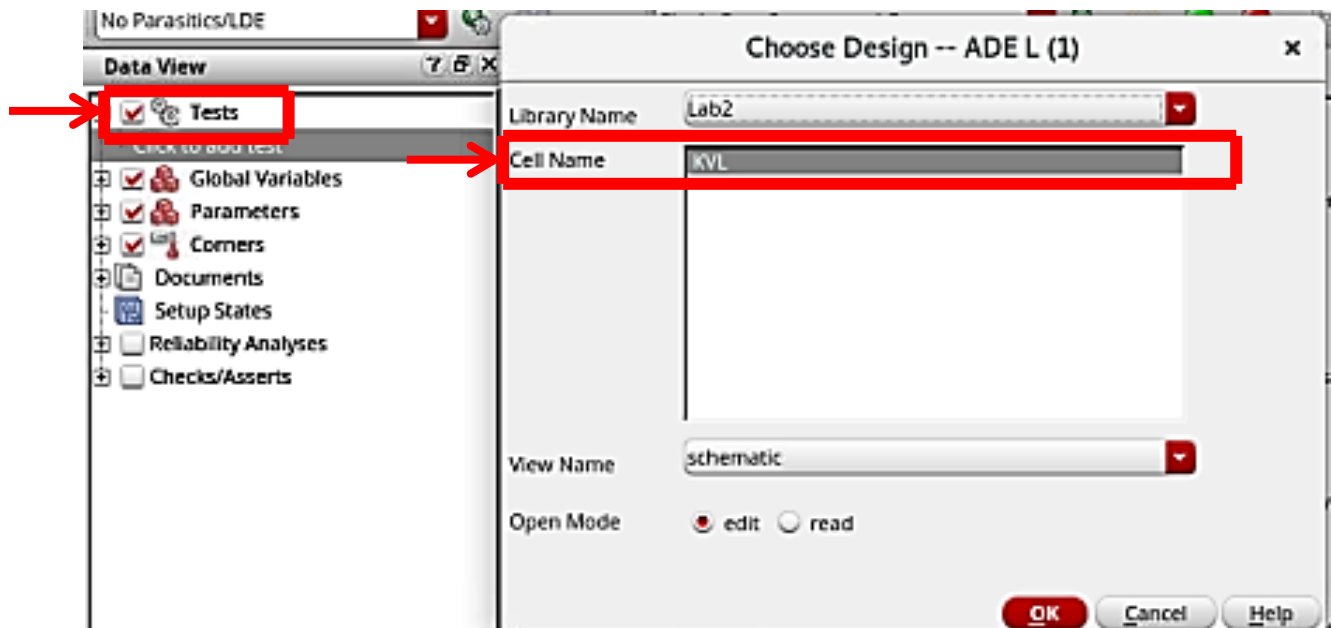
➤ Create New View => OK



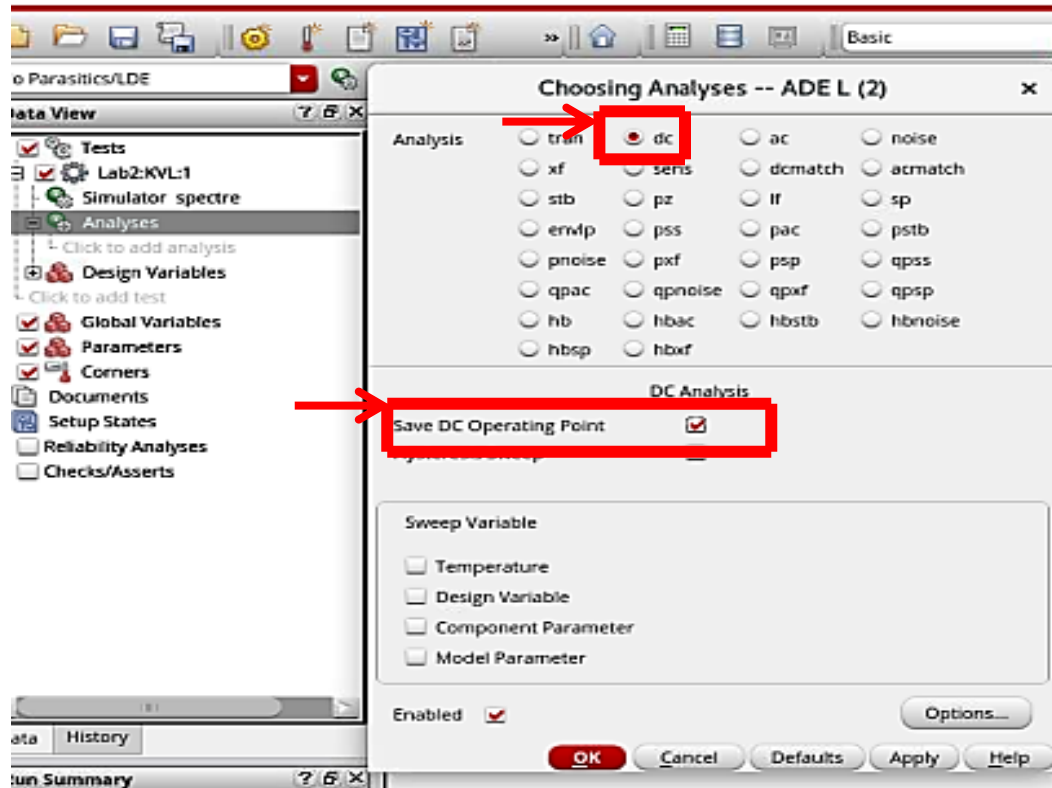
- Cell => “KVL” => OK



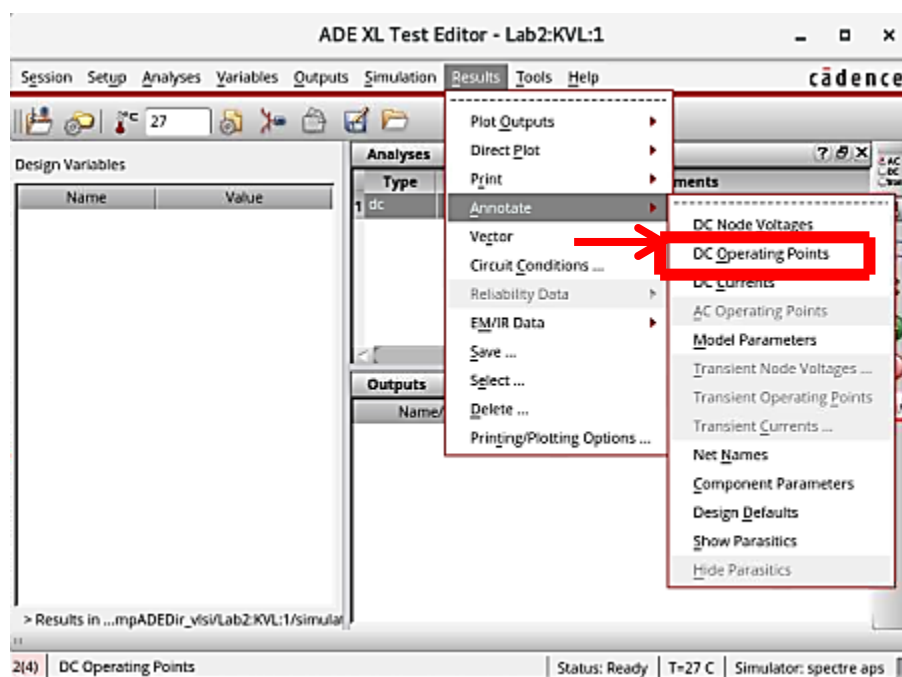
- Click “Tests” => Cell Name “KVL” => OK



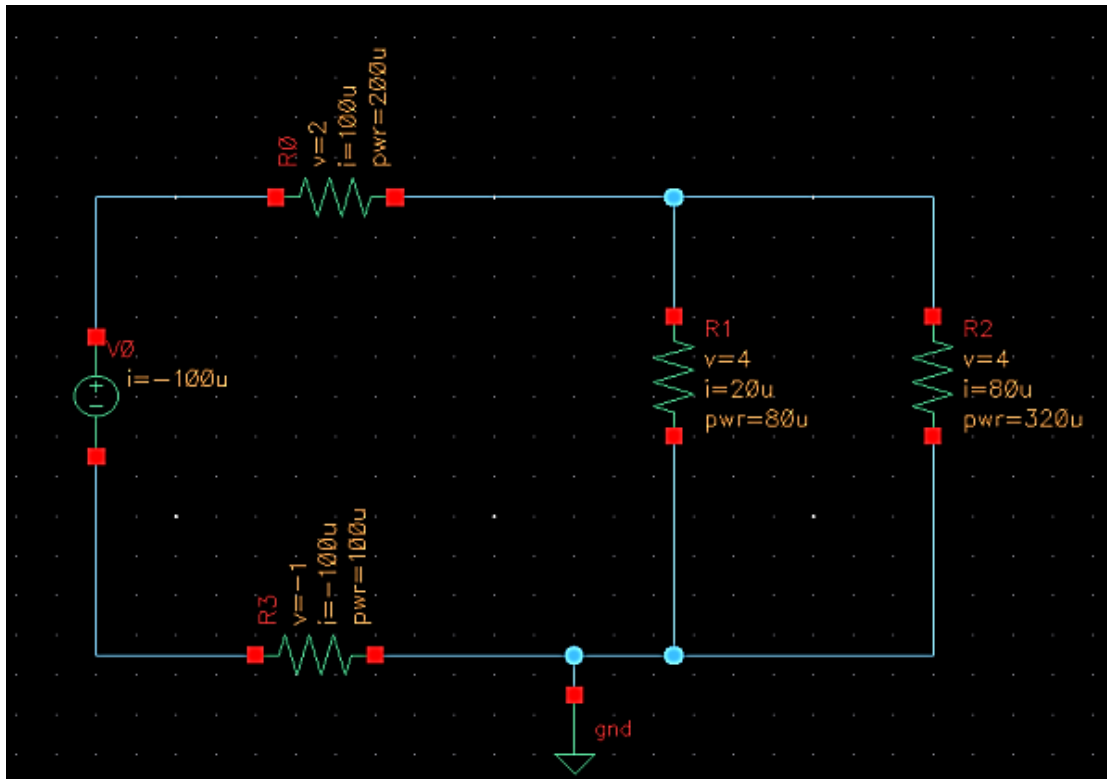
- Analysis => dc
- Save DC Operating Points => DC Analysis



➤ Annotate ⇒ DC Operating Points



➤ The Result



B- Kirchhoff's Current Law (KCL)

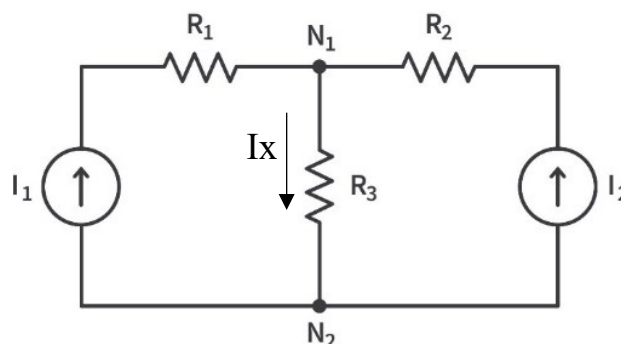
1. Introduction

"The algebraic sum of all currents entering and exiting a node must equal zero"

That is, if we assign a mathematical sign (polarity) to each current, denoting whether they enter (+) or exit (-) a node, we can add them together to arrive at a total of zero, guaranteed.

Taking our example node (number N_1), we can determine the magnitude of the current exiting from the left by setting up a KCL equation with that current as the unknown value:

$$I_1 + I_2 + I_x = 0$$



2. Experiment:

- 1- Connections are made as shown in Fig.2.
- 2- Measure I_{R1} , I_{R2} , and I_{R3} .

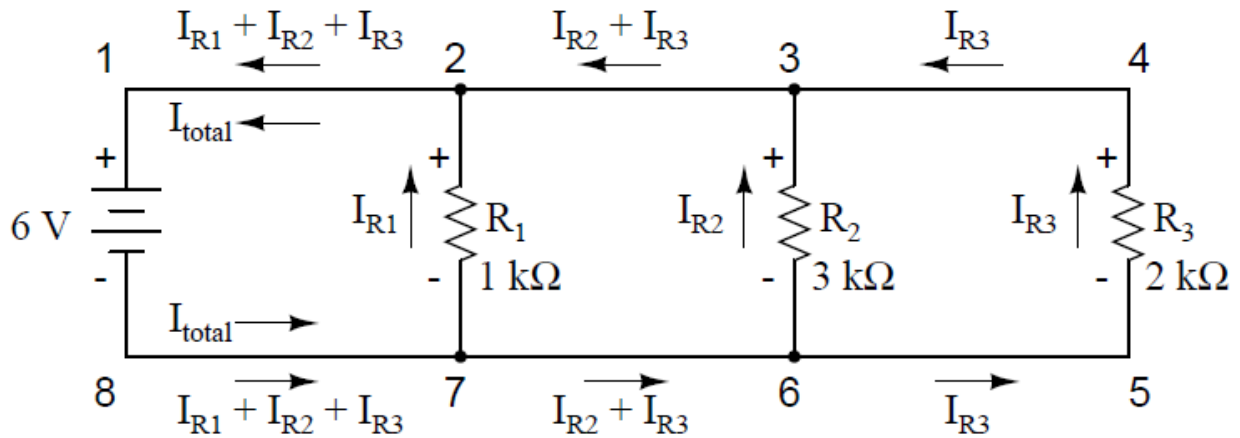
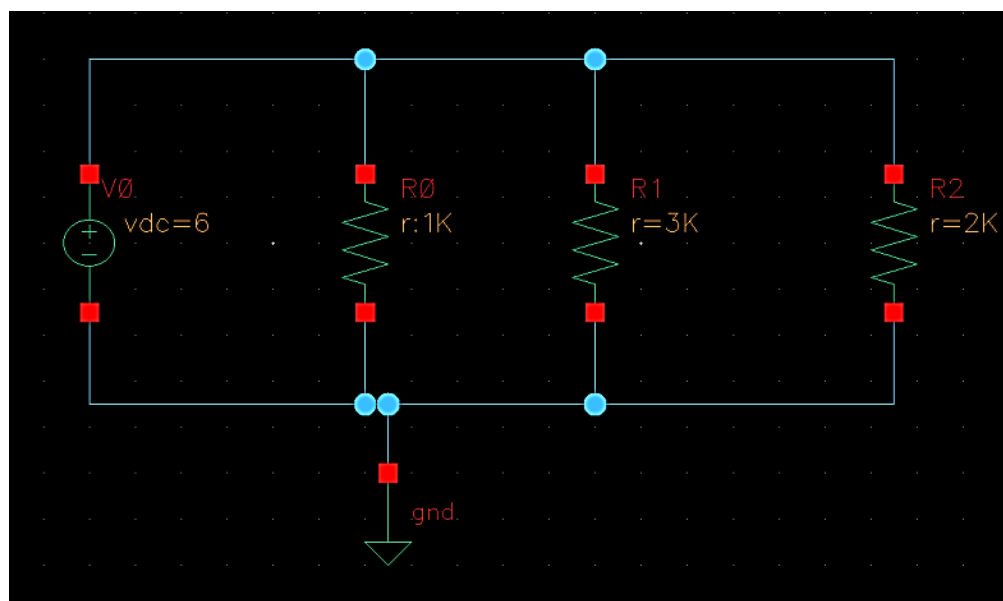


Figure 2: KCL Configuration

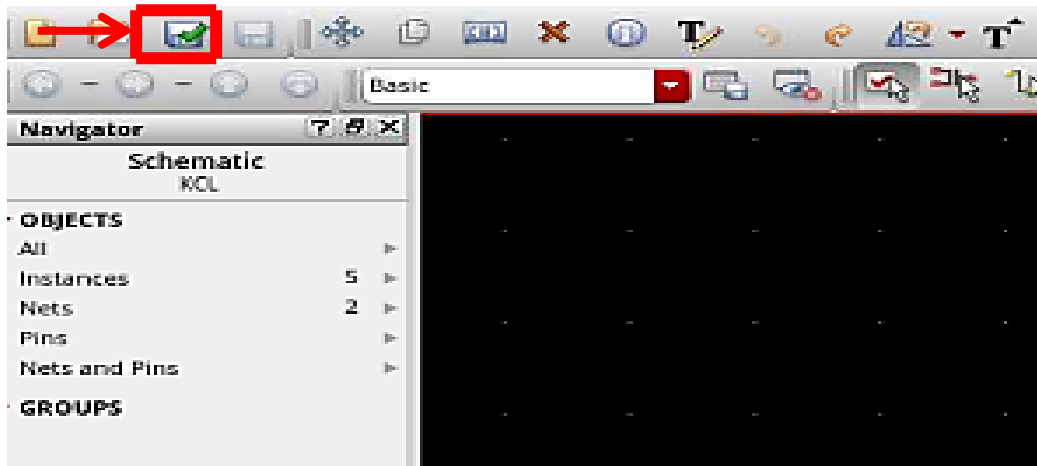
	R1	R2	R3	Total
Volts	6	6	6	6
Amps				
Ohms	1 KΩ	3 KΩ	2 KΩ	

1. Simulation procedures:

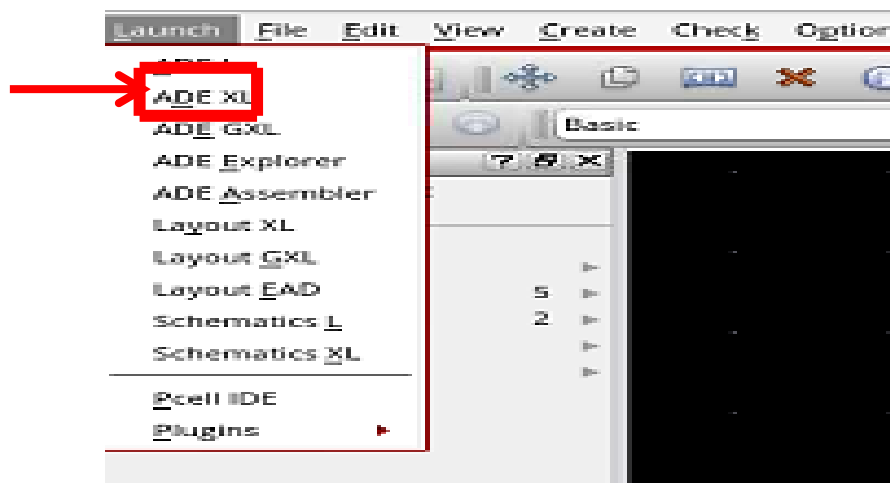
➤ Draw schematic:



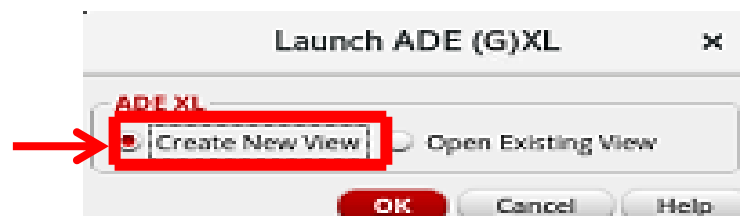
➤ Check and save



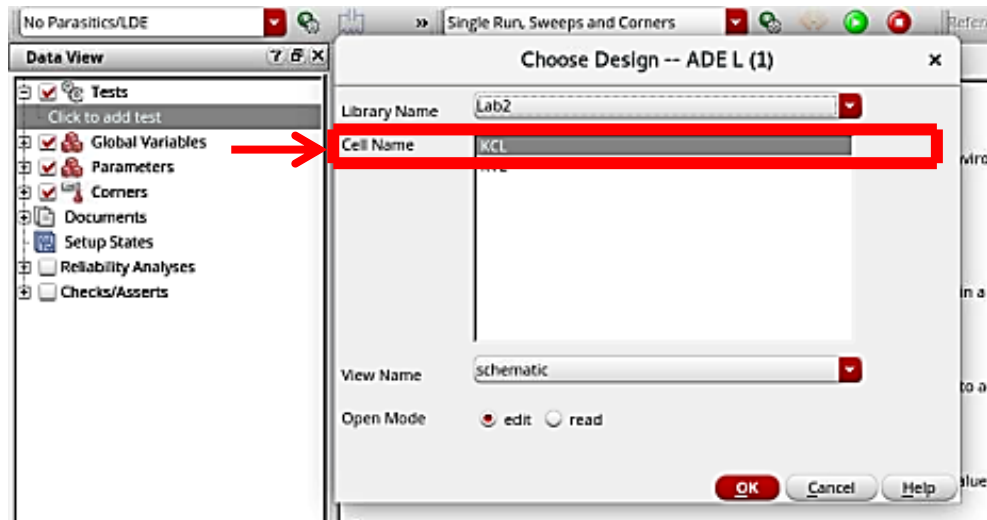
➤ Lunch => ADE XL



➤ Create New View => OK

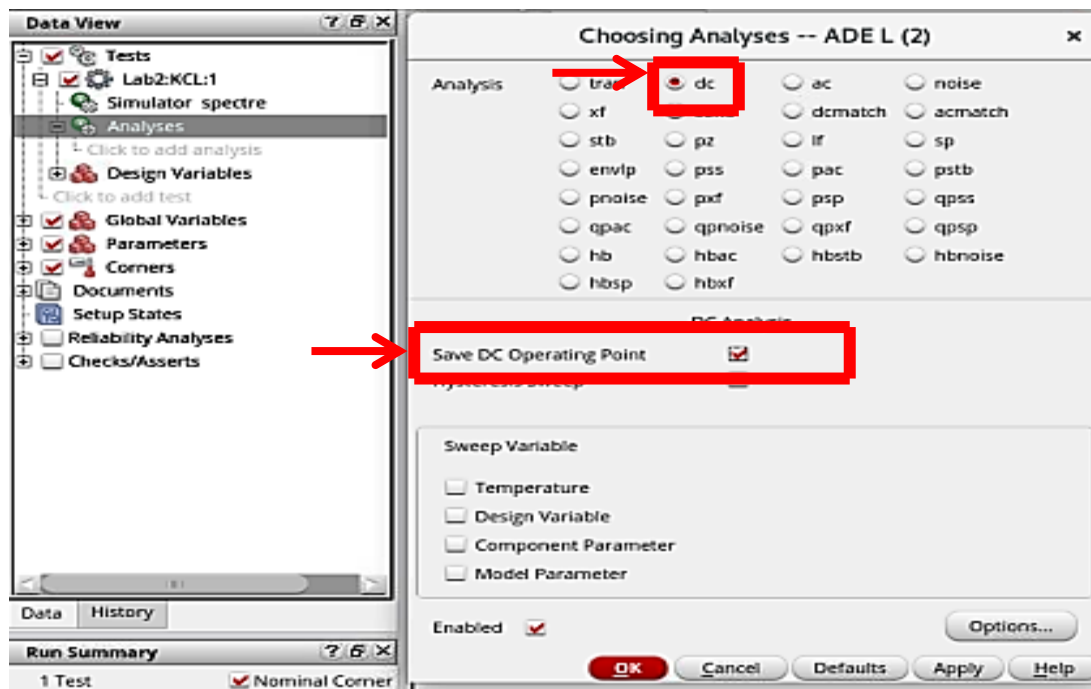


➤ Cell => “KCL” => OK

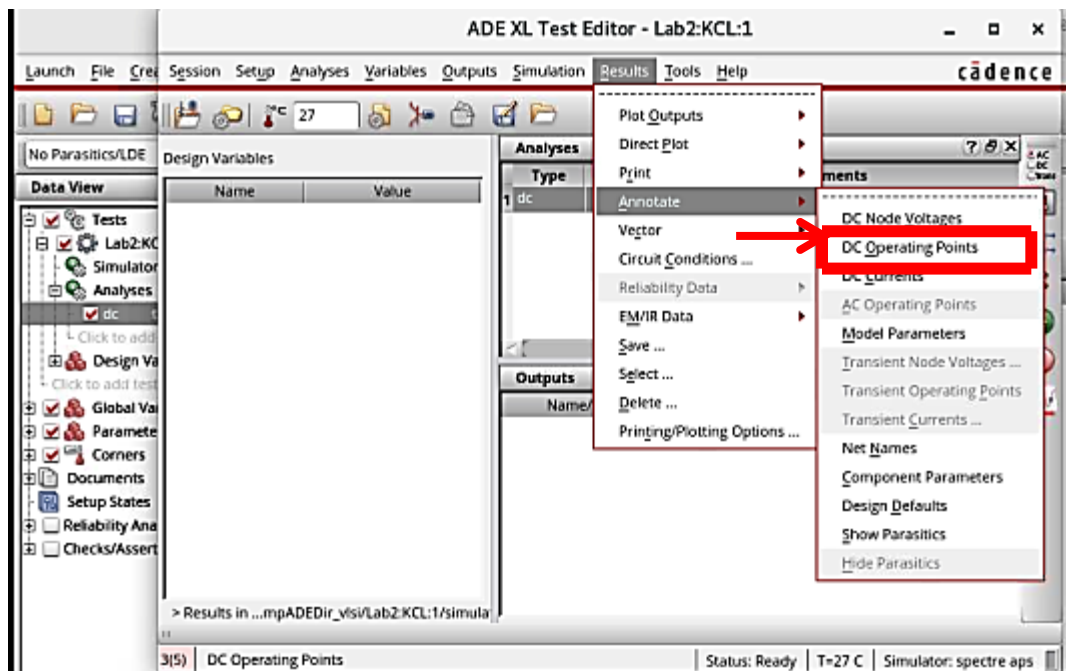


➤ Analysis => dc

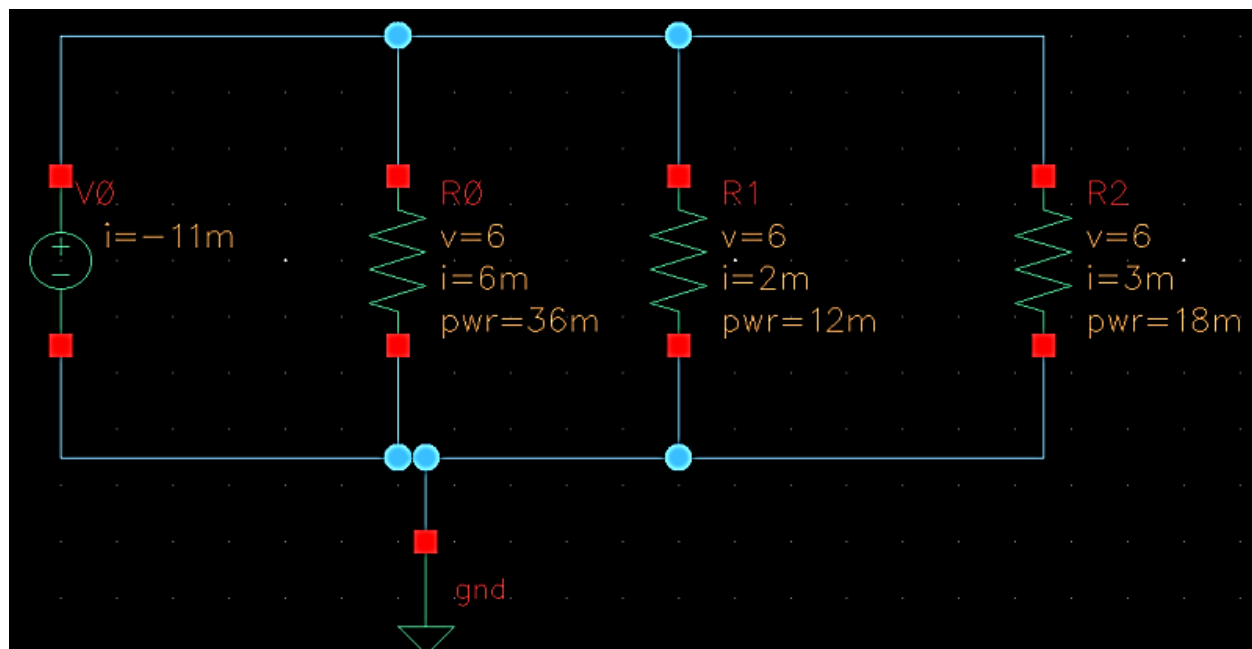
➤ Save DC Operating Points => DC Analysis



➤ Annotate => DC Operating Points



➤ The Result



Assignment 1

Calculate the current through each resistor and the voltage across each resistor within the following circuit.

