





### **CND 101 - LAB [2]**

**Student name: Karim Mahmoud Kamal** 

**Student ID: V23010174** 

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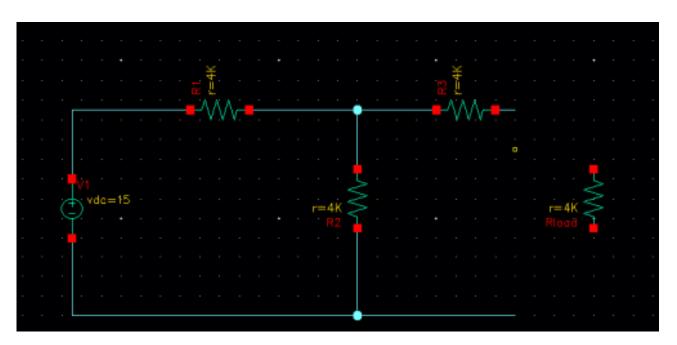
#### A- Thevenin's and Norton's theorems verification

	V across RL	I in IL
Original cct.	3v	750u
Thevenin's equivalent	3v	750u
Norton's equivalent	3v	750u

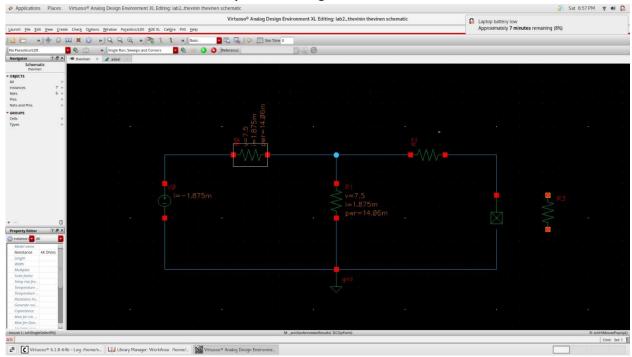
3- Comment on how this verifies Thévenin's and Norton's theorems

<u>Comment:</u> we have the same current and same voltage drop across RL when we solve the main circuit or Thevenin's equivalent or Norton's equivalent.

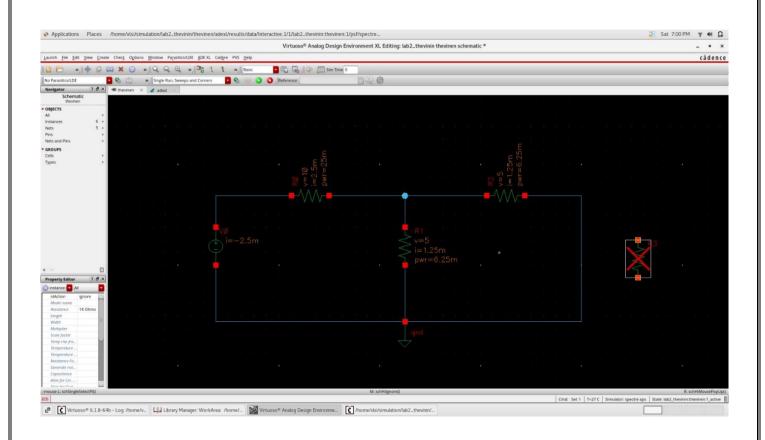
Additionally, Maximum power transfer happens when R Thevenin = R Load schematic:



#### open circuit to get V Thevenin



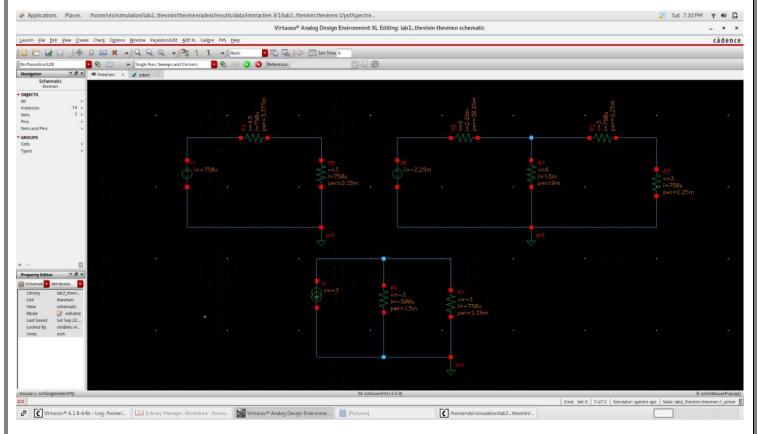
#### Short circuit to get I norton



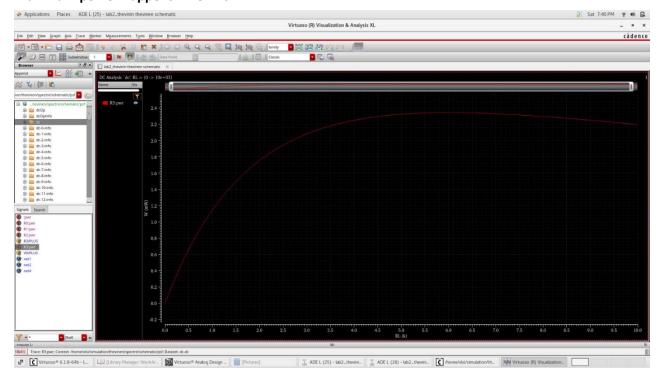
#### Main Circuit on the right

#### Norton equivalent on the left

#### Thevinin equivalent at the bottom

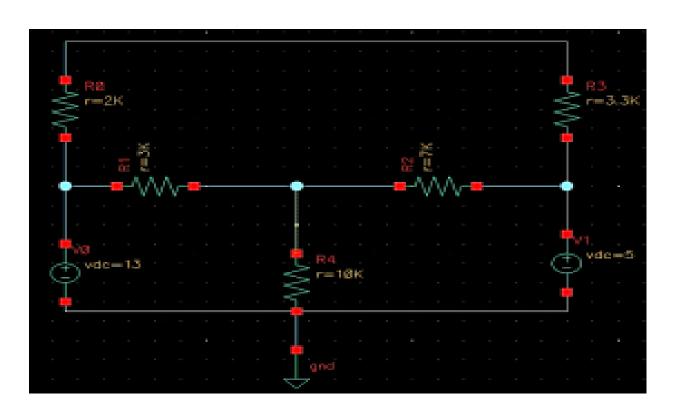


#### Maximum power happens when Rth = RL

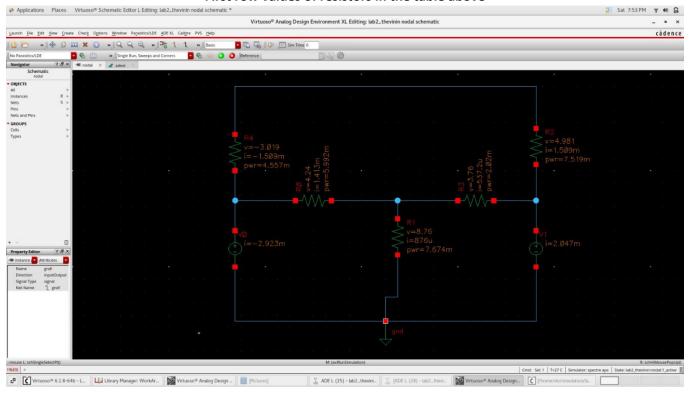


#### **B-Nodal-Analysis Technique:**

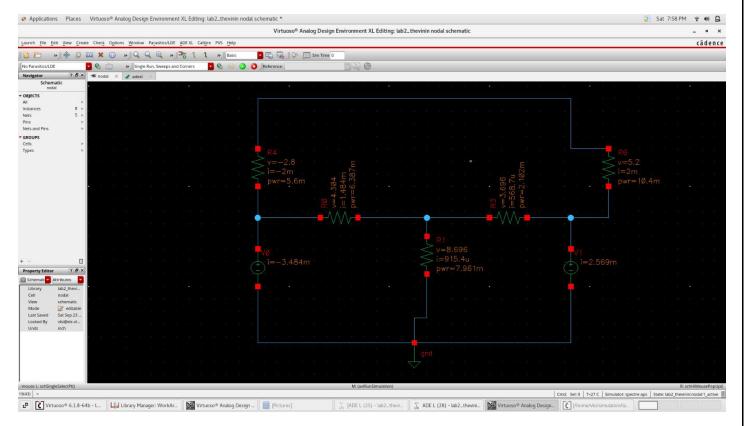
	Vs1	Vs2	R1	R2	R3	R4	RL
Value	13v	5v	2k	3k	7k	10k	3.3k
Value	13v	5v	1.4k	2.9k	6.5k	9.5k	2.6k



#### First row values of resistors in the table above



#### Second row values of resistors in the table above



	V1	V2	VL
For the first row values	8.76v	13v	5v
For the second row values	8.696v	13v	5v

	I1	12	13	14	ls1	ls2	IL
For the first row values	-1.509m	1.413m	537.2u	876u	-2.923m	2.047	1.509m
For the second row	-2m	1.484m	568.7u	915.4u	3.484m	2.569m	2m
values							

	Pvs1	Pvs2	∑Pvsj
For the first row values	-37.999m	10.235m	-27.764m
For the second row values	-45.292m	12.845m	-32.447m

	PR1	PR2	PR3	PR4	PRL	Sum PRi
For the first row values	4.557m	5.992m	2.02m	7.674m	7.519m	27.762m
For the second row values	5.6m	6.387m	2.102m	7.961m	10.4m	32.45m

	∑Pvsj	∑PRj	% out of balance
For the first row values	-27.764m	27.762m	0.002%
For the second row values	-32.447m	32.45m	0.003%

# **Assignment 2 Main Circuit** Applications Places Virtuoso® Schematic Editor L Editing: lab2\_thevinin assignment\_lab22 schematic Sat 8:13 PM ₹ ♠ € Virtuoso® Analog Design Environment XL Editing: lab2\_thevinin assignment\_lab22 schematic cādence Sim Time 0 🗜 🕻 Virtuoso® 6.1.8-64b - Log. /home/v... 🖳 Liptary Manager: WorkArea: /home/... 🔯 Virtuoso® Schematic Editor L Editin... 🔯 Virtuoso® Analog Design Environme... 🔯 Virtuoso® Analog Design Environme... I Norton (short circuit) → (RL is equal to 0 here) Applications Places Virtuoso® Schematic Editor L Editing; lab2\_thevinin assignment\_lab22 schematic Virtuoso® Analog Design Environment XL Editing: lab2\_thevinin assignment\_lab22 schematic \_ = x cādence Sim Time 0 -74.07u P Virtuoso® 6.1.8-64b - Log. //home/v... | Lip Ubrary Manager: WorkArea: //home/... | Wirtuoso® Schematic Editor L Editin... | Wirtuoso® Analog Design Environme... | Wirtuoso

# V Thevinin (open circuit) Applications Places Virtuoso® Schematic Editor L Editing: lab2\_thevinin assignment\_lab22 schematic Sat 8:14 PM 😨 🐠 🔒 Virtuoso® Analog Design Environment XL Editing: lab2\_thevinin assignment\_lab22 schematic cādence No Parastics/LDE No Parastic Sim Time 0 Reference: Cmd: Sel: 0 | T=27 C | Simulator: spectre aps | State: lab2\_thevinin:assignment\_lab22:1\_active | [J Virtuoso 6.1.8-64b - Log. /home/v... | Library Manager: WorkArex. /home/... | Wirtuoso 5 Schematic Editor L Editin... | Wirtuoso 9 Analog Design Environme... | Wir **Thevinin equivalent Circuit** Virtuoso® Analog Design Environment XL Editing: lab2\_thevinin assignment\_lab22 schematic \_ = × cādence Sim Time 0 > Single Run, Sweeps and Corners Solution Street Sweeps and Corners Solution Sweeps and Corners Solution Sweeps and Corners Reference: OBJECTS Cmd: Sel: 0 | T=27 C | Simulator: spectre aps | State: lab2\_thevinin:assignment\_lab22:1\_active | [P] [C] [Virtuoso® 6.1.8-64b - Log-/...] [Lid [Library Manager: WorkArea: /...] [Virtuoso® Schematic Editor L...] [W] Virtuoso® Analog Design Envir... [W] Virtuoso® Analog Design Envir... [W] Virtuoso® Analog Design Envir... /home/vlsi/simulation/lab2\_th...

## **Norton Equivalent circuit** Applications Places /home/vlsi/simulation/lab2\_thevinin/assignment\_lab22/adexl/results/data/interactive.2/1/lab2\_thevinin:assignment\_l... Virtuoso® Analog Design Environment XL Editing: lab2\_thevinin assignment\_lab22 schematic \_ a × cādence Sim Time 0 No Parastics/LDE Single Run, Sweeps and Corners Move Parastics/LDE Assignment, Jab22 X aded Schematic assignment, Jab22 X aded OBJECTS GROUPS Cells Types Cmd: Sel: 0 | T=27 C | Simulator: spectre aps | State: lab2\_thevinin:assignment\_lab22:1\_active | [P] [C] [Virtuoso® 6.1.8-64b - Log:/...] [Library Manager: WorkArex. /...] [Million | Workarex. /...] [Virtuoso® Schematic Editor L...] [Million | Wirtuoso® Analog Design Envir...] [Million | Wirtuoso® /home/vlsi/simulation/lab2\_th... Max power Transfer happens when RL = RTH Applications Places /home/vlsi/simulation/lab2\_thevinin/assignment\_lab22/adexl/results/data/interactive.2/1/lab2\_thevinin:assignment\_l... 🛜 Sat 8:34 PM 😨 🐠 🔒 Virtuoso (R) Visualization & Analysis XL \_ n x <u>File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help</u> cādence 107.0 103.5 · (Will 103.0 · 27(63) Trace: R15:pwr; Context: /home/vlsi/simulation/assignment\_lab22/spectre/schematic/psf; Dataset: dc-dc [C] [Virtuoso® 6.1.8-64b. Library Manager: Wo... Virtuoso® Schematic...