Lab 2

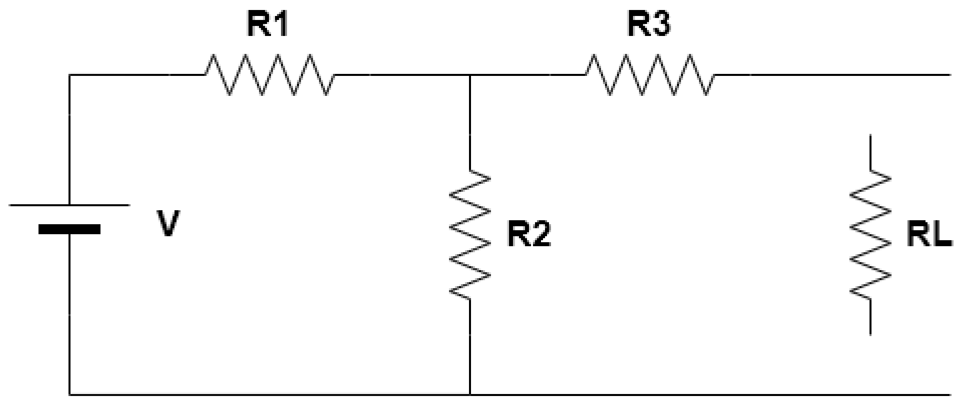
Circuit Analysis

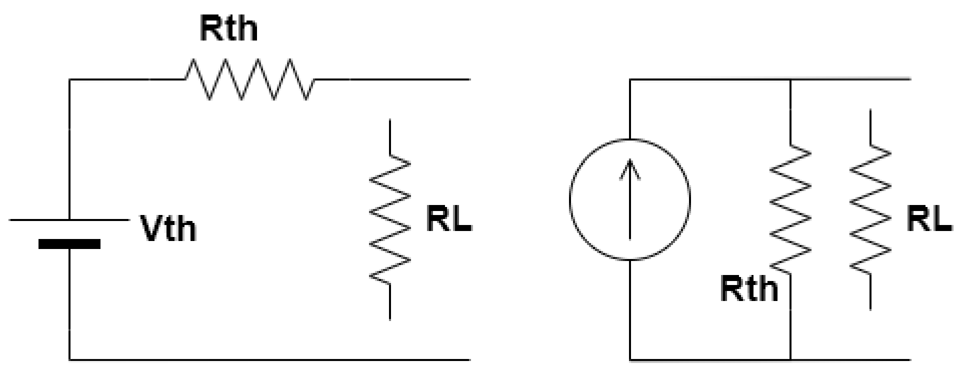
1. **<u>Introduction:</u>**
   The purpose of this lab is to verify the findings of Thevenin's and Norton's Theorems

A- <u>Thevenin's and Norton's theorems verification</u>

I. <u>Experiment:</u>

1- Consider the first circuit in Fig. 1 where R_L=2KΩ, and calculate its Thevenin's and Norton's equivalent circuits as depicted in Fig. 2.





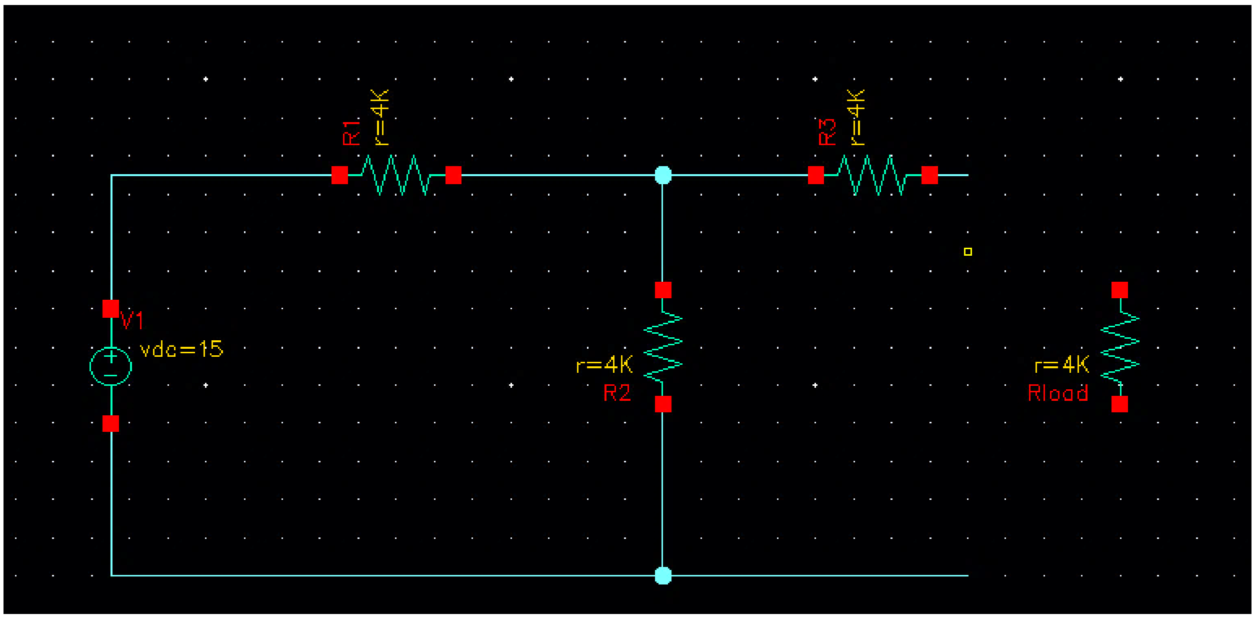
2- Measure the voltage across RL and the current passing through it, in the three circuits, and fill in the below table.

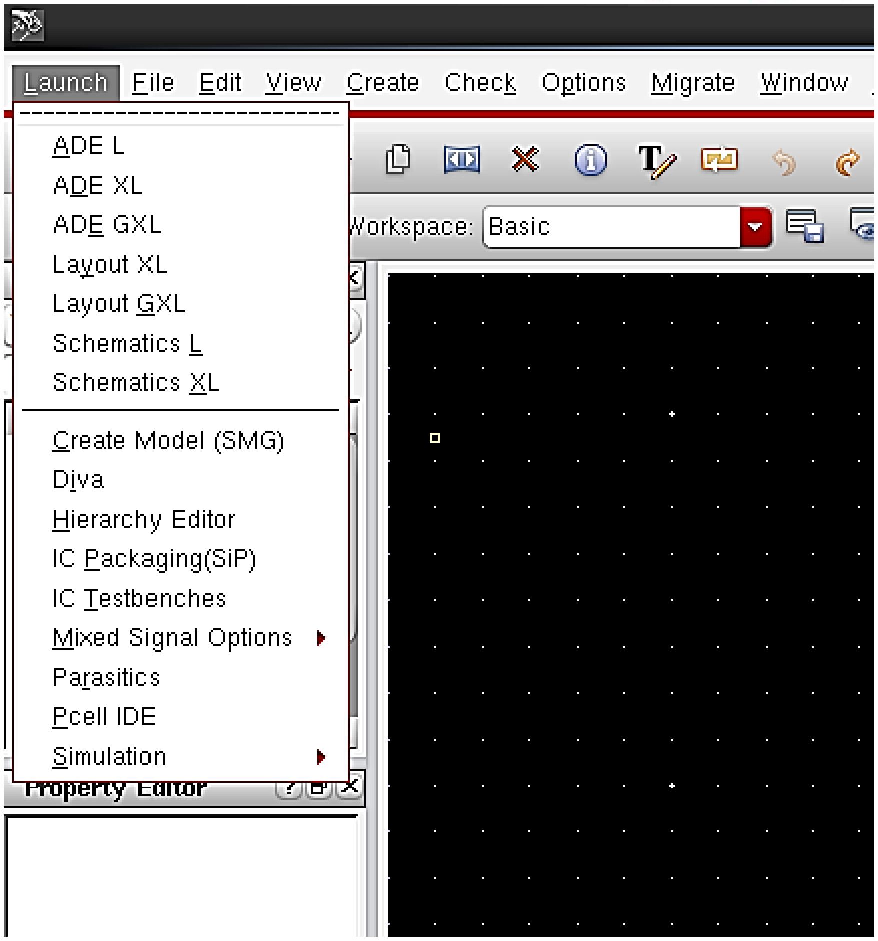
	V across R_L	I in I_L
Original cct.		
Thevenin's equivalent		
Norton's equivalent		

3- Comment on how this verifies Thévenin's and Norton's theorems.

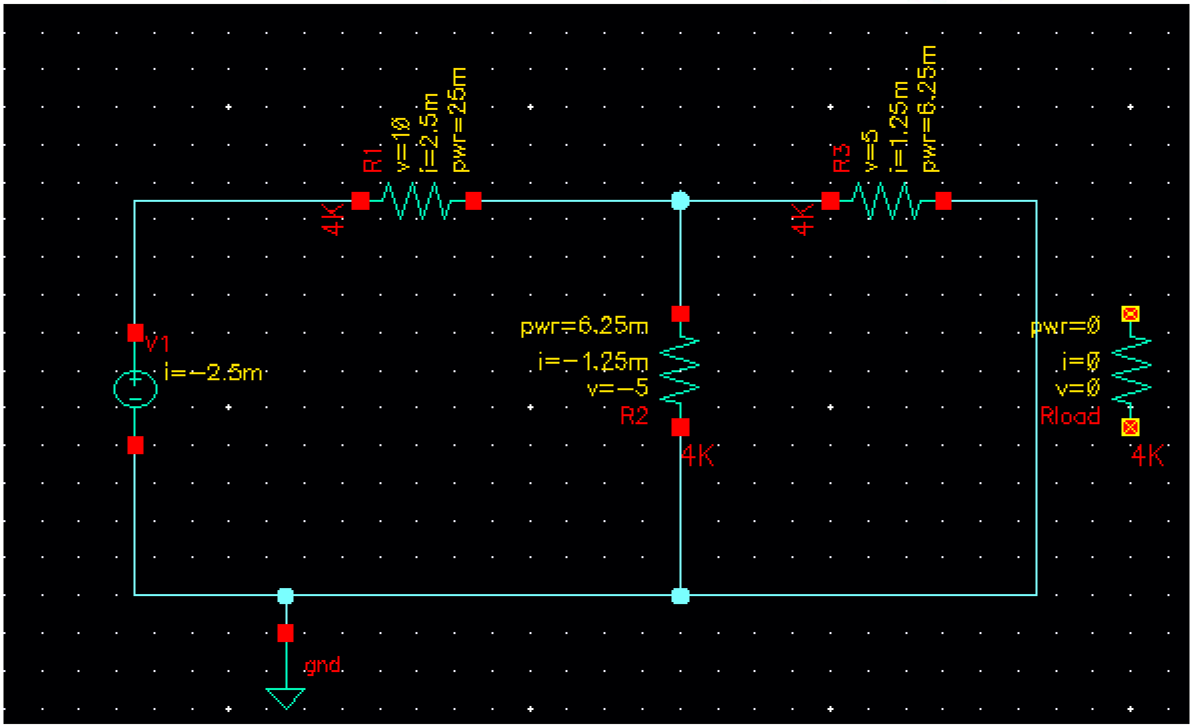
II. <u>Simulation Procedures:</u>

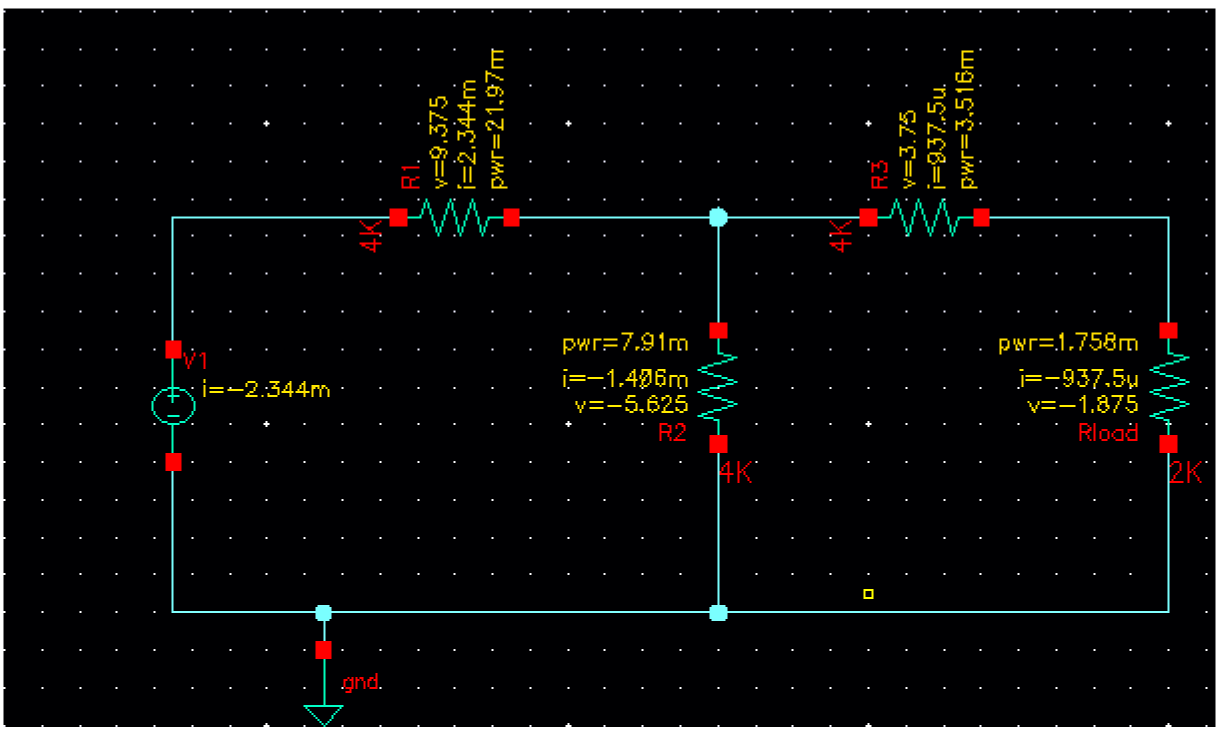
➢ **Draw schematic:**

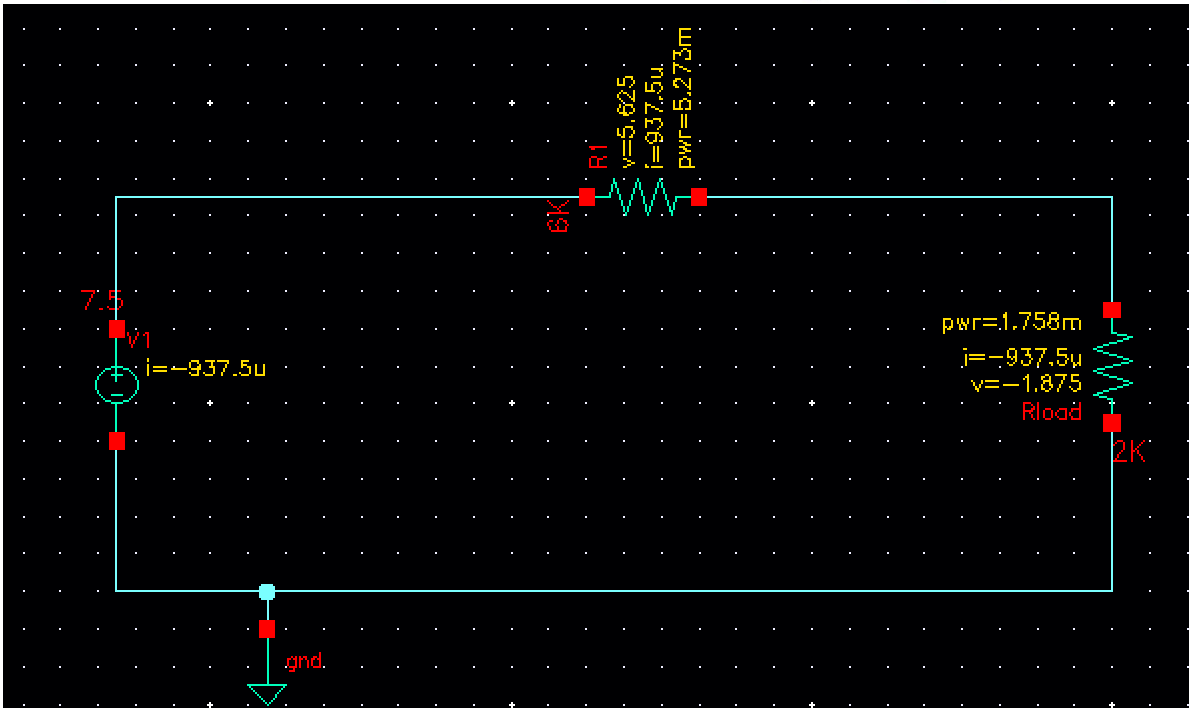


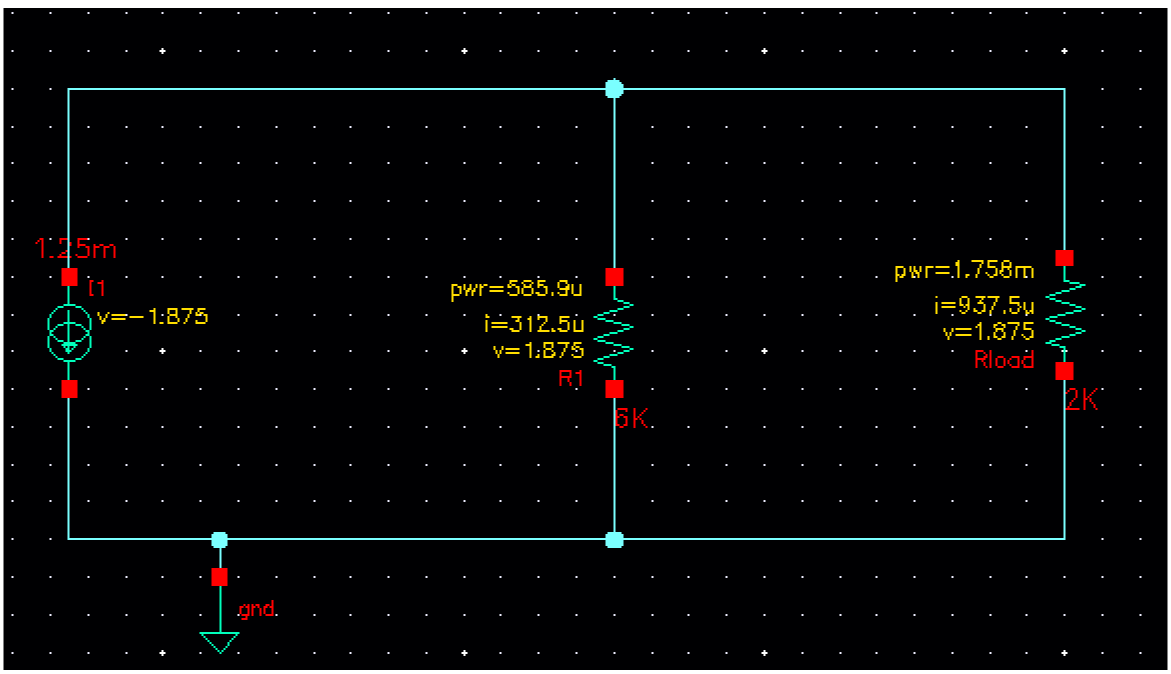

Launch
File
Edit
View
Create
Check
Options
Migrate
Window
ADE L
ADE XL
ADE GXL
Layout XL
Layout GXL
Schematics L
Schematics XL
Create Model (SMG)
Diva
Hierarchy Editor
IC Packaging(SiP)
IC Testbenches
Mixed Signal Options
Parasitics
Pcell IDE
Simulation
Workspace: Basic
Property Editor


Virtuoso® Analog Design Environment L Editing: AUC __ schematic
Virtuoso® Analog Design Environment (2) - AUC __ schematic
Launch
Session
Setup
Analyses
Variables
Outputs
Simulation
Results
Tools
Help
cādence
Design Variables
Name
Value
Analyses
Type
Enable
dc
Outputs
Name/Signal/Expr
Plot Outputs
Direct Plot
Print
Annotate
Vector
Circuit Conditions ...
Violations Display ...
Reliability Data
Save ...
Select ...
Delete ...
Printing/Plotting Options ...
DC Node Voltages
DC Operating Points
Model Parameters
Transient Node Voltages ...
Transient Operating Points
Net Names
Component Parameters
Design Defaults
Show Parasitics
Hide Parasitics
> Results in /home/buet/simulation/__/spe
Plot after simulation: Auto
Plotting mode: Replace
mouse L:
M:
R:
3(4)
Hide Parasitics
Status: Ready
T=27 C
Simulator: spectre
R3
r=4K
7.5
R2
r=4K
7,5
Ø


R1
v=10
i=2.5m
pwr=25m
4K
R3
v=5
i=1.25m
pwr=6.25m
4K
V1
i=-2.5m
pwr=6.25m
i=-1.25m
v=-5
R2
4K
pwr=0
i=0
v=0
Rload
4K
gnd


R1
v=9.375
i=2.344m
pwr=21.97m
4K
R3
v=3.75
i=937.5u
pwr=3.516m
4K
V1
i=-2.344m
pwr=7.91m
i=-1.406m
v=-5.625
R2
4K
pwr=1.758m
i=-937.5u
v=-1.875
Rload
2K
gnd


R1
v=5.625
i=937.5u
pwr=5.273m
6K
7.5
V1
i=-937.5u
pwr=1.758m
i=-937.5u
v=-1.875
Rload
2K
gnd


1.25m
I1
v=-1.875
pwr=585.9u
i=312.5u
v=1.875
R1
6K
pwr=1.758m
i=937.5u
v=1.875
Rload
2K
gnd

B- Nodal-Analysis Technique:

Multi-source DC circuits may be analyzed using the nodal analysis technique. The process involves identifying all of the circuit nodes, a node being a point where various branch currents combine. A reference node, usually ground, is included. Kirchhoff's Current Law is then applied to each node. Consequently, a set of simultaneous equations are created with an unknown voltage for each node with the exception of the reference.

1. Experiment:

- Connections are made as shown in Fig.1
- Measure actual values Table.1.

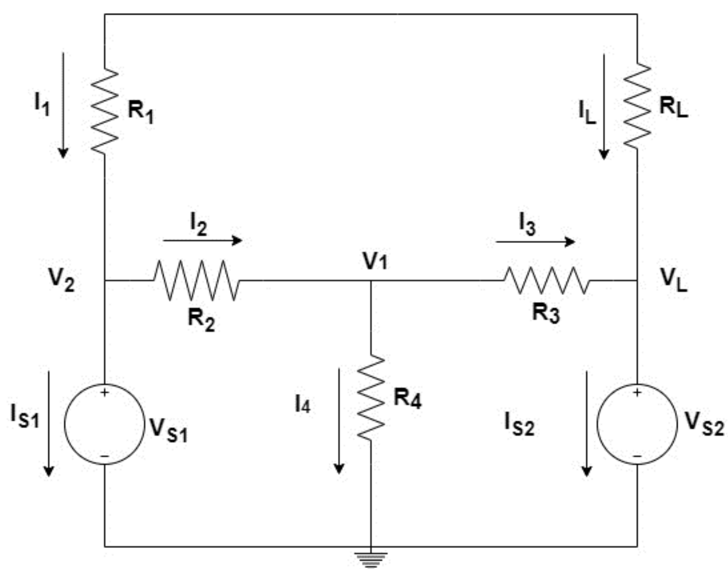


Figure 1: Connection Diagram for the Dual Voltage Supply Experimental Network.
Vs1 = 13V(nominal), Vs2 = 5V (nominal), R1 = 1.4-2.4 kΩ, R2 = 2.9-5.1 kΩ,R3 = 6.5-8 kΩ, R4 = 9.5-16 kΩ, RL = 2.6-3.6 kΩ (3.3 kΩ nominal)

Table 1 Component Actual values

	Vs1	Vs2	R1	R2	R3	R4	RL
Value							

- Calculate Node Voltages using the component's actual-values

$$\Delta\% = \frac{V_{j,meas} - V_{j,calc}}{V_{j,calc}} \times 100$$

Table 2 Node Voltages

	V1	V2	VL
Calculated			
Measured			
Δ%			

- Calculate Branch Currents using the component's actual-values

$$\Delta\% = \frac{I_{j,meas} - I_{j,calc}}{I_{j,calc}} \times 100$$

Table 3 Branch Currents:

	I1	I2	I3	I4	Is1	Is2	IL
Calculated							
Measured							
Δ%							

- For ALL power calculations assume that the PASSIVE Sign convention relates component voltage-polarities and current-directions.
- Calculation-1: Use the component's actual values.
- Calculation-2: Use the measured values of V-across, and I-through for the two supplies from the previous tables 2-3.

$$\Delta\% = \frac{P_{j,meas} - P_{j,calc}}{P_{j,calc}} \times 100$$

Table. 4 Power from sources

	Pvs1	Pvs2	∑Pvsj
Calculated			
Measured			
Δ%			

Table. 5 Power absorbed by resistors.

	P_{R1}	P_{R2}	P_{R3}	P_{R4}	P_{Rl}	$\sum P_{Rj}$
Calculated						
Measured						
Δ%						

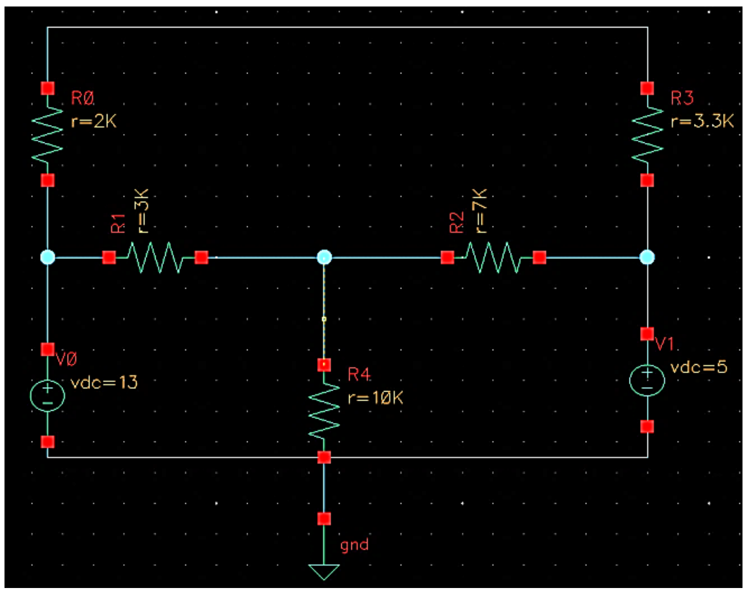
$$\Delta_{OB}\% = \frac{\sum P_{Vsj} - \sum P_{Rj}}{|\sum P_{Vsj}| + |\sum P_{Rj}|} \times 100$$

Table 6 Power balance

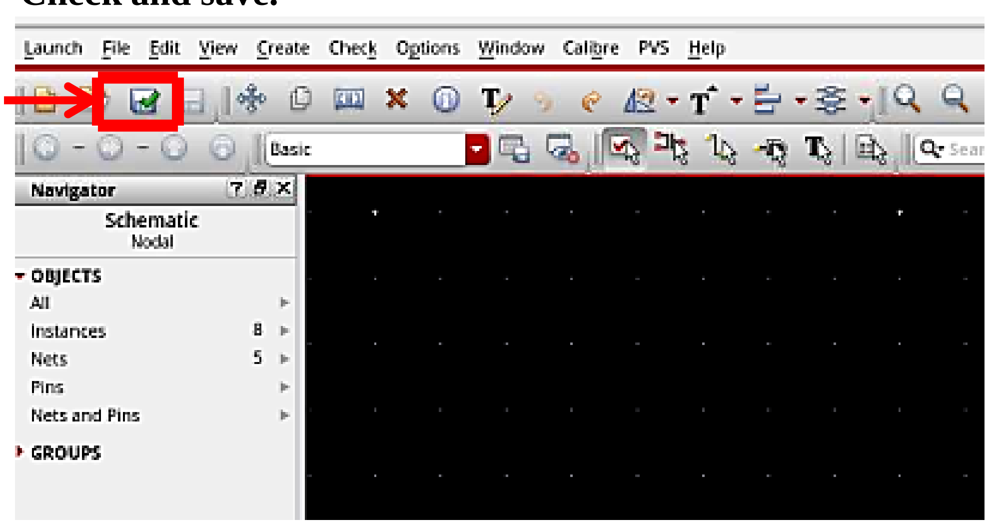
	$\sum P_{VSj}$	$\sum P_{Rj}$	% out of balance
Calculated			
Measured			

2. Simulation Procedures:

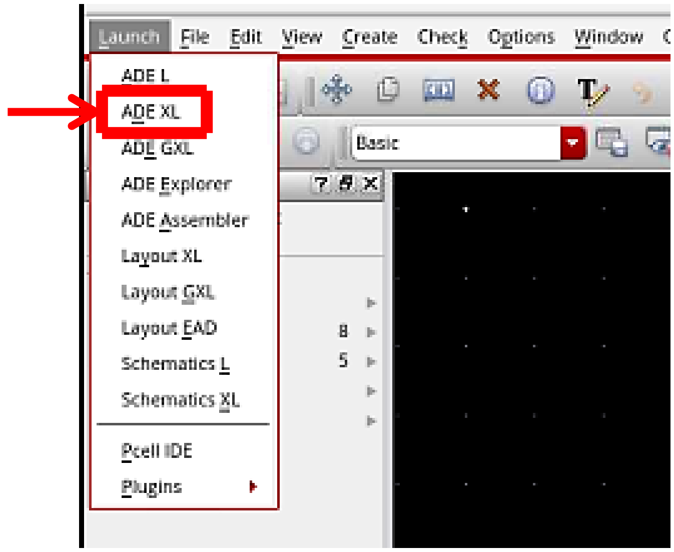
- Draw SCHEMATIC



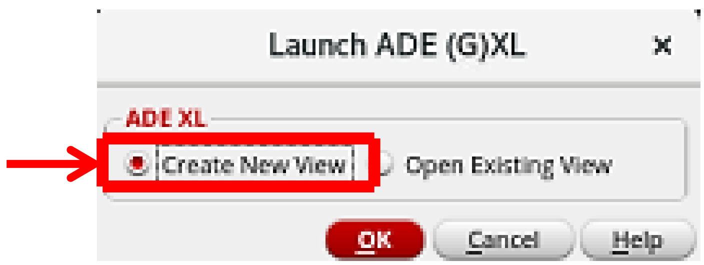
- **Check and save.**



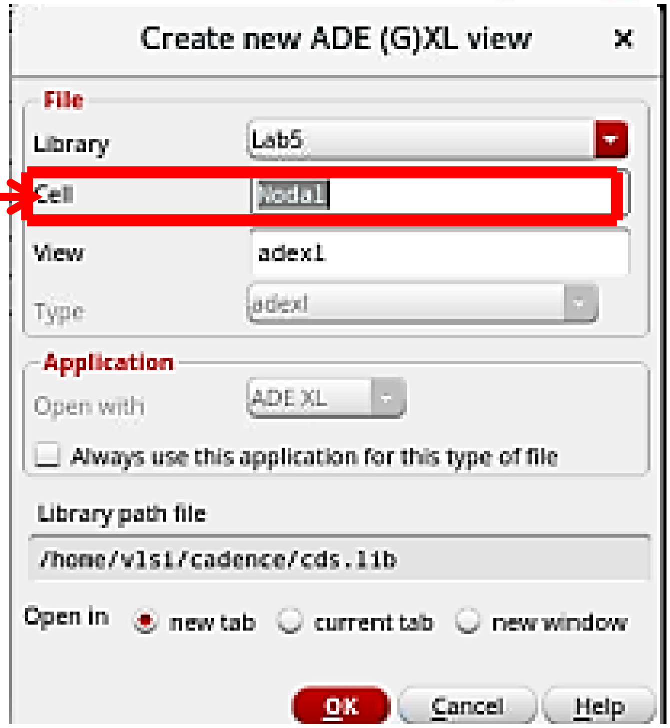
- **Lunch => ADE XL**



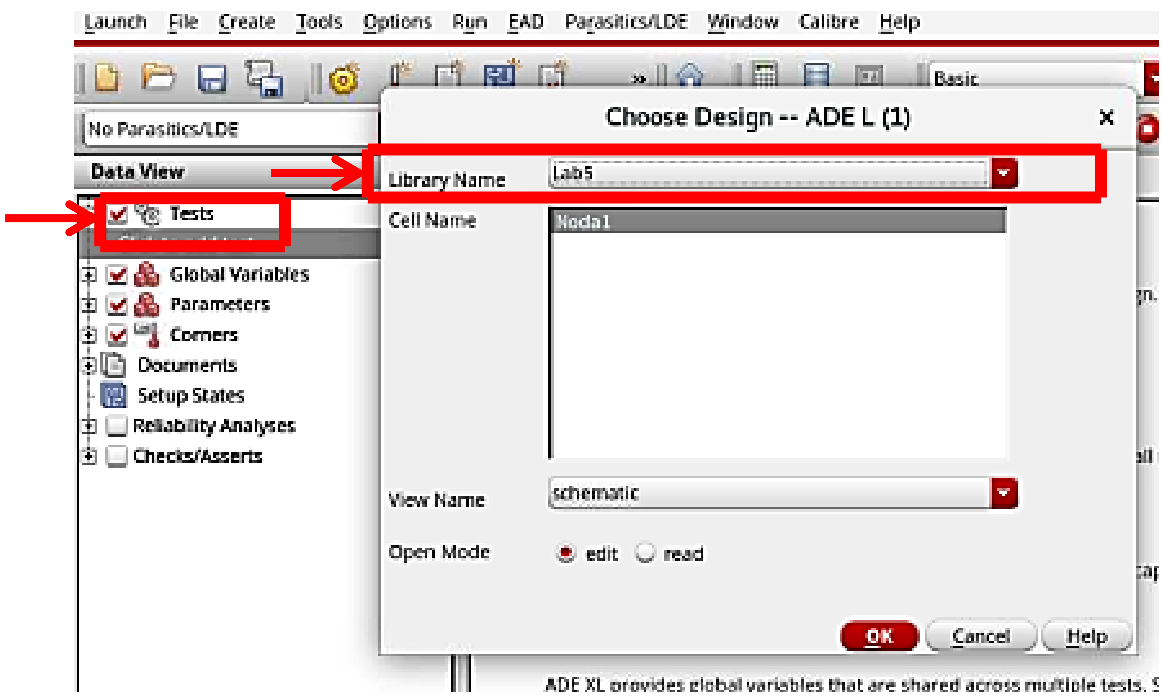
- **Create New View => OK**



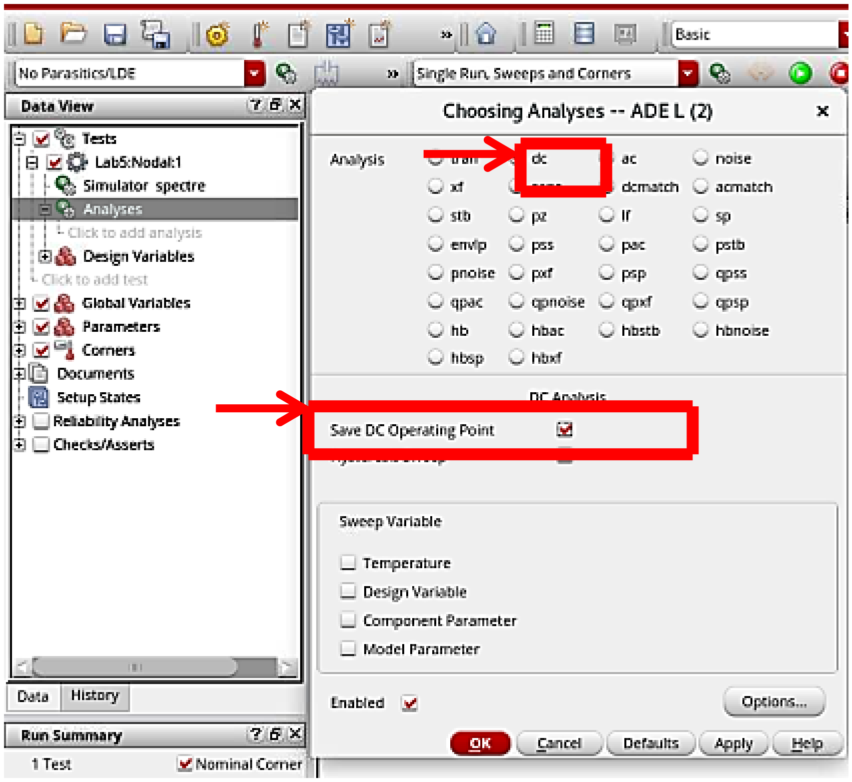
- **Cell => “nodel” => OK**



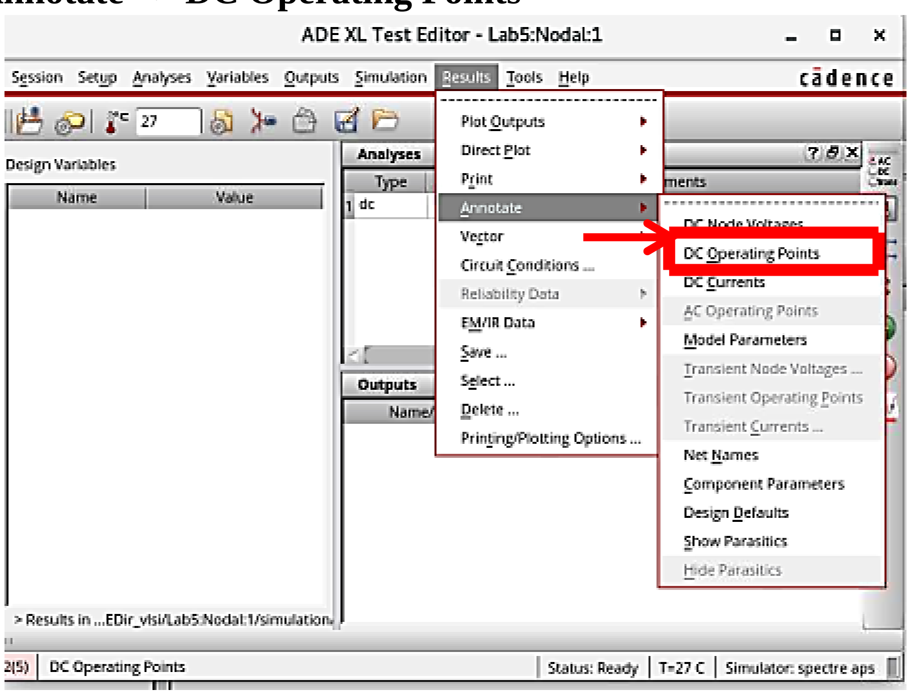
➢ **Click "Tests" => Cell Name "nodel" => OK**



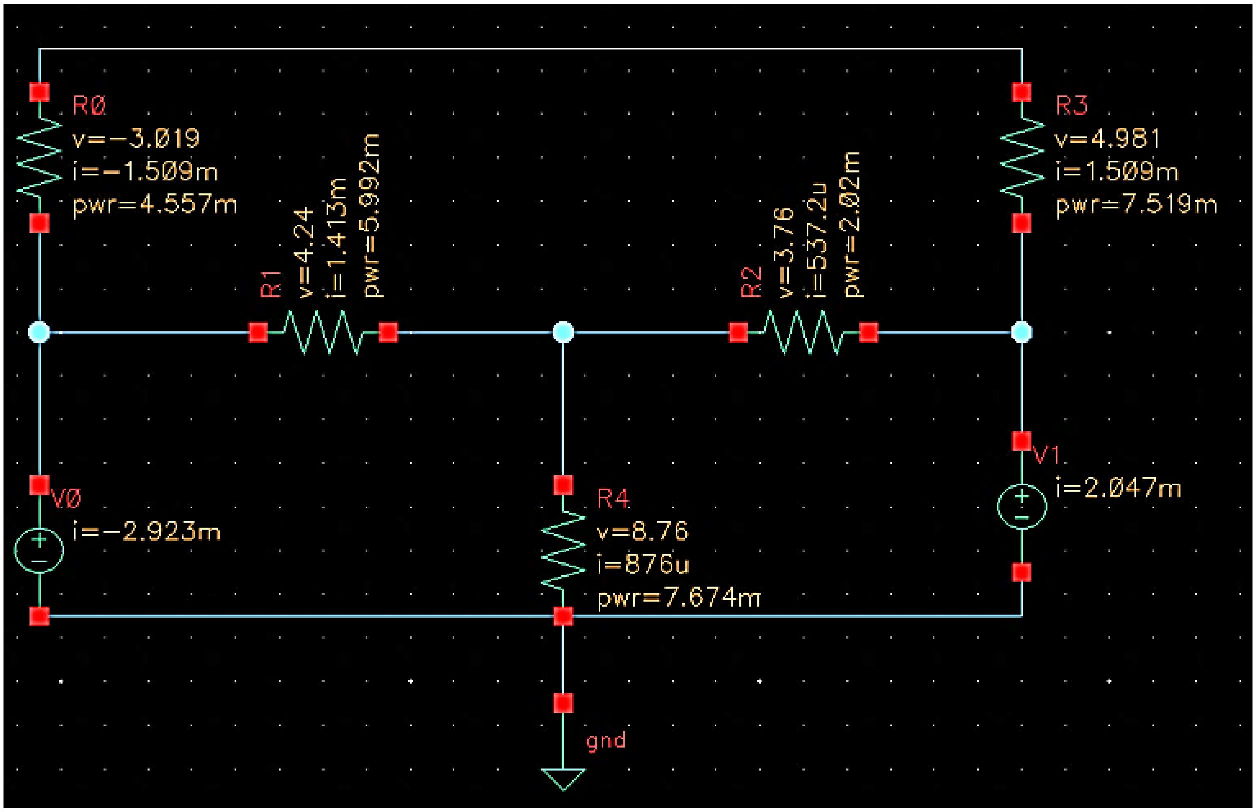
- **Analysis => dc**
- **Save DC Operating Points => DC Analysis**



- **Annotate => DC Operating Points**

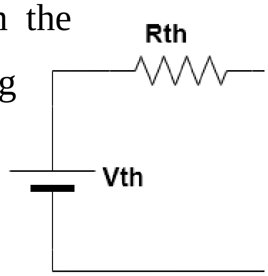


➢ The Result


R0
v=−3.019
i=−1.509m
pwr=4.557m
R1
v=4.24
i=1.413m
pwr=5.992m
R2
v=3.76
i=537.2u
pwr=2.02m
R3
v=4.981
i=1.509m
pwr=7.519m
V0
i=−2.923m
R4
v=8.76
i=876u
pwr=7.674m
V1
i=2.047m
gnd

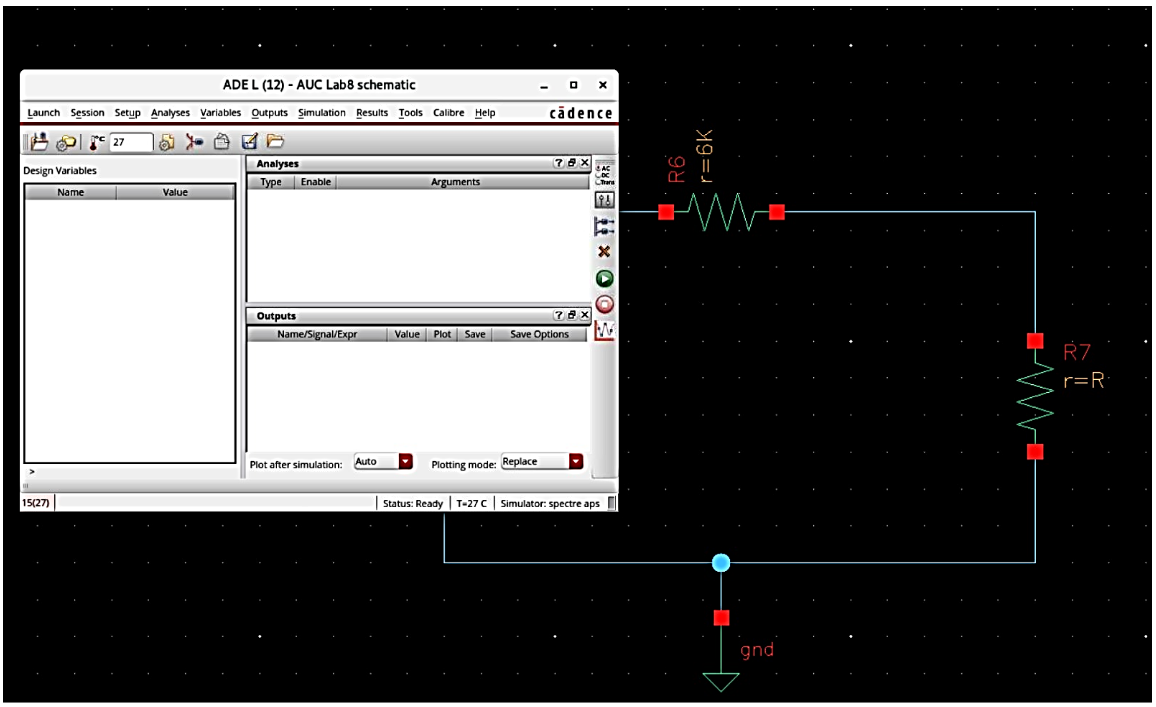
C- Maximum Power Transfer Verification

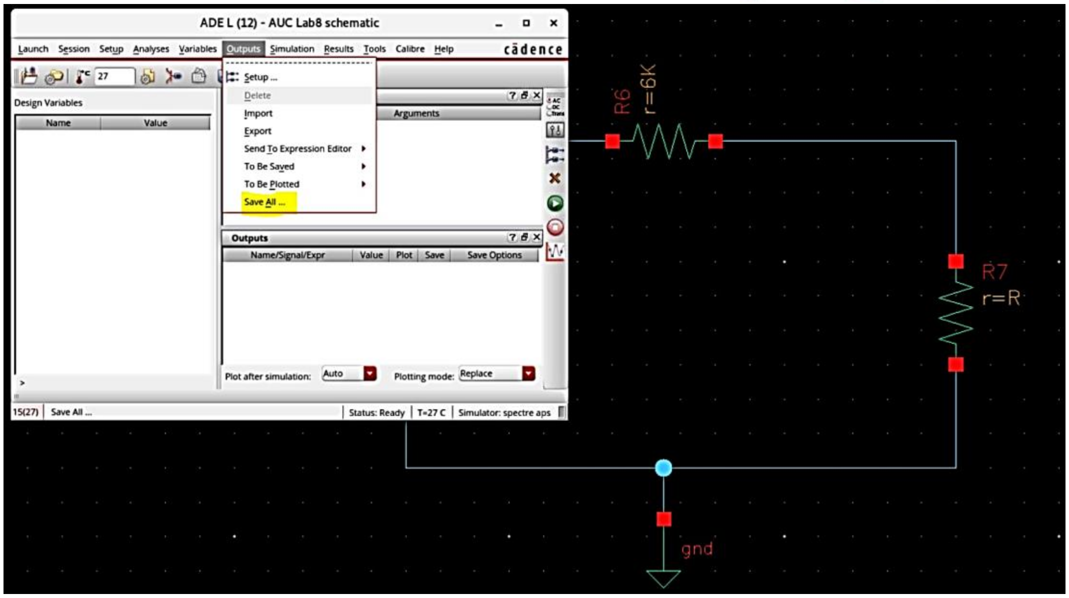
Using the simulator, add a potentiometer (variable resistor) as a load to terminals a-b in the circuit of Figure 3 (use the Vth and Rth values from the previous part of this lab). Then, measure the load average power using the wattmeter for different load values. Specify and connect the load that results in the maximum power transfer. Then, verify the max power transfer theory. Record your observations in the table below.

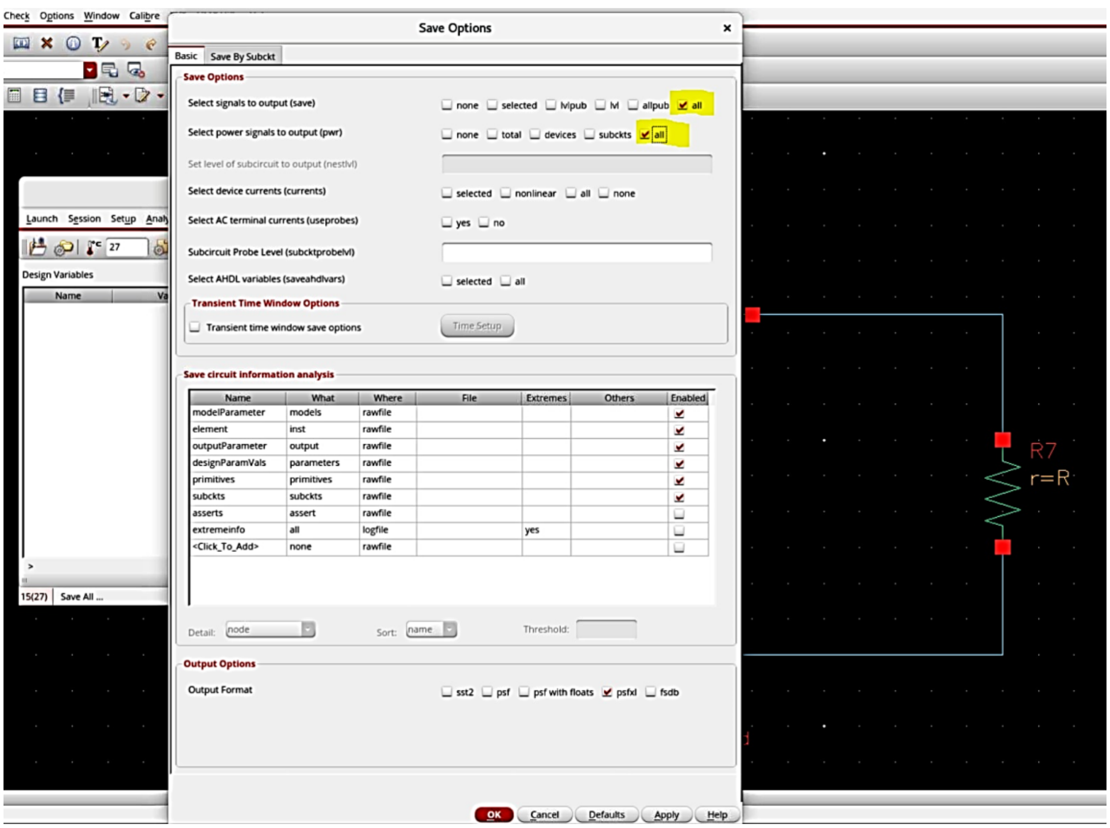


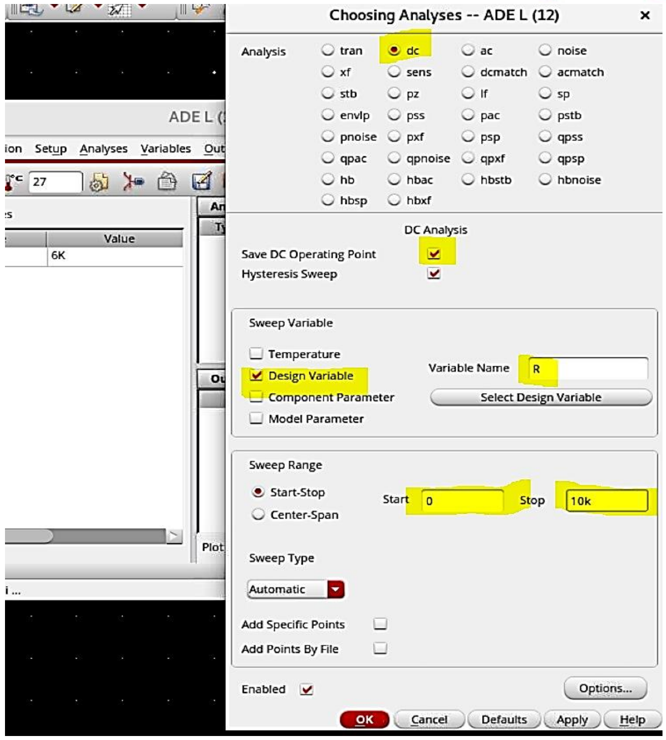
Q: Did the maximum power transfer to the load when R_L was equal to R_{th}?

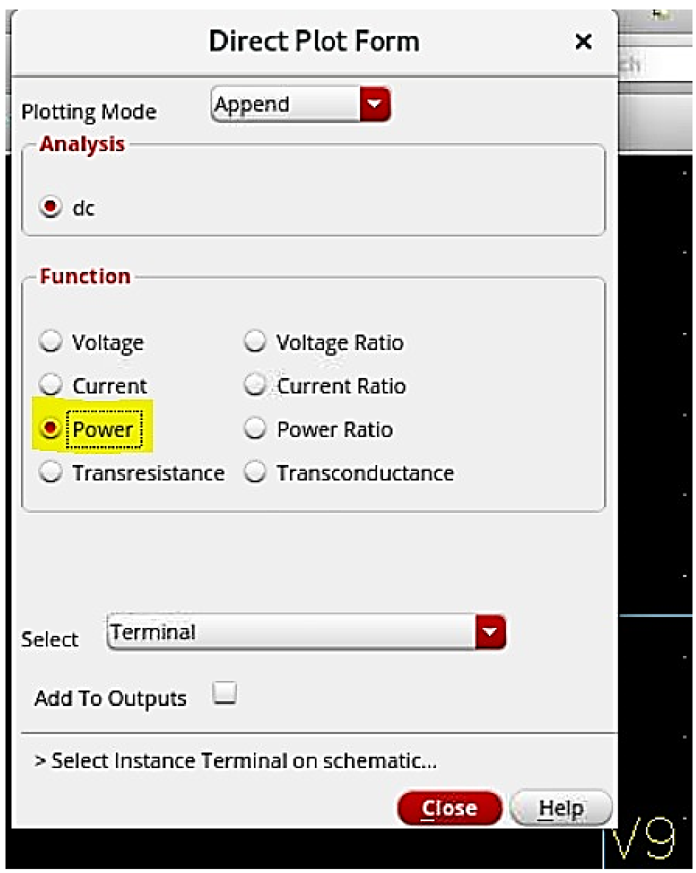
R_L											
P_L											

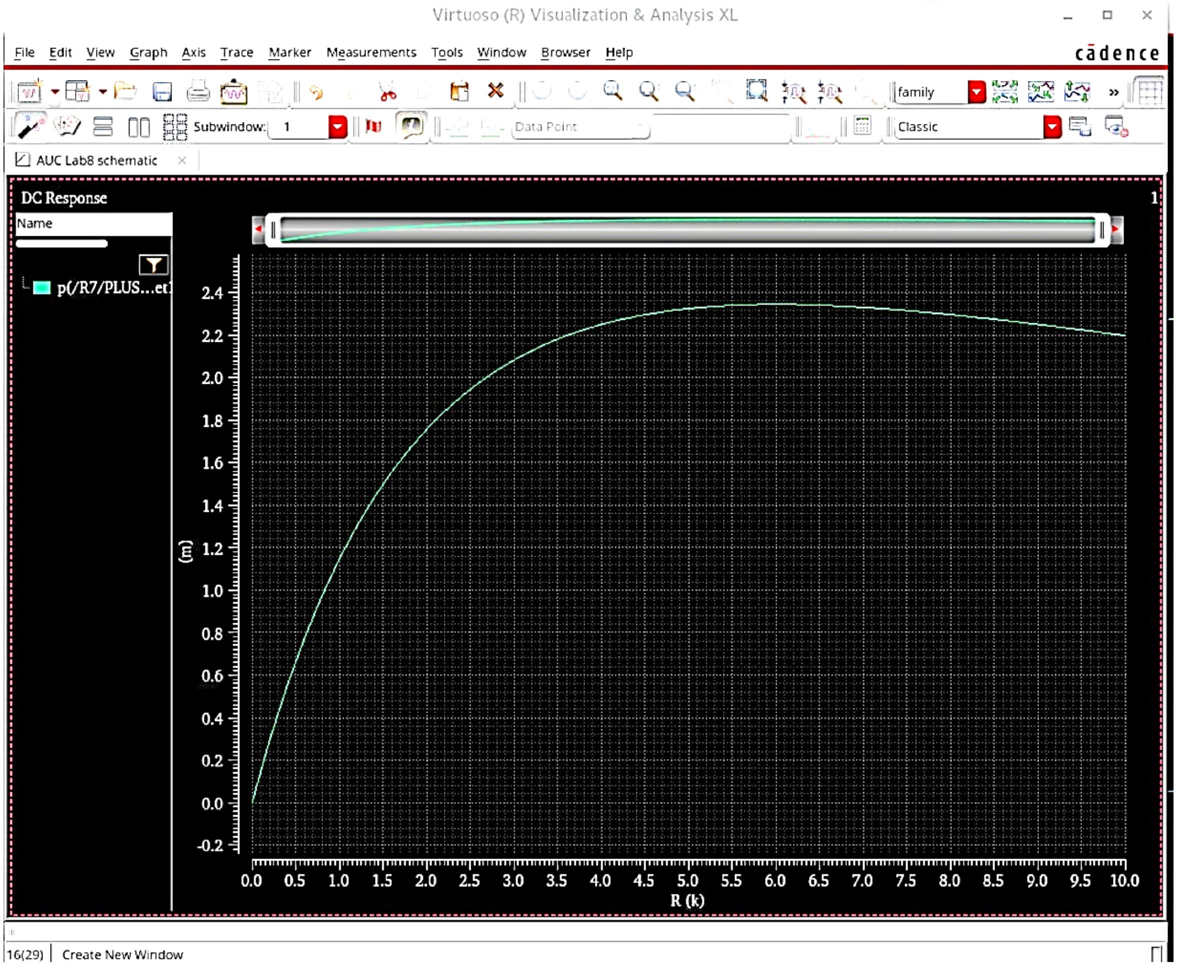


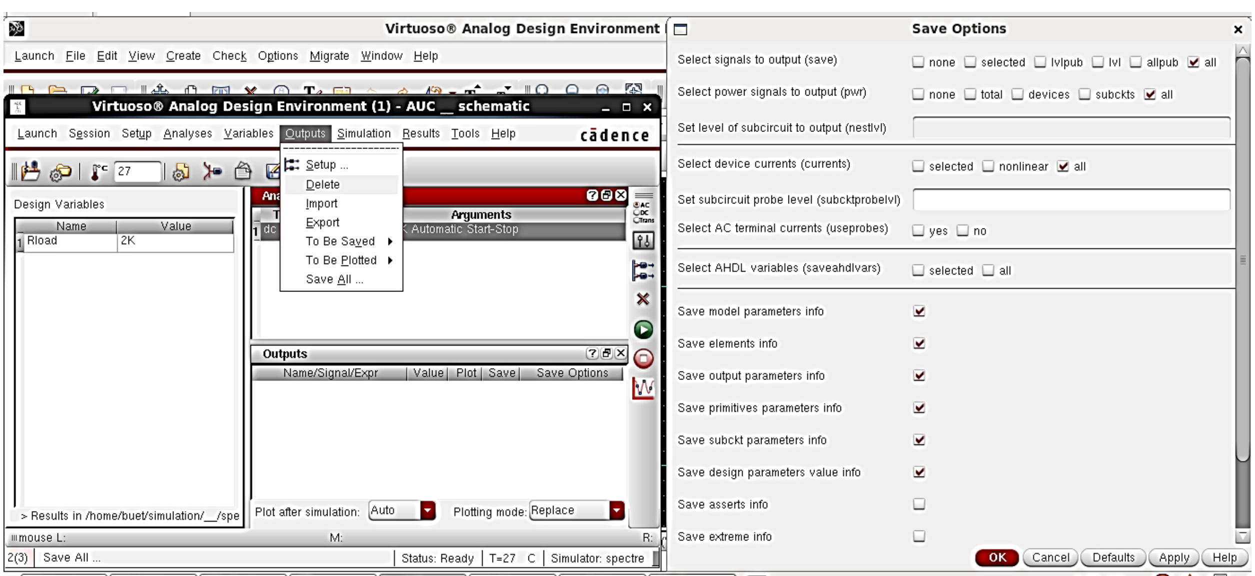

ADE L (12) - AUC Lab8 schematic
Launch Session Setup Analyses Variables Outputs Simulation Results Tools Calibre Help
cādence
Design Variables
Name Value
Setup ...
Delete
Import
Export
Send To Expression Editor
To Be Saved
To Be Plotted
Save All ...
Arguments
Outputs
Name/Signal/Expr Value Plot Save Save Options
Plot after simulation: Auto
Plotting mode: Replace
15(27) Save All ...
Status: Ready T=27 C Simulator: spectre aps
R6
r=6K
R7
r=R
gnd

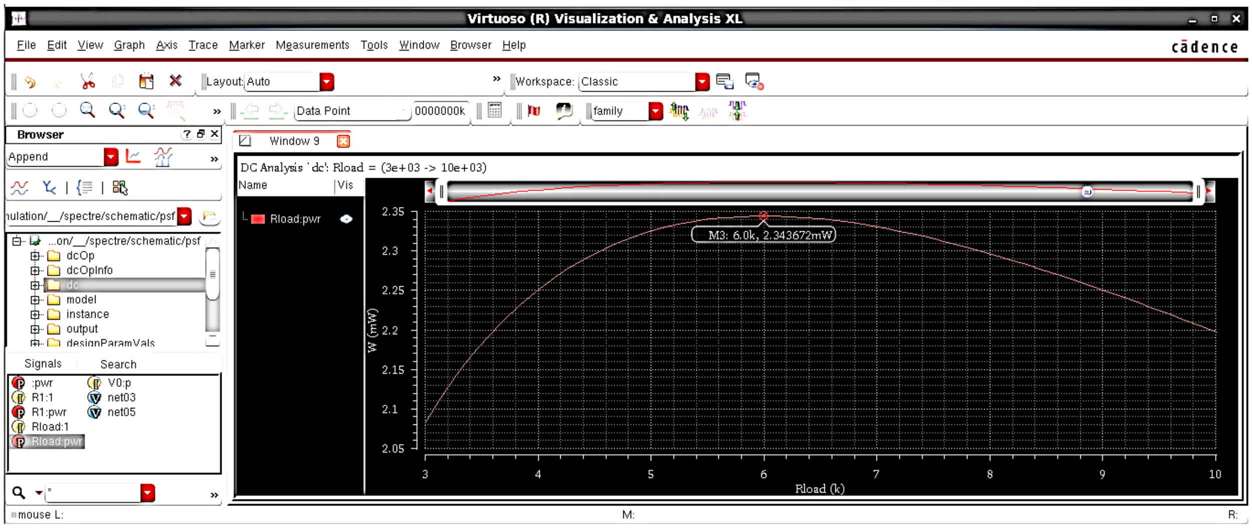

Save Options
Basic Save By Subckt
Save Options
Select signals to output (save) none selected lvlpub lvl allpub all
Select power signals to output (pwr) none total devices subckts all
Set level of subcircuit to output (nestlvl)
Select device currents (currents) selected nonlinear all none
Select AC terminal currents (useprobes) yes no
Subcircuit Probe Level (subcktprobelvl)
Select AHDL variables (saveahdlvars) selected all
Transient Time Window Options
Transient time window save options
Time Setup
Save circuit information analysis
Name What Where File Extremes Others Enabled
modelParameter models rawfile
element inst rawfile
outputParameter output rawfile
designParamVals parameters rawfile
primitives primitives rawfile
subckts subckts rawfile
asserts assert rawfile
extremeinfo all logfile yes
<Click_To_Add> none rawfile
Detail: node
Sort: name
Threshold:
Output Options
Output Format sst2 psf psf with floats psfxl fsdb
OK Cancel Defaults Apply Help
R7
r=R


Choosing Analyses -- ADE L (12)
Analysis
tran
dc
ac
noise
xf
sens
dcmatch
acmatch
stb
pz
lf
sp
envlp
pss
pac
pstb
pnoise
pxf
psp
qpss
qpac
qpnoise
qpxf
qpsp
hb
hbac
hbstb
hbnoise
hbsp
hbxf
DC Analysis
Save DC Operating Point
Hysteresis Sweep
Sweep Variable
Temperature
Design Variable
Component Parameter
Model Parameter
Variable Name
R
Select Design Variable
Sweep Range
Start-Stop
Center-Span
Start
0
Stop
10k
Sweep Type
Automatic
Add Specific Points
Add Points By File
Enabled
Options...
OK
Cancel
Defaults
Apply
Help


Direct Plot Form
Plotting Mode
Append
Analysis
dc
Function
Voltage
Voltage Ratio
Current
Current Ratio
Power
Power Ratio
Transresistance
Transconductance
Select
Terminal
Add To Outputs
> Select Instance Terminal on schematic...
Close
Help


Virtuoso (R) Visualization & Analysis XL
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
Subwindow: 1
Data Point
family
Classic
AUC Lab8 schematic
DC Response
Name
p(/R7/PLUS...et)
(m)
2.4
2.2
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
-0.2
0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0 4.5 5.0 5.5 6.0 6.5 7.0 7.5 8.0 8.5 9.0 9.5 10.0
R (k)
16(29)
Create New Window


Virtuoso® Analog Design Environment
Launch File Edit View Create Check Options Migrate Window Help
Virtuoso® Analog Design Environment (1) - AUC _ schematic
Launch Session Setup Analyses Variables Outputs Simulation Results Tools Help
cadence
Setup ...
Delete
Import
Export
To Be Saved
To Be Plotted
Save All ...
Design Variables
Name
Value
Rloat
2K
Arguments
Automatic Start-Stop
Outputs
Name/Signal/Expr
Value
Plot
Save
Save Options
Plot after simulation: Auto
Plotting mode: Replace
> Results in /home/buet/simulation/__/spe
mouse L:
M:
R:
Save All ...
Status: Ready
T=27 C
Simulator: spectre
Save Options
Select signals to output (save)
none
selected
lvlpub
lvl
allpub
all
Select power signals to output (pwr)
none
total
devices
subckts
all
Set level of subcircuit to output (nestlvl)
Select device currents (currents)
selected
nonlinear
all
Set subcircuit probe level (subcktprobelvl)
Select AC terminal currents (useprobes)
yes
no
Select AHDL variables (saveahdlvars)
selected
all
Save model parameters info
Save elements info
Save output parameters info
Save primitives parameters info
Save subckt parameters info
Save design parameters value info
Save asserts info
Save extreme info
OK
Cancel
Defaults
Apply
Help



Assignment 2

- Find the Thevenin and Norton equivalent for the following circuit at R_{load} = 6K. Also, verify that the maximum power transfer happens when $R_L = R_{th}$.

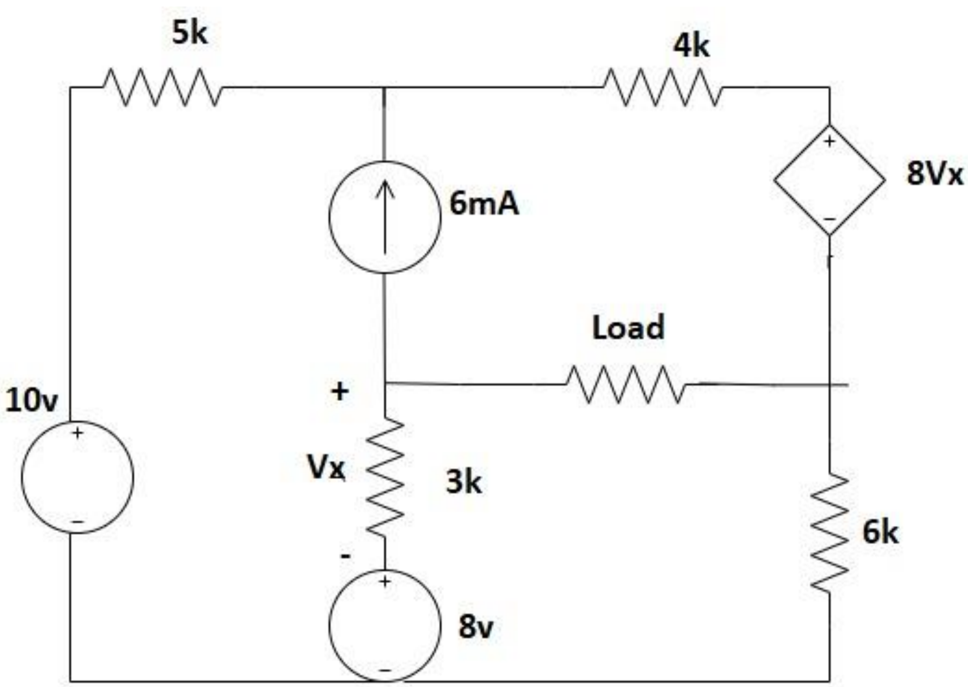


Figure 2 applied circuit

Bounus Questions of Lab 2

- Using Cadence, Find the Thevenin equivalent for the following circuit at RL=2ohm
- Also, verify that the maximum power transfer happens when RL = Rth.

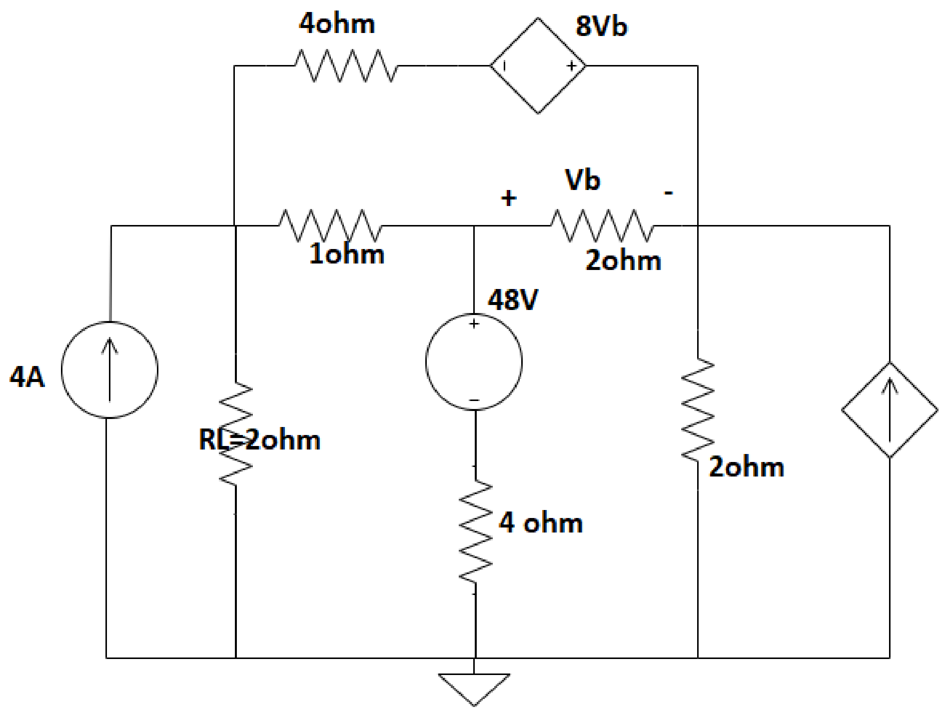


Figure 3 applied circuit 2