Design Project	CND 101 Introduction to Analog Design	Project #1

Title: Programmable CMOS Ring Oscillator
Supervisor: Dr. Reda – Dr. Samar

Description:

Ring oscillators are widely used in various applications, such as clock signal generation, frequency synthesis, and delay-line elements in digital systems. This project will focus on the design, analysis, and practical implementation of a ring oscillator for frequency generation. Ring oscillators are made of several inverting stages, with feedback.
Design and simulate a programmable CMOS ring oscillator.

Design Requirements:

- The oscillator should operate at frequencies (1 MHz, 5 MHz, 10 MHz). This can be achieved by changing one or more of the below:
  - Transistor sizing
  - Number of inverting stages

- The output waveform should be balanced (rise time = fall time) by optimizing the Gate width ratio.

Assessment Criteria:

- Circuit design and implementation --- 50%
- Functionality --- 30%
- Design metrics evaluation (Power, Number of transistors) --- 20%
- Bonus: output sinusoidal wave by using a filter.

The following need to be delivered:

- A technical report (word format)
- PowerPoint presentation for 20 minutes (PowerPoint format and recorded video)
- Simulation for the proposed electronic circuit using Cadence.

The technical report needs to include the following:

- Introduction about the selected electronic circuit
- Background about the application that is selected.
- Technical detail and simulation results
- Comparison between the circuit analysis and simulation results
- Discussion and conclusion

Best of Luck!

Design Project	CND 101 Introduction to Analog Design	Project #2

Title: Buck and Boost DC-DC Converter
Supervisor: Dr. Samar - Dr. Reda

Description:

A buck-boost DC-DC converter is a type of power electronics device used to efficiently regulate the voltage. It can both step down (buck) and step up (boost) the input voltage to provide a stable output voltage, making it versatile for various applications. This converter is capable of handling input voltage levels that are either higher or lower than the desired output voltage. By adjusting the duty cycle of its switching components, typically transistors or diodes, it can control the output voltage while maintaining good efficiency.
Design and simulate a Buck-Boost DC-DC converter circuit.

Design Requirements:

- The Buck-Boost circuit should operate in the voltage ranges (1-2)↔(3-4) VDC.
- Test the efficiency at different switching frequencies 100KHz – 10 MHz, plot the frequency response (AC analysis).

Assessment Criteria:

- Circuit design and implementation --- 50%
- Functionality --- 30%
- Design metrics evaluation (Stability, Efficiency, Power) --- 20%
- Bonus: add a control circuitry of the Buck-Boost for controlling the duty cycle.

The following need to be delivered:

- A technical report (word format)
- PowerPoint presentation for 20 minutes (PowerPoint format and recorded video)
- Circuit analysis for the proposed electronic circuit
- Simulation for the proposed electronic circuit using Cadence.

The technical report needs to include the following:

- Introduction about the selected electronic circuit
- Background about the application that is selected.
- Technical detail, circuit analysis, and simulation results
- Comparison between the circuit analysis and simulation results
- Discussion and conclusion

Best of Luck!

Design Project	CND 101 Introduction to Analog Design	Project #3

Title: Design of active second-order antialiasing filter
Supervisor: Dr. Mostafa Nawito

Description: Signal conditioning systems are often used to adjust sensor signals before they are measured with an analog-to-digital converter or an oscilloscope. Especially before sampling, it is important to remove high-frequency components, such as noise, to reduce aliasing effects as much as possible. For this purpose, active filters are important because they can perform impedance matching during filtering.

The objective of this project is to design and simulate a second-order active anti-aliasing filter used before sampling a signal with an analog-to-digital converter.
The following specifications are given:

- The maximum bandwidth of the input signal is 250 kHz.
- The analog-to-digital converter operates between 0V and 3.3V.
- A Sallen-Key topology must be chosen for the filter.
-

Requirements:

- Determine the sampling frequency of the analog-to-digital converter and the cutoff frequency of the filter.
- Prepare the circuit diagram of the filter circuit.
- Calculate the values of the passive components needed for the filter and explain the equations used to do so.
- For the simulation, implement the opamp either as a VCVS or use a suitable opamp model in the standard Cadence libraries, like basic or ahdllib
- Simulate the circuit of the active filter in the time domain and in the frequency domain and select an appropriate test signal to demonstrate the correct operation of the filter.
- Explain the simulation results and compare them with the calculated values of the cut-off frequency.

Assessment Criteria:

- Did the student correctly calculate the 3-db frequency and is it equal to half of the Nyquist rate?
- Is the circuit diagram correct and does it indeed show a Sallen-Key topology?
- Are the calculated values of the passive components correct?
- Is the modeling of the opamp correct?
- Does the filter work properly and is the output signal compatible with the ADC that follows?

The following need to be delivered:

- A technical report (word format)
- PowerPoint presentation for 20 minutes (PowerPoint format and recorded video)
- Circuit analysis for the proposed electronic circuit
- Simulation for the proposed electronic circuit using Cadence.

The technical report needs to include the following:

- Introduction about the selected electronic circuit
- Background about the application that is selected.
- Technical detail, circuit analysis, and simulation results
- Comparison between the circuit analysis and simulation results
- Discussion and conclusion

Best of Luck!

Design Project	CND 101 Introduction to Analog Design	Project #4

Title: Amplifier Design Using BJT
Supervisor: Dr. Maged Bekheit

Description:
The purpose of the project is to design, build, and test a bipolar junction transistor (BJT) amplifier circuit. The goal is to gain hands-on experience in designing and analyzing amplifiers, applying the principles of BJT operation, biasing, and small-signal analysis. Students will choose one of the common BJT amplifier configurations and optimize it for a specific application.

Objectives:
- Gain a deep understanding of BJT amplifier theory, including BJT operation and small-signal analysis.
- Learn how to select BJT components for an amplifier design.
- Design and build a BJT amplifier circuit.
- Optimize the amplifier for specific performance characteristics, such as gain and bandwidth.
- Gain practical experience in simulation and testing and troubleshooting amplifier circuits.

Requirements:
- Amplifier Configuration Selection: Students will choose one of the common BJT amplifier configurations, such as common-emitter (CE), common-base (CB), or common-collector (CC). The choice will depend on the desired characteristics and application.
- Component Selection: Students will research and select appropriate BJT transistors and passive components, including resistors, capacitors, and potentially inductors, for the amplifier design.
- Biasing Network Design: They will design the biasing network to set the DC operating point of the BJT in a stable and linear region.
- Small-Signal Analysis: Students will perform small-signal analysis of the amplifier, calculating gain, input impedance, and output impedance.
- Frequency Response verification: Students will verify the amplifier bandwidth.
- Simulation, Testing and Characterization: Students will simulate the circuit to verify all its characteristics.
- Circuit Building: Students will build the amplifier circuit on a protoboard or PCB, ensuring that all components are correctly connected.
- Measurements If applicable, test the built amplifier's performance by applying input signals and measuring the output response. This includes verifying gain, bandwidth, and other relevant characteristics.

Bonus:

- Reconstruct the same amplifier design using CMOS.
- Add a second stage to improve the gain in both technologies and make a comparison between the CMOS and BJT technologies in terms of the gain and the input impedance.

Assessment Criteria:

- Documentation: Assess the completeness and clarity of the project documentation. This should include circuit diagrams, component specifications, calculations, and design considerations.
- Design and Analysis: Evaluate the accuracy and effectiveness of the amplifier design, including biasing, component selection, small-signal analysis, and optimization (if applicable).
- Circuit simulation and Implementation: Examine the quality of the constructed circuit. This includes how well it adheres to the design. Also, any troubleshooting is needed if there is any gap between the designed performance and the actual performance.
- Testing and verification: Assess the practical testing of the amplifier. This includes measuring key performance parameters such as gain, bandwidth, distortion, and input/output impedance. Verify that measurements align with the design objectives. Note this can be done through simulation if no hardware implementation is available.
- Presentation: Evaluate the clarity and organization of the project presentation, which could be in the form of a report or an in-class presentation. This should include a summary of the project, design rationale, and key results.

The following need to be delivered:

- A technical report (word format)
- PowerPoint presentation for 20 minutes (PowerPoint format and recorded video)
- Circuit analysis for the proposed electronic circuit
- Simulation for the proposed electronic circuit using Cadence.

The technical report needs to include the following:

- Introduction about the selected electronic circuit
- Background about the application that is selected.
- Technical detail, circuit analysis, and simulation results
- Comparison between the circuit analysis and simulation results
- Discussion and conclusion

Best of Luck!

Design Project	CND 101 Introduction to Analog Design	Project #5

Title: Power Amplifier Class AB

Supervisor: Dr. Yehya Ghallab

Project Description: A Class AB power amplifier output stage is a common design in audio amplification. It combines the efficiency of Class B amplifiers with the linearity of Class A amplifiers. In a Class AB output stage, two transistors are used to amplify the positive and negative halves of the input signal, respectively.

Design and simulate a Power Amplifier Class AB.

The following need to be delivered:

- A technical report (word format)
- PowerPoint presentation for 20 minutes (PowerPoint format)
- Circuit analysis for the proposed electronic circuit
- Simulation for the proposed electronic circuit using Cadence.

The technical report needs to include the following:

- Introduction about the selected electronic circuit
- Background about the application that is selected.
- Technical detail, circuit analysis, and simulation results
- Comparison between the circuit analysis and simulation results
- Discussion and conclusion

Best of Luck!

Design Project	CND 101 Introduction to Analog Design	Project #6

Title: Two-Stage Differential Input Single-Ended Output CMOS Amplifier

Supervisor: Dr. Mamdouh Abdelmejeed

Project Overview:

In this analog course design project, students will design, simulate, and analyze a two-stage differential input single-ended output CMOS amplifier with specific specifications. This project aims to develop students' skills in CMOS analog circuit design and analysis while addressing the unique challenges of designing amplifiers that meet precise performance requirements.

Project Specifications:

Design a two-stage CMOS amplifier with differential input and single-ended output according to the specified specifications. You may incorporate a single current source for bias generation using a current mirror, as illustrated in the suggested topology below. However, you have the flexibility to explore and employ alternative circuit topologies that best meet the project specs.

Technology	65 nm UMC
VDD	3V
Voltage Gain	2500 V/V
Bandwidth	120 MHz
Common Mode range	1V
Maximum Output Swing	2.2V
Phase margin	70
CMRR	??dB
Power	minimize
Iref	150 uA

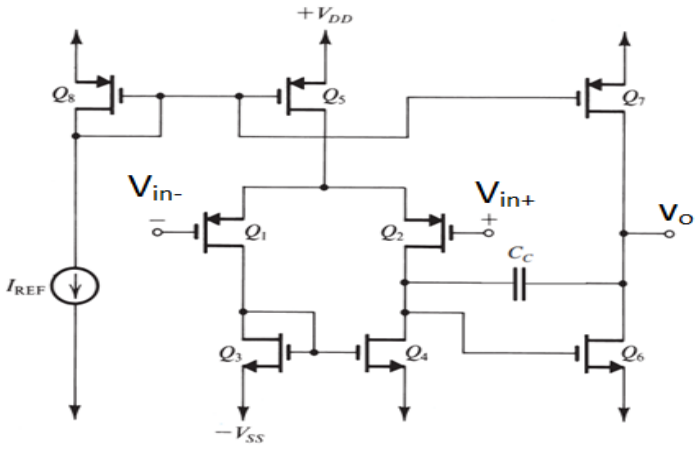


Figure 1 Suggested 2-stage amplifier circuit

Project Deliverables:

1. **Project Proposal:**
    - A detailed project proposal outlining your approach to meeting the specifications and your initial design choices.

2. **Schematic Design:**
    - Create the schematic of the two-stage CMOS amplifier using appropriate design tools, specifying component values and transistor sizes.
3. **DC Analysis:**
    - Perform DC biasing analysis to determine the operating point, including quiescent voltage levels, currents, and transistor regions of operation.
4. **AC Analysis:**
    - Conduct AC analysis to determine the gain, bandwidth, and input/output impedance of the amplifier.
5. **Transient Analysis:**
    - Simulate the amplifier's response to transient input signals to ensure proper amplification and signal fidelity.
6. **Final Report:**
    - Present a comprehensive report detailing the design process, simulation results, analysis, optimization, and conclusions. Include a discussion of how well the specifications were met.

Evaluation Criteria:

Students' performance will be evaluated based on the following criteria:

- Meeting the specified performance specifications.
- Thoroughness and accuracy of the amplifier design and analysis.
- Ability to optimize the design effectively while considering trade-offs.
- Quality of simulation results and alignment with theoretical predictions.
- Clarity, organization, and completeness of the final project report.

Bonus:

- Add an output buffer stage to be able to drive $R_L = 100\Omega$

Best of Luck!

Design Project	CND 101 Introduction to Analog Design	Project #7

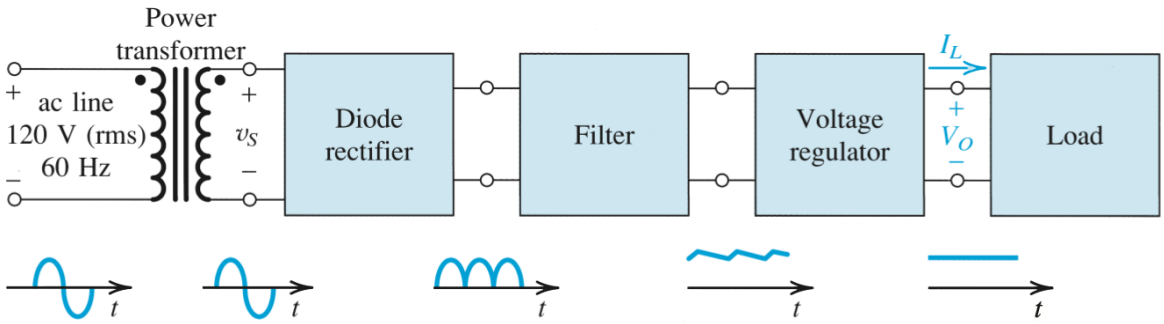
NOTE: the project is in two parts, and both parts need to be done

Part1 Title: DC Power Supply Design

Supervisor Dr. Moataz – Dr. Abdullah

Design and Simulate a DC power supply to include all stages: a full wave rectifier (using a bridge rectifier) and Zener diode if needed. The desired output of the DC power supply is 5V and the load can be up to 25mA. The power supply is fed from a 120-V (rms) 60-Hz AC line. The ripple voltage should be less than 20mV at the output at all conditions of the load.

Note: in Cadence, use the "xfmr" in analogLib to model the transformer. Use the Diode and Zener models provided in the lab.



Part2 Title: Designing a Common Emitter Amplifier

The CE amplifier circuit shown below is biased with a constant-current source *I*. It is required to design the circuit (i.e., find values for *I*, *RB*, and *RC*) to meet the following specifications:

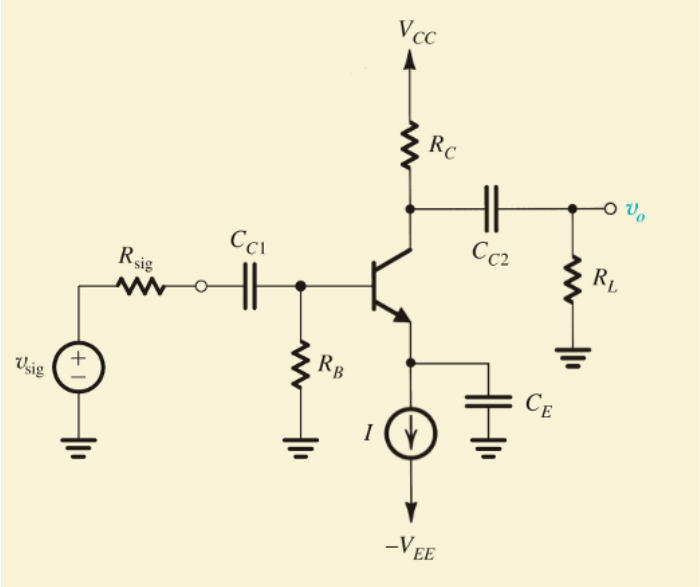
(a) *R*in ≃ 10 Kohm.
(b) The dc voltage drop across *RB* is approximately 0.2 V.

(c) The open-circuit voltage gain from base to collector is the maximum possible, consistent with the requirement that the collector voltage never fall by more than approximately 0.4 V below the base voltage with the signal between base and emitter being as high as 5 mV.

Assume that vsig is a sinusoidal source, the available supply *VCC* = 5 V, and the transistor has β = 9. Use standard resistance values from the table below.

1) Find the *I*, *RB*, and *RC* to achieve the above design specifications.
2) What base-to-collector open-circuit voltage gain does your design provide? (i.e. when CC1 and CC2 are open circuit)
3) If *R*sig = 20 Kohm, RL = 200 Kohm, what is the overall voltage gain (from vsig to vo) ?

4) Find values of the coupling capacitors (Cc1, Cc2, CE) that would make the cut-off frequency of the low frequency band (FL) less than or equal 1KHz
5) Simulate the amplifier and find its frequency response. What is the high frequency band cut-off (FH)?
6) Simulate the transient response of the amplifier to a 5mV Sinusoid input with a 100KHz frequency. Find the magnitude and frequency of the output waveform. How are they related to the input magnitude and frequency?
7) If the input magnitude is 5mV, use the frequency response from part (5) to find which signal frequency will have an output magnitude of 5mV. Simulate the transient response at this frequency (plot Vo).



Standard Resistor Values

	1% Resistor Values (kΩ)			
5% Resistor Values (kΩ)	100–174	178–309	316–549	562–976
10	100	178	316	562
11	102	182	324	576
12	105	187	332	590
13	107	191	340	604
15	110	196	348	619
16	113	200	357	634
18	115	205	365	649
20	118	210	374	665
22	121	215	383	681
24	124	221	392	698
27	127	226	402	715
30	130	232	412	732
33	133	237	422	750
36	137	243	432	768
39	140	249	442	787
43	143	255	453	806
47	147	261	464	825
51	150	267	475	845
56	154	274	487	866
62	158	280	499	887
68	162	287	511	909
75	165	294	523	931
82	169	301	536	953
91	174	309	549	976

The following need to be delivered:

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Best of Luck!