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## *Final project (project #2) Buck and Boost DC-DC Converter*

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## Problem definition

A Buck-Boost DC-DC converter is a type of power converter that can step up (boost) or step down (buck) an input voltage to provide a stable output voltage. This versatility makes it useful in various applications where the input voltage may vary, and a constant output voltage is required. Let's break down the terms:

### Buck Converter

In a buck converter, the output voltage is lower than the input voltage. It operates by turning the input voltage on and off at a high frequency using a switching element (usually a transistor) to control the energy flow to the output. The energy is stored in an inductor during the on-state and released to the output during the off-state.

### Boost Converter

In a boost converter, the output voltage is higher than the input voltage. Similar to the buck converter, it uses a switching element and an inductor, but the energy flow is such that the output voltage is increased. Energy is stored in the inductor during the on-state and released to the output, combined with the input voltage, during the off-state.

### Buck-Boost Converter

A buck-boost converter combines the features of both buck and boost converters. It can step down (buck) or step up (boost) the input voltage to maintain a stable output voltage. This is achieved by controlling the duty cycle of the switching element, which determines the time the energy is stored in the inductor.

## Applications of Buck-Boost Converters

- **Battery-Powered Devices:** Buck-boost converters are commonly used in battery-powered devices where the input voltage from the battery can vary as the battery discharges.
- **Photovoltaic Systems:** In solar power systems, the output voltage from solar panels can vary based on sunlight conditions. Buck-boost converters help maintain a consistent output voltage.
- **Electric Vehicles:** Buck-boost converters are employed in electric vehicles to accommodate the varying voltage levels from the battery.
- **Power Supplies:** Buck-boost converters are used in power supplies to regulate output voltage, especially when the input voltage may fluctuate.

## Buck-boost circuit design and implementation

In our implementation, we used 2 switches 2 control the circuit (we implement them using n-mos transistors), coil with value 1.17uH, capacitor with value of 100uF and load resistance of 100Ω and to control the circuit we use 2 pulse sources to on and off the n-mos transistor(our switch) and its period is 1us which means that we uses 1MHZ frequency in our designed circuit exists in circuit in figure 1.

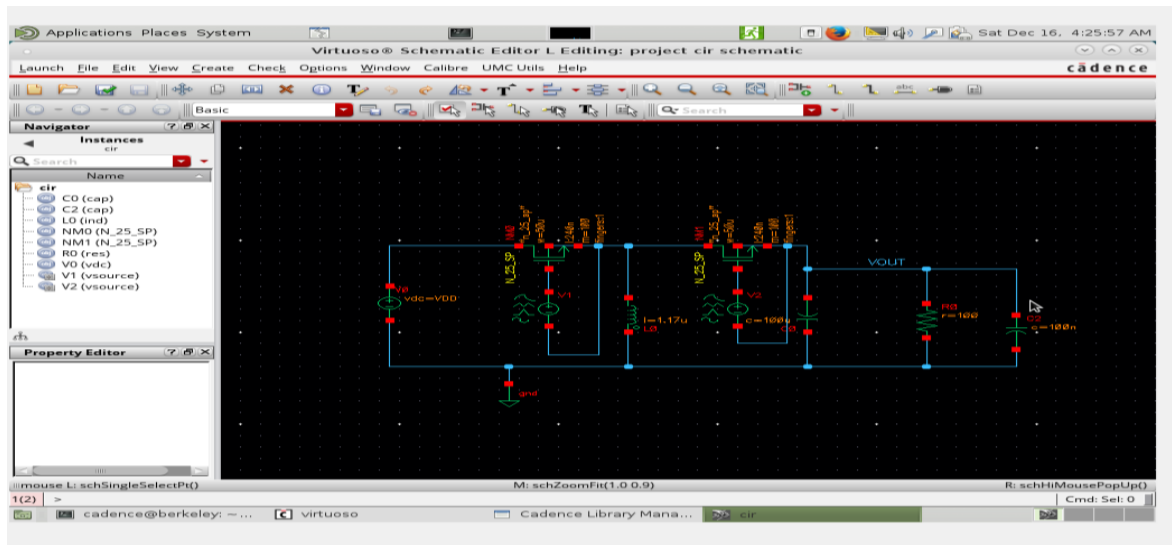


Figure 1 buck-boost DC-DC converter circuit implementation.

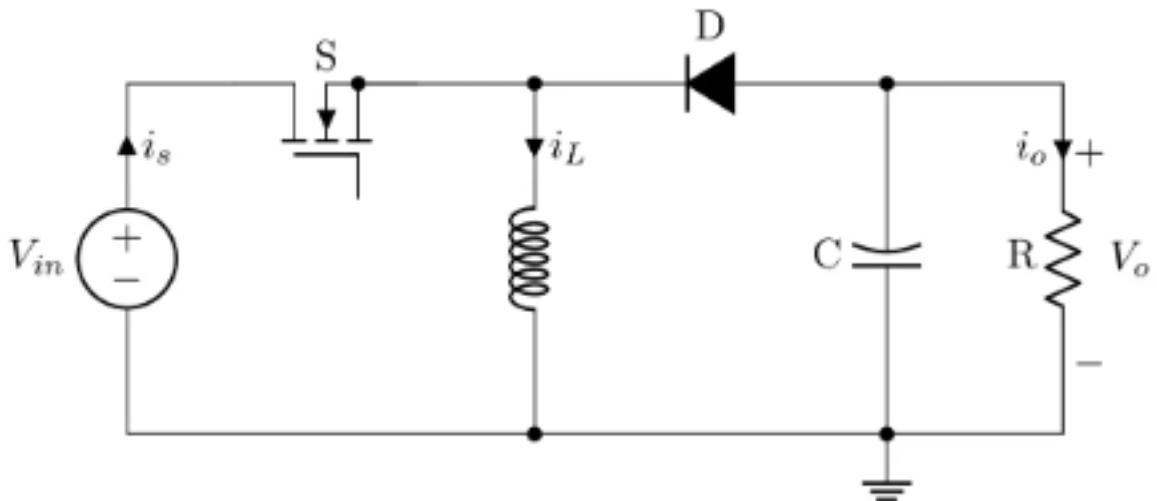


Figure 2 buck boost DC-DC converter circuit with diode.

To understand how the buck-boost converter works, let's understand this simple circuit is shown below:

The input voltage source is connected to a solid-state device. The second switch used is a diode. The diode is connected, in reverse to the direction of power flow from source to a capacitor and the load and the two are connected in parallel as shown in the figure.

## Modes of operation

Switch is ON, Diode is OFF:

The Switch is ON and therefore represents a short circuit ideally offering zero resistance to the flow of current so when the switch is ON all the current will flow through the switch and the inductor and back to the DC input source.

The inductor stores charge during the time the switch is ON and when the solid-state switch is OFF the polarity of the Inductor reverses so that current flows through the load and through the diode and back to the inductor. So, the direction of current through the inductor remains the same.

Let us say the switch is on for a time  $T_{ON}$  and is off for a time  $T_{OFF}$ . We define the time period (T), as

$$T = T_{on} + T_{off}$$

And the switching frequency

$$f = 1/t$$

Let us now define another term, the duty cycle

$$D = t_{on}/T$$

Let us analysis the Buck Boost converter in steady state operation for this mode using KVL.

$$V_{in} = V_L$$

$$V_L = L \, di/dt$$

$$di/dt = \Delta i_L / \Delta t = \Delta i_L / DT = V_{in}/L$$

Since the switch is closed for a time,

$$T_{on} = DT$$

we can say that  $\Delta t = DT$

$$(\Delta i_L)_{closed} = (V_{in}/L) * DT$$

While performing the analysis of the Buck-Boost converter we must keep in mind that:

1. The inductor current is continuous, and this is made possible by selecting an appropriate value of L.
2. The inductor current in steady state rises from a value with a positive slope to a maximum value during the ON state and then drops back down to the initial value with a negative slope. Therefore, the net change of the inductor current over any one complete cycle is zero.

switch is off, and Diode is ON.

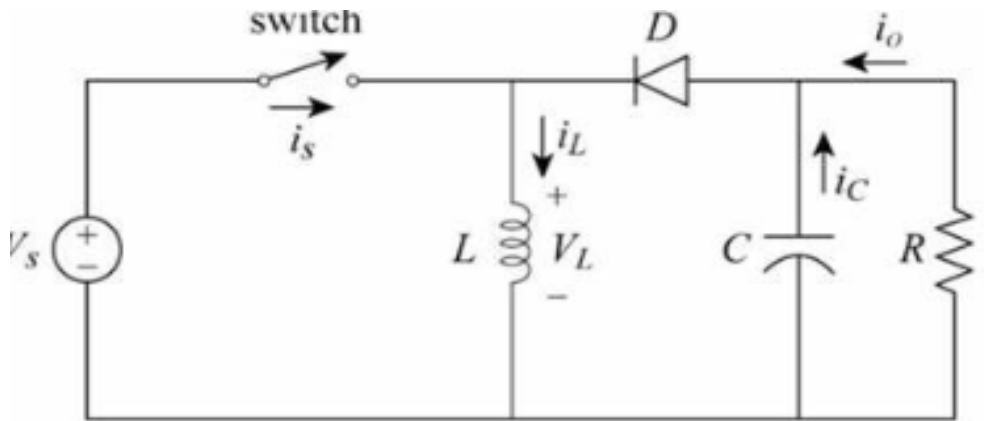


Figure 3 buck-boost circuit implementation using diode.

Since the switch is open for a time

$$T_{off} = T - T_{on} = T - DT = (1-D) T$$

we can say that

$$\Delta t = (1-D) T$$

It is already established that the net change of the inductor current over any one complete cycle is zero.

$$\frac{V_0}{V_{in}} = -\frac{D}{1-D}$$

## transient analysis of Buck-Boost converter

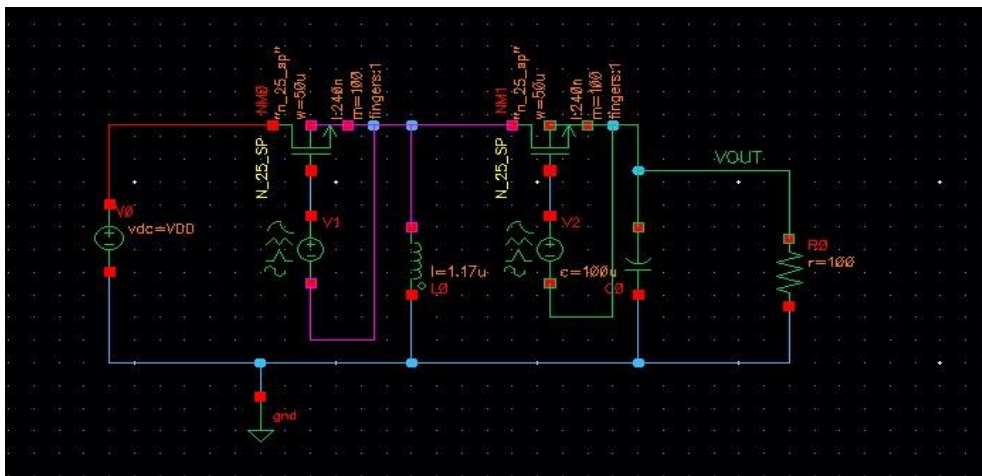


Figure 4 buck-boost circuit with 2 switches implementations (ideal switches).

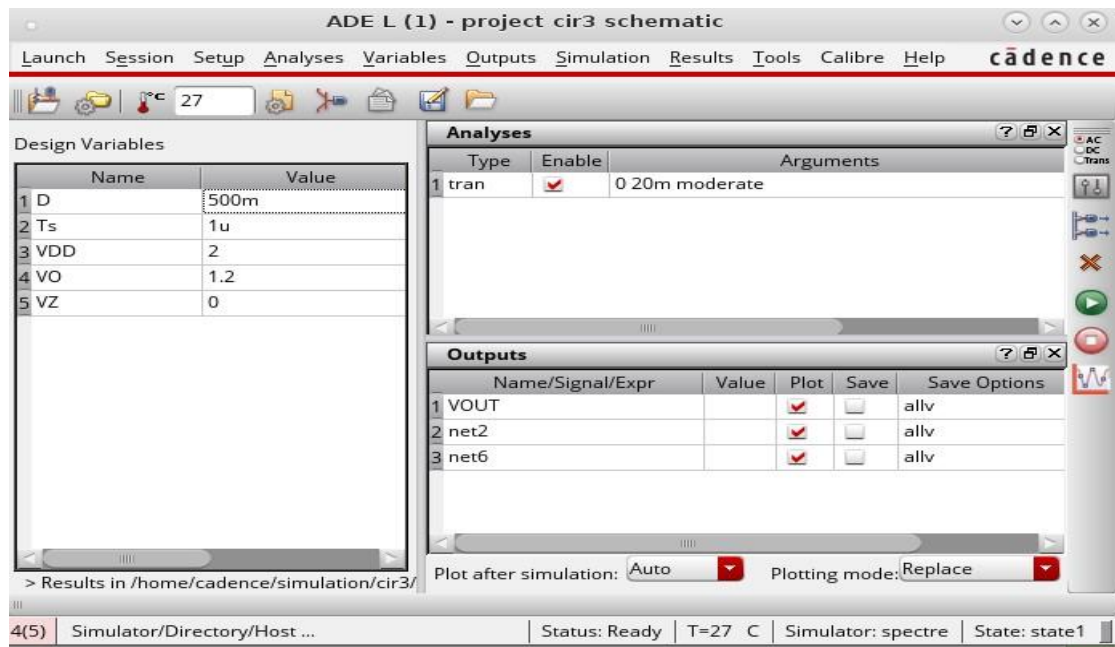


Figure 5 parameters used  $D=0.5$

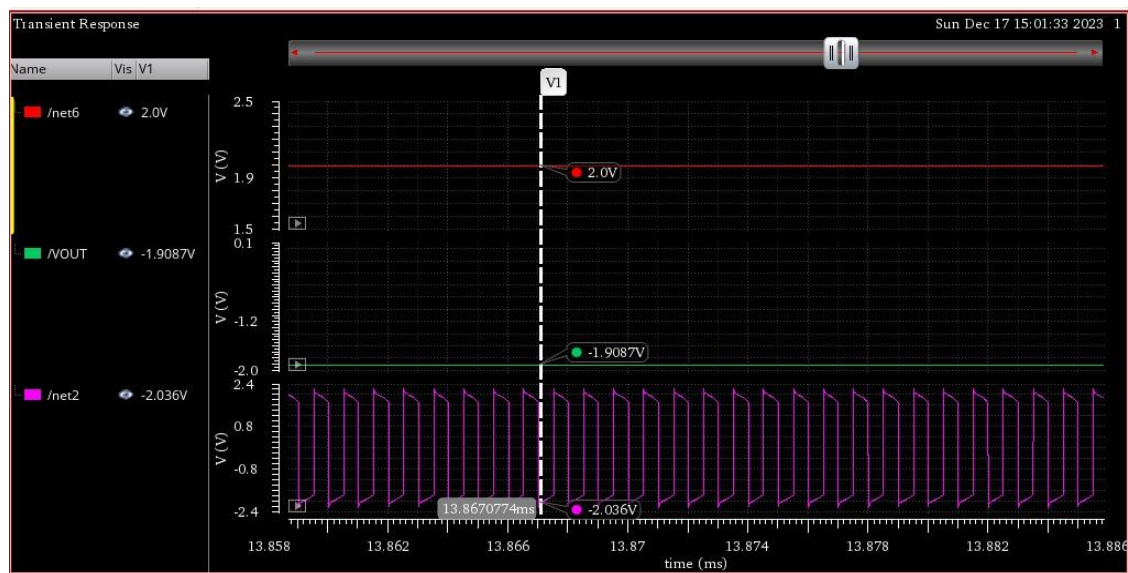


Figure 6 output from Buck-Boost converter when  $D=0.5$

# Comments

when  $D=0.5$ , output voltage will be equal to input voltage and in this case the circuit won't buck or boost the input voltage.

# Boost voltage case

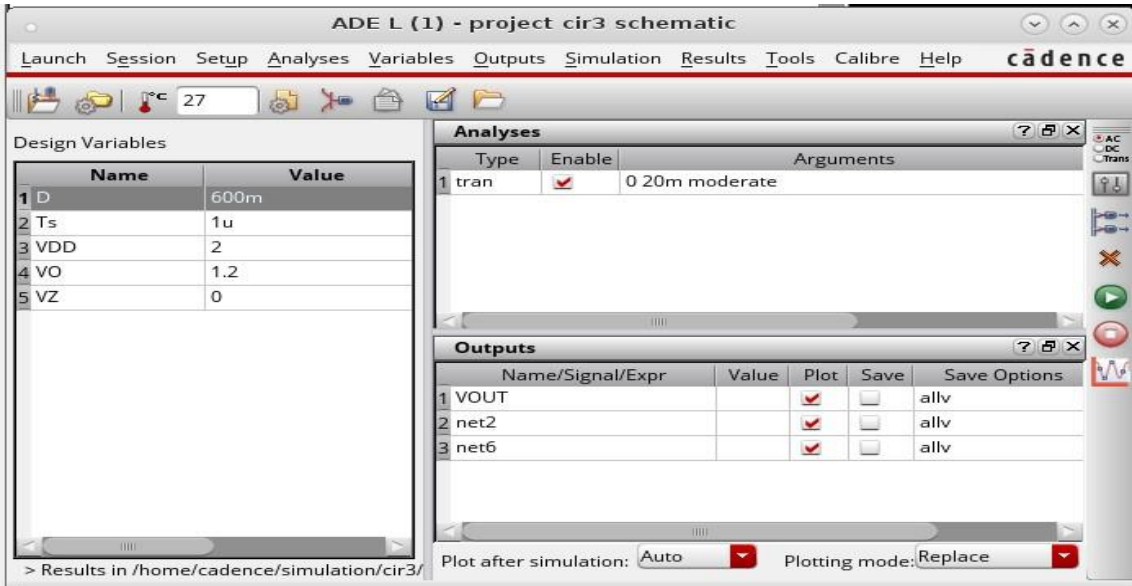


Figure 7 output from Buck-Boost converter when  $D=0.6$ .

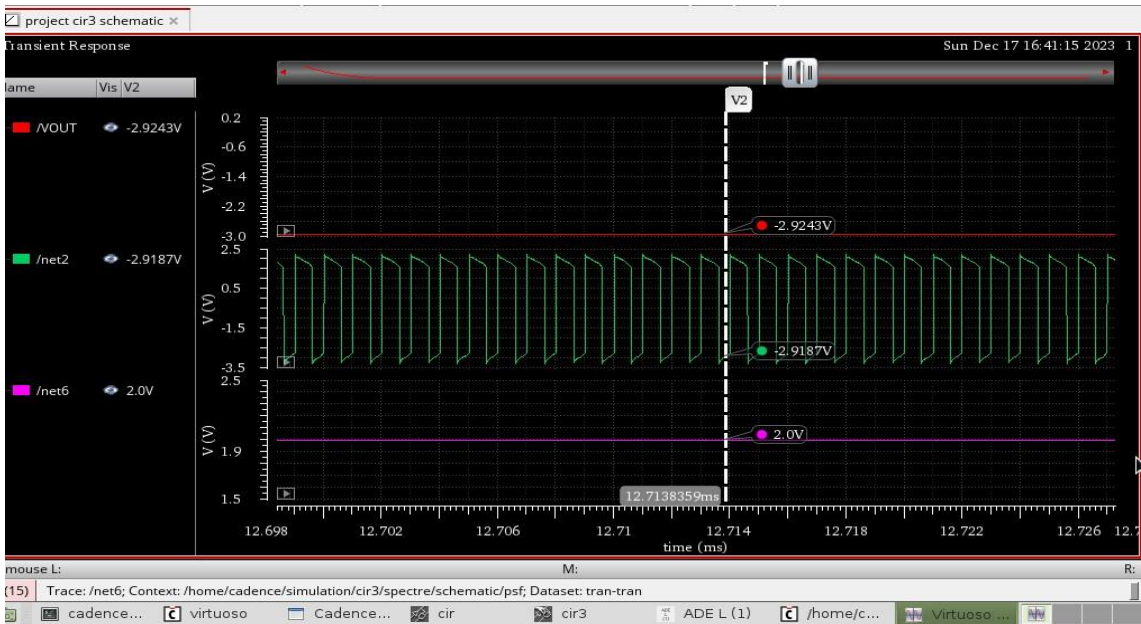


Figure 8 Boost signal case when duty cycle  $D=0.6$



## Comments

When duty cycle is more than 0.5 the circuit behaves as a boost circuit and boost the value of the input voltage according to the duty cycle value.

## Circuit efficiency

Expected  $V_{out} = -3V$

Actual  $v_{out}$  value = -2.9243

Efficiency =  $100 - 100 * \frac{3 - 2.9243}{3} = 97.48\%$  and this value of efficiency we will design it in design problems that we faced later.

## Buck voltage case

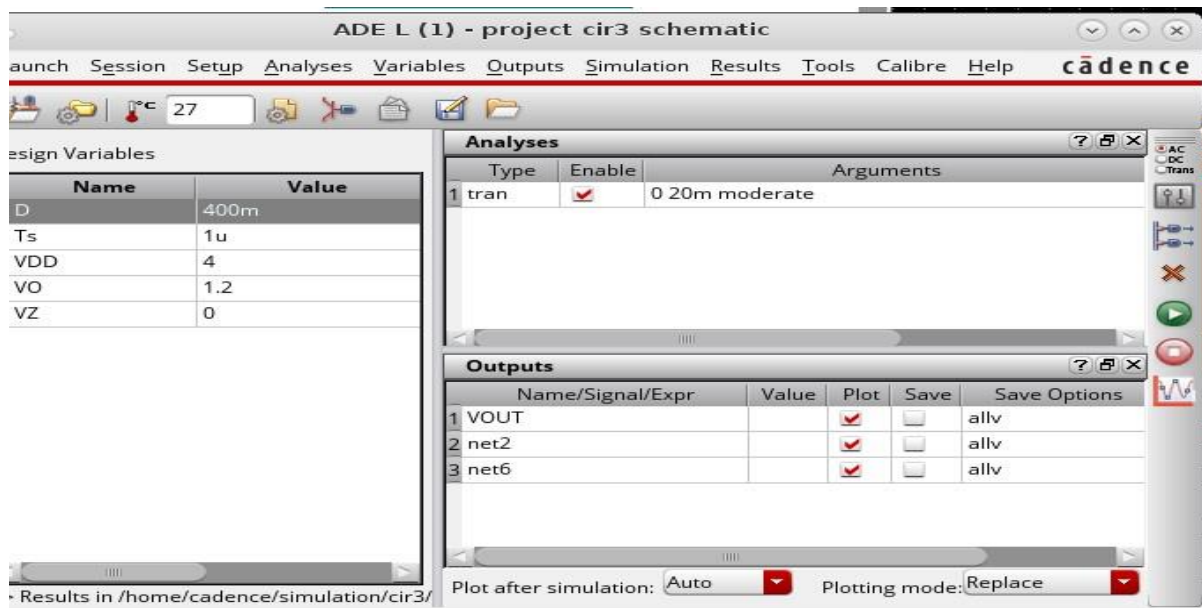


Figure 9 Buck voltage circuit parameters  $D=0.4$

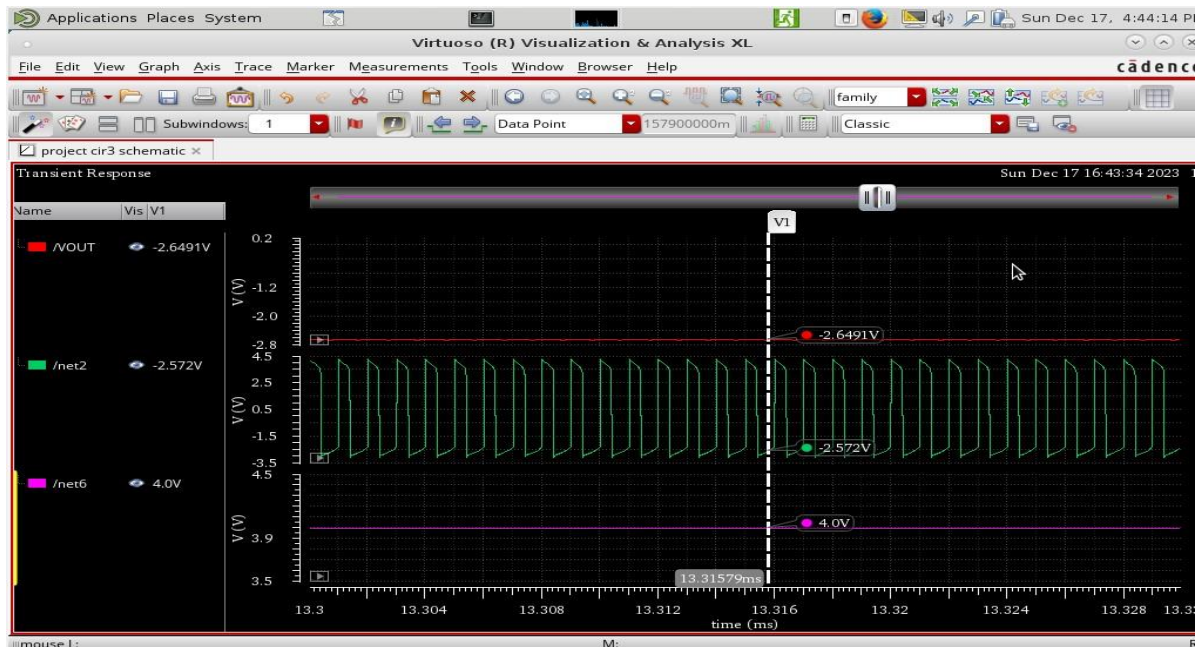


Figure 10 Buck voltage output when  $D=0.4$

## Comments

When duty cycle is less than 0.5 the circuit behaves as a buck circuit and buck the value of the input voltage according to the duty cycle value.

## Circuit efficiency

Expected  $V_{out} = -2.67V$

Actual  $v_{out}$  value  $= -2.649$

Efficiency  $= 100 - 100 * \frac{2.67 - 2.649}{2.67} = 99.2\%$  and this value of efficiency we will design it in design problems that we faced later.

## Design problems and constrains

In our design we faced a problem when we used n-mosfet as a switch in our circuit. Firstly, the output voltage value was in mv range before sizing the transistor and this happens because of the on resistance of transistor which was very high, and voltage drop in this case will be and affects the efficiency of the circuit badly. So, to overcome this problem, we increased transistor width to be 50u and the multiplier value of transistor will be 100 to get much smaller Ron for the transistor to work as an ideal switch (not ideal switch but close to it).

Property	Value	Display
Library Name	umc65sp	off
Cell Name	N_25_SP	value
View Name	symbol1	off
Instance Name	NM0	off

CDF Parameter	Value	Display
Model Name	n_25_sp	off
Multiplier	100	off
Length	240n M	off
Total Width	50u M	off
Finger Width	50u M	off
Fingers	1	off
SC ref. well edge to gate	<input checked="" type="radio"/> perpendicular <input type="radio"/> parallel	off
SC	450n M	off
Threshold	320n M	off
Apply Threshold	<input type="checkbox"/>	off
Gate Connection	<input checked="" type="radio"/> None <input type="radio"/> Top <input type="radio"/> Bottom <input type="radio"/> Both <input type="radio"/> Alternate	off
Contact Specification	S/D Metal Width	off
S/D Metal Width	90n M	off

Figure 11 transistor parameters.

Results Display Window	
Window	Expressions Info Help
cgd	-3.66532p
cgdbo	-2.20583p
cgg	7.89784p
cggbo	4.51709p
cgs	-3.89621p
cgsbo	-1.97494p
cjd	2.10352p
cjs	2.10352p
covlgb	0
covlgd	1.69038p
covlgs	1.69038p
csb	-417.652f
csd	-4.44722p
csg	-3.94817p
css	8.81304p
fug	0
gbd	103.715p
gbs	103.715p
<b>gds</b>	<b>5.1439</b>
gm	0
gmb	0
gmbs	0
gmoverid	0
ibe	13.4549e-3
ibulk	13.0562e-3
id	-6.52808e-
idb	-46.4048e-3
ide	-7.32561e-
ids	0
igb	0
igbacc	0
igbinv	0
igcd	0
igcs	0
igd	0
iqdt	0

Figure 12 gds value of transistor after modifying parameters.

As shown in figure 12, that gds value is 5.1439 which will lead to small Ron resistance as ( $R_{on}=1/gds$ ) and it will lead us to good efficiency.

Another constraint we take into consideration is that we want our output voltage to have positive polarity, so we designed CMOS inverter to be able to solve this problem.

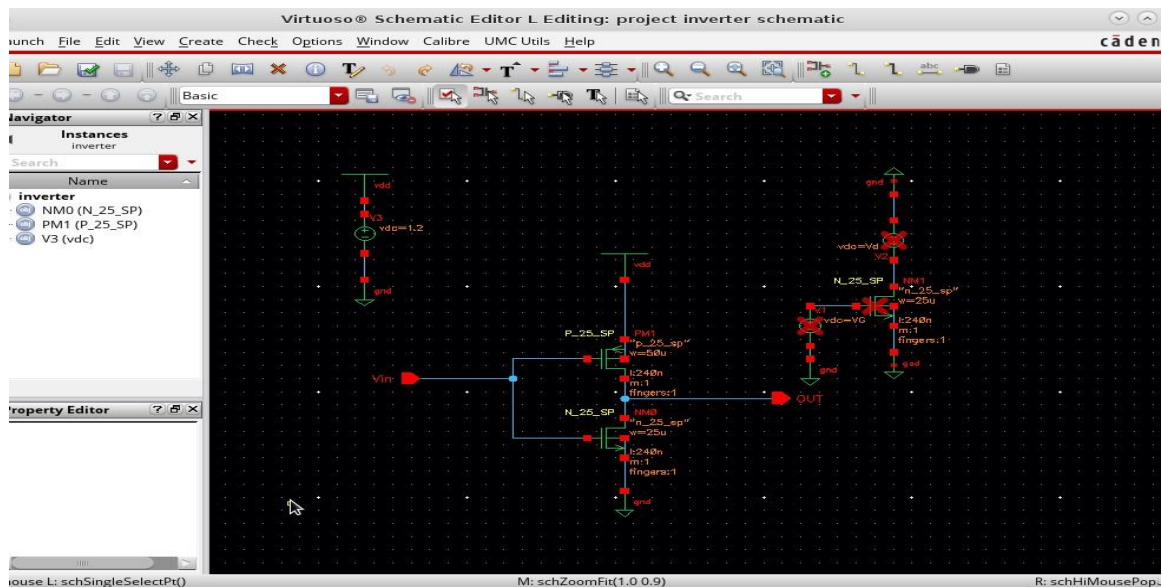


Figure 13 CMOS inverter design.



Figure 14 CMOS transient analysis output.

but the problem of CMOS inverter that it considers that any voltage value in NML will act as a zero value and vice versa and won't give us the inverted version of  $V_{in}$  so we need to use operational amplifier to be able to get the inverted version of the voltage.