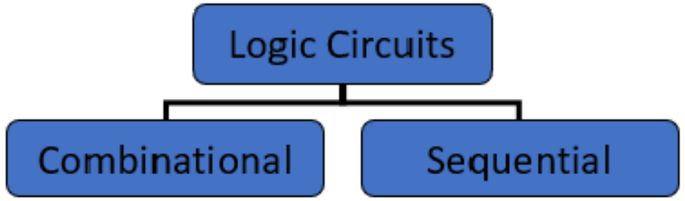


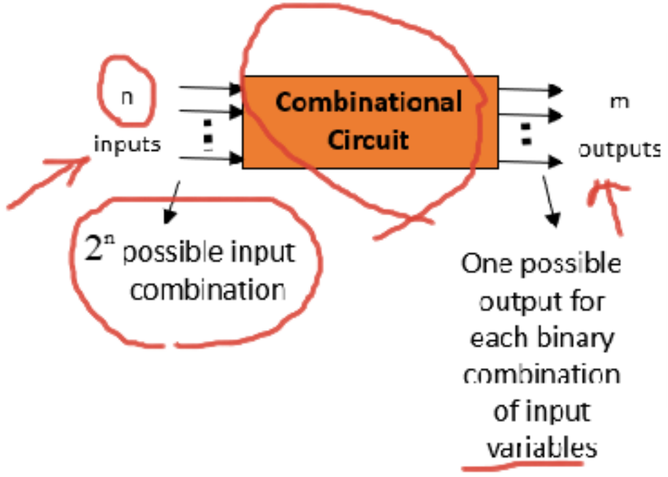
- Consists of logic gates whose outputs at any time are determined directly from the values of the present inputs.
- No feedback or storage elements are involved.

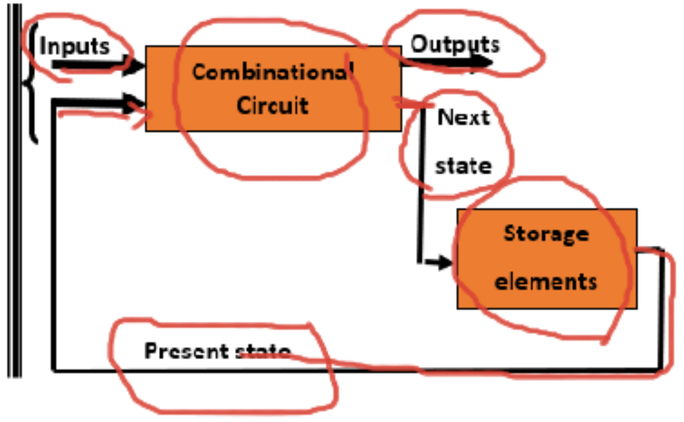
- It involves storage elements (Flip-Flops).
- Outputs are a function of inputs and the state of the storage elements, where the state of the storage elements is a function of the previous inputs.
- Circuit behavior must be specified by a time sequence of inputs and internal states.

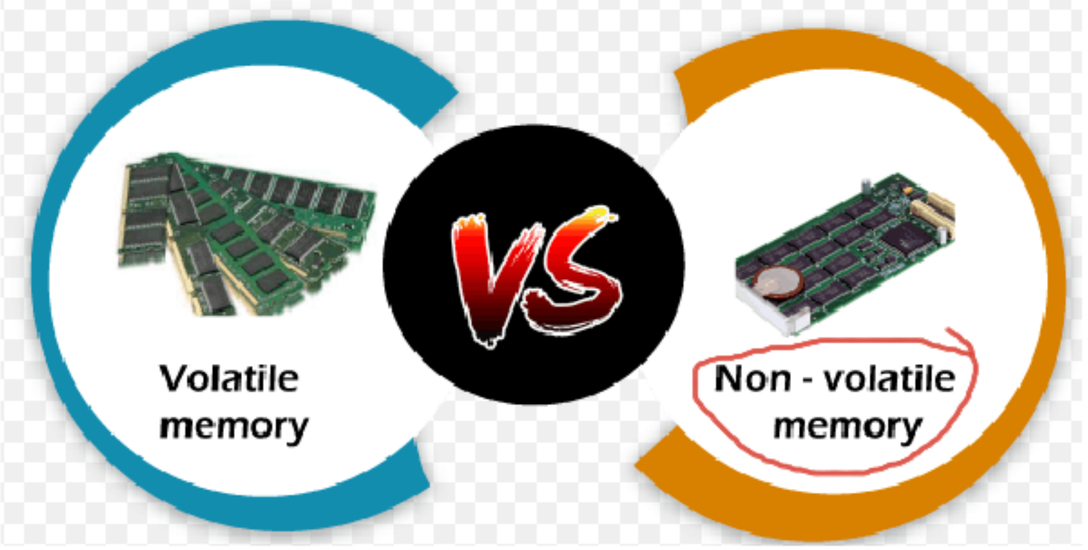
- A sequential circuit is specified by a time sequence of inputs, outputs and internal states. It contain memory and thus can remember the changes of input signals that occurred in the past.
- Inputs for the sequential circuit are functions of external inputs and the present state of the storage elements.
- Both external inputs and the present states determine the binary value of the outputs and the condition for changing the state of the storage state.

Outputs = f(external inputs , present states)

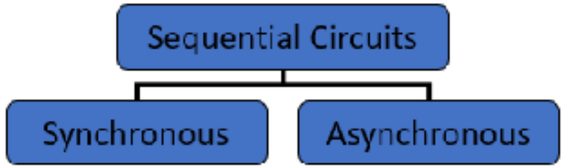
Next state = f(external inputs , present states)







Sequential Circuits

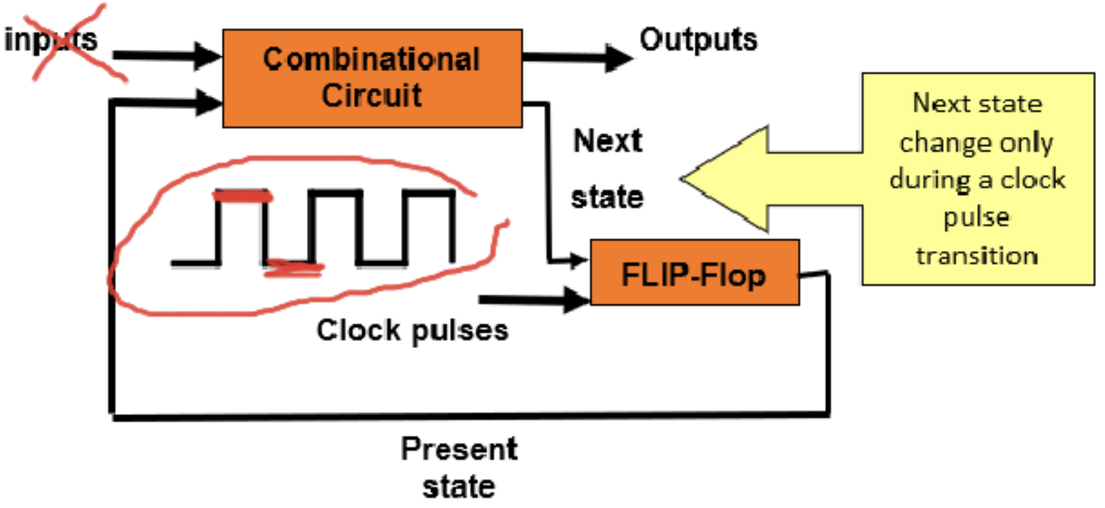


- It is a system whose behavior can be defined from the knowledge of its signals at discrete instants of time

- It is a system whose behavior depends upon the order in which the inputs change, and the state of the circuit can be affected at any instant of time

- An asynchronous sequential circuit may be regarded as a combinational circuit with feedback, thus the system may operate in an unpredictable manner and sometimes may even become unstable.
- The various problems encountered in asynchronous systems impose many difficulties on the designer, and for this reason they are seldom used.
- A synchronous sequential circuit employs signals that affect the storage elements only at discrete instant of time, as synchronization is achieved by a timing device called a "Clock Generator" that produces a periodic train of clock pulses.

- The clock pulses are distributed throughout the system in such a way that storage elements are affected only upon the arrival of each pulse, the outputs of the storage elements change only when clock pulses are present.
- The storage elements employed in clocked sequential circuits are called "Flip-Flops".
- A Flip-Flop is a binary storage device capable of storing one bit of information.
- When a clock pulse is not active, the feedback loop is broken because the Flip-Flop outputs cannot change even if the outputs of the combinational circuit change in value, thus the transition from one state to the other occurs only at predetermined time intervals dictated by the clock pulses.

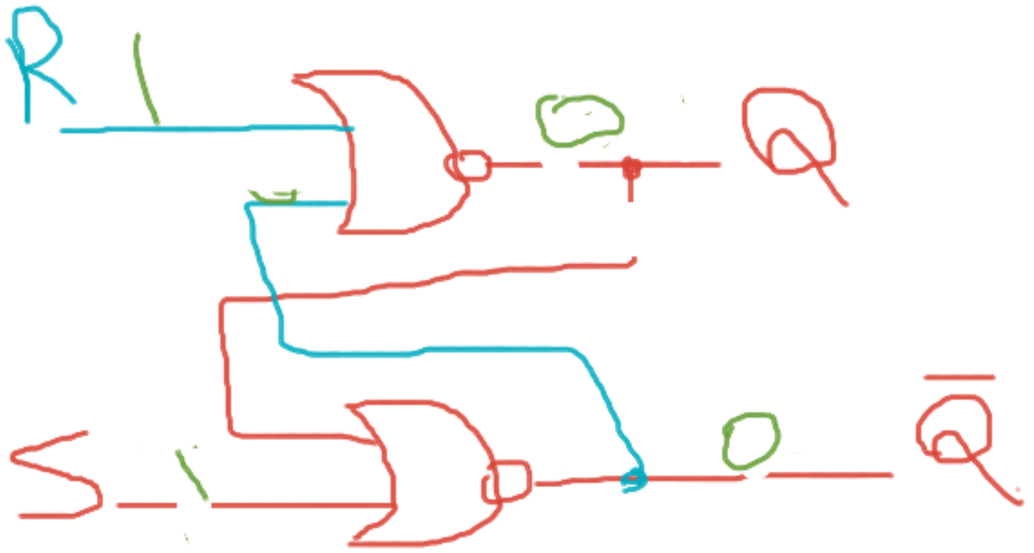


Synchronous clocked sequential circuit

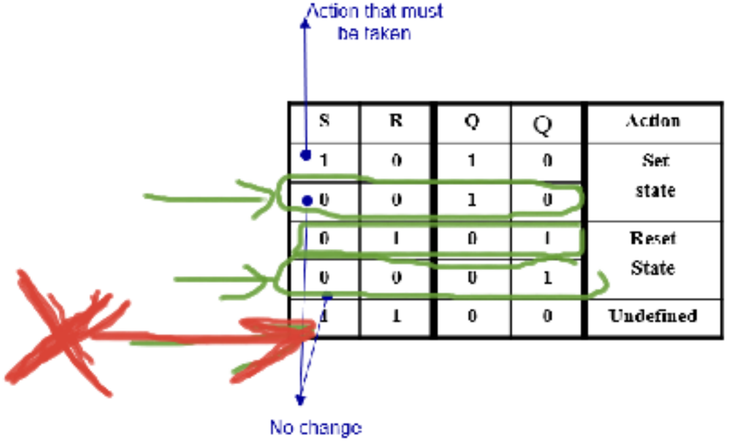
- A Flip-Flop circuit has two outputs, one for the normal value and the other for the complemented value of the bit that is stored in it.

Latches

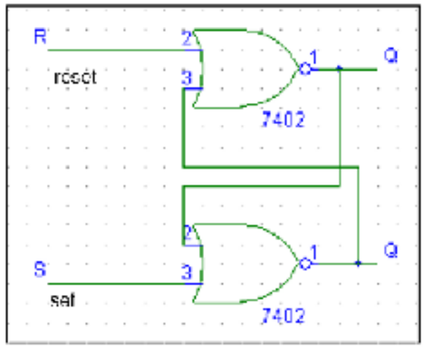
- A Flip-Flop circuit can maintain a binary state indefinitely (as long as power is delivered to the circuit), until directed by an input signal to switch states.
- Latches are the basic circuit from which all Flip-Flops are constructed.



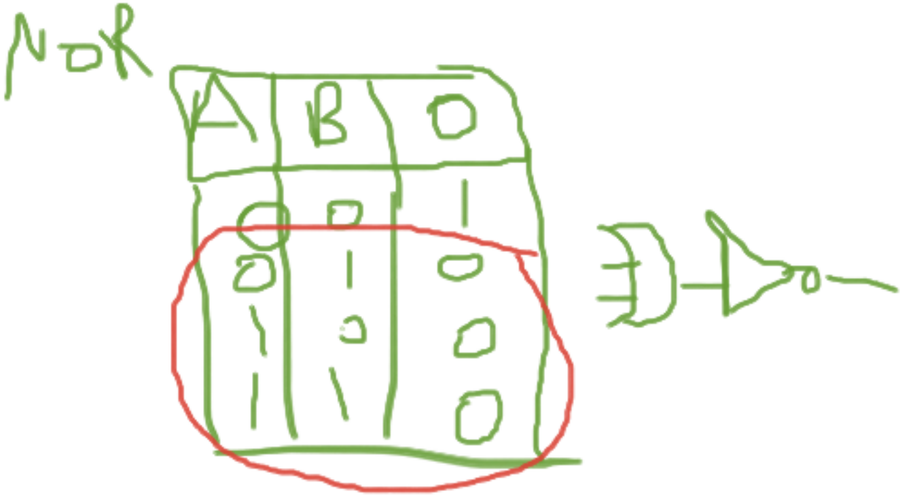
SR-Latch (NOR gates)

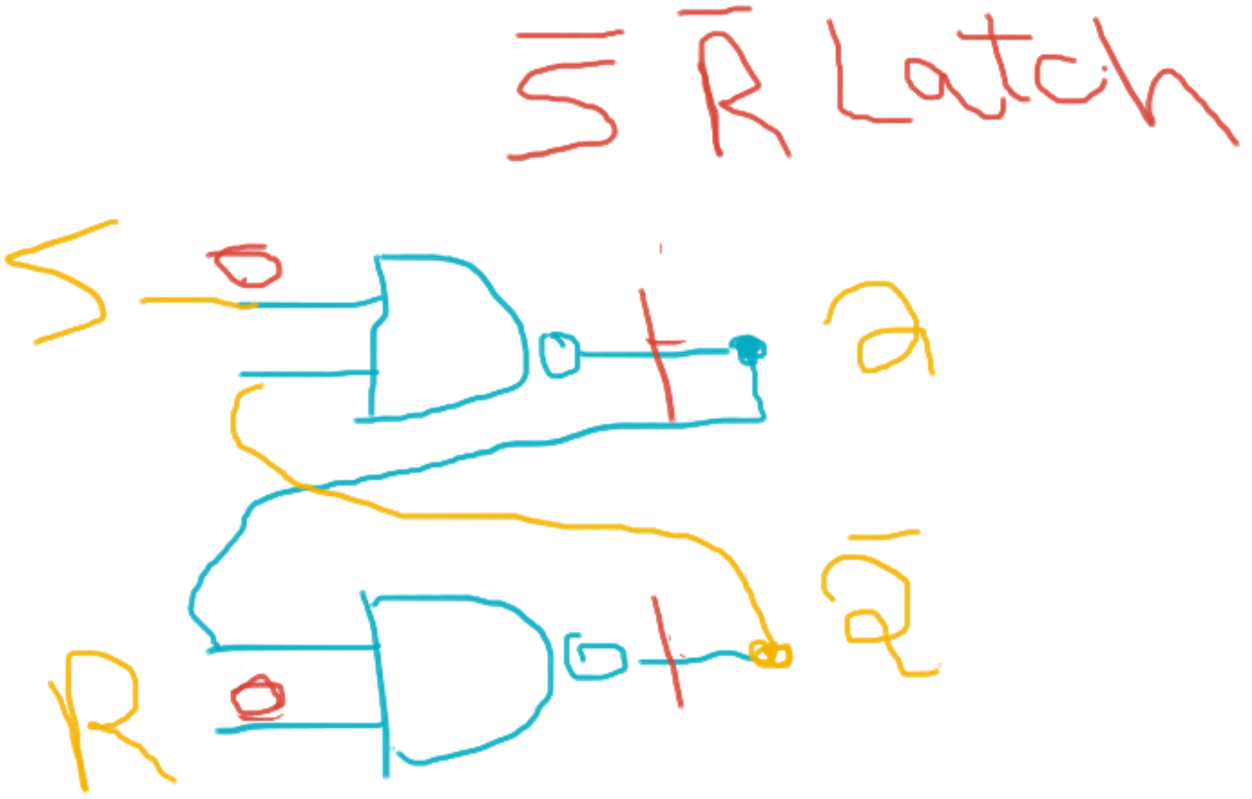


S	R	Q	Q	Action
1	0	1	0	Set state
0	0	1	0	
0	1	0	1	Reset State
0	0	0	1	
1	1	0	0	Undefined

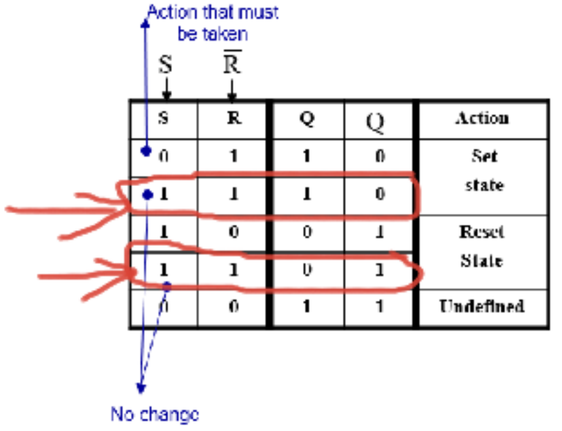


SR-Latch with NOR gates

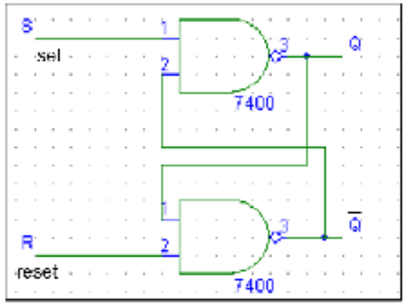




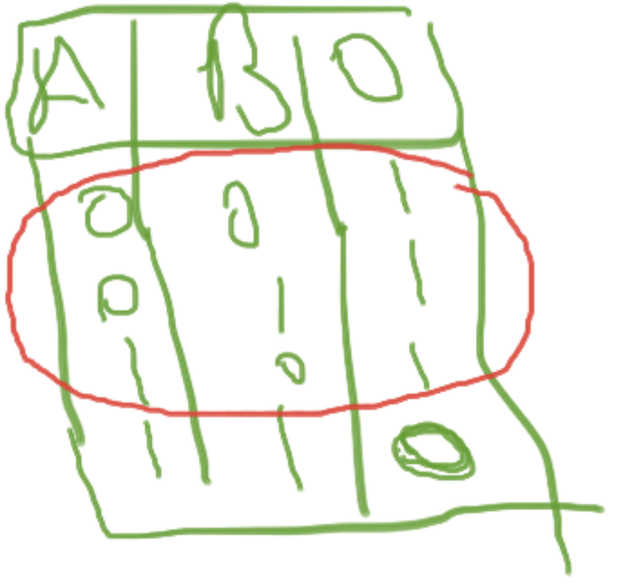
SR-Latch (NAND gates)



S	R	Q	Q	Action
0	1	1	0	Set state
1	1	1	0	
1	0	0	1	Reset State
1	1	0	1	
0	0	1	1	Undefined



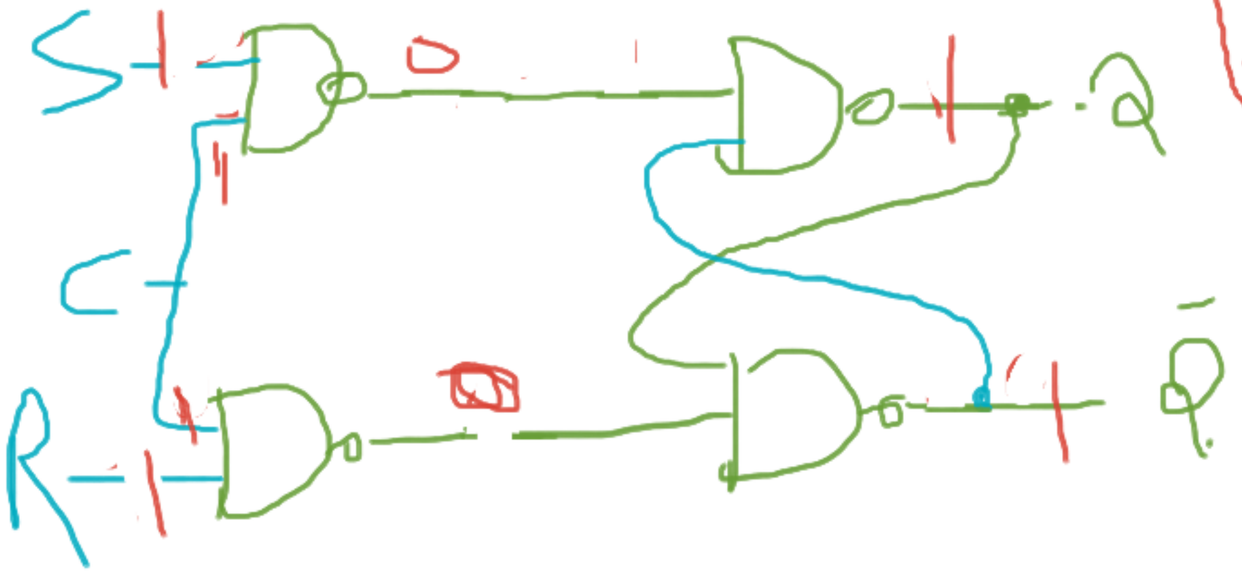
SR-Latch with NAND gates



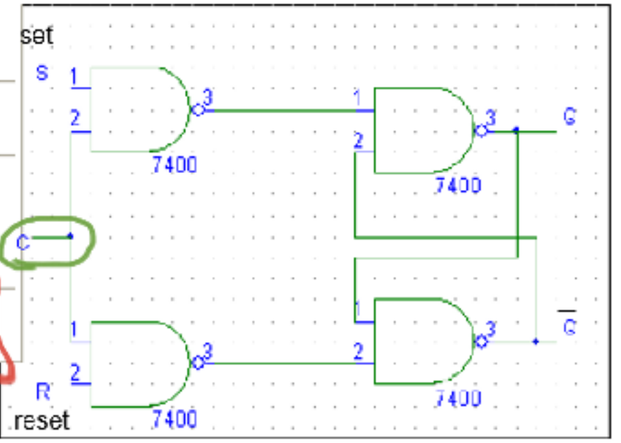
- Notice that, the S input in the SR NOR-Latch must go back to "0" before any other changes can occur.
- There are two input conditions that cause the circuit to be in the SET state, the first is the action that must be taken by input S to bring the circuit to the SET state, the second is the removing of the active input from S leaving the circuit in the same state.
- When S=R=1 (NOR-gate latch), both outputs go to "0", this produces an undefined state and it also violates the requirement that output Q and $\overline{Q}$ be the complement of each other.

- Comparing the SR NAND-Latch and the SR NOR-Latch, we note that the input signals for the NAND required the complement values of those used for the NOR-Latch.
- Because the NAND-Latch require a "0" signal to change its state, it is sometimes referred to as an $\overline{S}$-$\overline{R}$ Latch, the bar above the letters designates the fact that the inputs must be in their complement form to activate the circuit.

SR-Latch (NAND gates)



C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	Q=0 : reset state
1	1	0	Q=1 : set state
1	1	1	undetermined

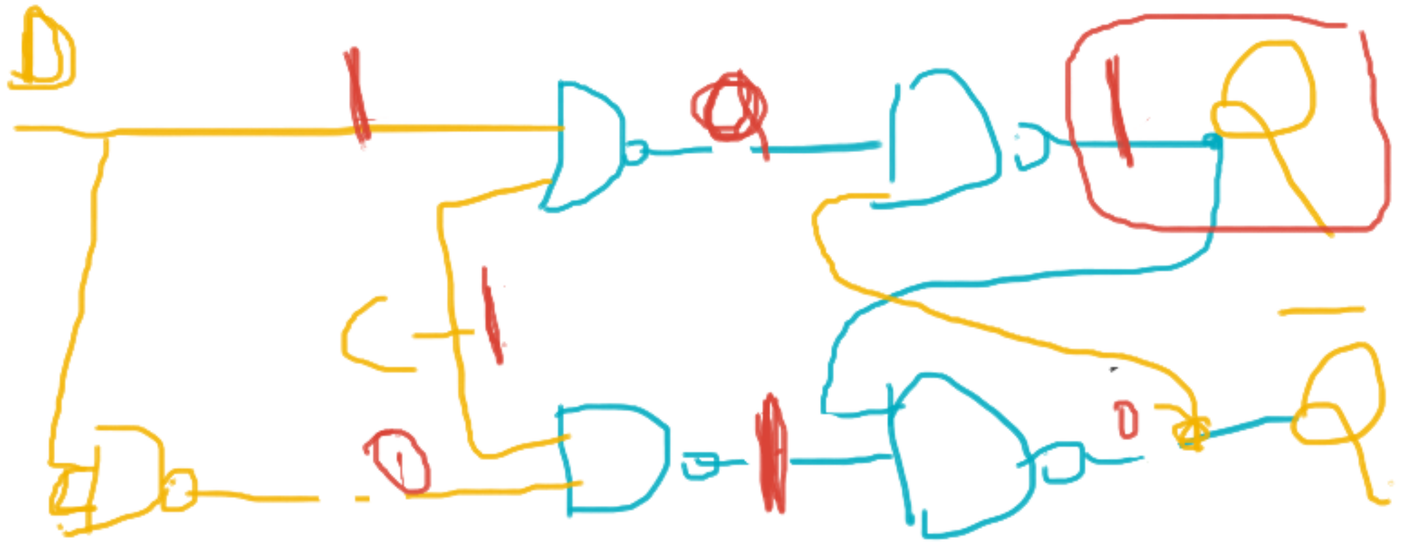


SR-Latch with NAND gates

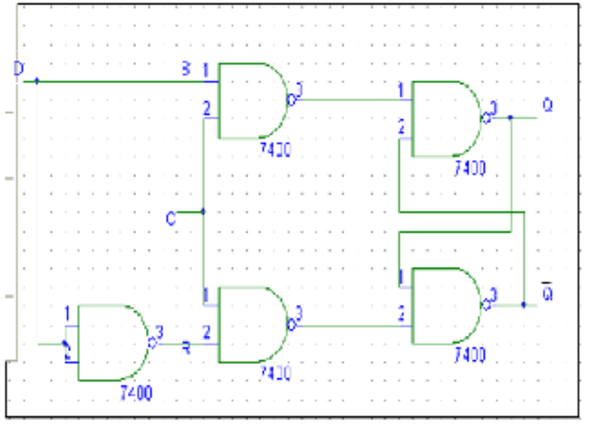
and a control input

- An additional control input which determines when the state of the latch can be changed is added to the basic SR-Latch to improve its operation
- The control input C acts as an enable signal for the other two inputs.

D-Latch

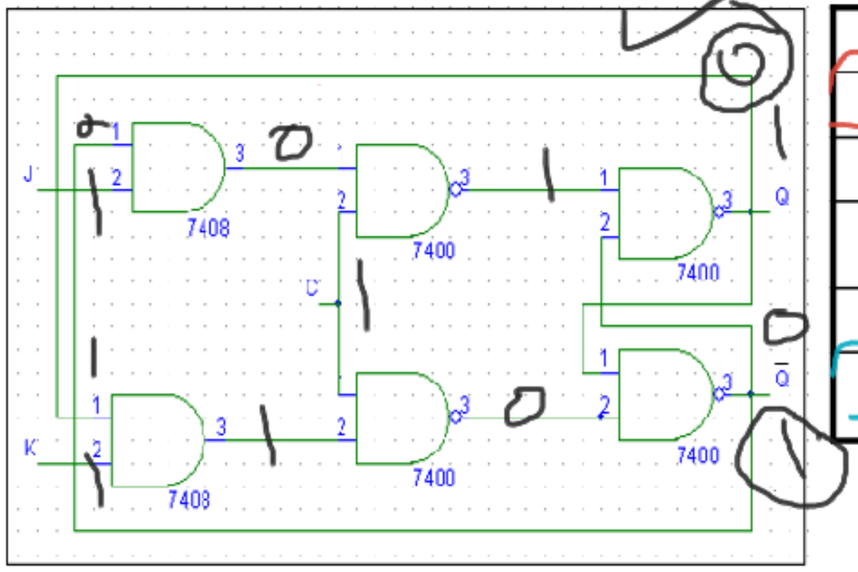


C	D	Next state of Q
0	X	No change
1	0	Q=0: reset state
1	1	Q=1: set state



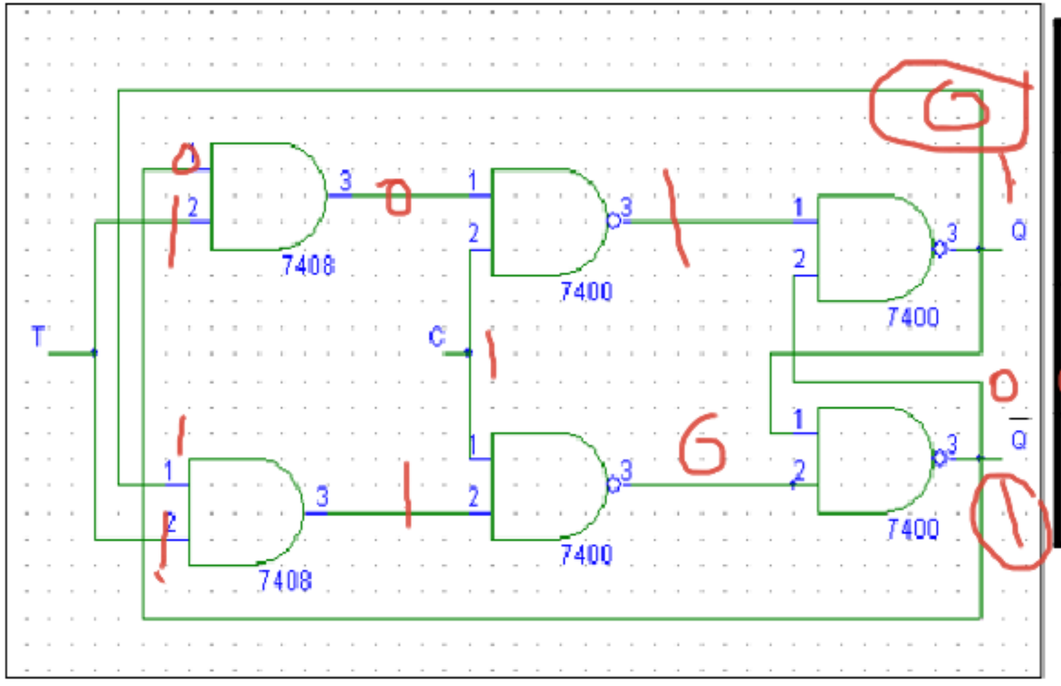
- One way to eliminate the undesirable condition of the indeterminate state in the SR-Latch is to insure that inputs S & R are never equal to 1 at the same time.
- As long as the control input is at “0”, the cross-coupled SR latch has both inputs at the 1 level and the circuit can not change regardless of the value of D.

JK Flip-Flop



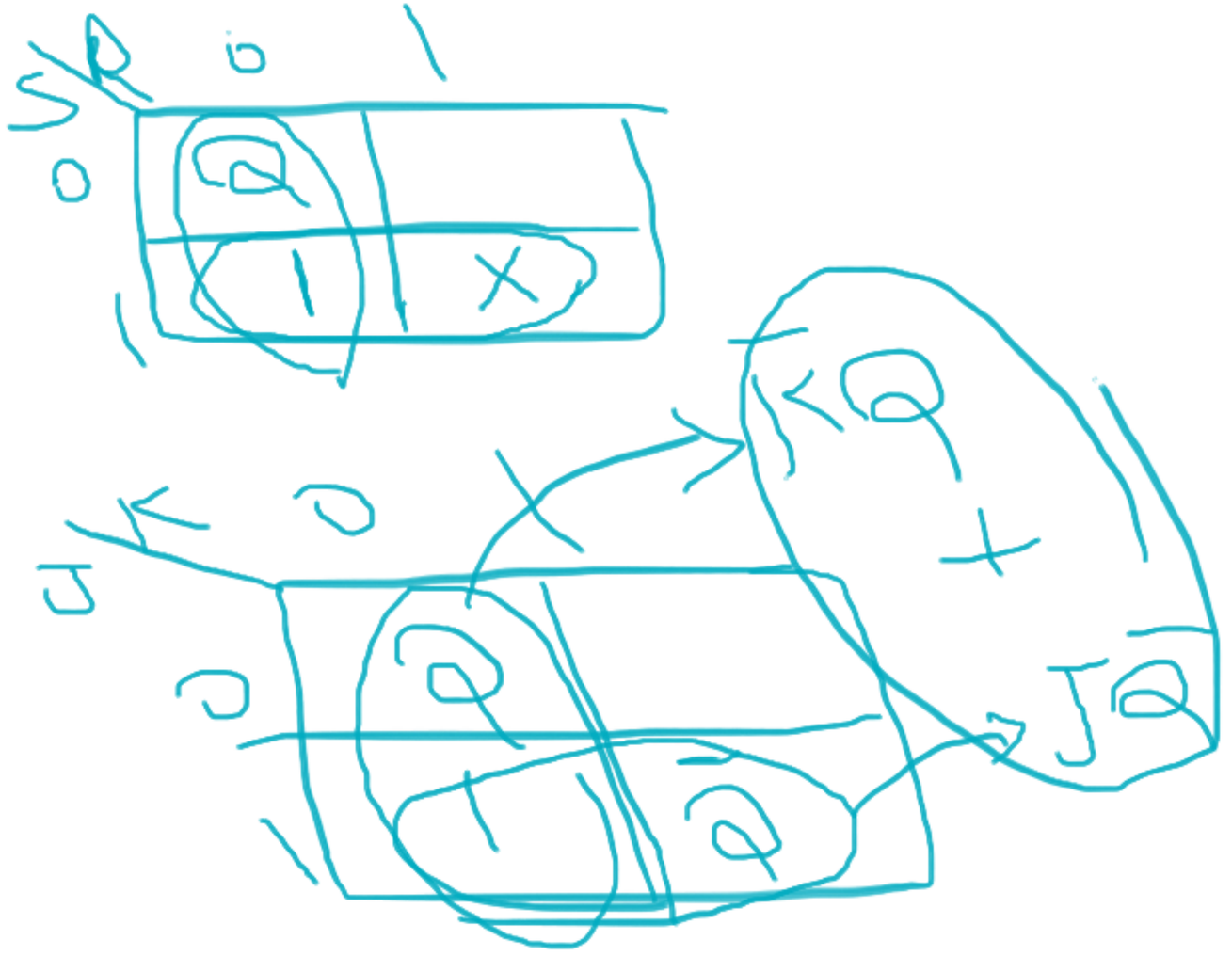
C	J	K	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	Q=0 : reset state
1	1	0	Q=1 : set state
1	1	1	Complement (toggle)

T Flip-Flop



C	T	Next state of Q
0	X	No change
1	0	No change
1	1	complement

Flip-Flops Characteristic Tables & Equations



SR Flip-Flop			
S	R	Q(t+1)	Operation
0	0	Q(t)	No change
0	1	0	Reset
1	0	1	Set
1	1	N/A	Indeterminate

$$Q(t+1) = S + \overline{R}Q, \qquad SR = 0$$

JK Flip-Flop			
J	K	Q(t+1)	Operation
0	0	Q(t)	No change
0	1	0	Reset
1	0	1	Set
1	1	$\overline{Q(t)}$	Complement

$$Q(t+1) = J\overline{Q} + \overline{K}Q$$

D Flip-Flop		
D	Q(t+1)	Operation
0	0	Reset
1	1	Set

$$Q(t+1) = D$$

T Flip-Flop		
T	Q(t+1)	Operation
0	Q(t)	No change
1	$\overline{Q(t)}$	Complement

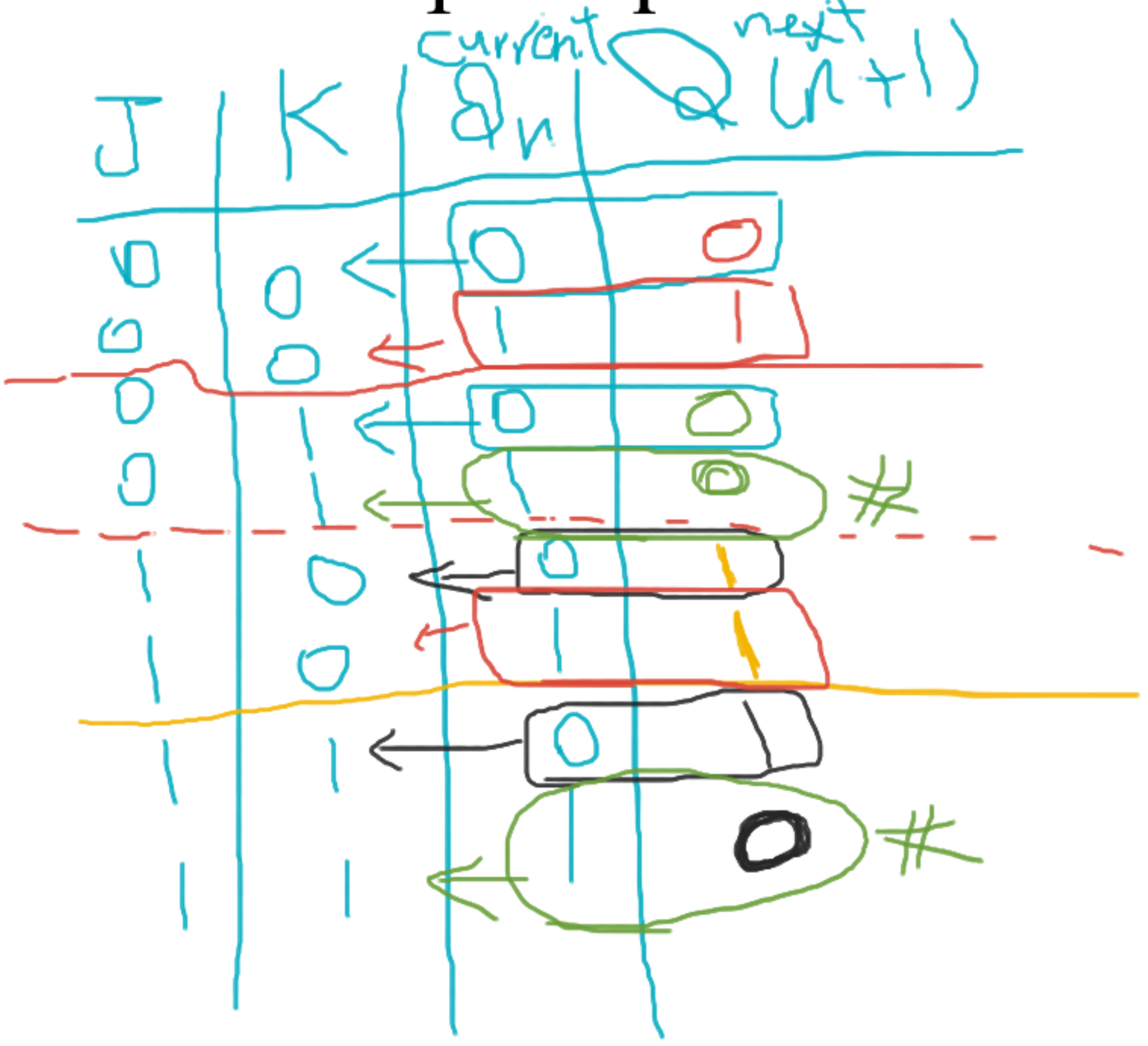
$$Q(t+1) = T\overline{Q} + \overline{T}Q$$

Analysis Procedure

- Obtain the binary values of each Flip-Flop input equation in terms of the present state and input variables
- Use the corresponding Flip-Flop characteristic table to determine the next state.

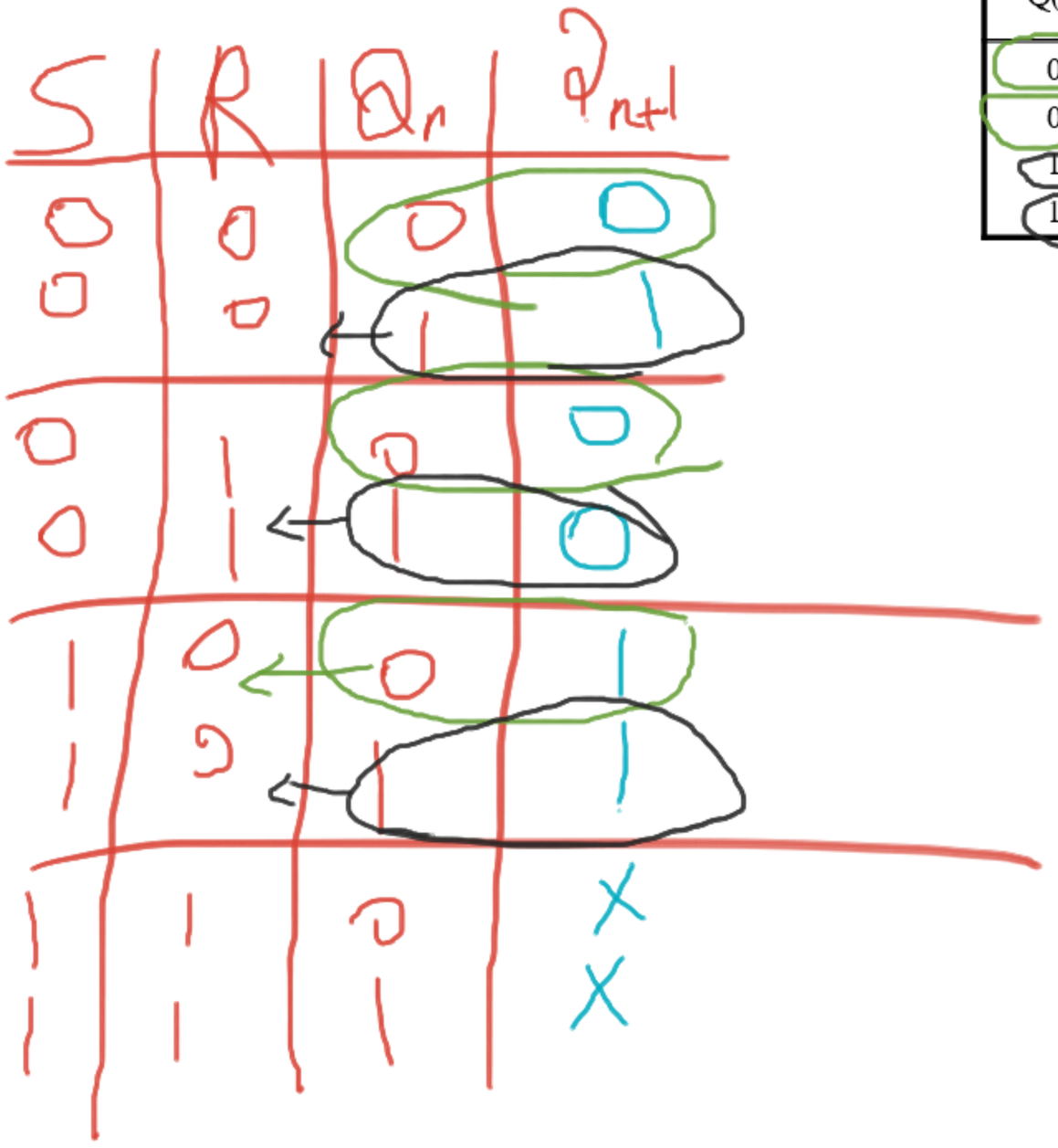
- The characteristic tables are a shorter version of the truth table, it gives for every set of input values and the state of the Flip-Flop before the rising-end (edge) the corresponding state of the Flip-Flop after the rising edge of the clock signal.
- By using K-map we can derive the characteristic equation for each Flip-Flop

Flip-Flop Excitation Tables



JK Flip-Flop			
J	K	Q(t+1)	Operation
0	0	Q(t)	No change
0	1	0	Reset
1	0	1	Set
1	1	Q(t)	Complement

JK Flip-Flop Excitation Table			
Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

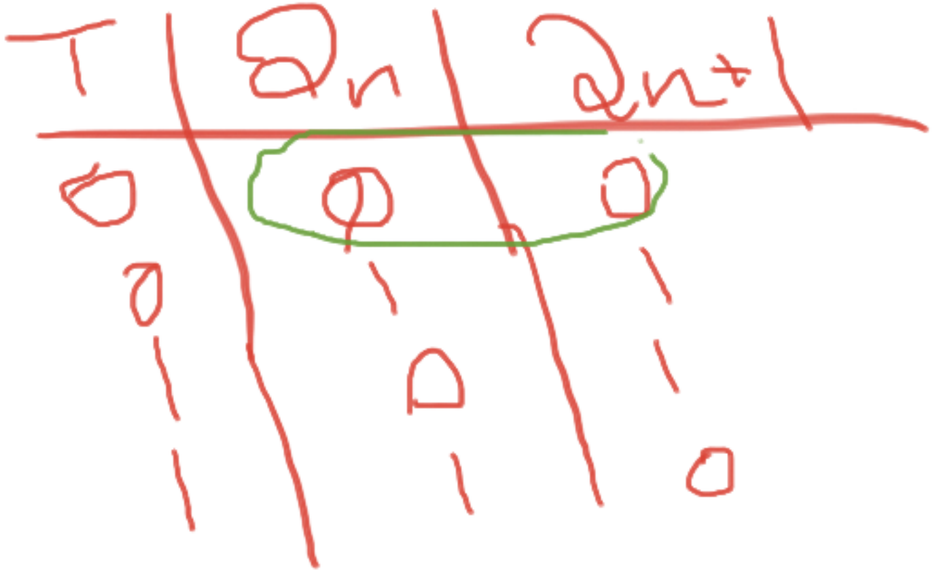


SR Flip-Flop Excitation Table			
Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

SR Flip-Flop			
S	R	Q(t+1)	Operation
0	0	Q(t)	No change
0	1	0	Reset
1	0	1	Set
1	1	N/A	Indeterminate

D Flip-Flop		
D	Q(t+1)	Operation
0	0	Reset
1	1	Set

D Flip-Flop Excitation Table		
Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1



T Flip-Flop Excitation Table		
Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

T Flip-Flop		
T	Q(t+1)	Operation
0	Q(t)	No change
1	$\overline{Q(t)}$	Complement

- The excitation for each Flip-Flop, is used during the analysis of sequential circuits. It is derived from the characteristic table by transposing input and output columns.
- It gives the value of the Flip-Flop's inputs that are necessary to change the Flip-Flop's present state to the desired next state after the rising edge of the clock signal.

Charactestic Table

D Flip-Flop		
D	Q(t+1)	Operation
0	0	Reset
1	1	Set

$$Q(t+1) = D$$

Current State A	Current State B	Input I	Flip Flop Inputs D_A	Flip Flop Inputs D_B	Next State Anext	Next State Bnext
0	0	0	0	0	0	0
0	0	1	0	1	0	1
0	1	0	0	0	0	0
0	1	1	1	0	1	0
1	0	0	0	0	0	0
1	0	1	1	0	1	0
1	1	0	X	X	X	X
1	1	1	X	X	X	X

JK Flip-Flop		Excitation Table	
Q(t)	Q(t-1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Current State A	Current State B	Input I	Next State Anext	Next State Bnext	Flip Flop Inputs J_A	Flip Flop Inputs K_A	Flip Flop Inputs J_B	Flip Flop Inputs K_B
0	0	0	0	0	0	X		
0	0	1	0	1	0	X		
0	1	0	0	0	0	X		
0	1	1	1	0	1	X		
1	0	0	0	0	X	1		
1	0	1	1	0	X	0		
1	1	0	X	X	X	X		
1	1	1	X	X	X	X		

State-Table

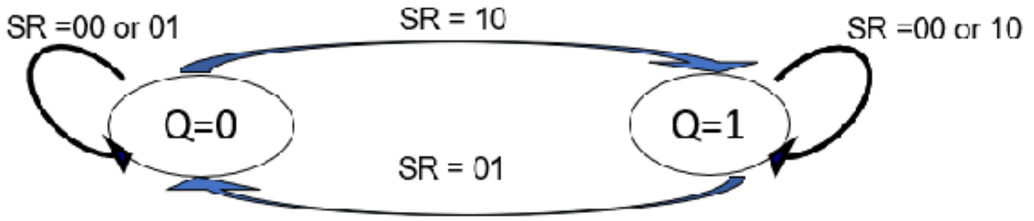
JK Flip-Flop Excitation Table			
Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Current State		Input	Next State		Outputs	Flip Flop Inputs	
A	B	I	Anext	Bnext	Y	D_A	D_B
0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	1
0	1	0	0	0	1	0	0
0	1	1	1	0	1	1	0
1	0	0	0	0	0	0	0
1	0	1	1	0	0	1	0
1	1	0	X	X	X	X	X
1	1	1	X	X	X	X	X

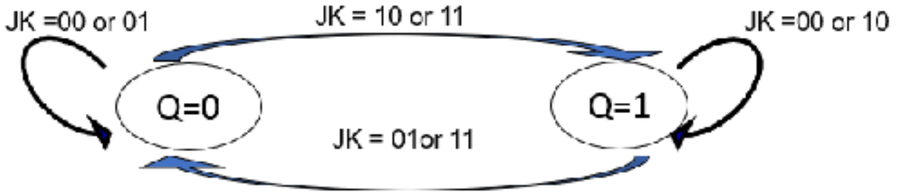
Current State		Input	Next State		Outputs	Flip Flop Inputs			
A	B	I	Anext	Bnext	Y	J_A	K_A	J_B	K_B
0	0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	0	X	1	X
0	1	0	0	0	1	0	X	X	1
0	1	1	1	0	1	1	X	X	1
1	0	0	0	0	0	X	1	0	X
1	0	1	1	0	0	X	0	0	X
1	1	0	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X

- In addition to graphical symbols, tables, or equations, Flip-Flops can also be described uniquely by means of State diagrams or State graphs, in which case each state would be represented by a circle , and a transition between state would be represented by an arrow.

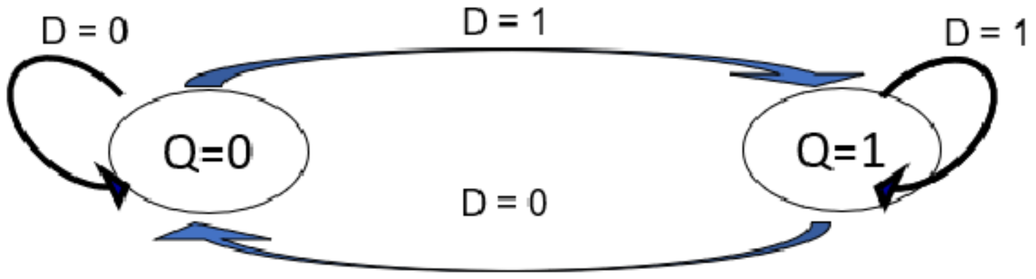
State Diagram for various Flip-Flops



SR Flip-Flop

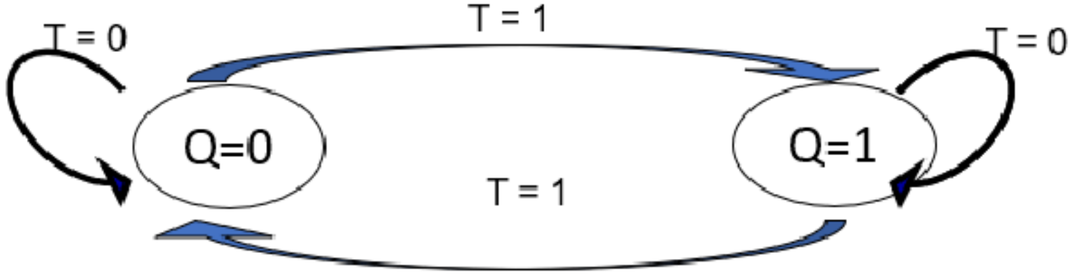


JK Flip-Flop



D Flip-Flop

- The state diagram can be obtained directly from the state table.
- The state is represented by a circle and the transition between state is indicated by a directed lines connecting the circles.
- The directed lines are labeled with two binary numbers separated by a slash, the input value during present state and the second is the output during the present state.
- Same state can represent both the source and destination of a transition.
- Each state can be thought of as a time interval between two rising edges of the clock signal.



T Flip-Flop