Revision Lab
Combinational Circuits

1) Combinational circuit 1

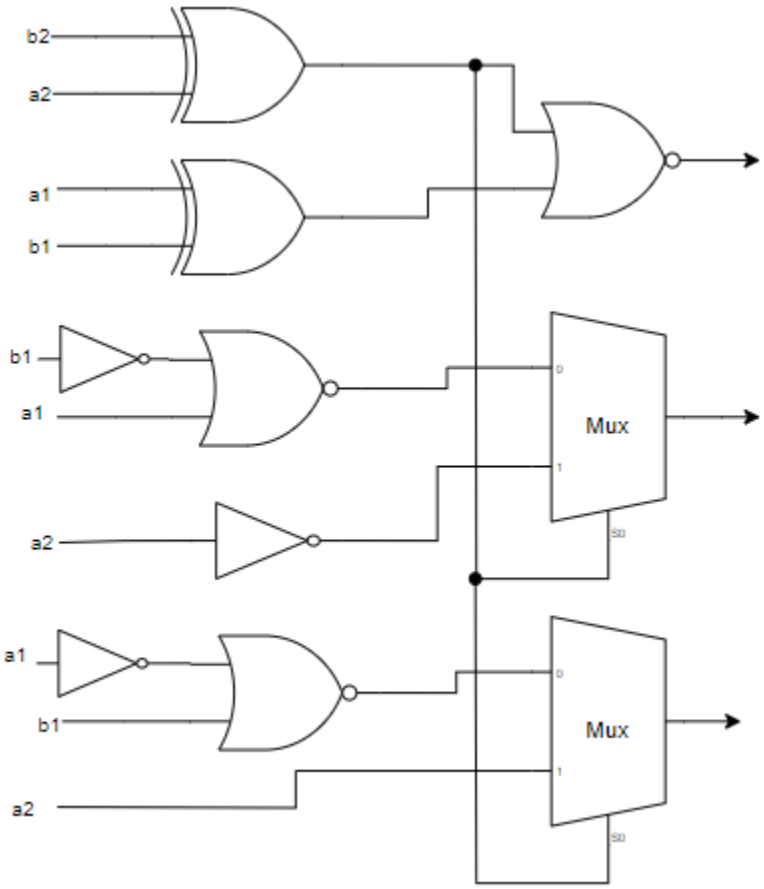

Figure 1

Requirements:

I. Write a structural Verilog model to build the circuit in figure 1.

II. From the simulation results, what is the function of this circuit?

III. From II, build a behavioral Verilog HDL model for the same function.

IV. Build a complete testbench file for this design.

2) Combinational circuit 2: Carry look-ahead adder

To reduce the delay caused by the effect of carry propagation through the ripple-carry adder, we can attempt to evaluate quickly for each stage whether the carry-in from the previous stage will have a value of 0 or 1. If a correct evaluation can be made in a relatively short time, then the performance of the complete adder will be improved.

For the carry look-ahead adder in Figure 2 the following computations are done for every bit i:

$$s_i = a_i \oplus b_i \oplus c_i$$

$$c_{i+1} = g_i + p_i \cdot c_i$$

Where:

$$g_i = a_i \cdot b_i$$

$$p_i = a_i \oplus b_i$$

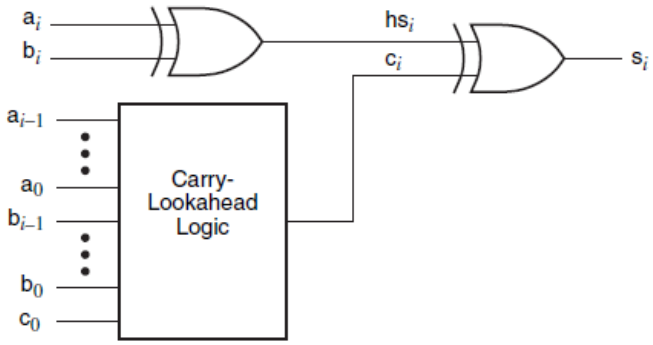

Figure 2: Carry look-ahead adder

Requirements:

I. Design a Verilog HDL model to implement the above design.

II. Simulate and test your design using a testbench.