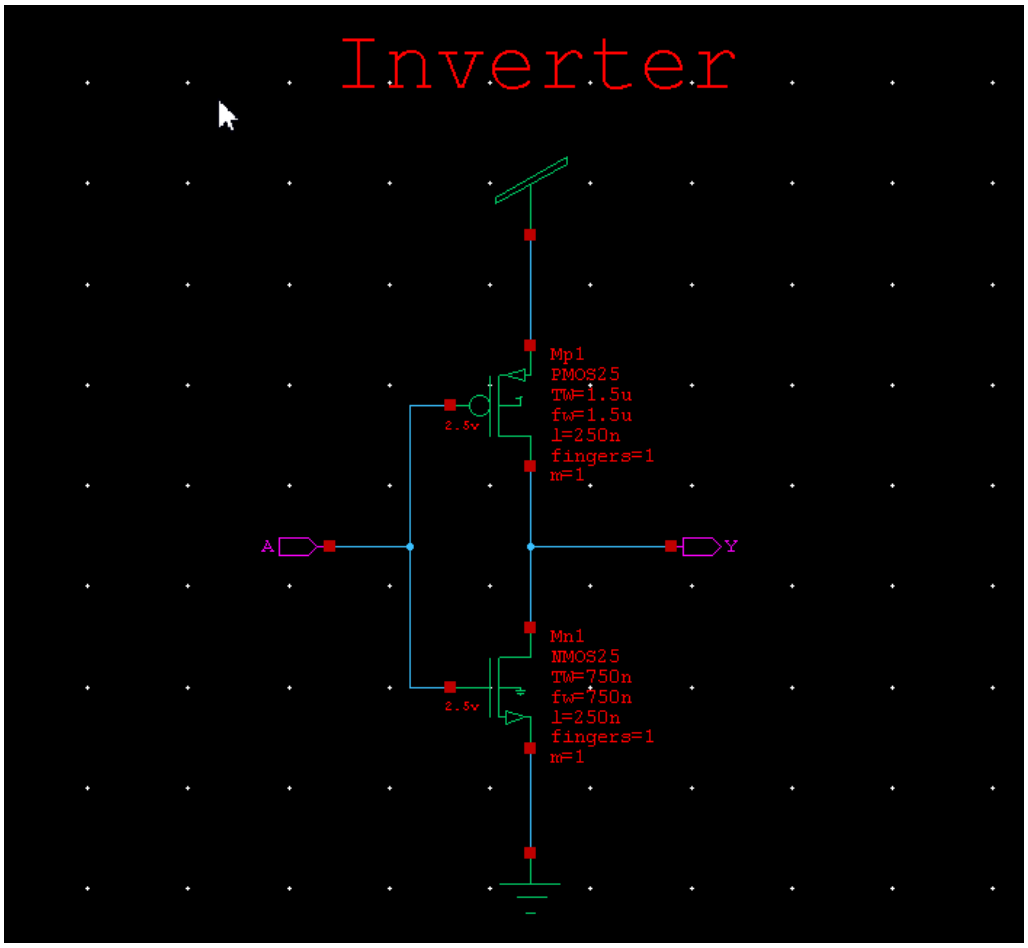
Lab 2: The INVERTER

OBJECTIVE

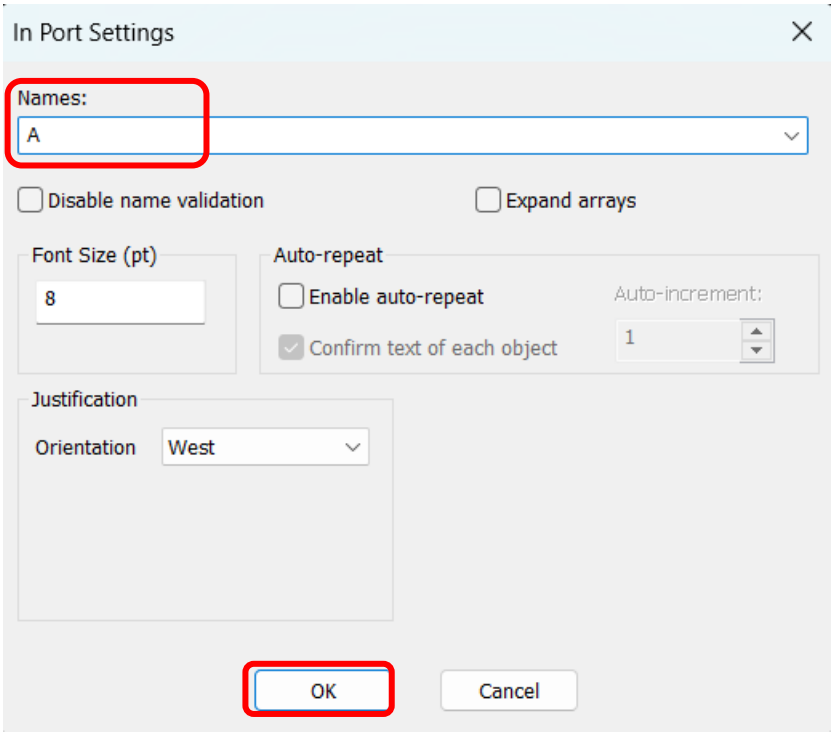
The objective of this lab is to characterize the CMOS inverter and obtain the input-output transfer characteristics.

SCHEMATIC ENTRY

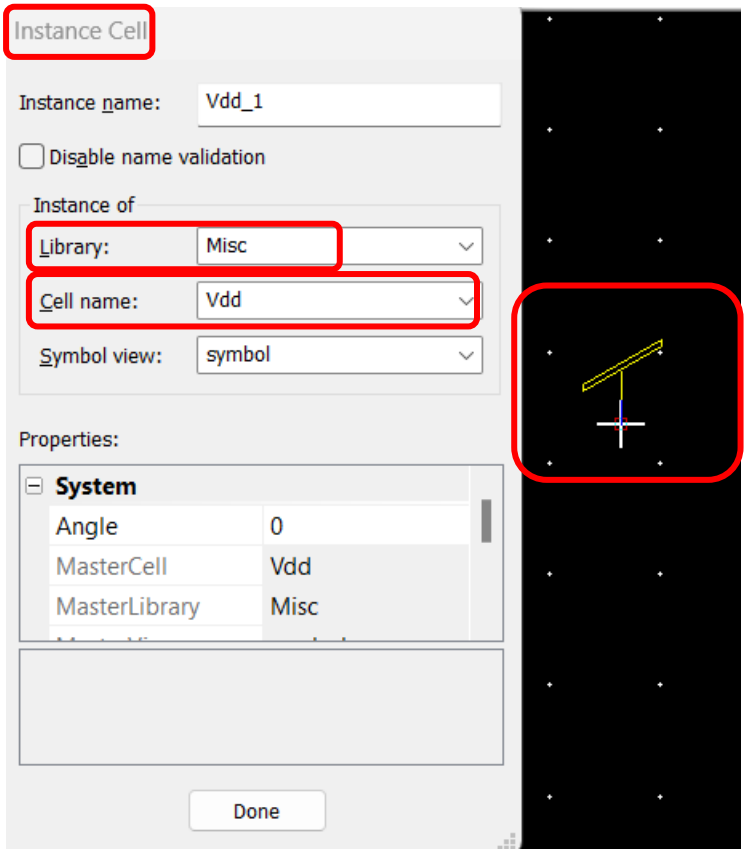
1. To build a schematic for the Inverter you have to follow the previous steps in the Schematic Entry section with respect of the changes that will occur in the schematic circuit.



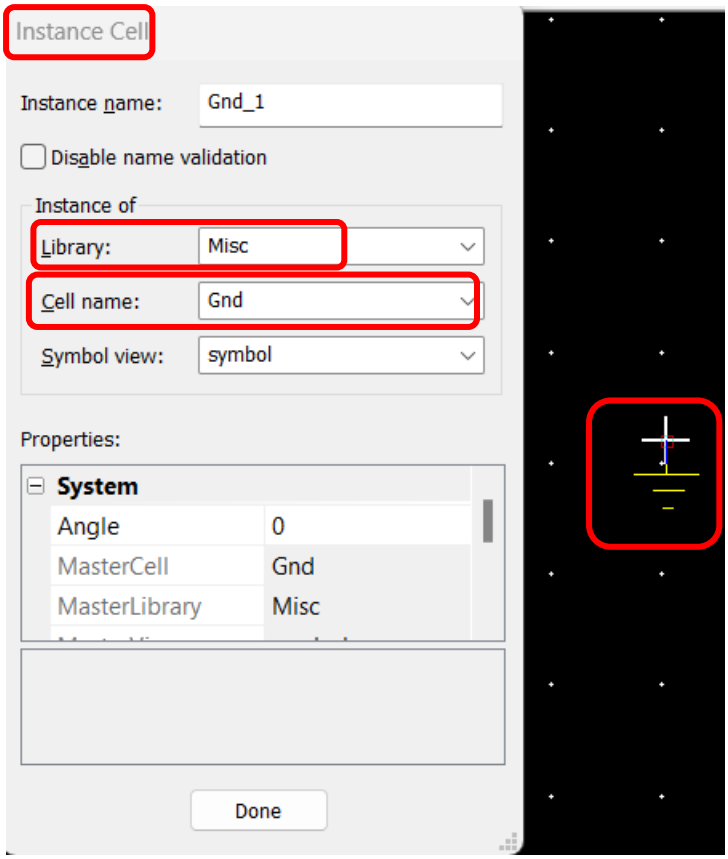
2. There are some several instances to add here to help us simulate the inverter. For the A and Y, input and output ports respectively you will find them in the top of the S-Edit window.  **For the Input port press**  **and for the Output port press**  **a window will open for you with the port settings with a default name of In and Out change them to A and Y and PRESS OK.**



3. Now to add the Vdd and Ground. **Reminder press I to add an instance choose the Misc Library we have add before and then choose Vdd.**



Now repeat the same steps for the ground.



To add a label choose L this Icon and change the text!

4. The last step to do is to wire all things together with respect to the circuit diagram.

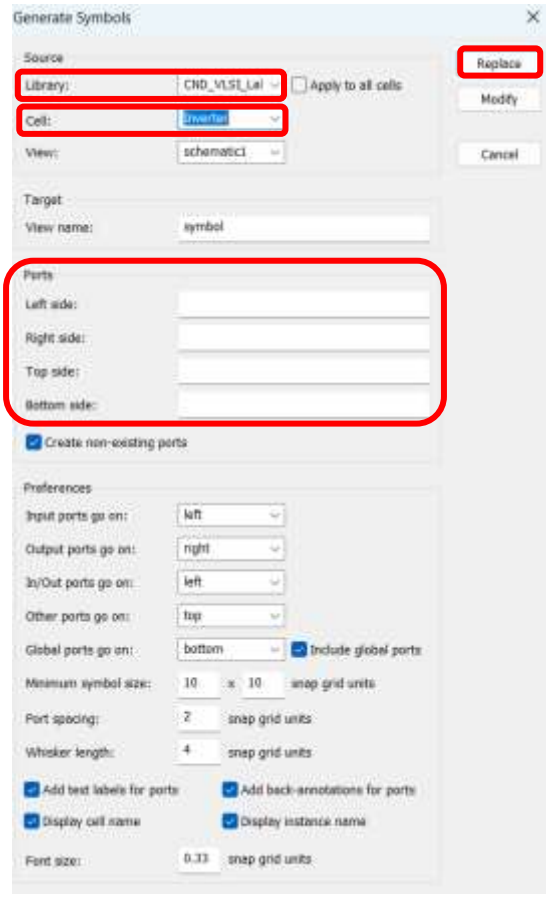
Note that edited files that isn't saved will be followed by a * so don't forget to save it

Remember to check your design by pressing ✓ on top left hand side.

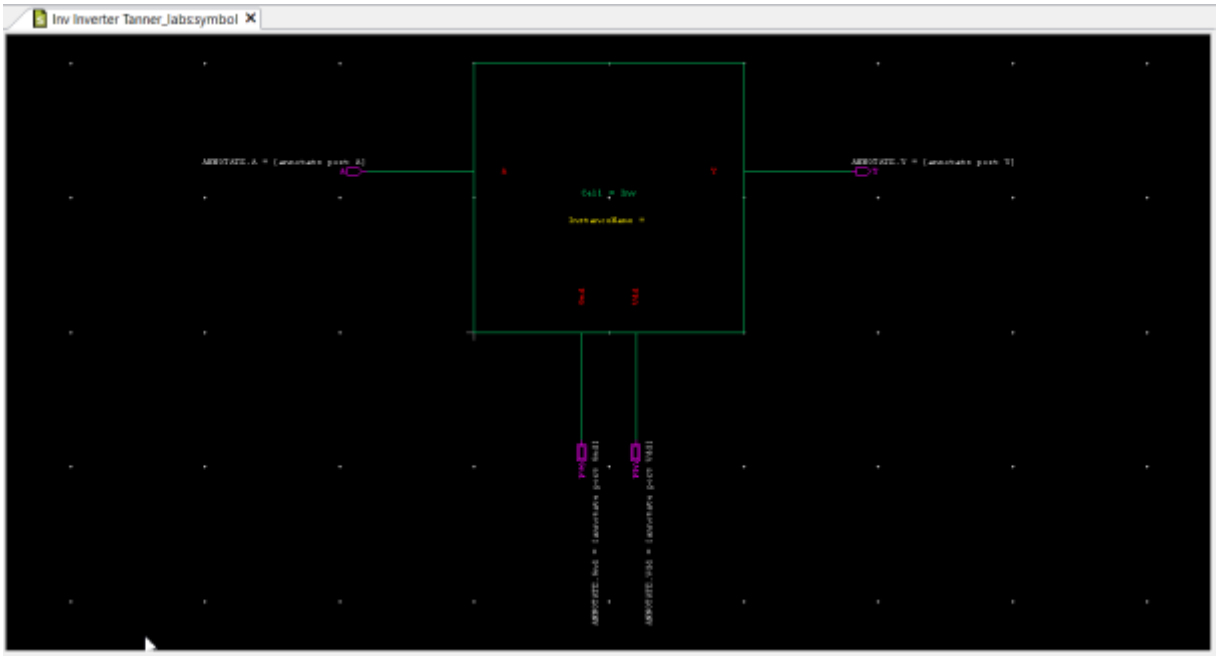
SYMBOL CREATION

After we make sure that, the design is actually correct and there is no errors or warnings. Now the inverter can be created as a symbol.

1. Click on Cell >> Generate Symbols and a window will occur.

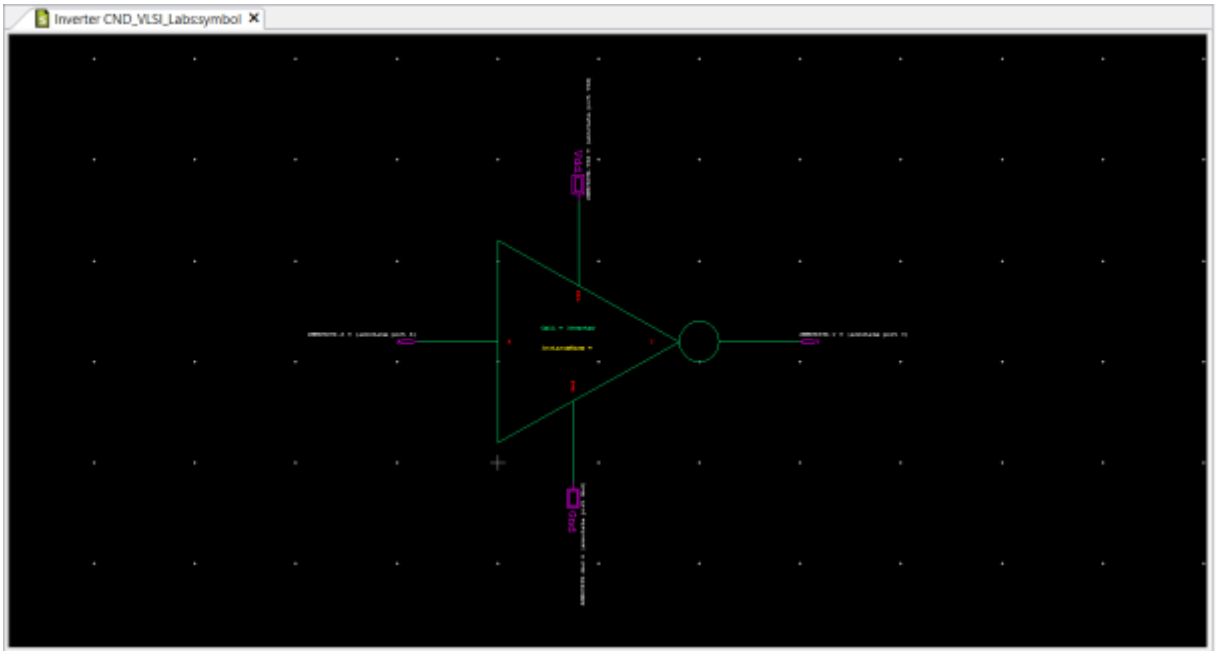


   a) Now choose your library for this symbol **(MUST BE THE SAME LIBRARY AS THE INVERTER)**.
   b) Then choose the cell you would like to create a symbol for it.
   c) Then choose which ports positions. For most cases, the inputs are in the left side, the outputs are in the Right, Vdd on top, and ground on the bottom.
   d) You can keep it empty it will be generated as default.
   e) Now **press replace** and a new window cell will open with the Inverter Symbol.



2. You can also edit the symbol by these tools. 

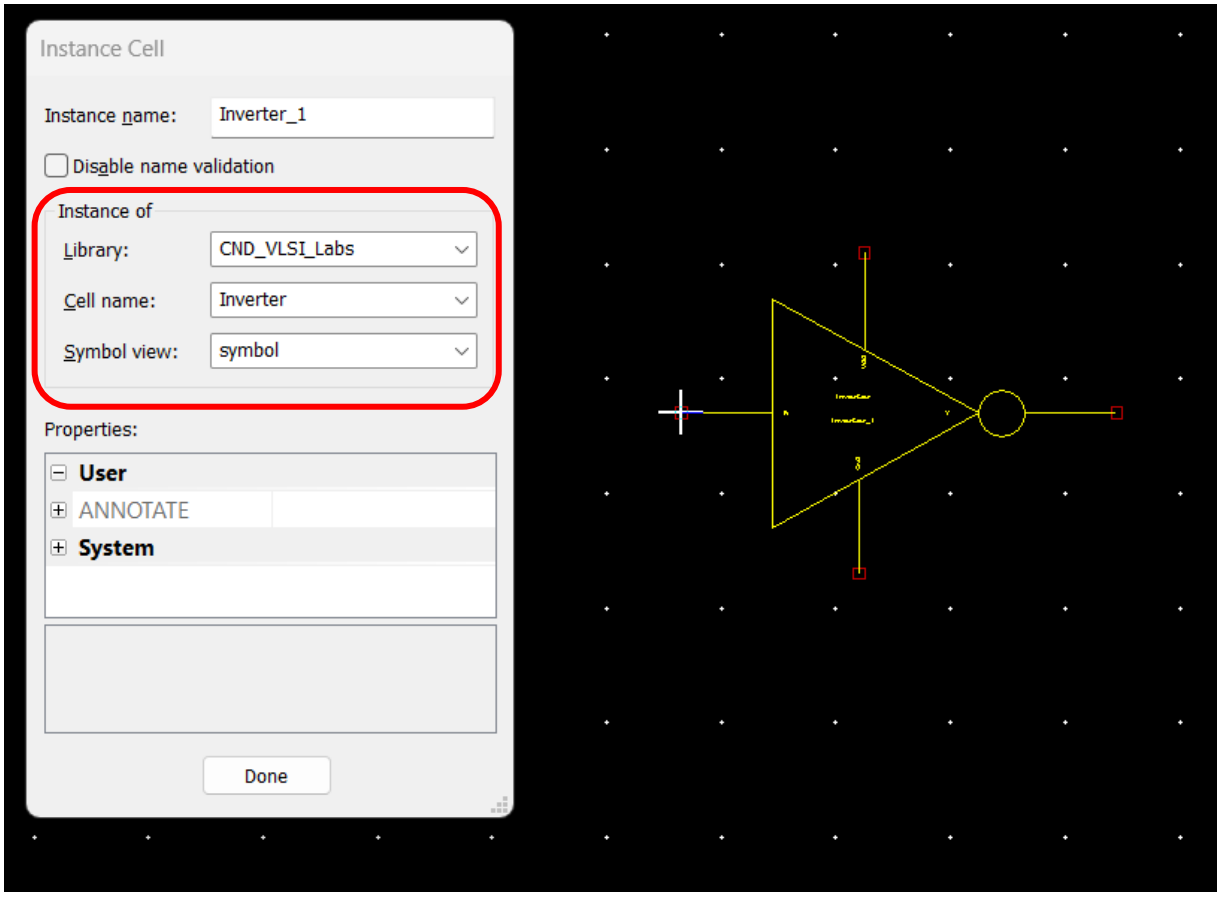
   Therefore, the final inverter Symbol will look like this:



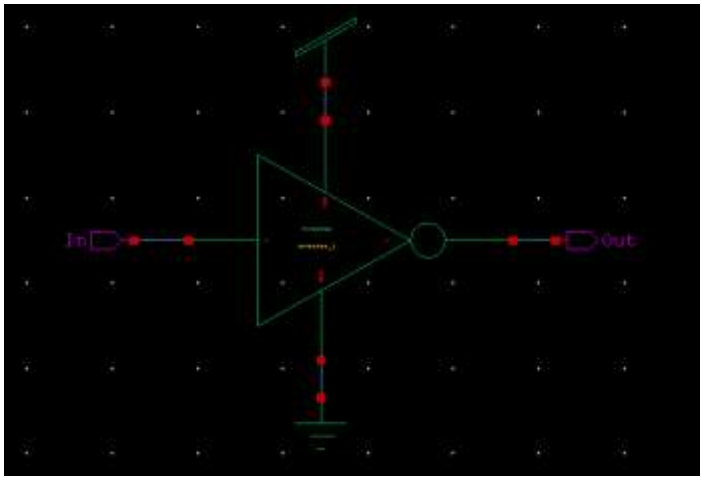
DO NOT FORGET TO SAVE IT!

SCHEMATIC TESTBENCH

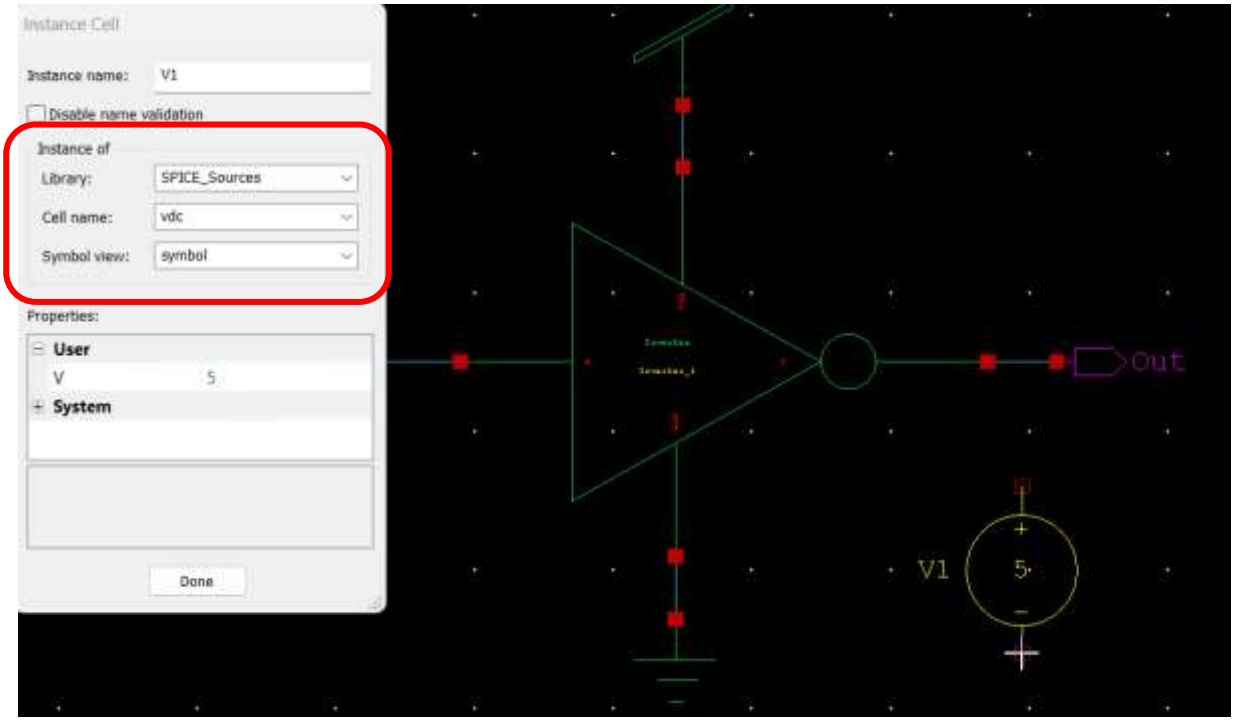
1. For the Inverter Testbench circuit you will need to open a new view by clicking Cell >> New View. **Do not forget to save it in the same library.**
2. Now press I to add and Instance then choose the library we created you will find the Inverter Symbol created before.



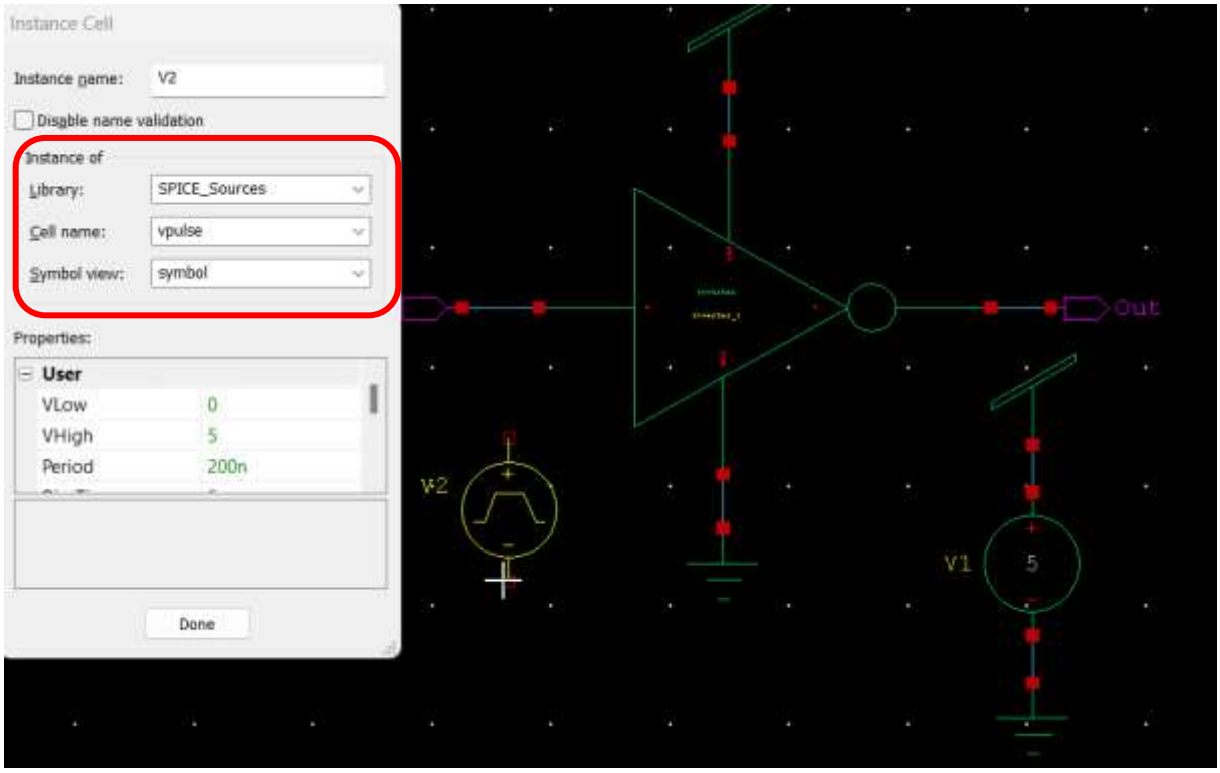
3. Now put the Input, output, Vdd, and ground ports.



4. To add a DC voltage source to assign it to the Vdd press I and choose it from the library called **SPICE_Sources >> Vdc.**

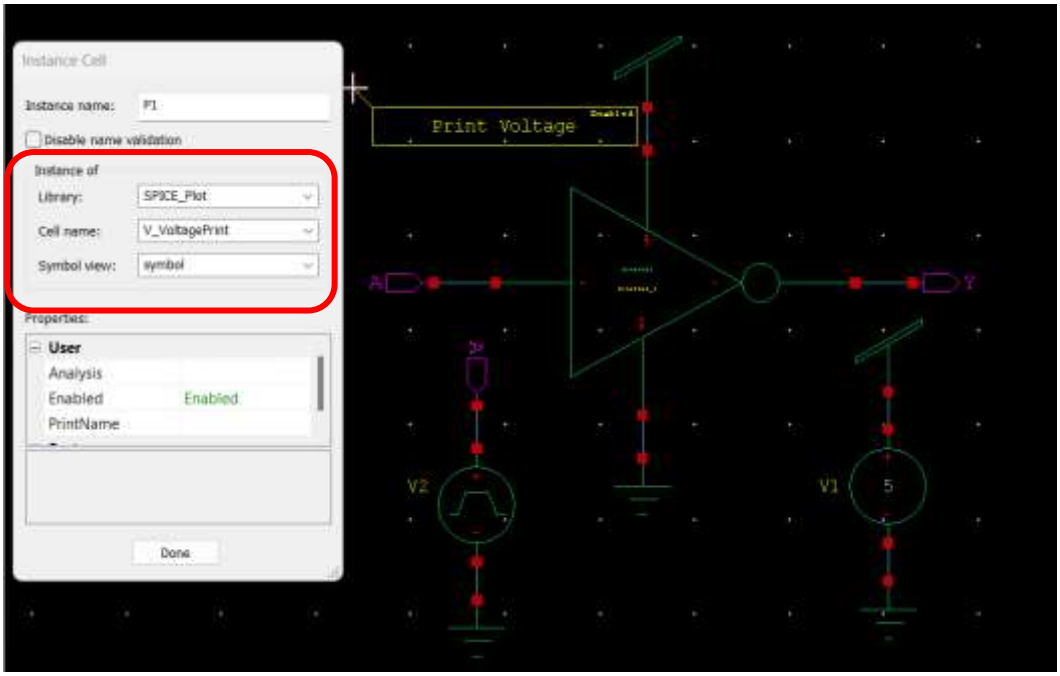


5. To add an input digital signal source to assign it to the Input press I and choose it from the library called **SPICE_Sources >> Vpulse.**

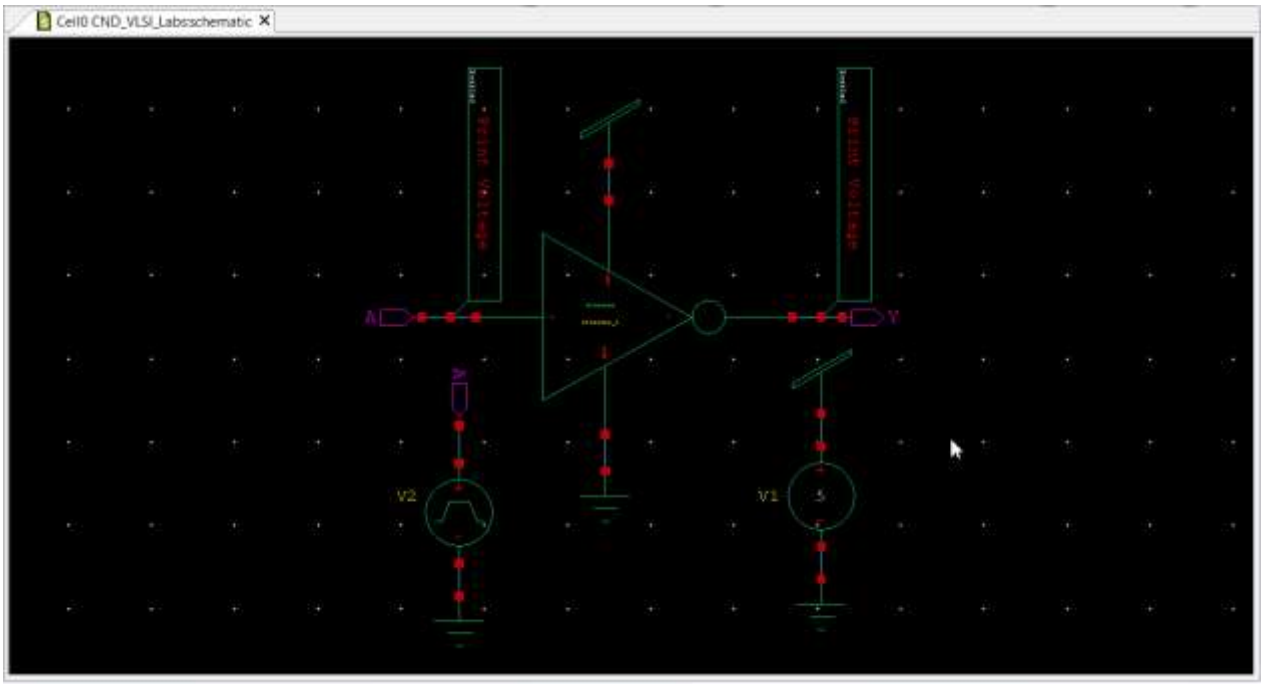


6. Now to show the Input and Output signals, The Print Voltage block will secure the job done.

   You can get it by pressing I and then choose SPICE_Plot Library and then choose cell name V_VoltagePrint.



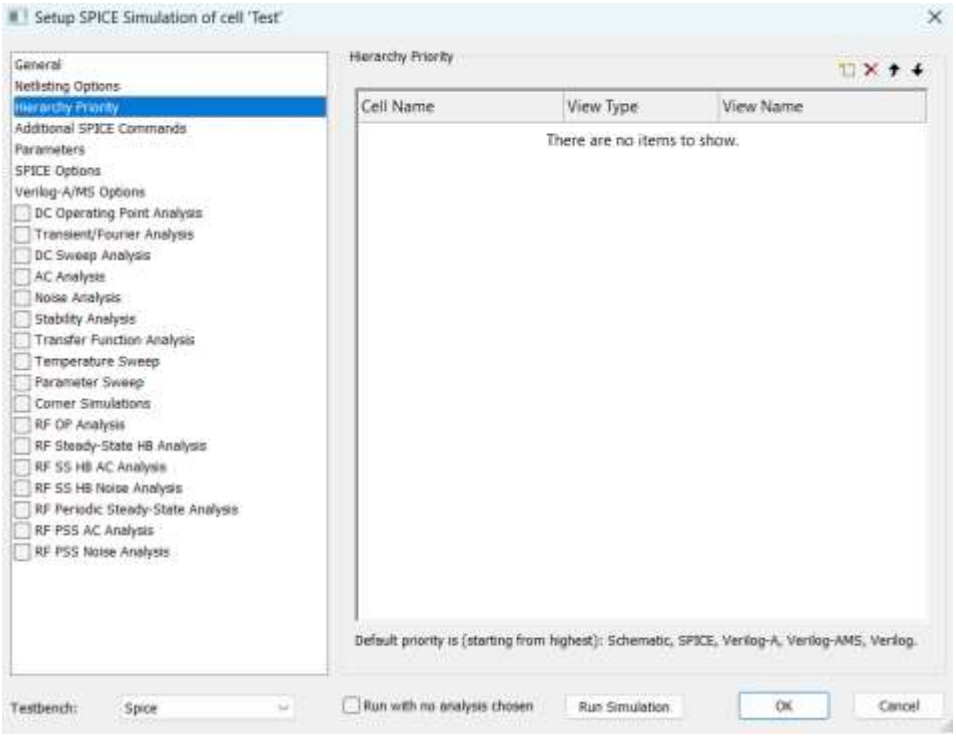
Now place it in the input and output wires. Here how the final schematic should look.



Remember to check your design by pressing ✓ on top left hand side.

SIMULATION SETUP

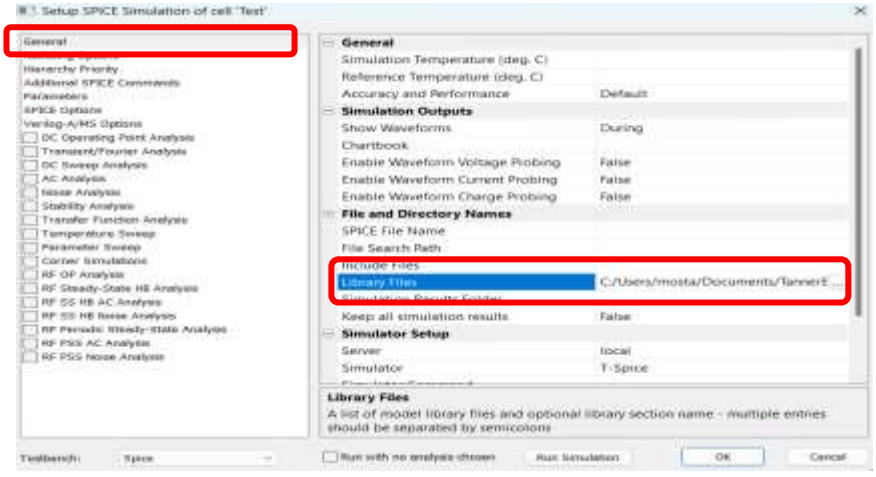
1. To setup the simulation the first thing to do is pressing this icon  from the toolbar the Setup Spice Simulation window will open.



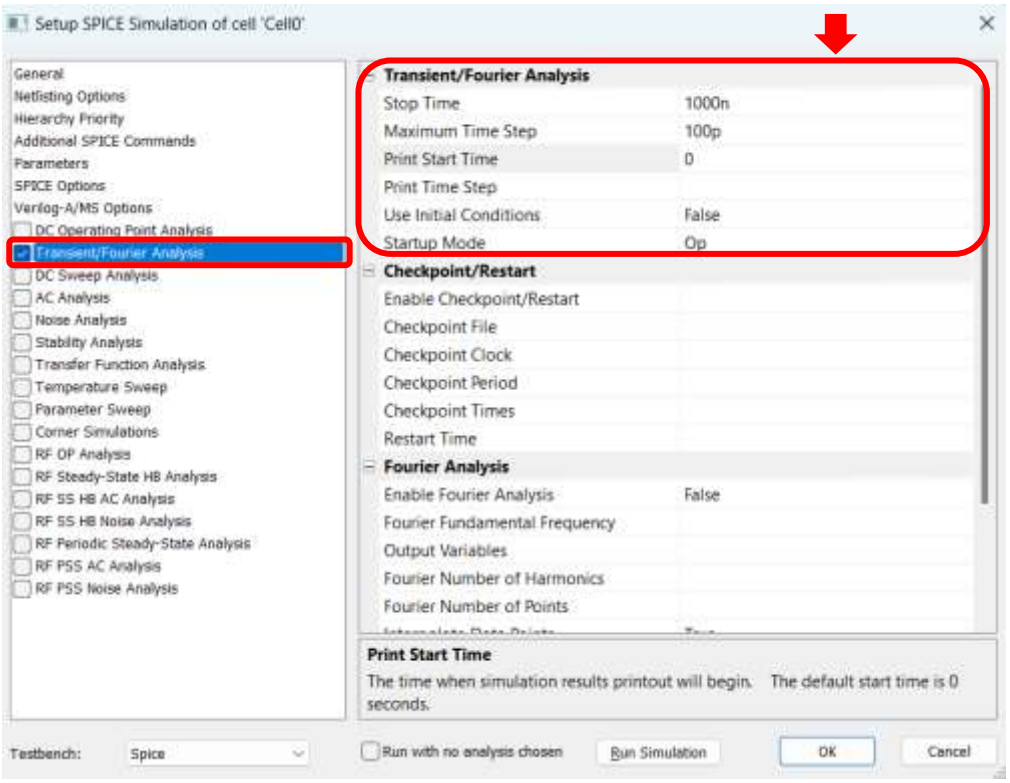
2. Begin with Highlighting “General” from the dialog on the left hand side. On the right, click in the “Library Files” field. This is where you will specify any SPICE models you will be using in your simulations. Browse & select:

“C:/Users/Documents/TannerEDA/TannerTools_v2019.2/Process/Generic_250nm/Models/Generic_250nm.lib TT”

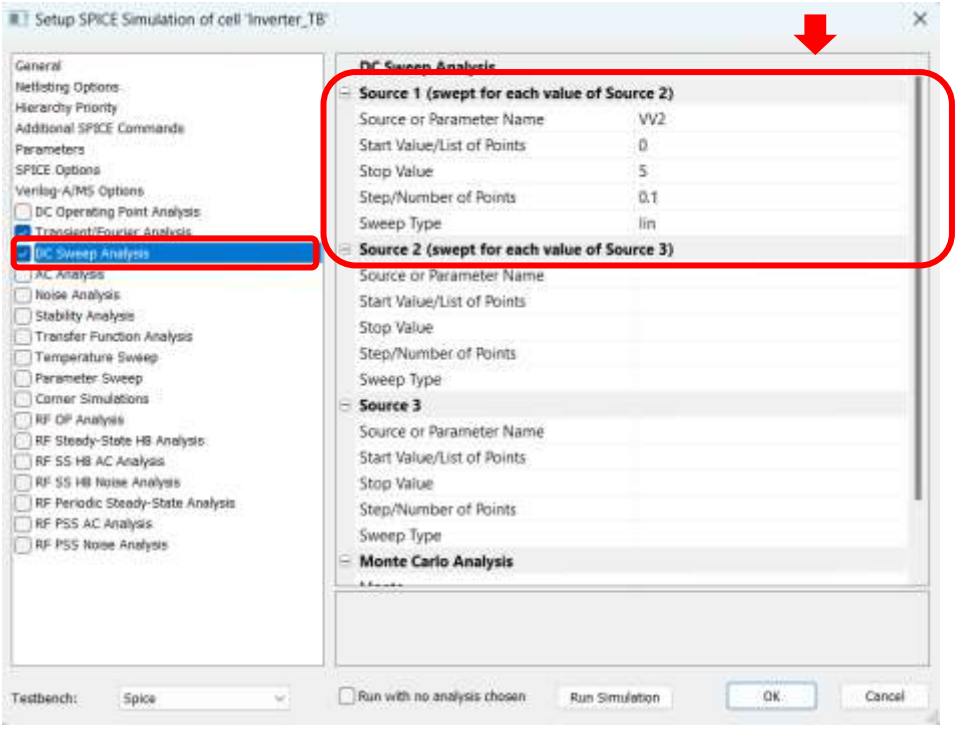
Remember to add ‘TT’ after the lib file manually



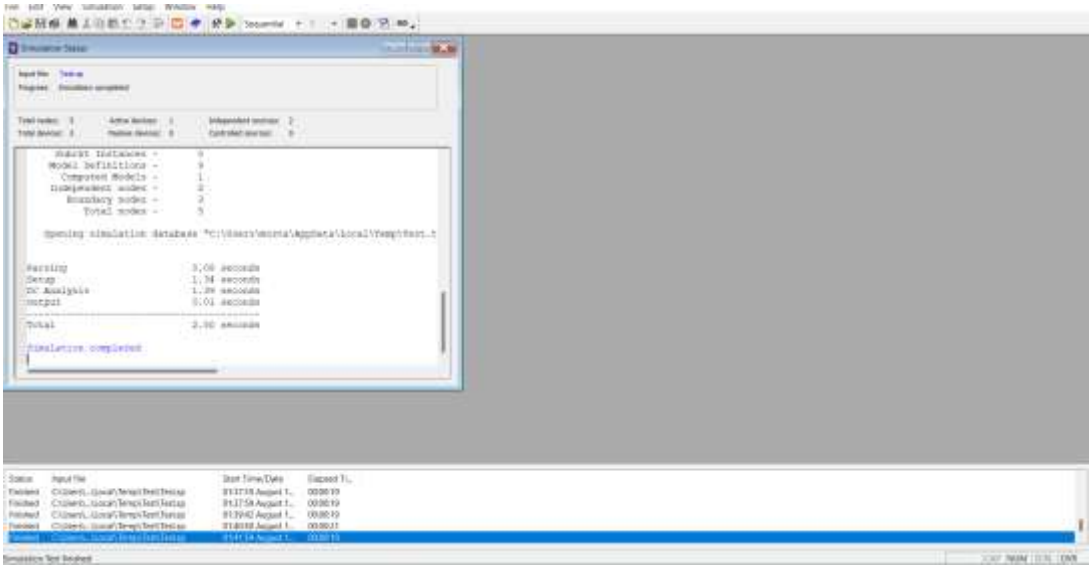
3. Now for the Inverter you will use Transient/Fourier Analysis to run the circuit for a certain time with a certain maximum time step. Now set the characteristics as follows:



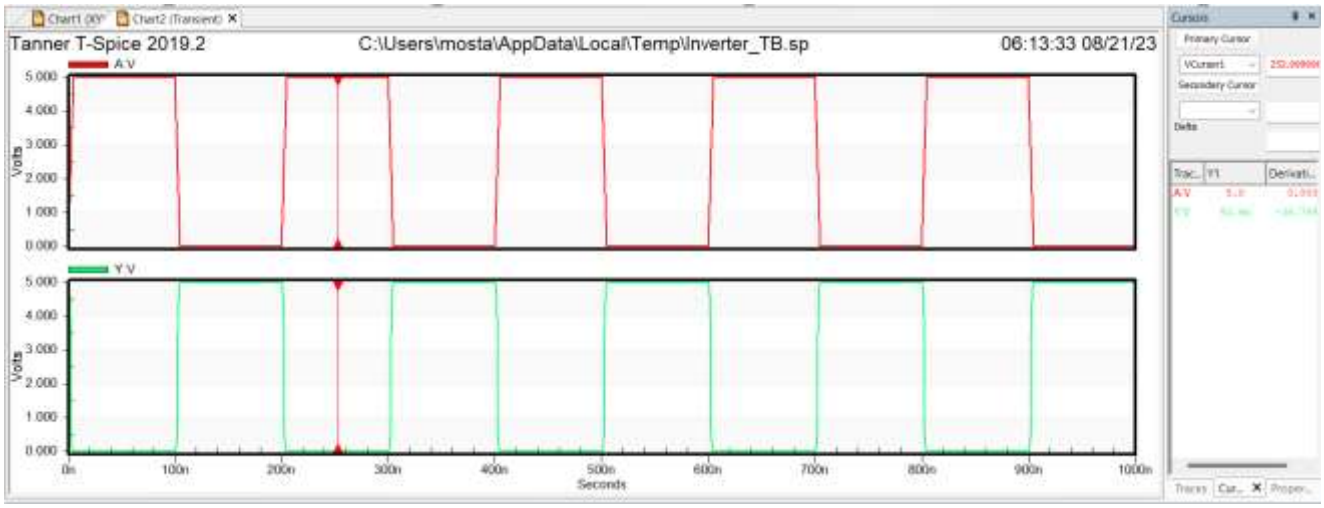
4. For the Transfer curve, you will be **sweeping the Input Pulse**. So you use DC Sweep Analysis as Follows:

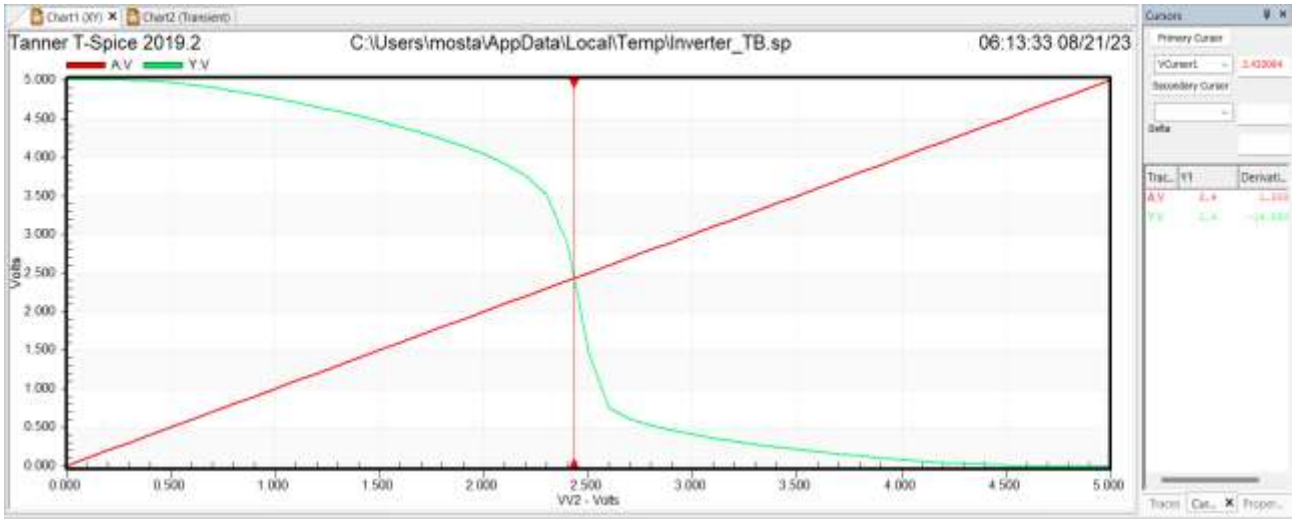


5. Now we SAVE and run Simulation by simply clicking  it should open another window holding the name “T-Spice” to run the spice file of the cell. It should give us Simulation completed.



6. You can separate the traces in separate plots by pressing this icon  . Therefore, the results will look like this.





ALL DONE NOW!

Assignment(2):

- Do the same as in this Lab, but for **CMOS Buffer**.
- Do the same as in this Lab, but for **CMOS NAND**.
- **Bonus**:
  1) Analyze changing **W_p/W_n** ratio over **Transfer Characteristics** of CMOS Inverter and comment on the results.
  2) Calculate the **NM_H** (Noise margin high) and **NM_L** (Noise margin low) for CMOS Inverter.
  3) Calculate the **propagation delay** of the CMOS inverter, and suggest solutions to minimize it.
  4) Analyze the **effects of changing VDD over propagation delay** and comment on the results.