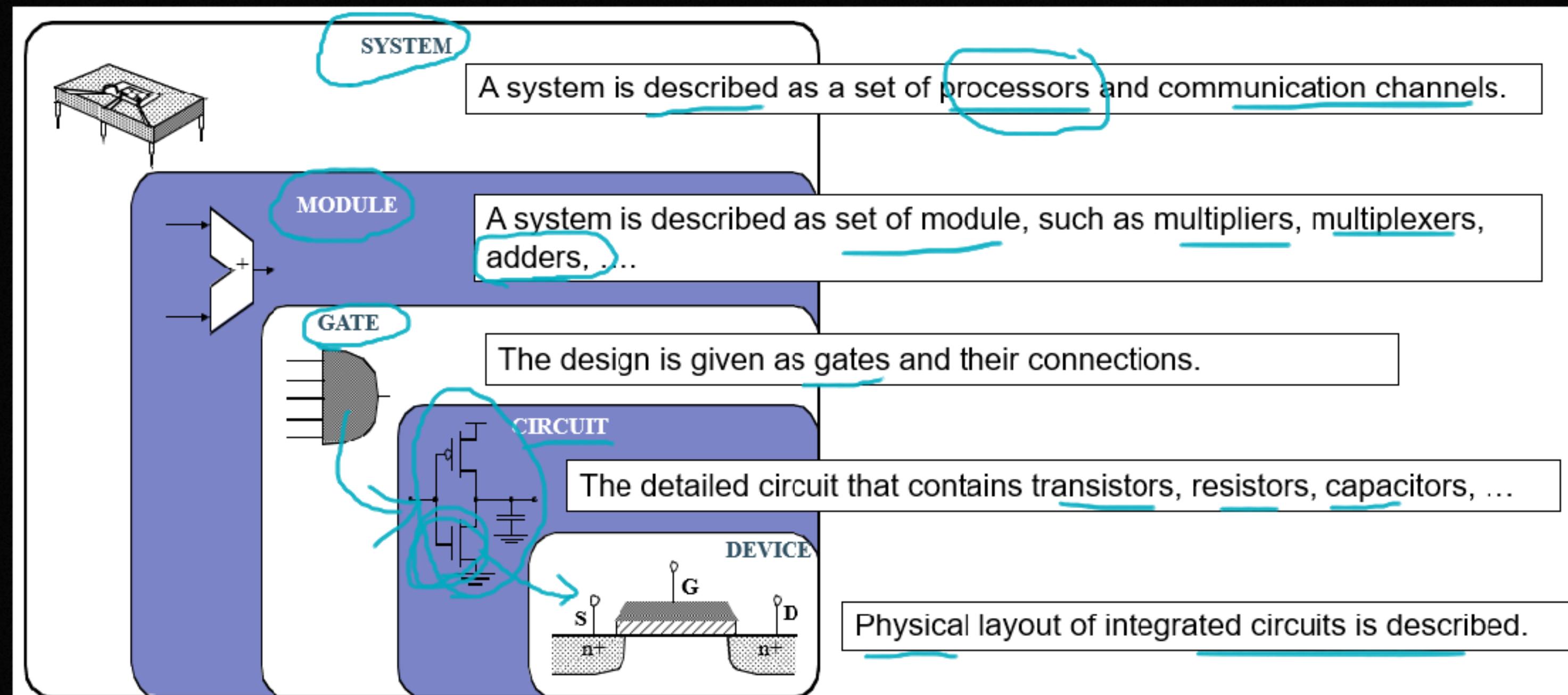


# IC Design Flows

with  
low



# Design Approach

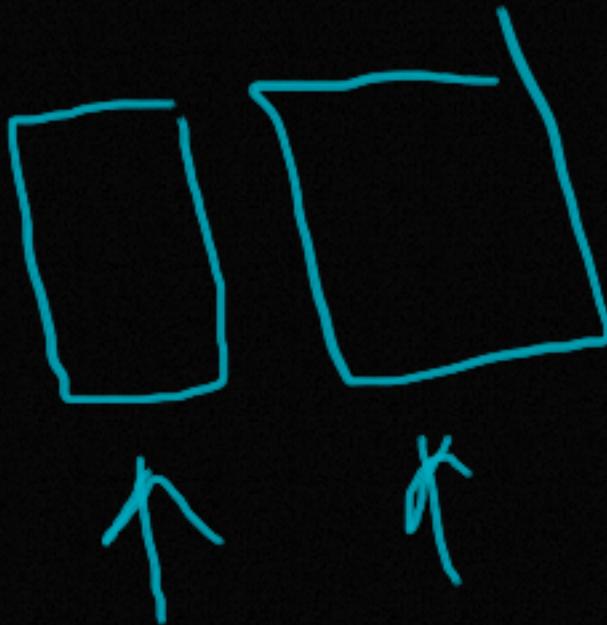
- Custom/Handcrafted:

==> Early designs were truly hand-crafted.

==> Every transistor was laid out and optimized individually and carefully fitted into its environment, for example the design of the Intel 4004 microprocessor.

==> This approach is not appropriate when more than a million devices have to be created and assembled.

==> With the rapid evolution of the design technology, time-to-market is one of the crucial factors in the ultimate success.



- Hierarchical:

==> A circuit is constructed in a hierarchical way:

=====> A processor is a collection of modules, each of which consists of a number of cells on its own.



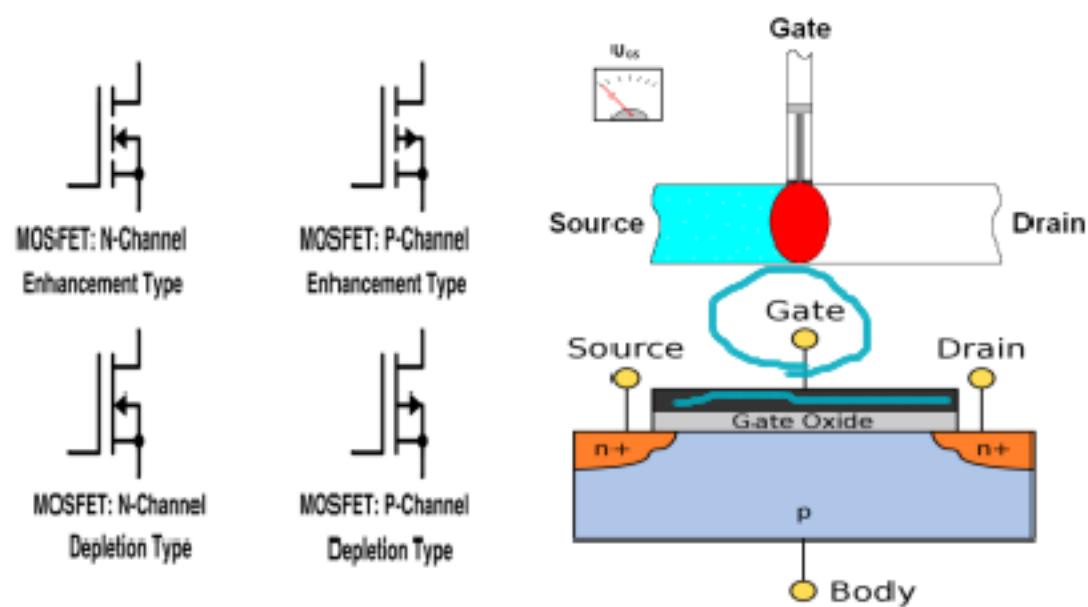
==> Cells are reused as much as possible to reduce the design effort and to enhance the chances for a first-time-right implementation.

Reusability

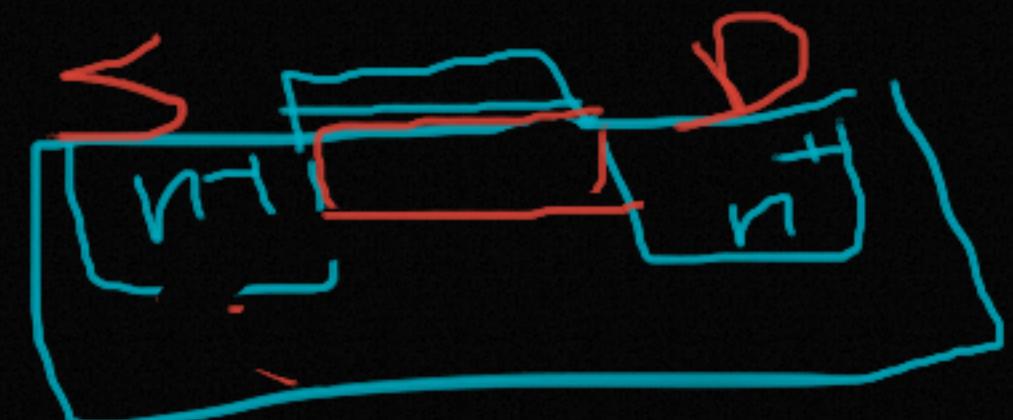
The fact that this hierarchical approach is at all possible is the key ingredient for the success of digital circuit design.

# MOS Field-Effect Transistors - MOSFET

- **MOSFET stands for Metal-Oxide-Silicon Field-Effect Transistor.**
- MOSFET can be used as an amplifier (voltage or current) or as a switch. The three terminals are called **Gate (G)**, **Source (S)** and **Drain (D)**. The change of voltage between Gate and Source controls the flow of current through the Drain to Source channel. Hence MOSFET is regarded as a voltage-controlled-current device.

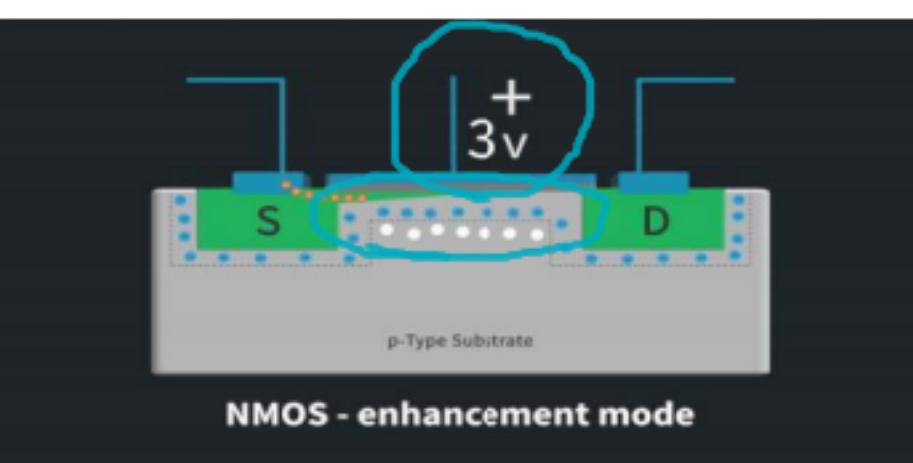
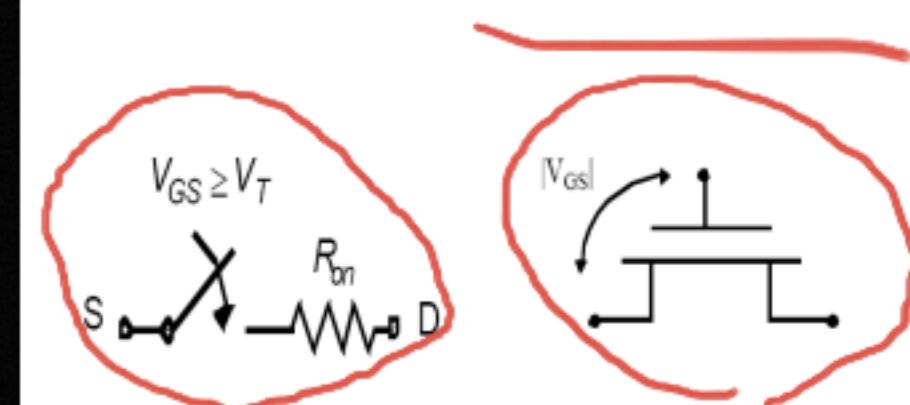


1. M - Metal: This refers to the metal gate electrode that is used in the MOSFET to control the flow of current.
2. O - Oxide: The oxide layer, typically made of silicon dioxide, separates the gate electrode from the semiconductor material. It acts as an insulator.
3. S - Semiconductor: MOSFETs are made from semiconductor materials, usually silicon, which is the most common material used in their construction.
4. F - Field-Effect: This indicates the principle by which a MOSFET operates. It relies on the electric field created by the gate voltage to control the flow of current between the source and drain terminals.
5. E - Transistor: A MOSFET is a type of transistor, which is a fundamental electronic device used to amplify or switch electronic signals.



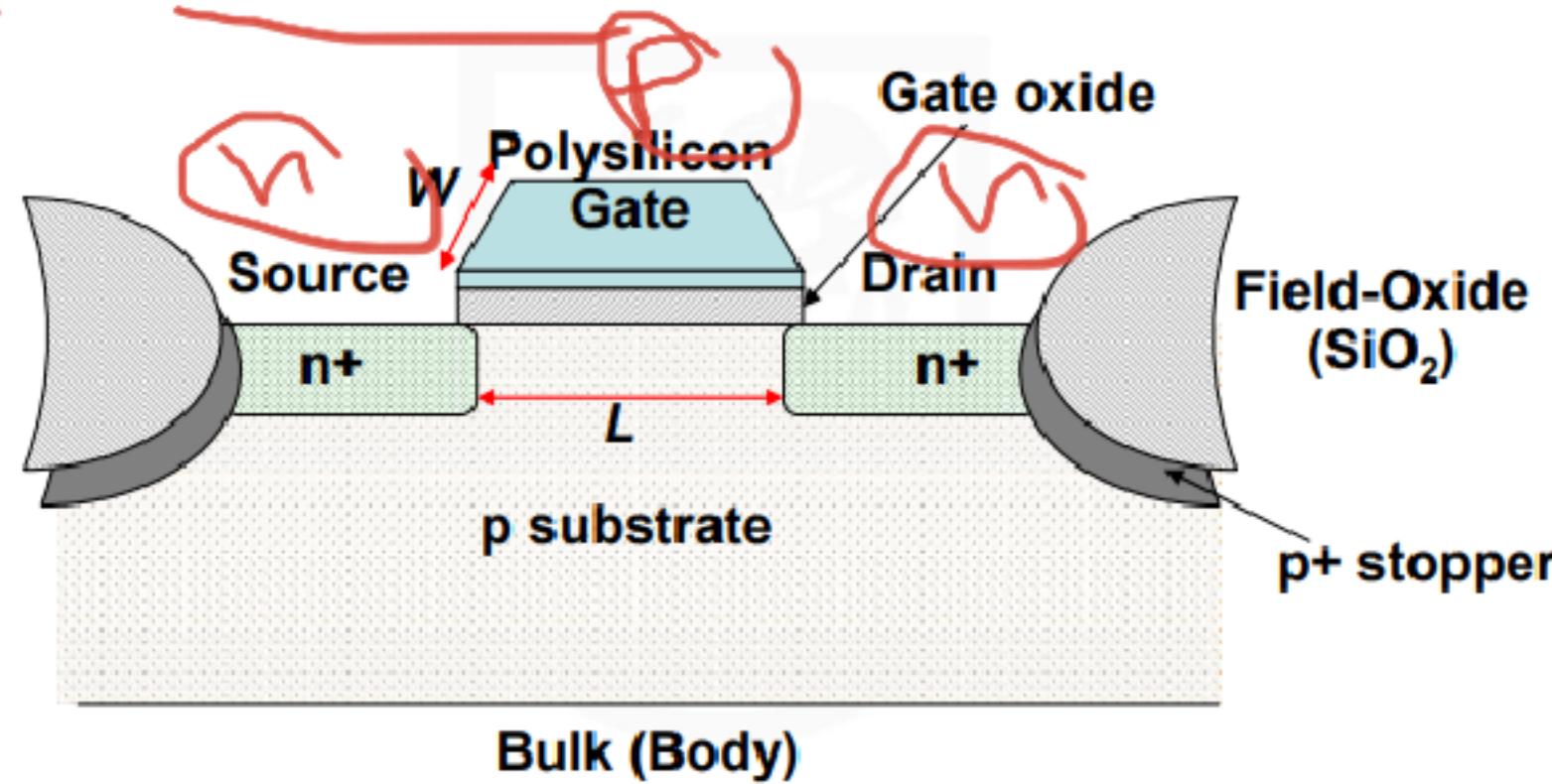
A Switch!

- When the voltage applied to the gate is larger than  $V_T$ , a conducting channel is formed between the drain and source.
- In the presence of a voltage difference between D & S, electrical current flows between them. When the gate voltage is lower than the threshold, no channel exists, and the switch is considered open.



# The NMOS Transistor Cross Section

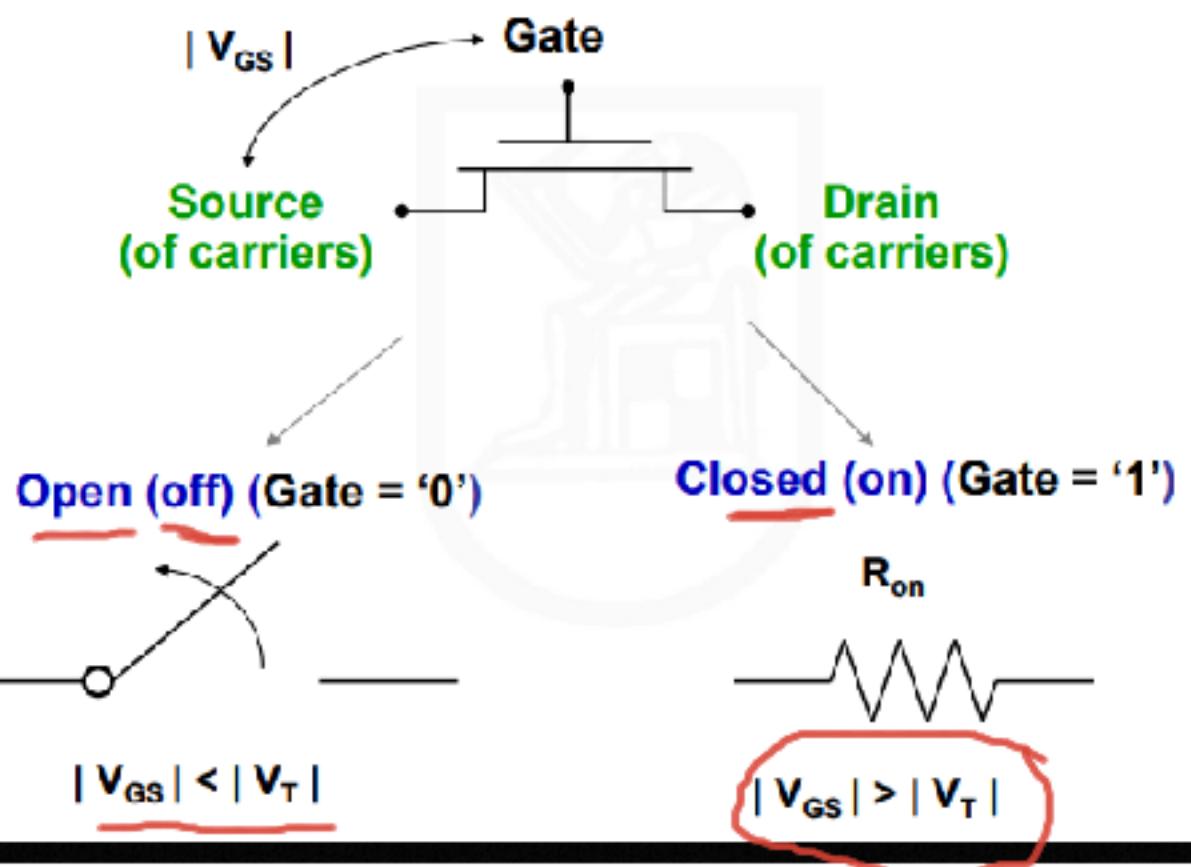
n areas have been doped with donor ions (arsenic) of concentration  $N_D$  -  
electrons are the majority carriers



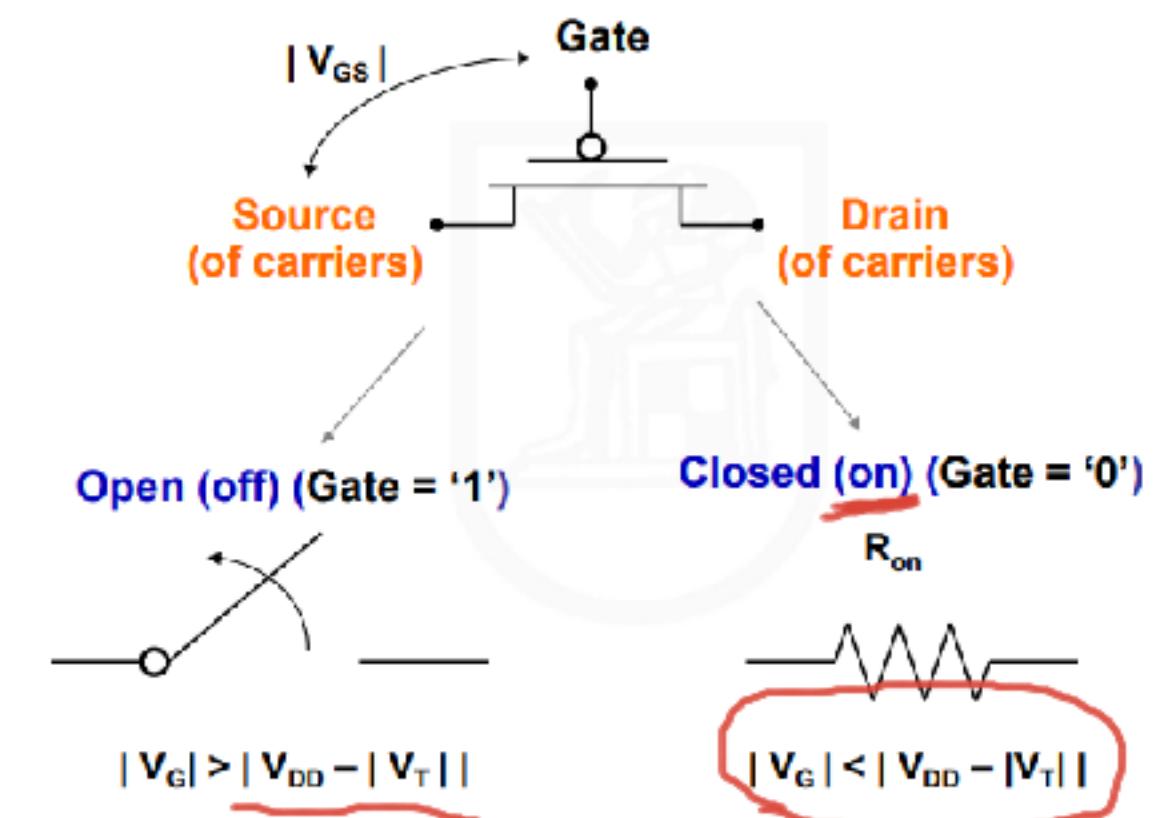
p areas have been doped with acceptor ions (boron) of concentration  $N_A$  -  
holes are the majority carriers



# Switch Model of NMOS Transistor



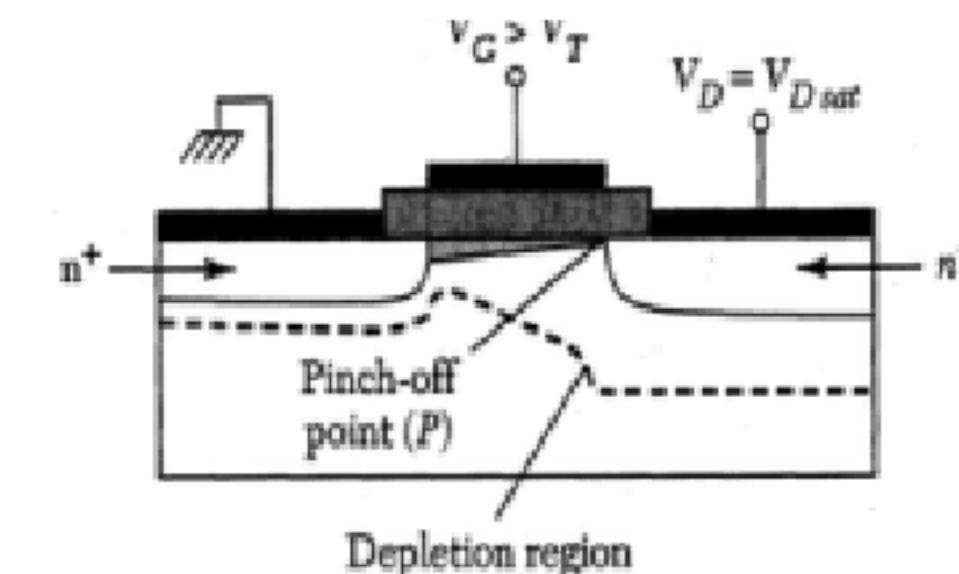
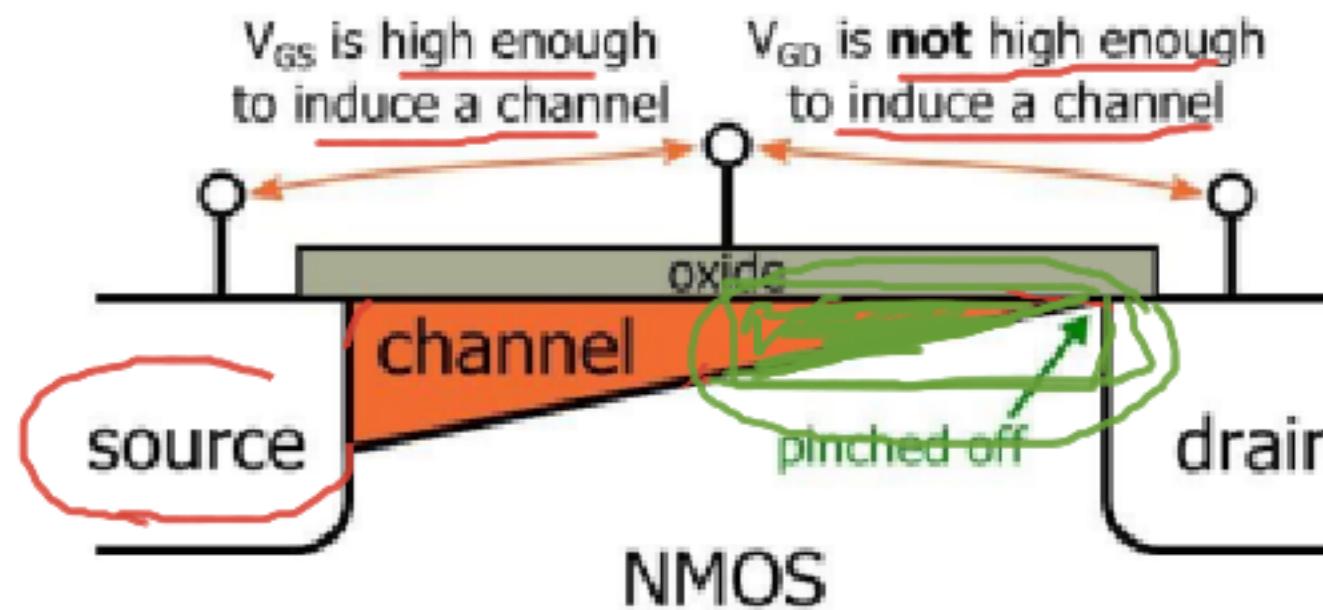
# Switch Model of PMOS Transistor



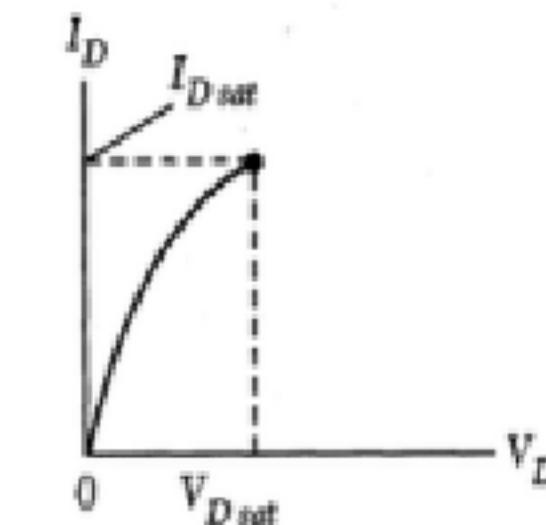
# What's Pinch off?



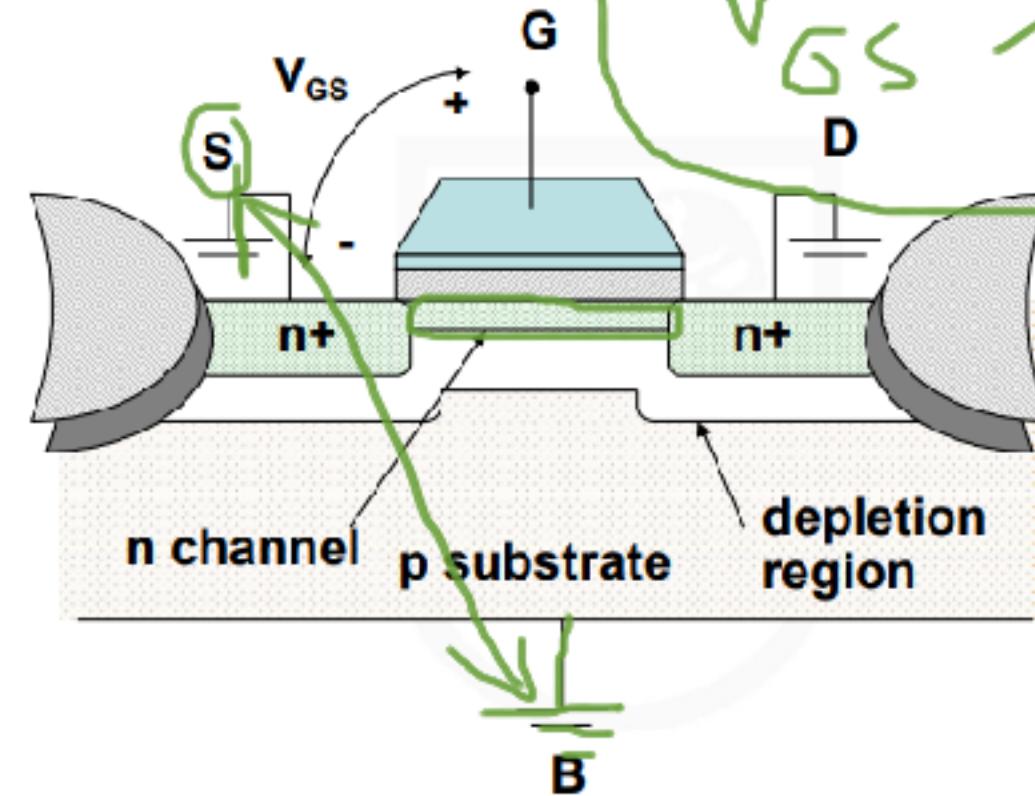
- Now add in the drain voltage to drive a current. Initially you get an increasing current with increasing drain bias.
- When you reach  $V_{Dsat} = V_G - V_T$  inversion is disabled at the drain end (pinch-off), but the source end is still inverted. Therefore the channel thickness at this end goes to zero. The charges still flow, just that you can't draw more current with higher drain bias, and the current saturates.
- The pinch-off region can limit the performance of CMOS devices because it can introduce non-linearities and limit the maximum drain current that can be achieved in the saturation region.



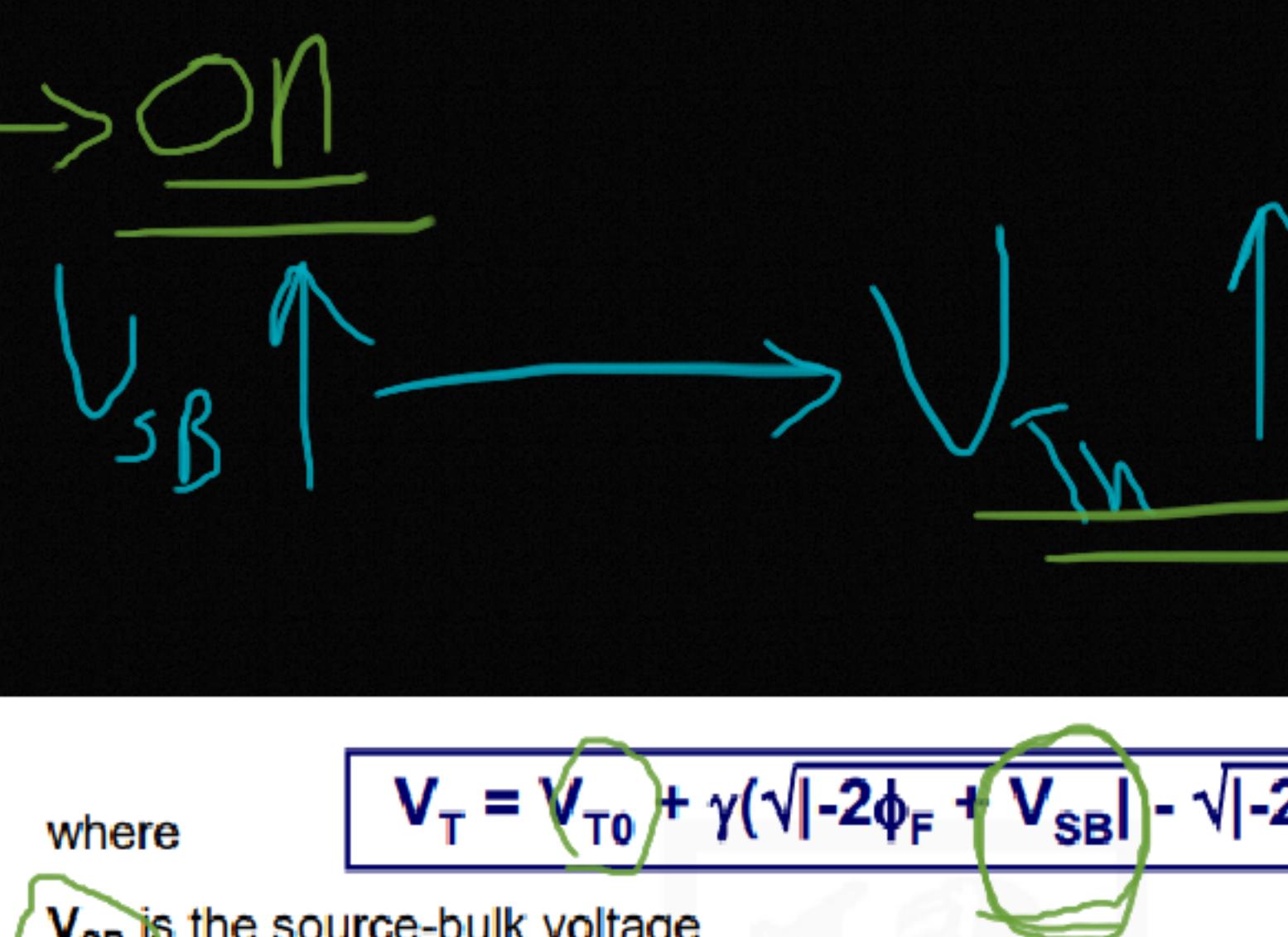
(b)



# Threshold Voltage Concept



The value of  $V_{GS}$  where strong inversion occurs is called the threshold voltage,  $V_T$



$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F|} + |V_{SB}| - \sqrt{|-2\phi_F|})$$

$V_{SB}$  is the source-bulk voltage

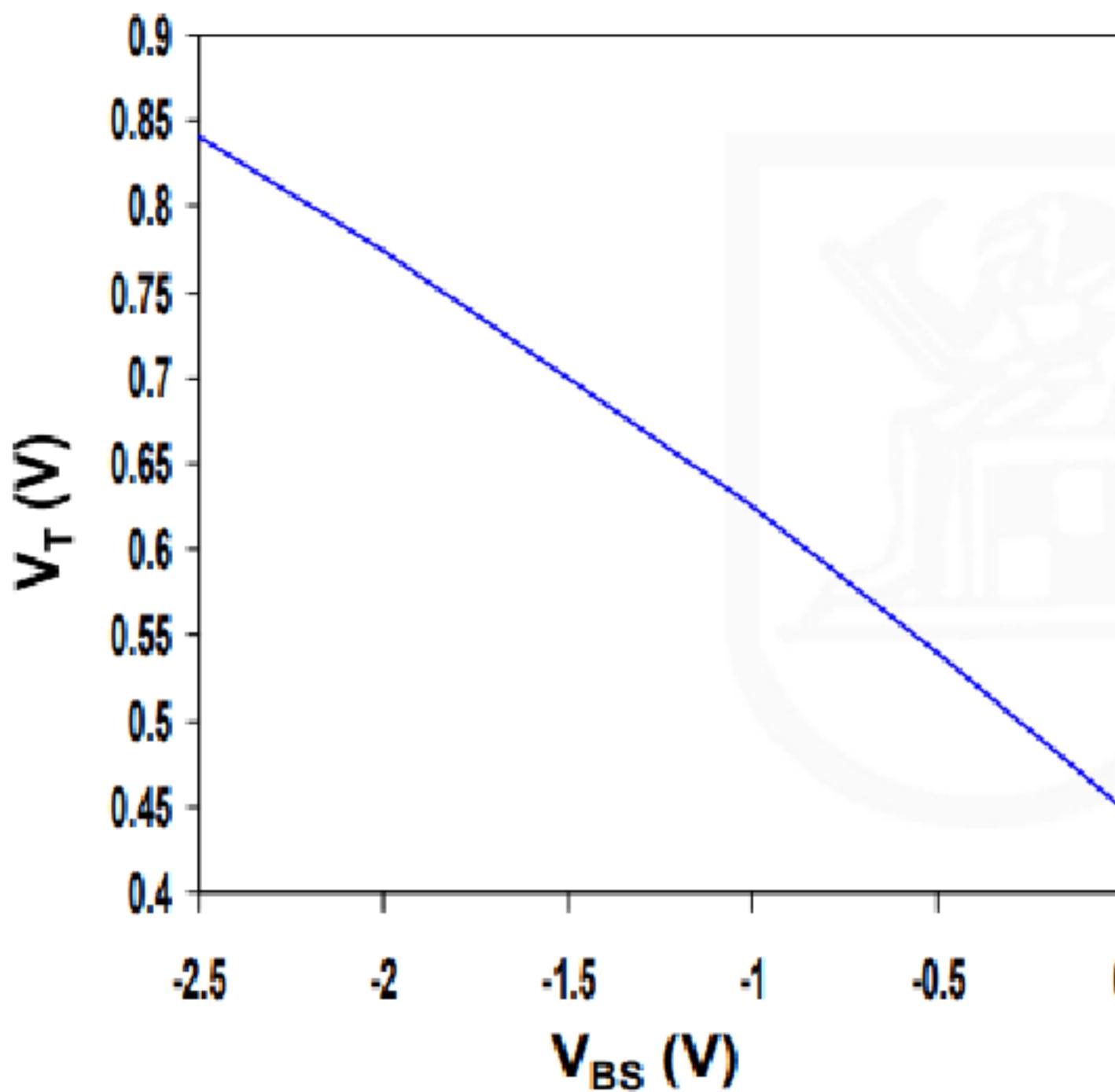
$V_{T0}$  is the threshold voltage at  $V_{SB} = 0$  and is mostly a function of the manufacturing process

Difference in work-function between gate and substrate material, oxide thickness, Fermi voltage, charge of impurities trapped at the surface, dosage of implanted ions, etc.

$\phi_F = -\phi_T \ln(N_A/n_i)$  is the Fermi potential ( $\phi_T = kT/q = 26mV$  at 300K is the thermal voltage;  $N_A$  is the acceptor ion concentration;  $n_i \approx 1.5 \times 10^{10} \text{ cm}^{-3}$  at 300K is the intrinsic carrier concentration in pure silicon)

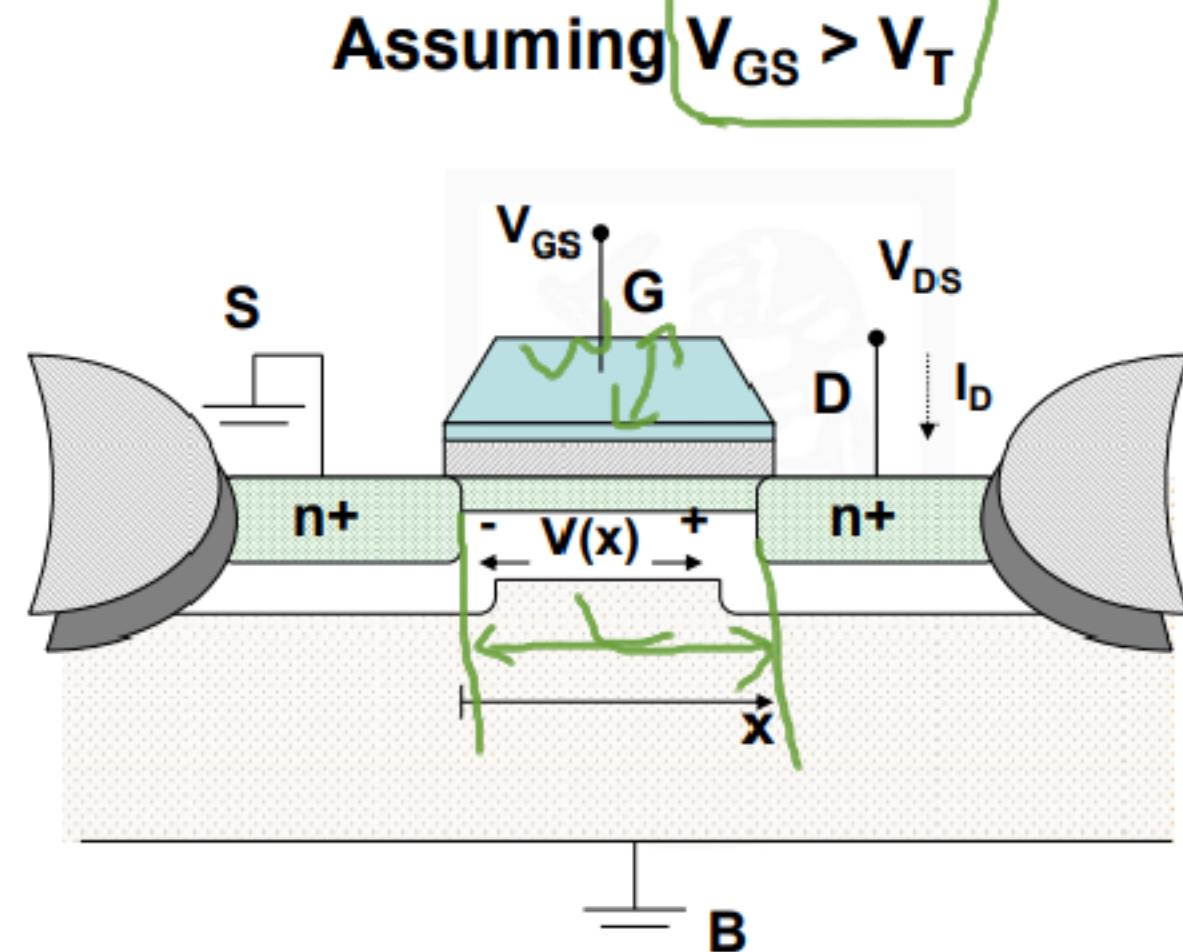
$\gamma = \sqrt{(2q\epsilon_{si}N_A)/C_{ox}}$  is the body-effect coefficient (impact of changes in  $V_{SB}$ ) ( $\epsilon_{si} = 1.053 \times 10^{-10} \text{ F/m}$  is the permittivity of silicon;  $C_{ox} = \epsilon_{ox}/t_{ox}$  is the gate oxide capacitance with  $\epsilon_{ox} = 3.5 \times 10^{-11} \text{ F/m}$ )

# The Body Effect



- $V_{SB}$  is the substrate bias voltage (normally positive for n-channel devices with the body tied to ground)
- A negative bias causes  $V_T$  to increase from 0.45V to 0.85V

# Transistor in Linear Mode



## Voltage-Current Relation: Linear Mode

- For long-channel devices ( $L > 0.25$  micron)
- When  $V_{DS} \leq V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L} [(V_{GS} - V_T)V_{DS} - V_{DS}^2/2]$$

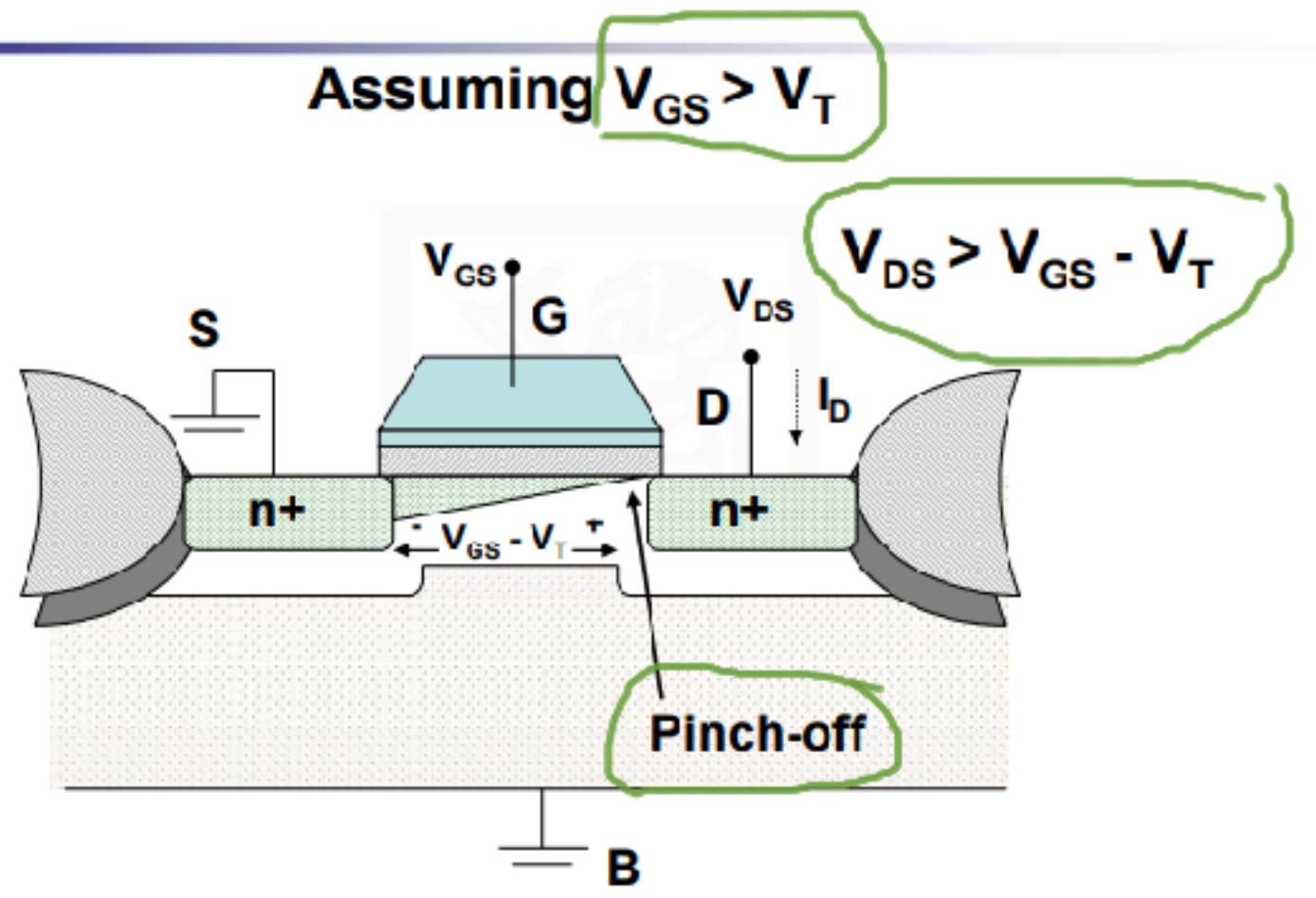
where

$k'_n = \mu_n C_{ox} = \mu_n \epsilon_{ox} / t_{ox}$  is the process transconductance parameter ( $\mu_n$  is the carrier mobility ( $m^2/Vsec$ ))

$k_n = k'_n W/L$  is the gain factor of the device

For small  $V_{DS}$ , there is a linear dependence between  $V_{DS}$  and  $I_D$ , hence the name resistive or linear region

# Transistor in Saturation Mode



The current remains constant (transistor saturates)

## Voltage-Current Relation: Saturation Mode

For long channel devices

- When  $V_{DS} \geq V_{GS} - V_T$

$$I_D' = k'_n / 2 W/L [(V_{GS} - V_T)^2]$$

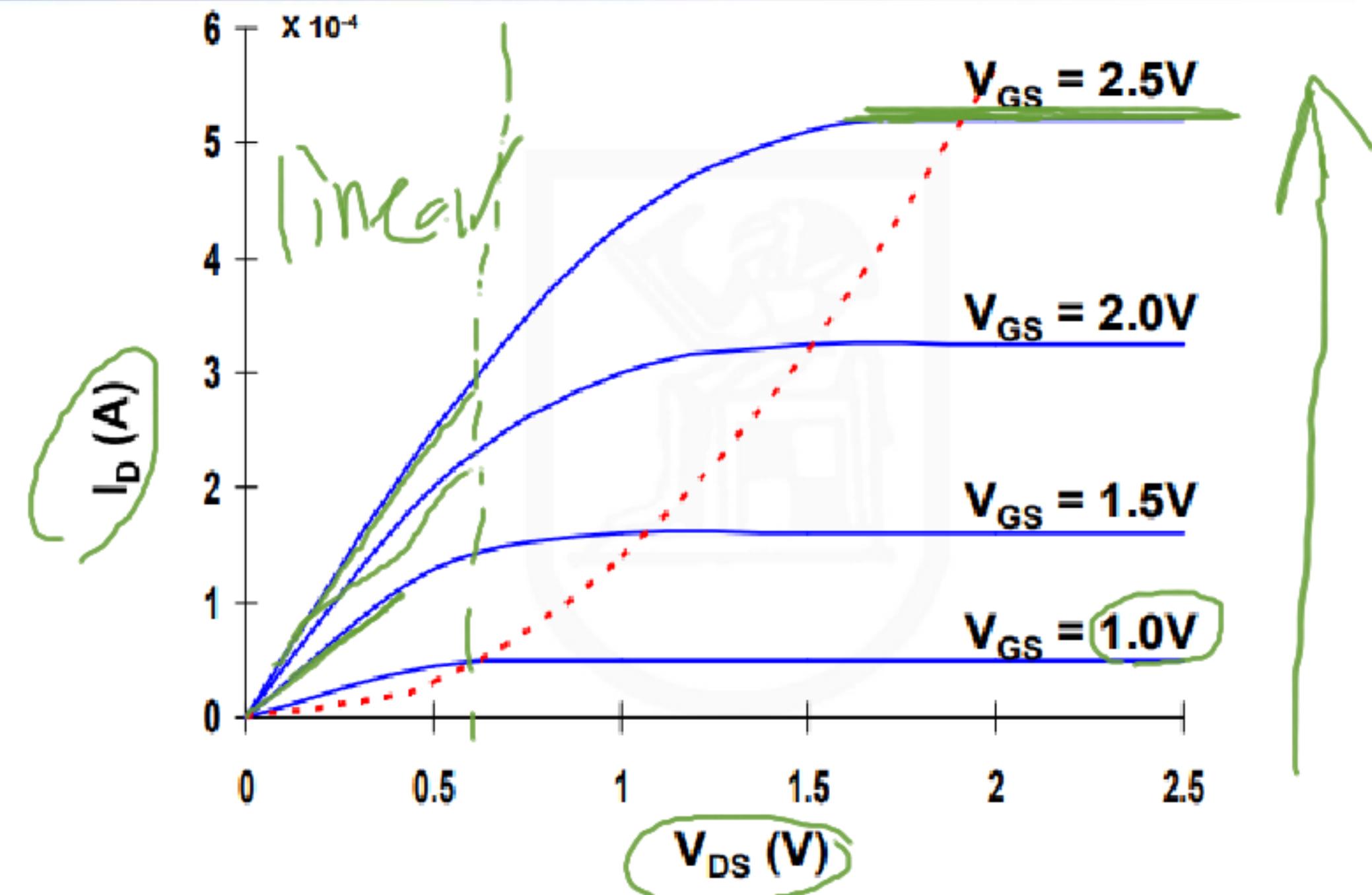
since the voltage difference over the induced channel  
(from the **pinch-off** point to the source) remains fixed at  
 $V_{GS} - V_T$

- However, the effective length of the conductive channel is modulated by the applied  $V_{DS}$ , so

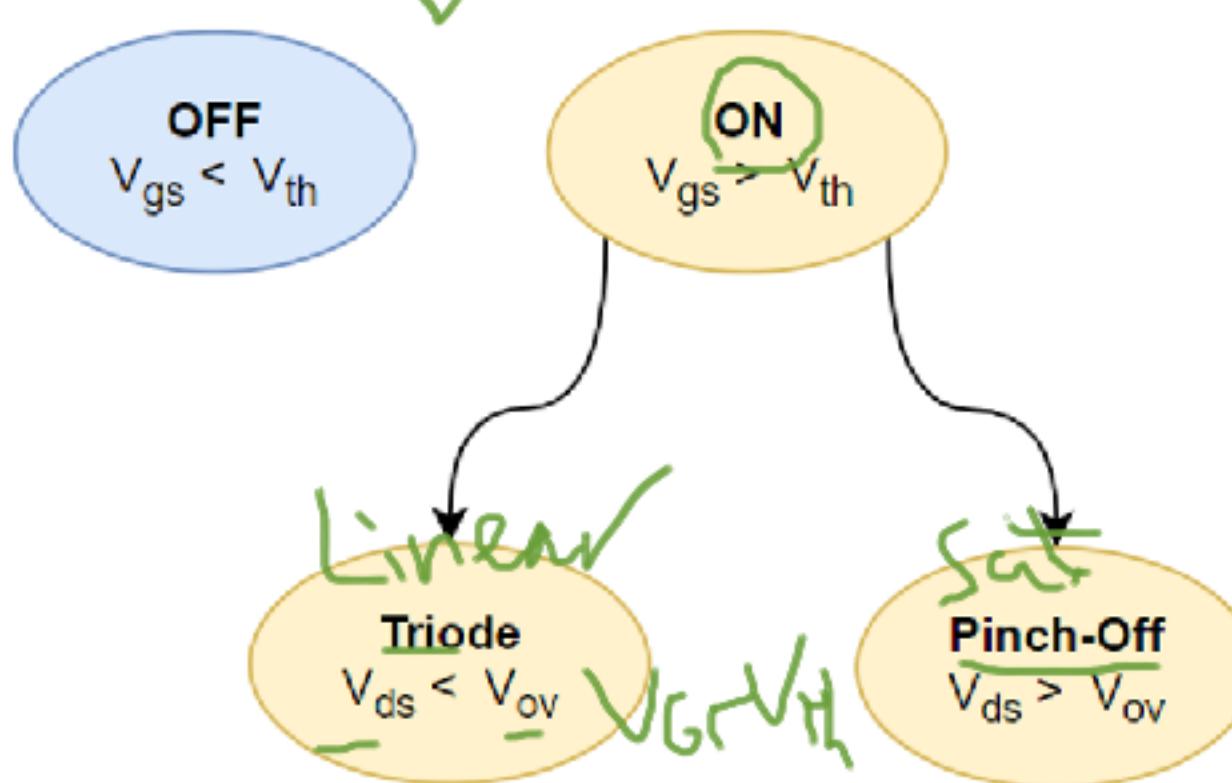
$$I_D = I_D' (1 + \lambda V_{DS})$$

where  $\lambda$  is the **channel-length modulation** (varies with the inverse of the **channel length**)

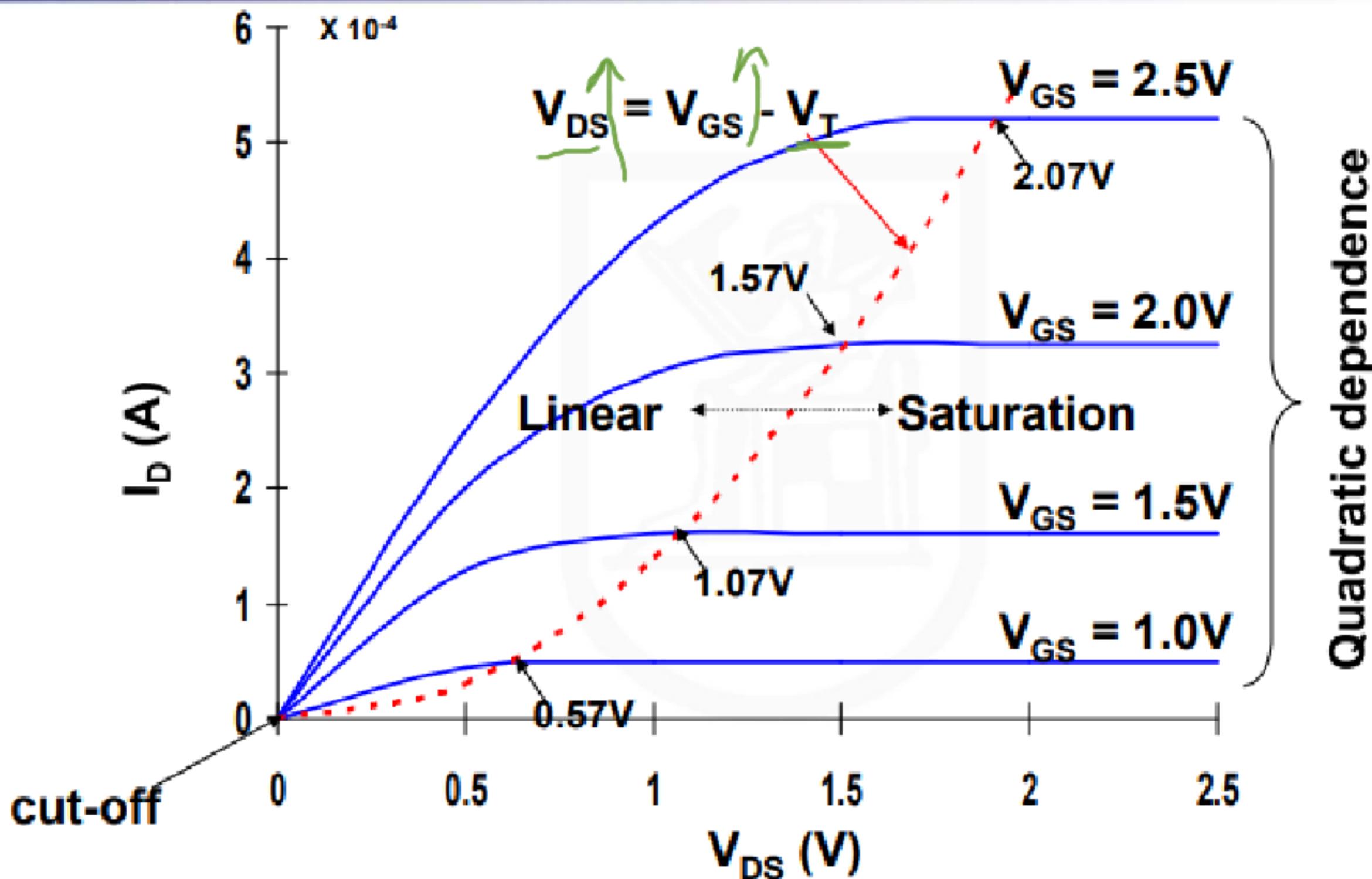
# Long Channel I-V Plot (NMOS)



NMOS transistor,  $0.25\mu m$ ,  $L_d = 10\mu m$ ,  $W/L = 1.5$ ,  $V_{DD} = 2.5V$ ,  $V_T = 0.43V$



# Long Channel I-V Plot (NMOS)



NMOS transistor,  $0.25\mu m$ ,  $L_d = 10\mu m$ ,  $W/L = 1.5$ ,  $V_{DD} = 2.5V$ ,  $V_T = 0.43V$

# Current Determinates

$I_D$

- For a fixed  $V_{DS}$  and  $V_{GS} (> V_T)$ ,  $I_{DS}$  is a function of
  - the distance between the source and drain –  $L$
  - the channel width –  $W$
  - the threshold voltage –  $V_T$
  - the thickness of the  $\text{SiO}_2$  –  $t_{\text{ox}}$
  - the dielectric of the gate insulator (e.g.,  $\text{SiO}_2$ ) –  $\epsilon_{\text{ox}}$
  - the carrier mobility
    - for n-fets:  $\mu_n = 500 \text{ cm}^2/\text{V}\cdot\text{sec}$
    - for p-fets:  $\mu_p = 180 \text{ cm}^2/\text{V}\cdot\text{sec}$

## Channel-Length Modulation - Short Channel Effects

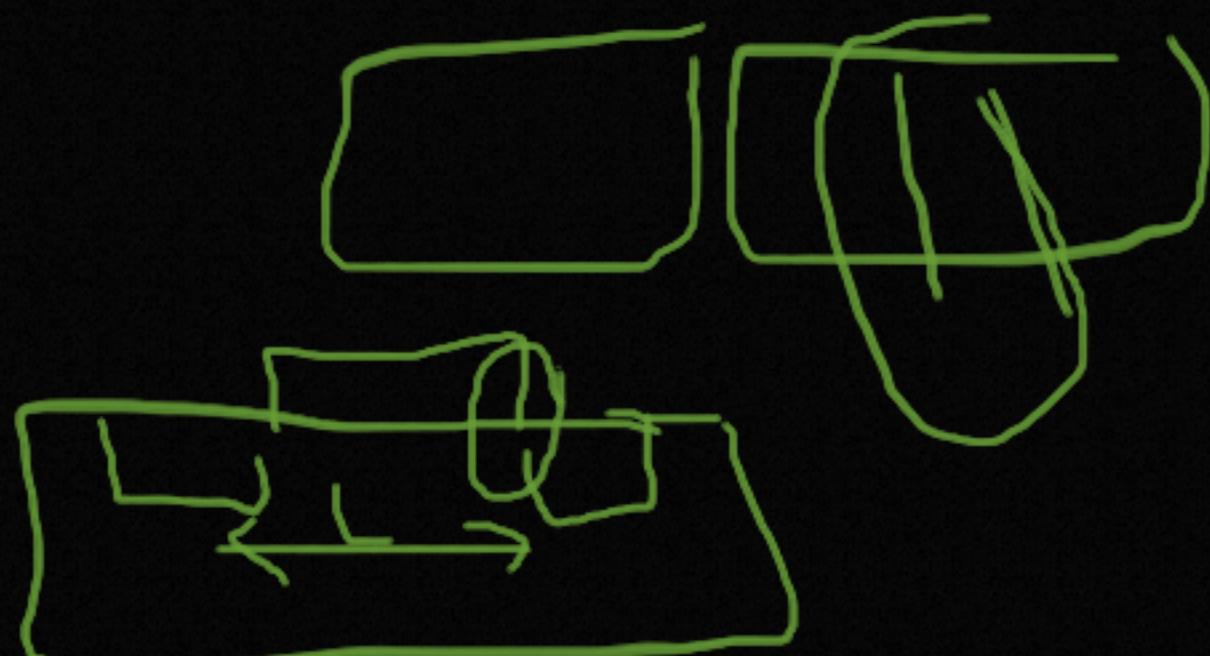
- The long channel transistor in the **saturation mode** acts as a perfect current source.
- This is not entirely correct. The effective length of the conductive channel is modulated by the applied  $V_{DS}$ . **increasing  $V_{DS}$  causes the depletion region at the drain to grow, reducing the length of the effective channel.**

$$I_D = \frac{k_n}{2} \frac{W}{L} (V_{GS} - V_T)^2$$

$$I_D = \frac{k_n}{2} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

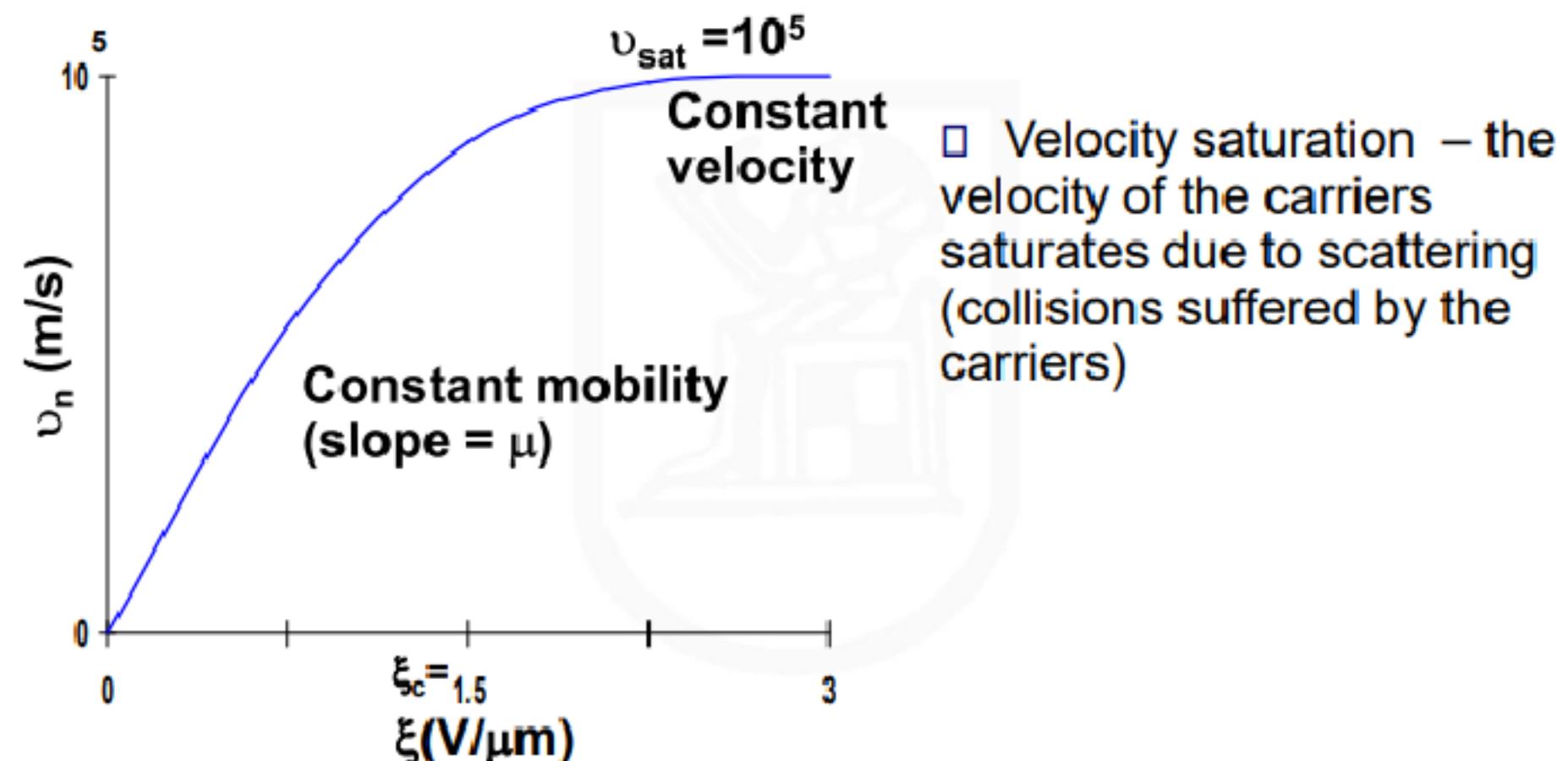
$\lambda$  is the channel-length modulation  $\propto 1/L$

In short channels, the drain-junction depletion region presents a larger fraction of the channel, and the channel-modulation effect is more pronounced. **That's why long channel transistors are used when high-impedance current sources are designed.**



## Short Channel Effects

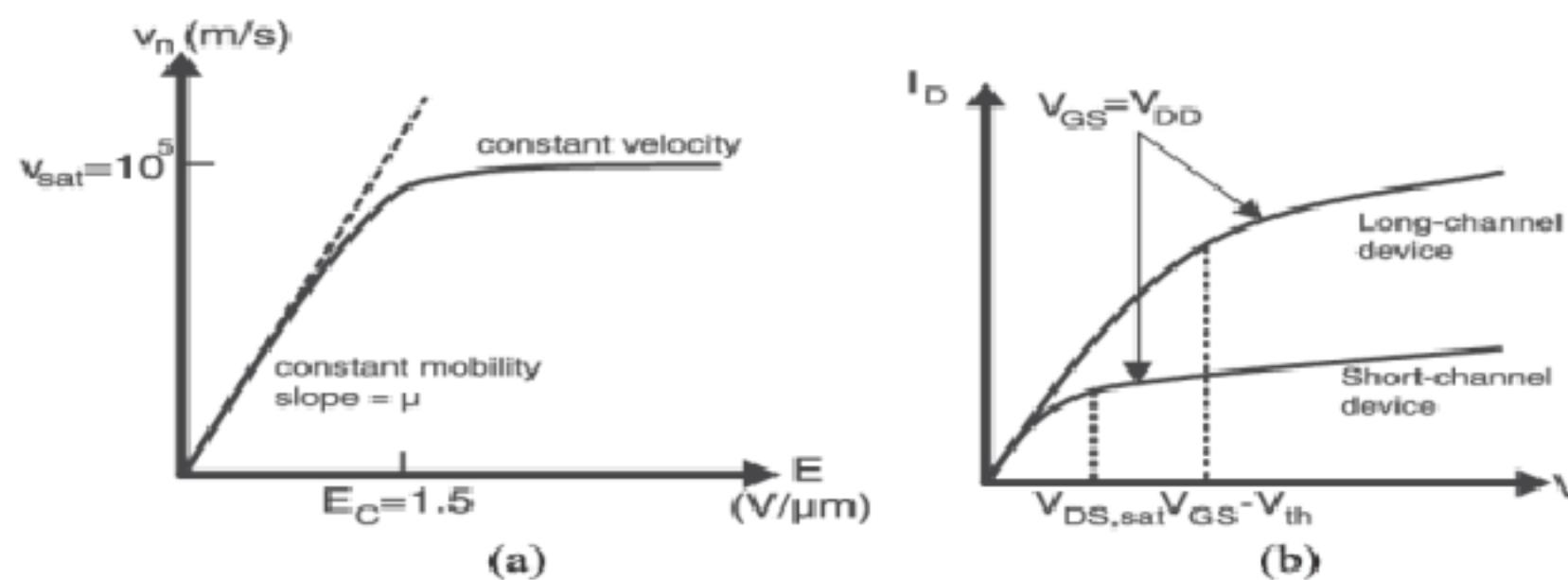
Behavior of short channel device mainly due to



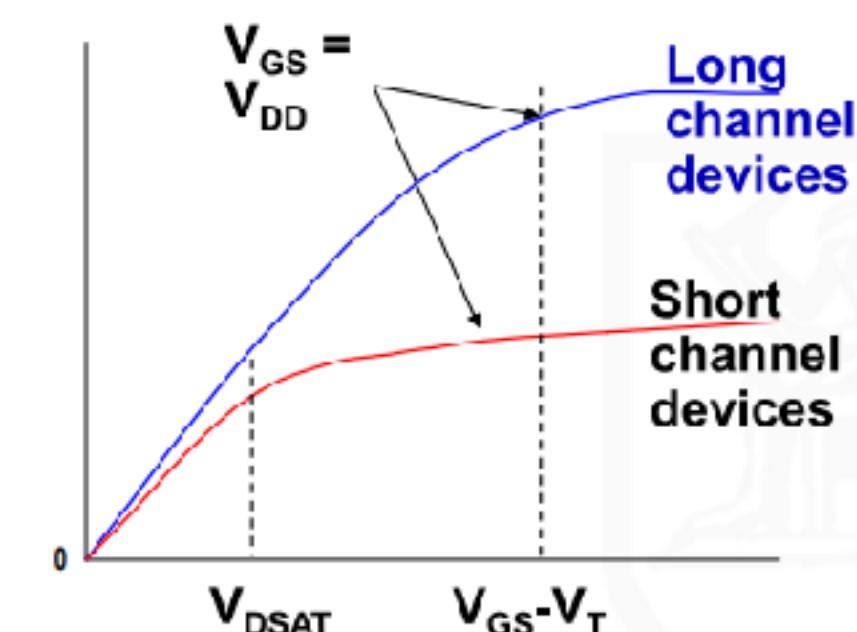
For an NMOS device with L of  $0.25\mu\text{m}$ , only a couple of volts difference between D and S are needed to reach velocity saturation

# Velocity Saturation

- The behavior of transistors with very short channel lengths (called *short-channel devices*) deviates considerably from the resistive and saturated models. The main culprit for this deficiency is the velocity saturation effect.
- Increasing the drain-source voltage does not yield more current, and the transistor current saturates at  $I_{DSAT}$ . This leads to two observations:



## Velocity Saturation Effects



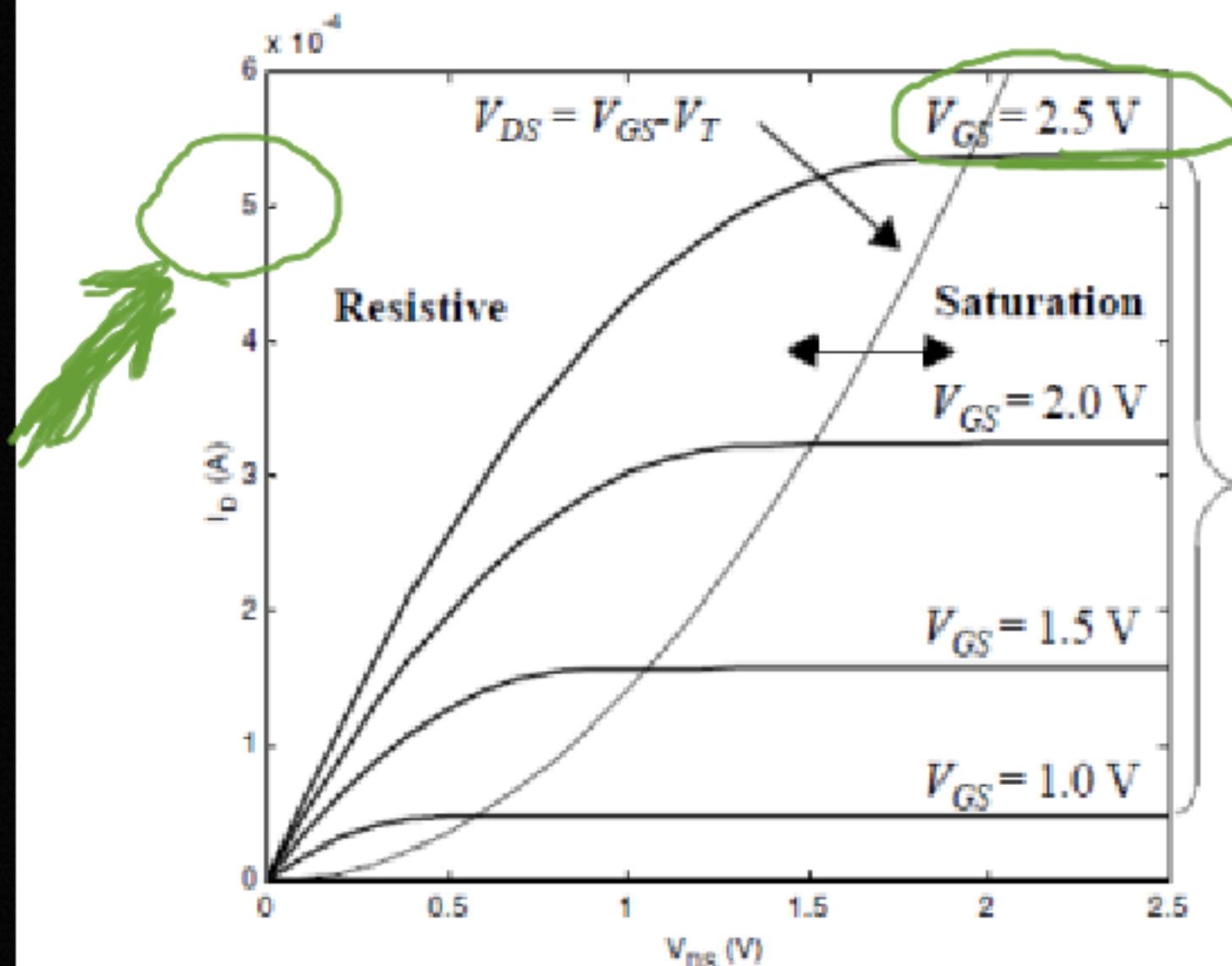
For short channel devices and large enough  $V_{GS} - V_T$

$V_{DSAT} < V_{GS} - V_T$  so the device enters saturation before  $V_{DS}$  reaches  $V_{GS} - V_T$  and operates more often in saturation

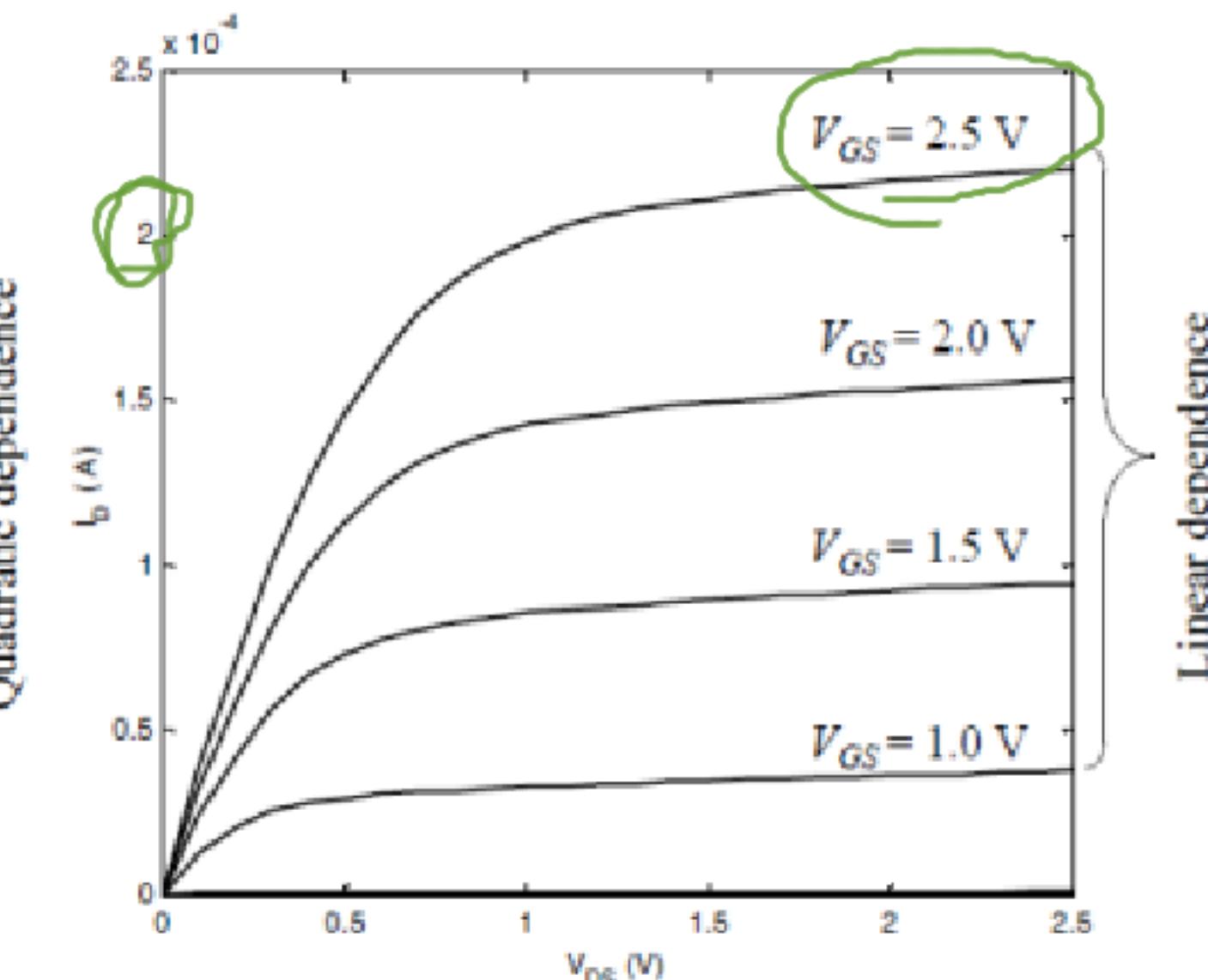
- $I_{DSAT}$  has a linear dependence w.r.t.  $V_{GS}$  so a reduced amount of current is delivered for a given control voltage

# Velocity Saturation in Short channel device

- Same technology and identical W/L ratio

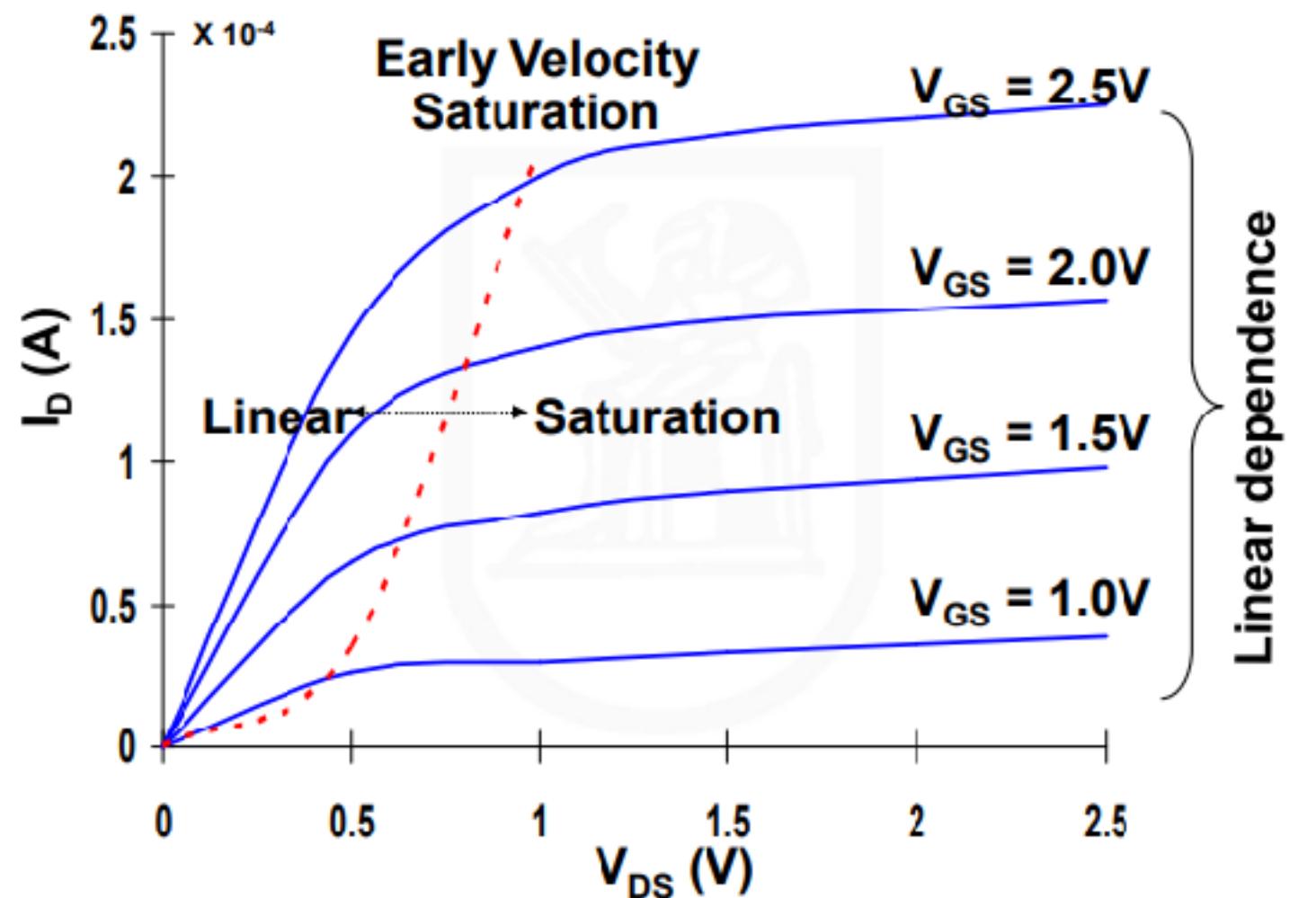


(a) Long-channel transistor ( $L_d = 10 \mu\text{m}$ )



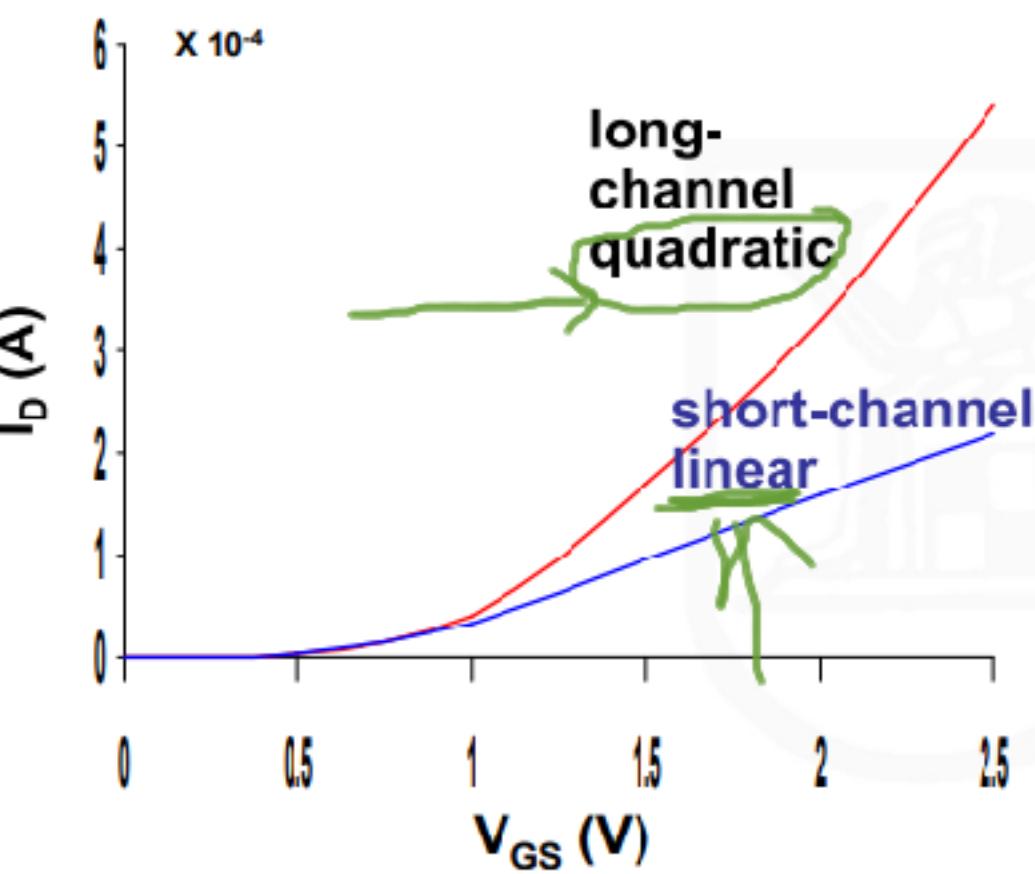
(b) Short-channel transistor ( $L_d = 0.25 \mu\text{m}$ )

# Short Channel I-V Plot (NMOS)



NMOS transistor, 0.25um,  $L_d$  = 0.25um, W/L = 1.5,  $V_{DD}$  = 2.5V,  $V_T$  = 0.43V

## MOS $I_D$ - $V_{GS}$ Characteristics



(for  $V_{DS}$  = 2.5V, W/L = 1.5)

- Linear (short-channel) versus quadratic (long-channel) dependence of  $I_D$  on  $V_{GS}$  in saturation
- Velocity-saturation causes the short-channel device to saturate at substantially smaller values of  $V_{DS}$  resulting in a substantial drop in current drive

# Other (Submicon) MOS Transistor Concerns

- Velocity saturation
- Sub-threshold conduction (aka weak inversion)
  - Transistor is already partially conducting for voltages below  $V_T$
- Threshold variations
  - In long-channel devices, the threshold is a function of the length (for low  $V_{DS}$ )
  - In short-channel devices, there is a drain-induced threshold barrier lowering (DIBL) at the upper end of the  $V_{DS}$  range (for small L)
- Parasitic resistances
  - resistances associated with the source and drain contacts
- Latch-up

