CENTER OF NANOELECTRONICS & DEVICES

CND 121: Introduction to Silicon Process & VLSI

Assignment #: 2

Section #: 16

Submitted by:

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Date: 5/10/2023

1. CMOS Buffer

i. Add screenshot from your **schematic:**

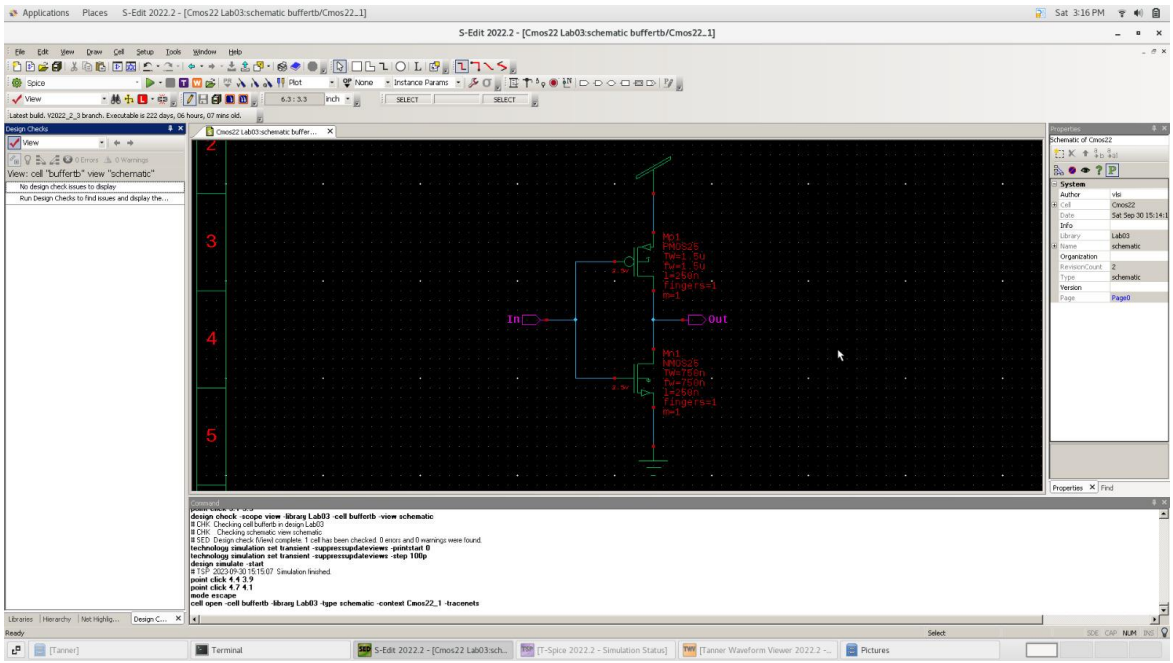


Figure 1 CMOS Inverter

We forgot to take a screenshot of buffer (it is 2 CMOS inverter symbols connected in series) due to our focusing to solve the bonus but there are some issues that we faced and can not solve the bonus (please, consider this in your grade and Thanks for your attention).

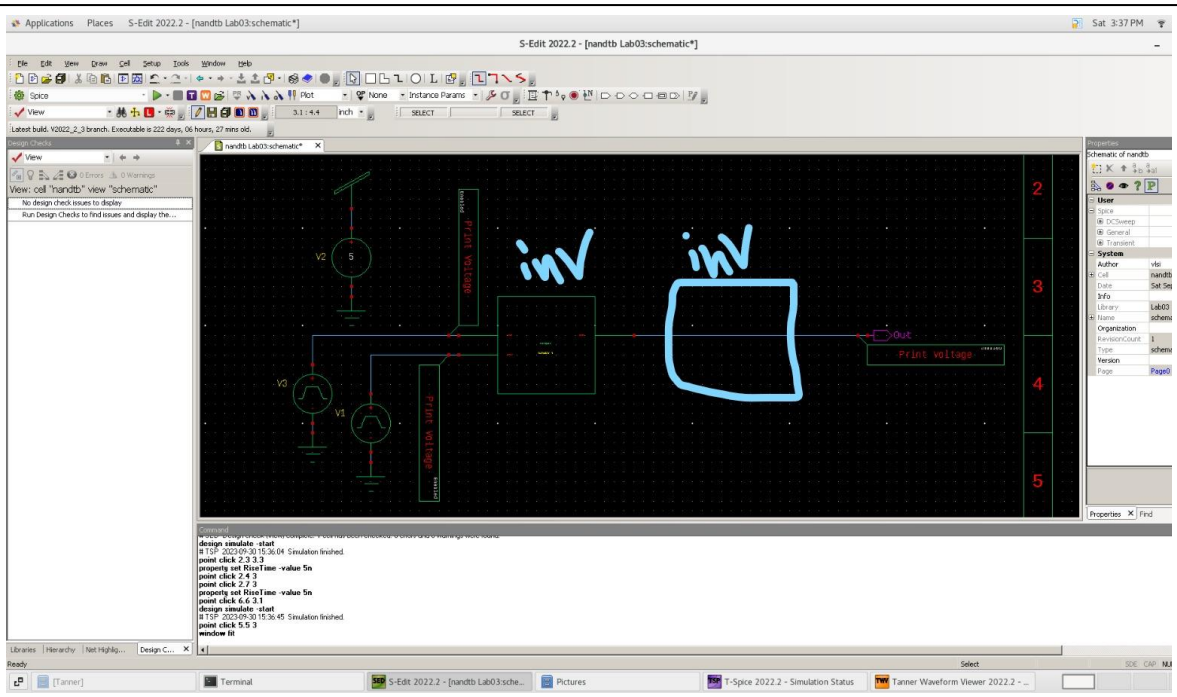
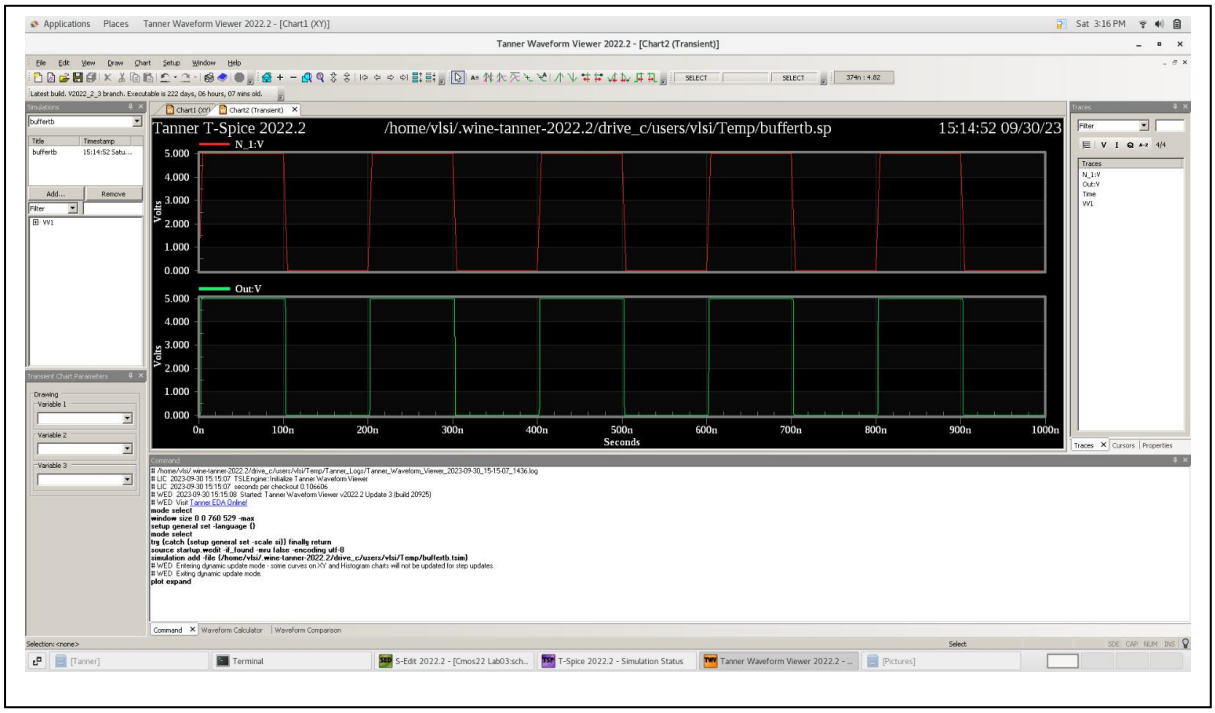


Figure 2CMOS Buffer

ii. Add screenshot from your waveform viewer:



iii. **Comment** on the results:

1- The input signal is applied to the gates of both the PMOS and NMOS transistors, controlling their conduction and determining the output state.

2- The well-designed layout ensures a symmetrical and efficient operation of the CMOS buffer, minimizing power consumption and delay.

3- As the input rises, the PMOS transistor begins to turn off, while the NMOS transistor turns on, pulling the output (Vout) towards ground.

4- The transition period, represented by the rising edge, shows the delay introduced by the CMOS buffer, which is typically minimal.

5- Once the input signal reaches a high level, the output stabilizes at a low logic state, indicating successful signal buffering.

6- Similarly, if the input transitions from high to low, the CMOS buffer will pull the output from low to high, maintaining signal integrity.

7- The waveform illustrates the complementary operation of the PMOS and NMOS transistors, ensuring a robust and noise-immune signal transmission.

8- The transition times and signal levels are consistent with the specifications of a CMOS buffer, demonstrating its ability to maintain logic levels while minimizing propagation delay.

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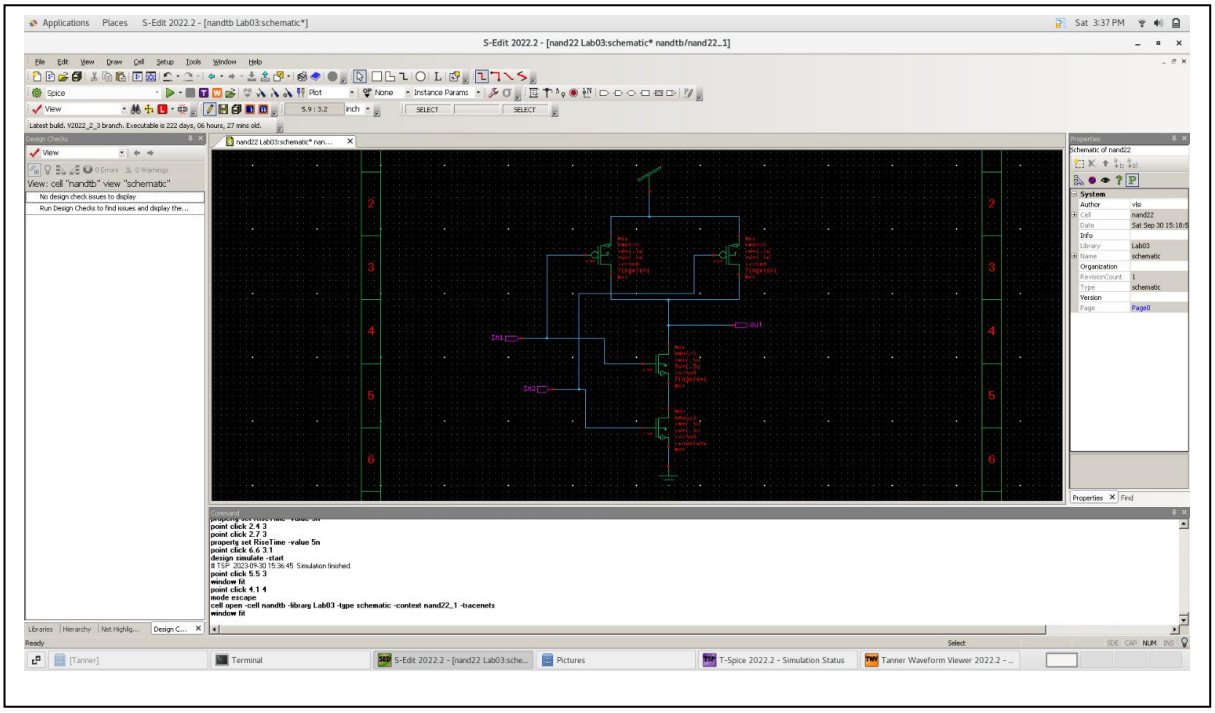
2. CMOS NAND

i. Add screenshot from your **schematic:**



ii. Add screenshot from your waveform viewer**:**

iii. **Comment** on the results:

1- NAND gate produces a low output only when all of its inputs are high.

2- The NAND gate is implemented using two parallel-connected transistors: a PMOS transistor for the pull-up network and an NMOS transistor for the pull-down network.

3- The output is low (logic 0) when all inputs are high (logic 1), and it goes high (logic 1) when any input is low.

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