CENTER OF NANOELECTRONICS & DEVICES

# CND 121: Introduction to Silicon Process & VLSI

## Assignment #: 5

## Section #: 16

**Submitted by:**


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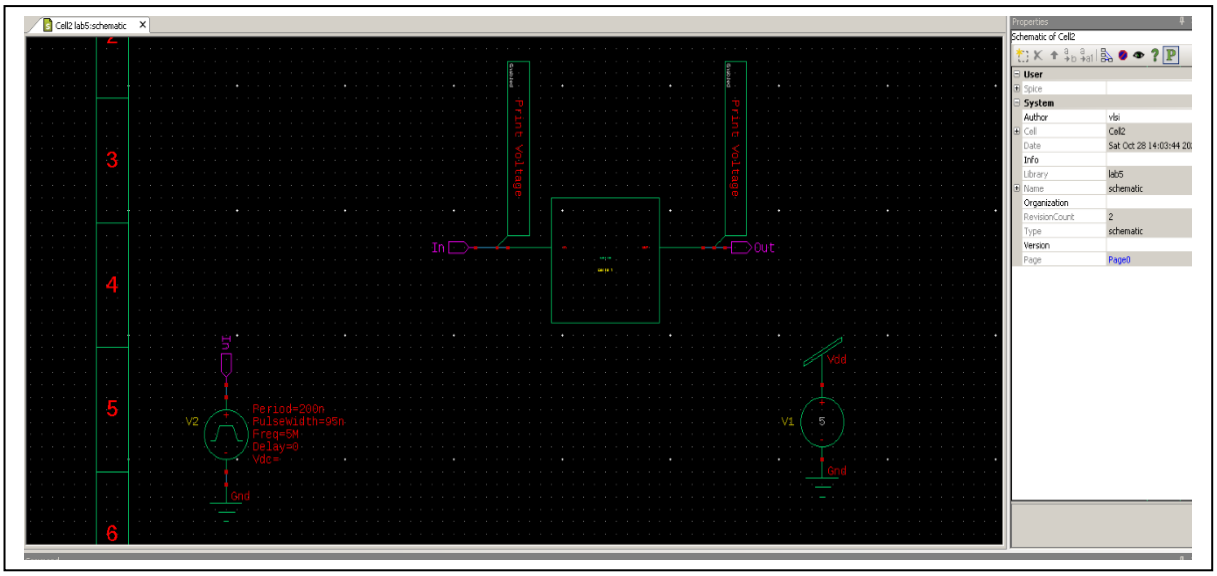
**Submitted to TA: Mariam Taher**

**Date: 9/11/2023**

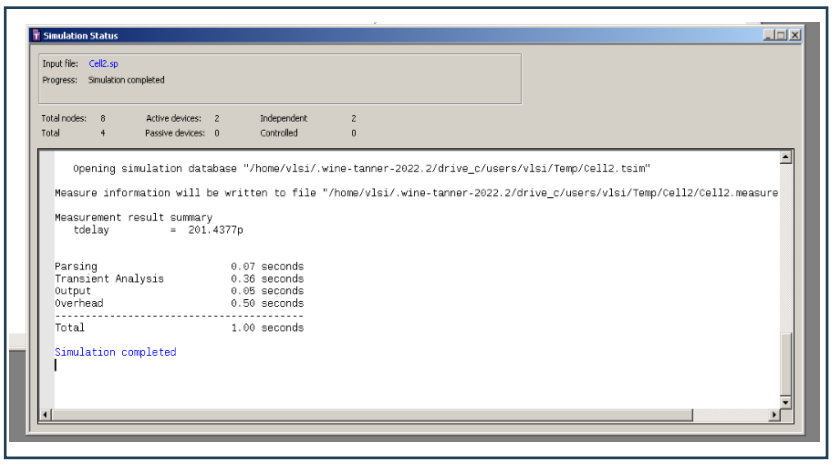
# 1. Frontend flow

i. Add screenshot from your **schematic:**



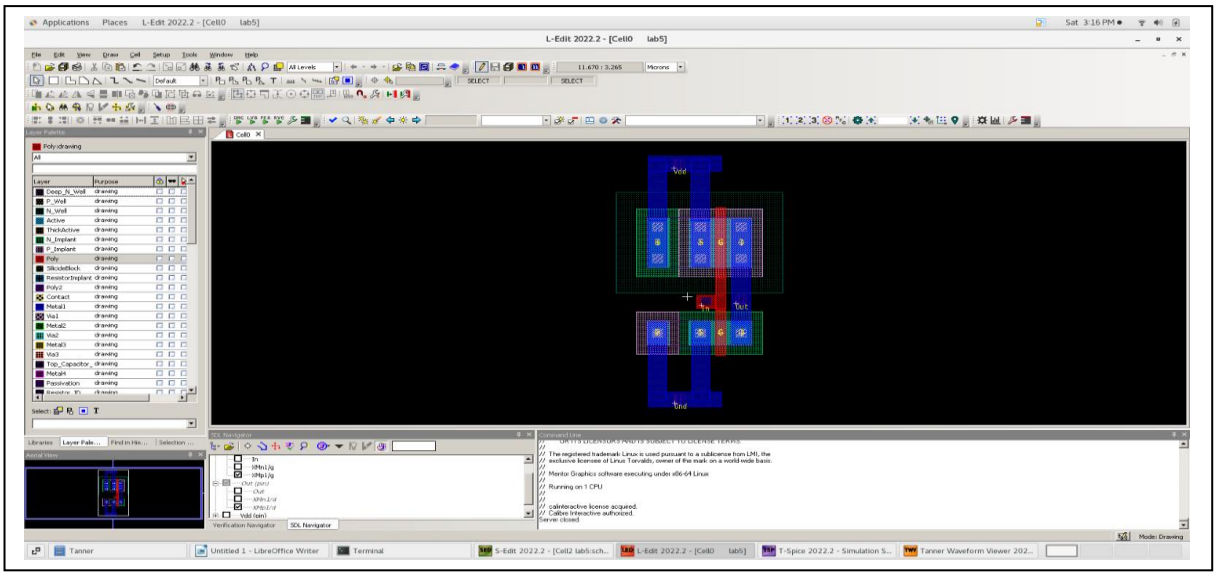

ii. Add screenshot from your **testbench:**


iii. Propagation delay = **201.4371psec**

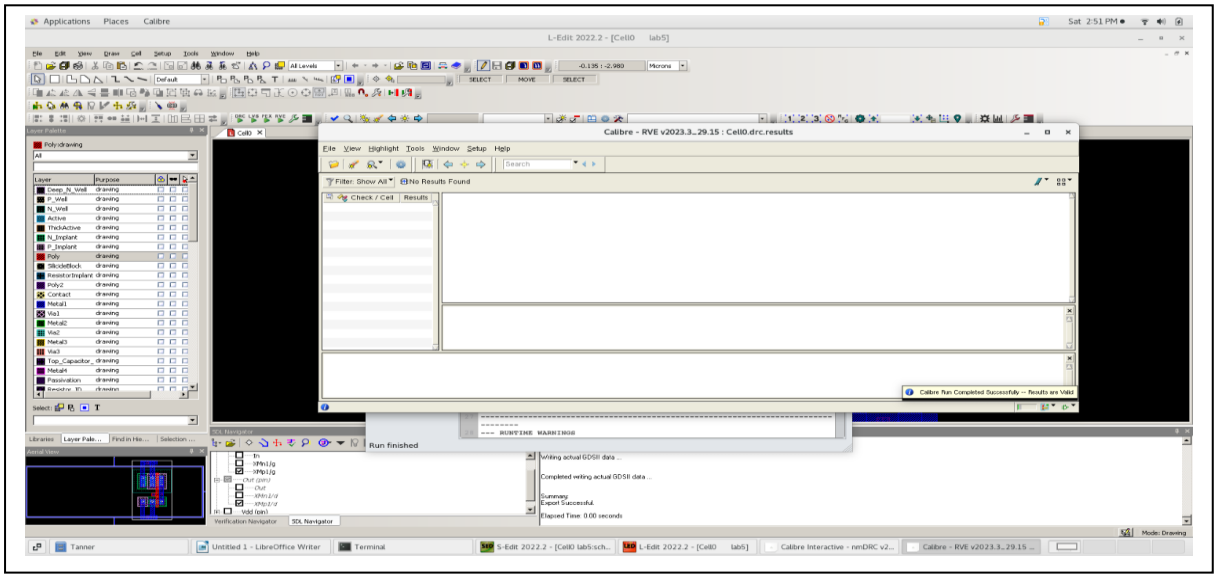


# 2. Backend flow

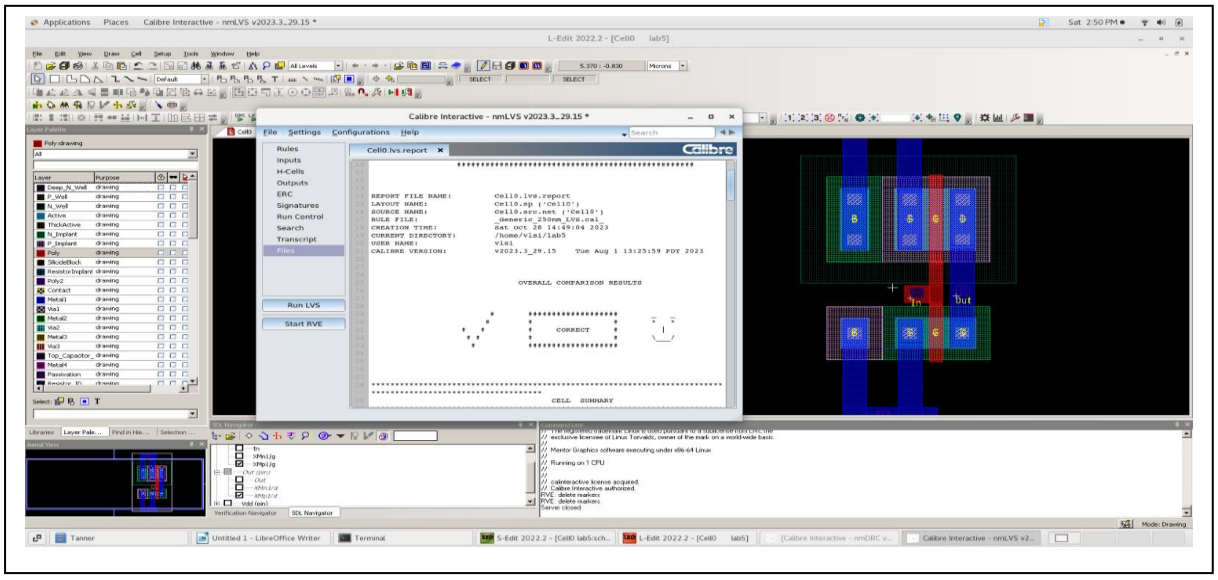
i. Add screenshot from your **Layout**:



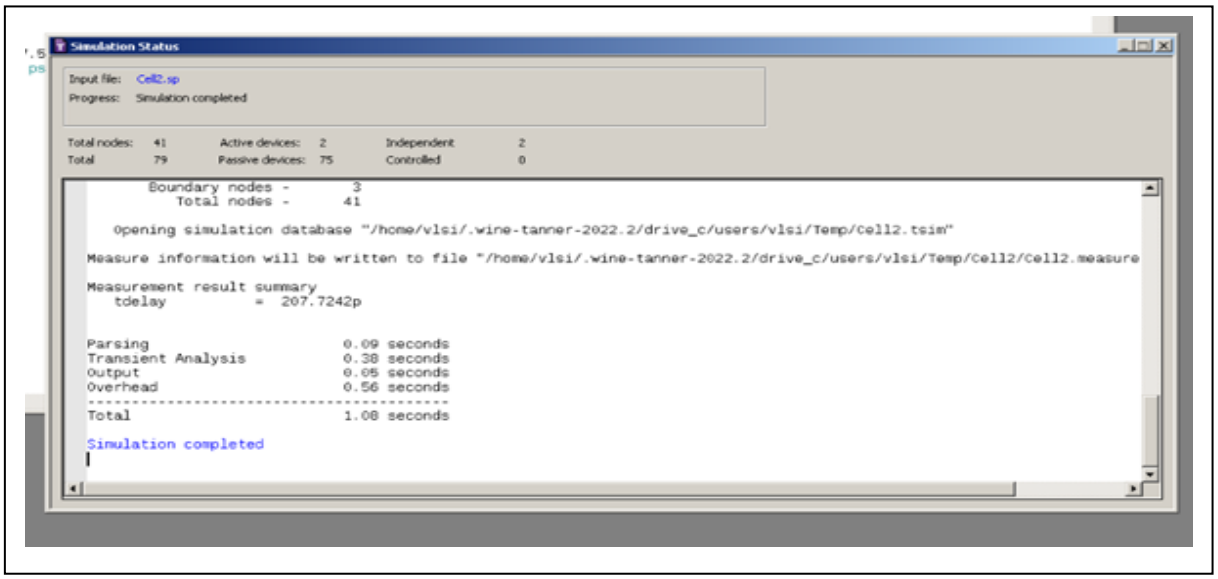
ii. Add screenshot after finishing **DRC** to grantee that no errors:



iii. Add screenshot after finishing **LVS** to grantee that your design is matched:




iv. Propagation delay after post layout simulation = **207.7242psec**



## 3. Describe the all flow steps in brief:

1. Develop a design for an inverter.
2. Generate a symbol to represent the inverter.
3. Perform a simulation of the designed circuit.
4. Create the layout for the circuit and configure the Calibre setup.
5. Set up Design Rule Checking (DRC) to ensure error-free design.
6. Set up Layout versus Schematic (LVS) to verify design consistency.
7. Configure the extraction setup and execute the PEX (Parasitic Extraction) process.