CENTER OF NANOELECTRONICS & DEVICES

CND 121: Introduction to Silicon Process & VLSI

Assignment #: 3

Section #: 16

Submitted by:

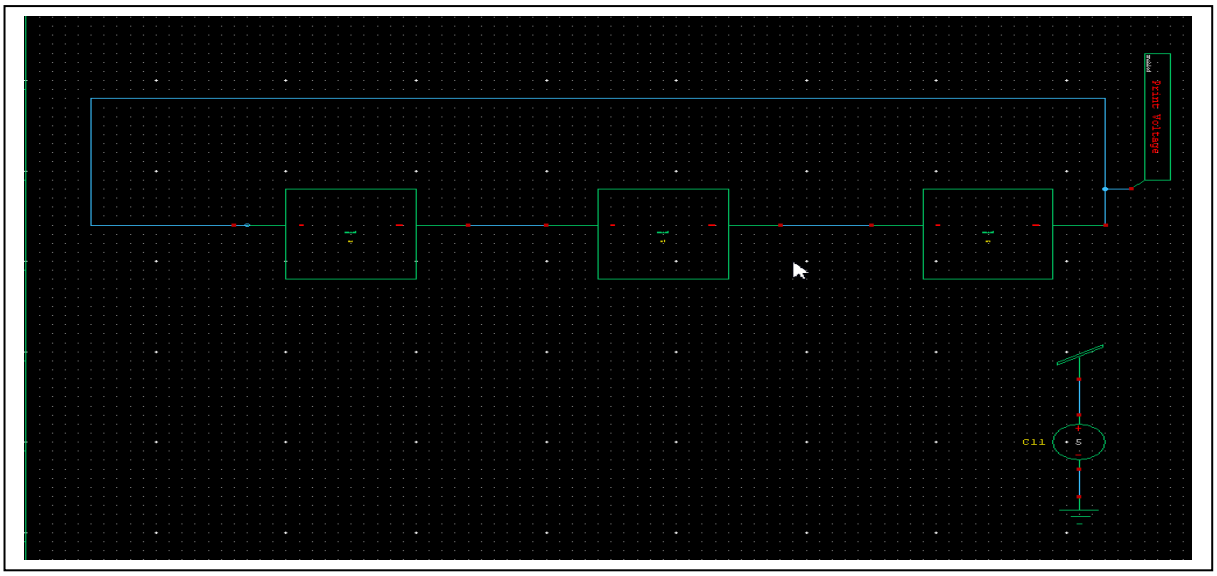
Student Name	ID
Aya Ahmed Abdelrahman	V23010284
Karim Mahmoud Kamal	V23010174
Nada Abdelkader Sharaf	V23010519
Kholoud Rafat	V23010199

Submitted to TA: Mariam Taher

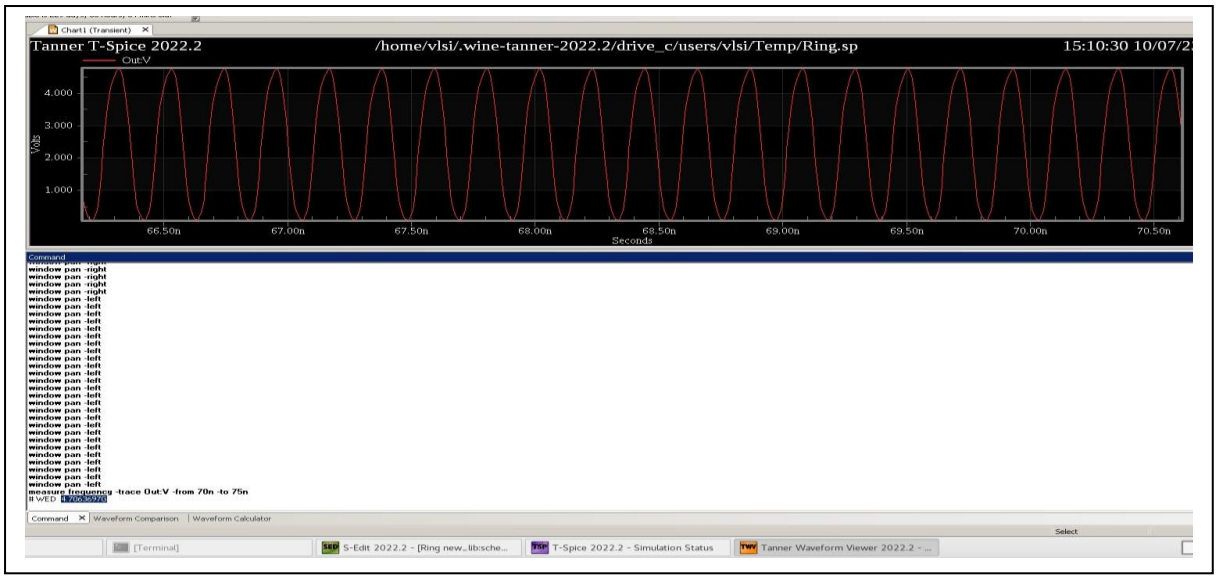
Date: 8/10/2023

1. Ring Oscillator

i. Add screenshot from your **schematic**:

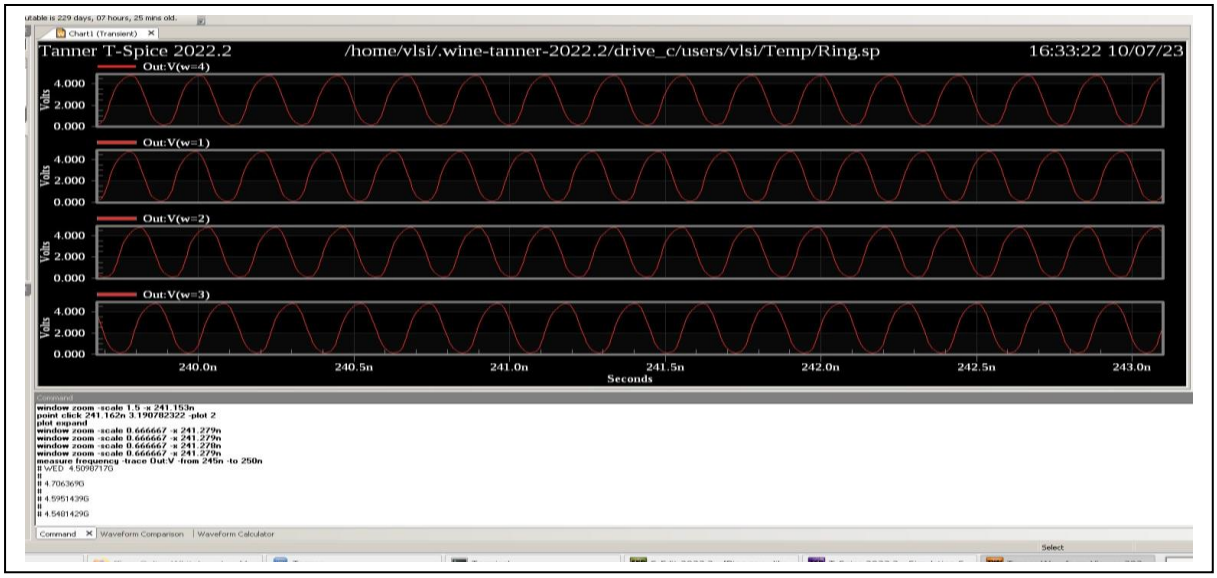


ii. Add screenshot from your waveform viewer:

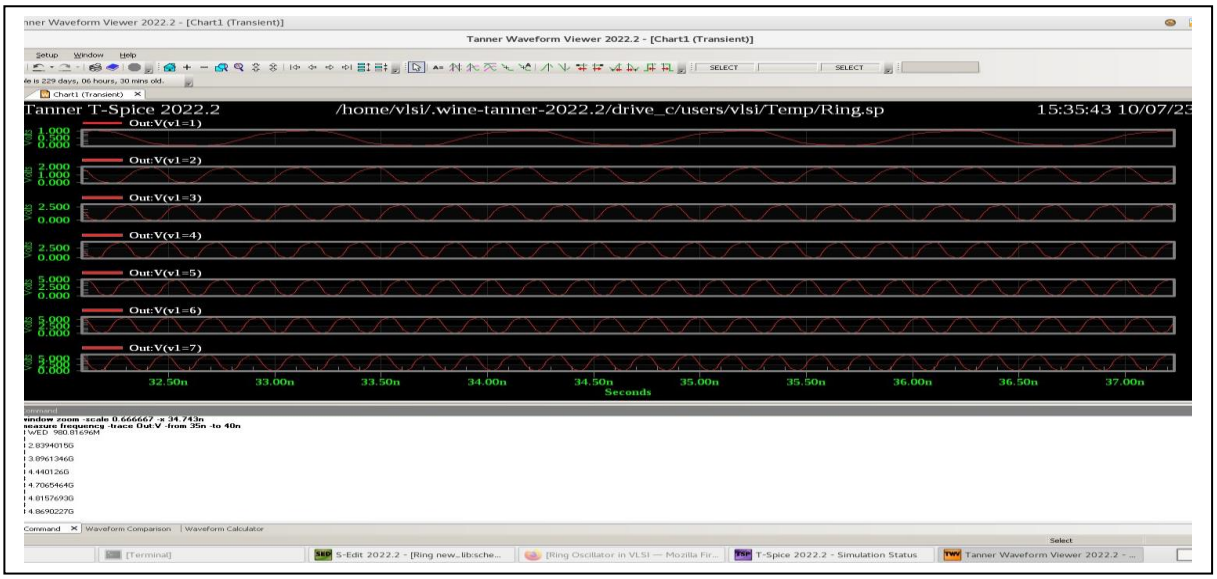


iii. Frequency = 4.706GHz

iv. Analyze the effect of changing the transistors width over Frequency?

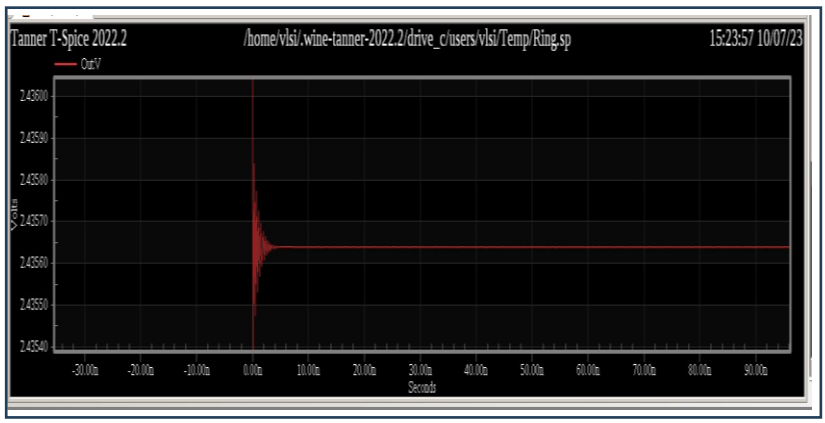


v. Analyze the effect of changing the Vdd over Frequency?



vi. Do you think that the single stage ring oscillator will work? Give an explanation of your answer.

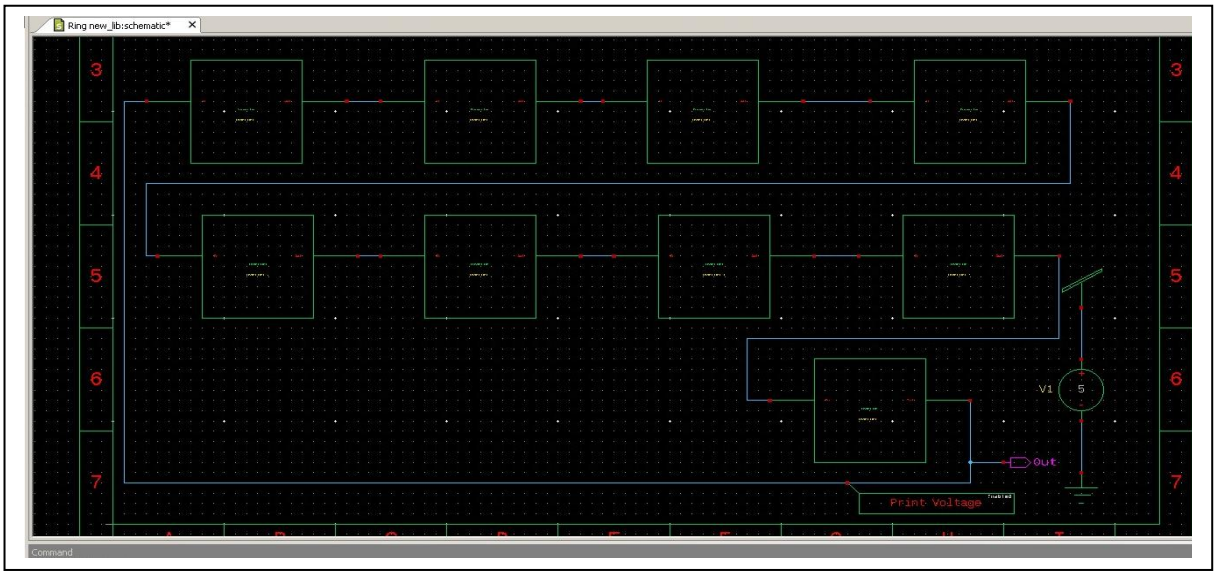
Now one stage ring oscillator won't oscillate as shown in the figure that after a specific time the signal amplitude will damp. According to Barkhausen's criteria, for oscillation the feedback should



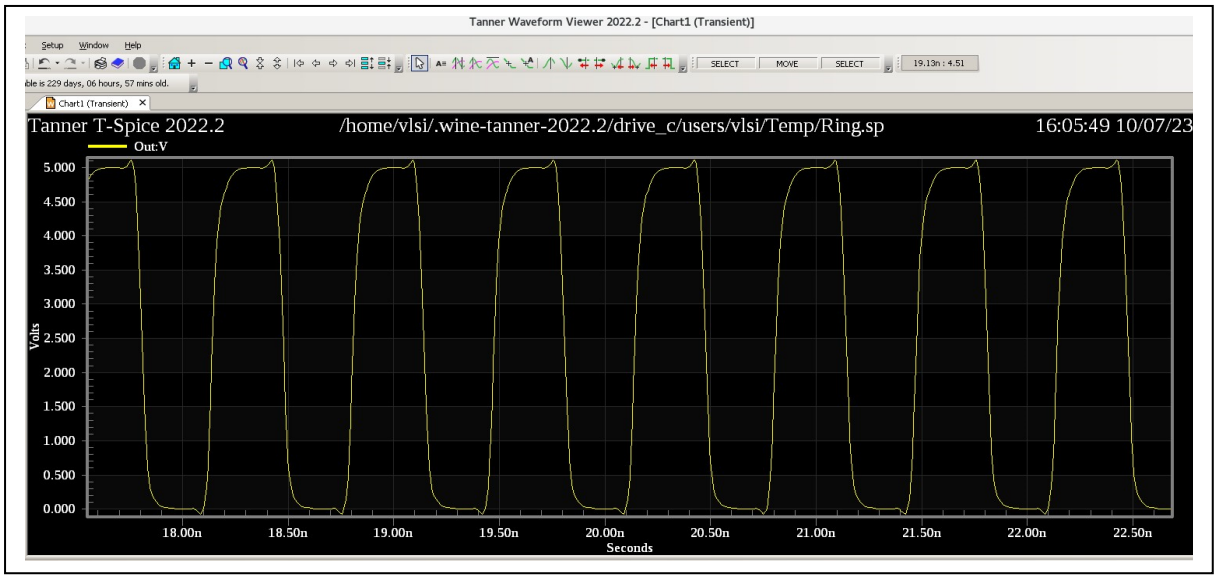
be made after phase difference of 2pi, and gain must be >=1.So, a single inverter generally does not have enough delay to oscillate; instead, it drives itself to an intermediate analog state.

2. Square Wave

i. Add screenshot from your **schematic**:

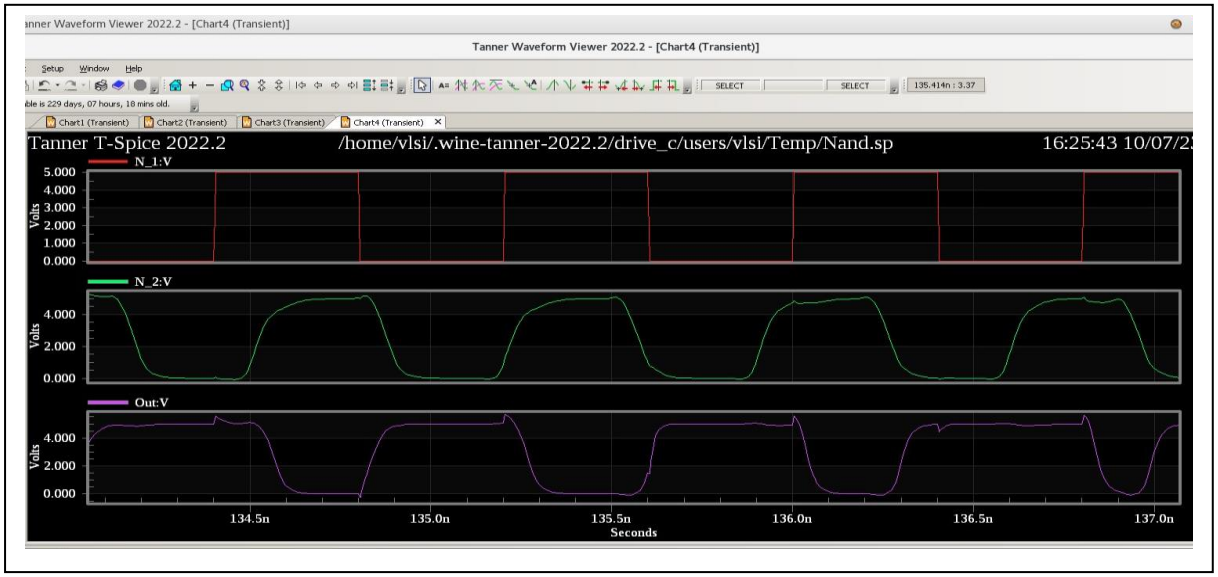


ii. Add screenshot from your waveform viewer:



iii. Number of stages used =9 stages.

iv. Apply your square wave into a NAND gate and explain the output waveform.

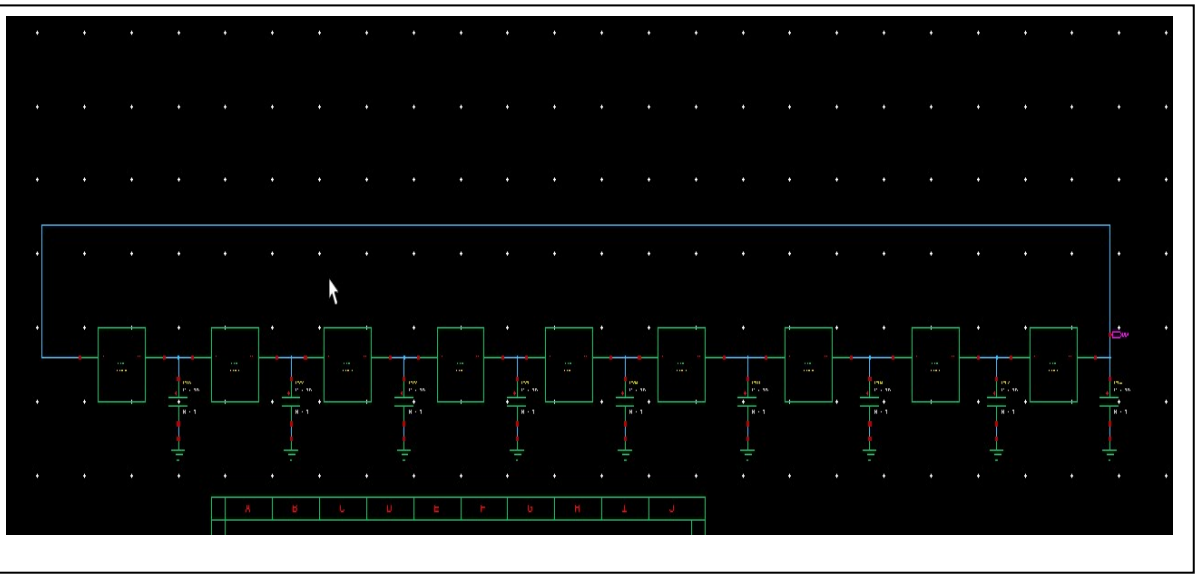


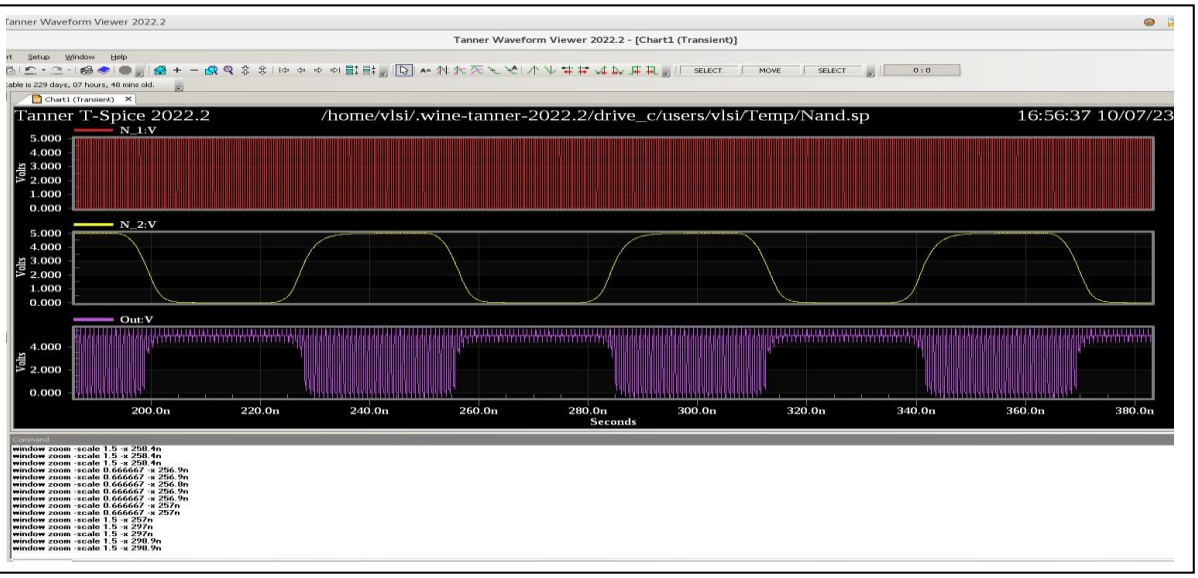
Explaination?

As shown from the above 2 figures when we apply a square wave voltage source on a terminal of NAND and on the other terminal the square wave oscillator, we designed the when the input voltage is (VDD, 0) or (0, VDD) or (0,0) the output will be VDD and when the input is (VDD, VDD) the output will be zero which is expected. Because of different periods of the 2 inputs the output will have glitches, but the NAND will give us clear zero and VDD not like the input to it.

3. BONUS

i. Try to smooth your output.

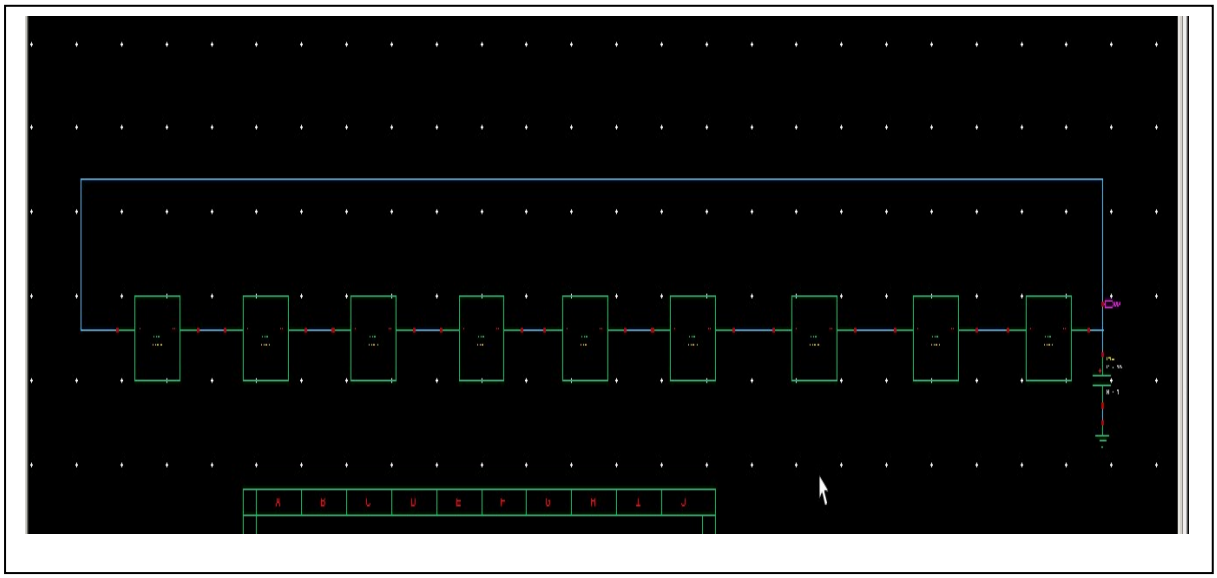


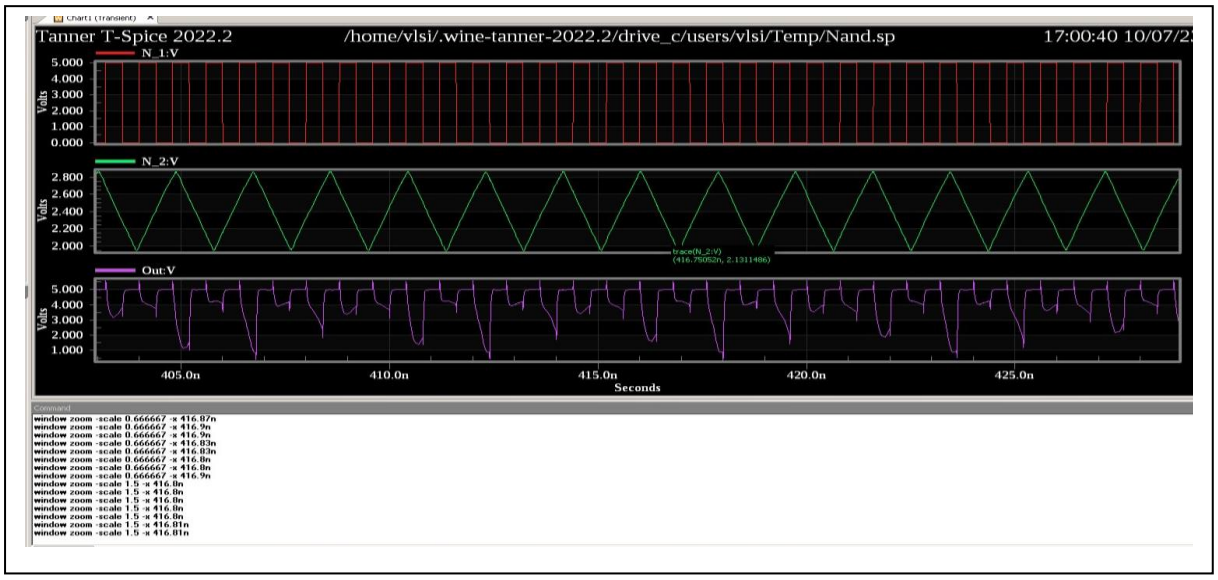


Explaination?

As shown in the above figures, when we add a capacitor to each inverter stage the capacitor will help to smooth the output signal as the ring oscillator works on the principle of capacitive delay switching of the transistor. There is a time delay from the time signal is applied to the gate terminal and the transistor turning on. This time delay is caused by capacitance that exists between the gate and the source. The parasitic capacitor is formed by an oxide layer (dielectric) between the gate and the source and the drain. The period is needed to charge the parasitic capacitor after which it turns on the transistor.so when we use added capacitor, it helps to charge and discharge the signal with more delay so signal results will be smoother with no spikes.

i. Triangle Wave





Explaination?

As shown in the above figures, when we use a capacitor in the final stage it integrates the output signal to be triangle instead of square wave as when the capacitor charges or discharges, it accumulates charge proportional to the input signal voltage, so it will integrate square wave signal to be triangle wave.