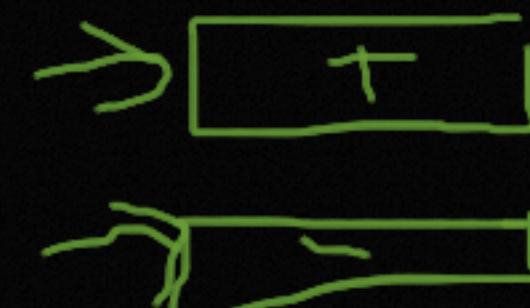


Technology Generations

- We refer to the smallest feature size or Critical Dimension (CD).
- 10um 5um 2um 1um 0.8um 0.5um 0.35um
0.25um 0.18um 0.13um 90nm 65nm 45nm 32nm
22nm
- Possible through the magic of device scaling
- Desirable due to manufacturing economics (wafer and batch processing)
- Usually limited by lithography, implies new patterning technology, equipment for each node. **\$\$\$\$\$**

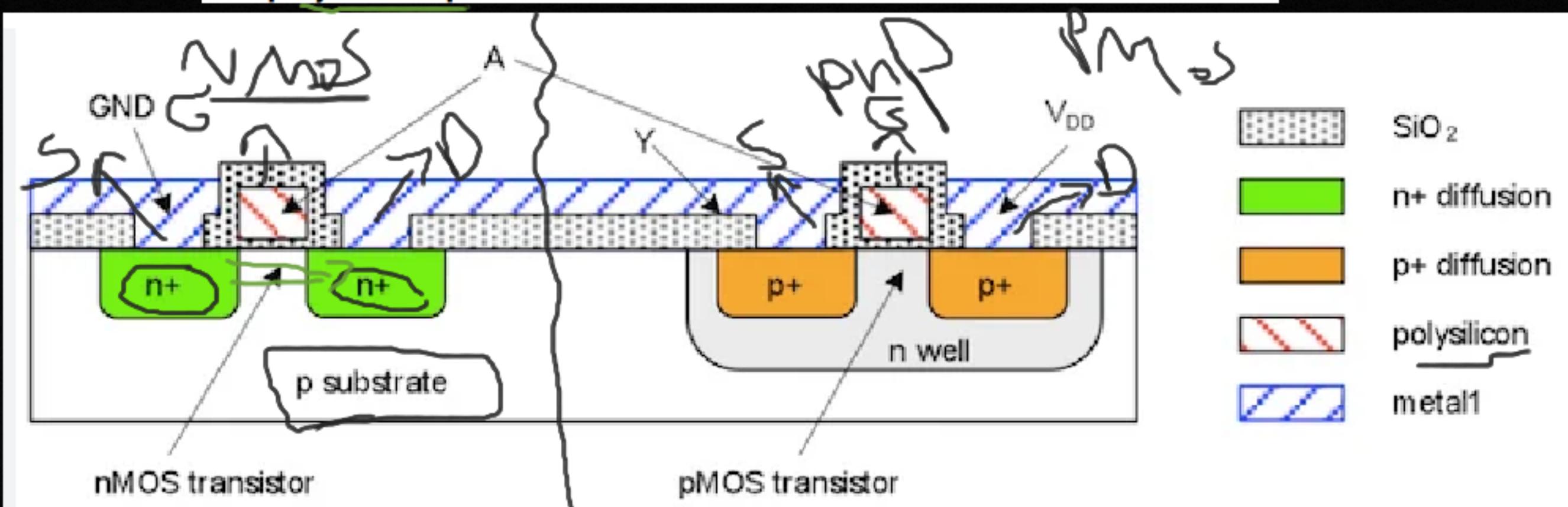
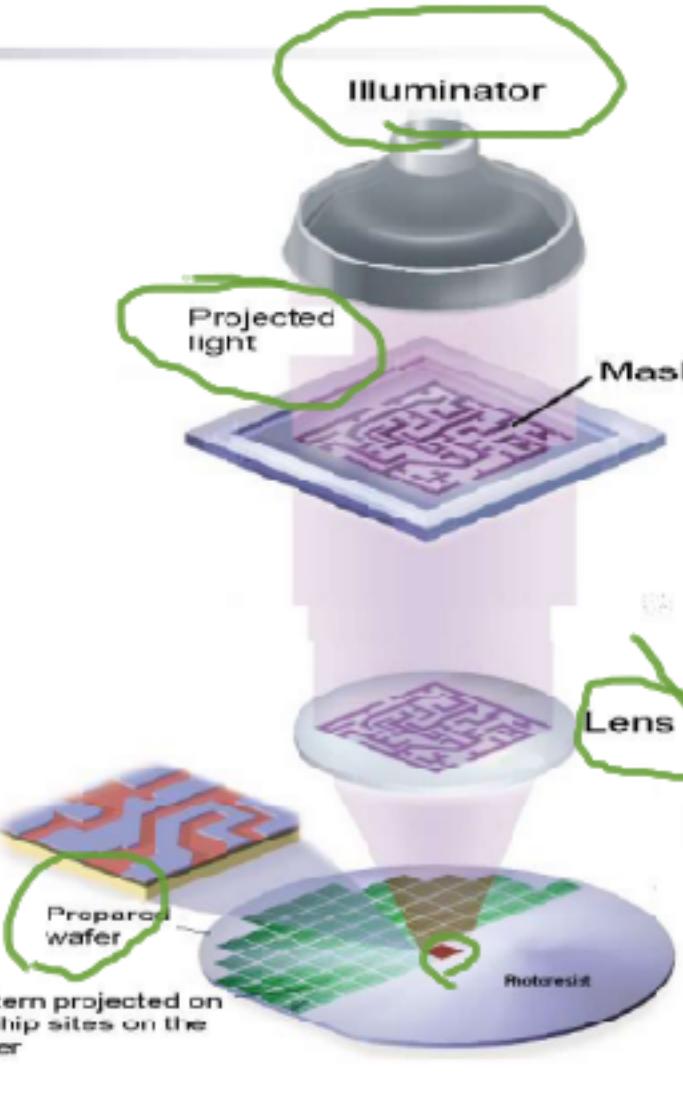
- Num. of transistors is not limiting factor
 - Currently ~1 billion transistors/chip
 - Problems:
 - Too much Power, Heat, Latency
 - Not enough Parallelism



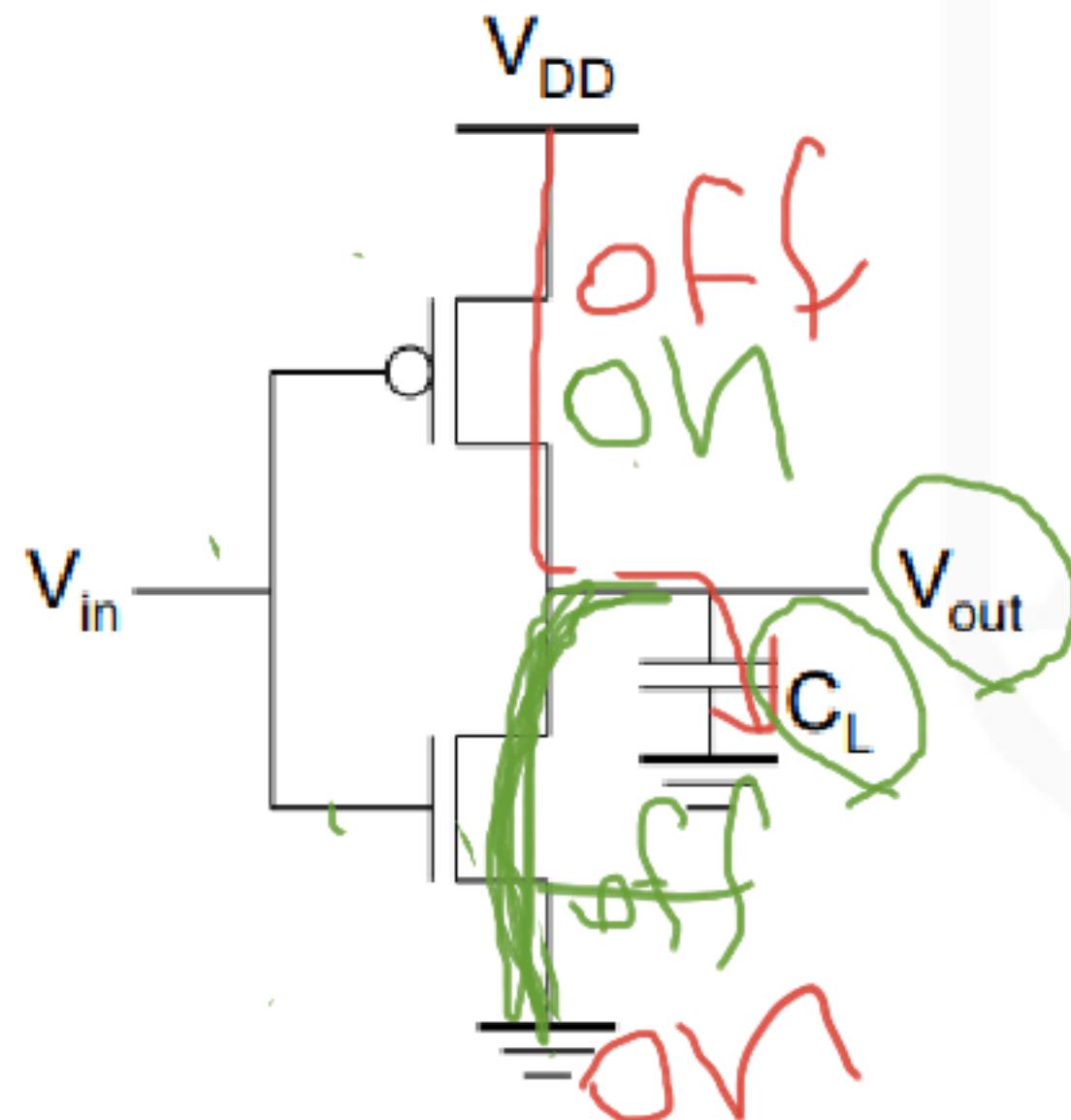
Critical Dimension

$$\text{CD} = P_{\min} / 2$$
$$= k_1 \cdot \lambda / \text{NA}$$

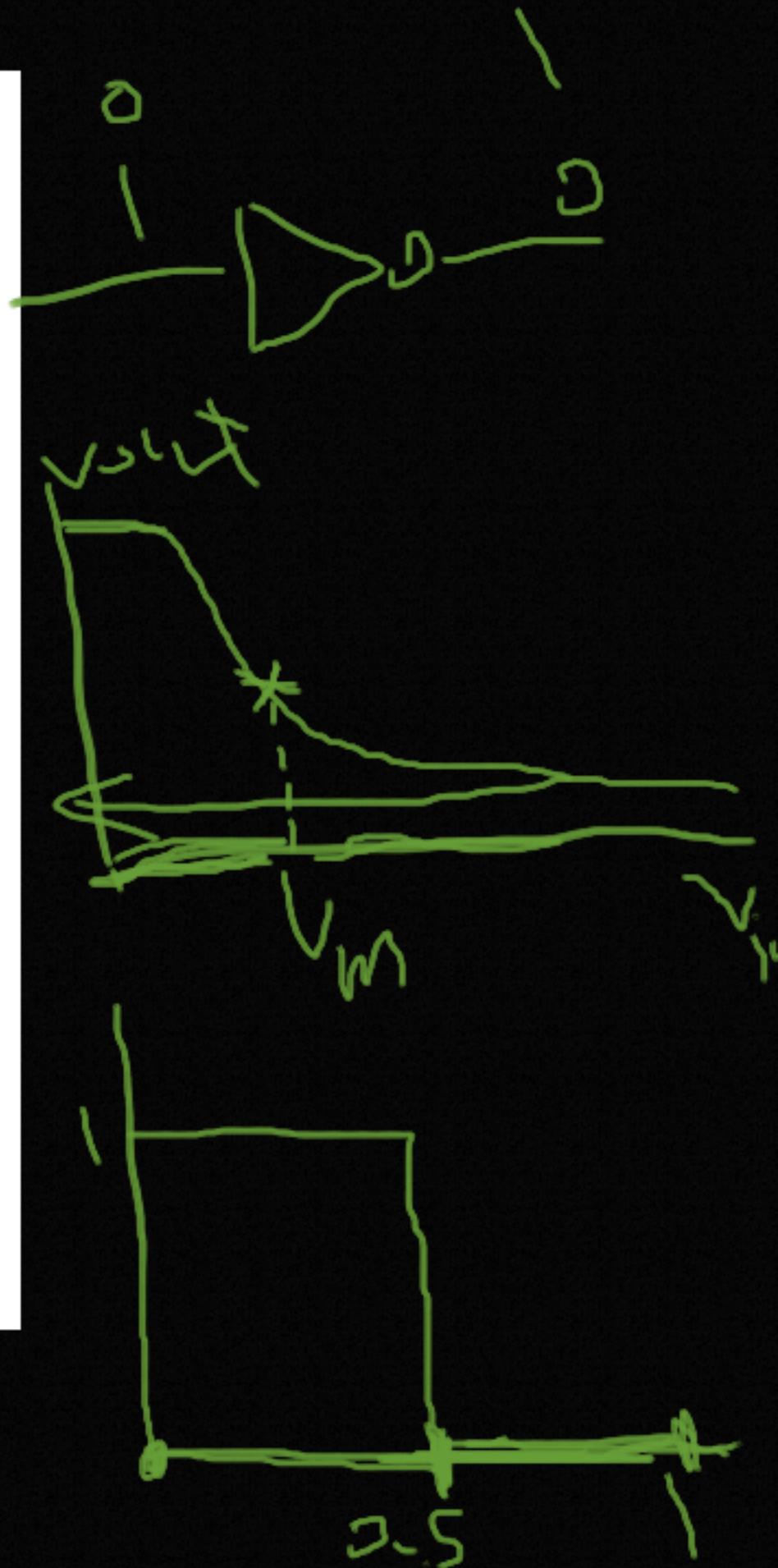
- CD is the critical dimension
- P_{min}/2 is the minimum half pitch
- k₁ is a process factor
- λ is the wavelength of the exposure light
- NA is the numerical aperture of the projection optics.



CMOS Inverter

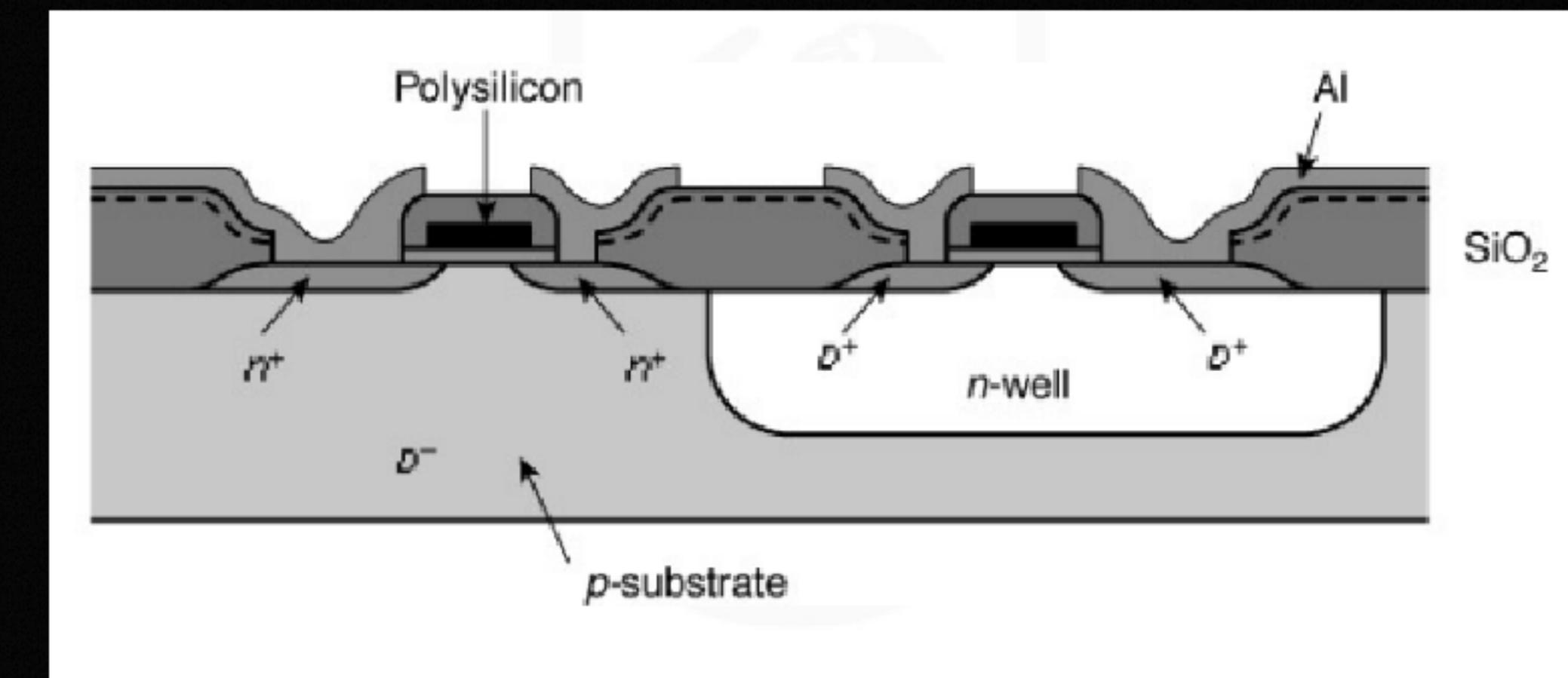


- Full rail-to-rail swing \Rightarrow high noise margins
- Low output impedance
- High input impedance
- No direct path steady-state between power and ground \Rightarrow no static power dissipation
- Propagation delay a function of load capacitance and on resistance of transistors

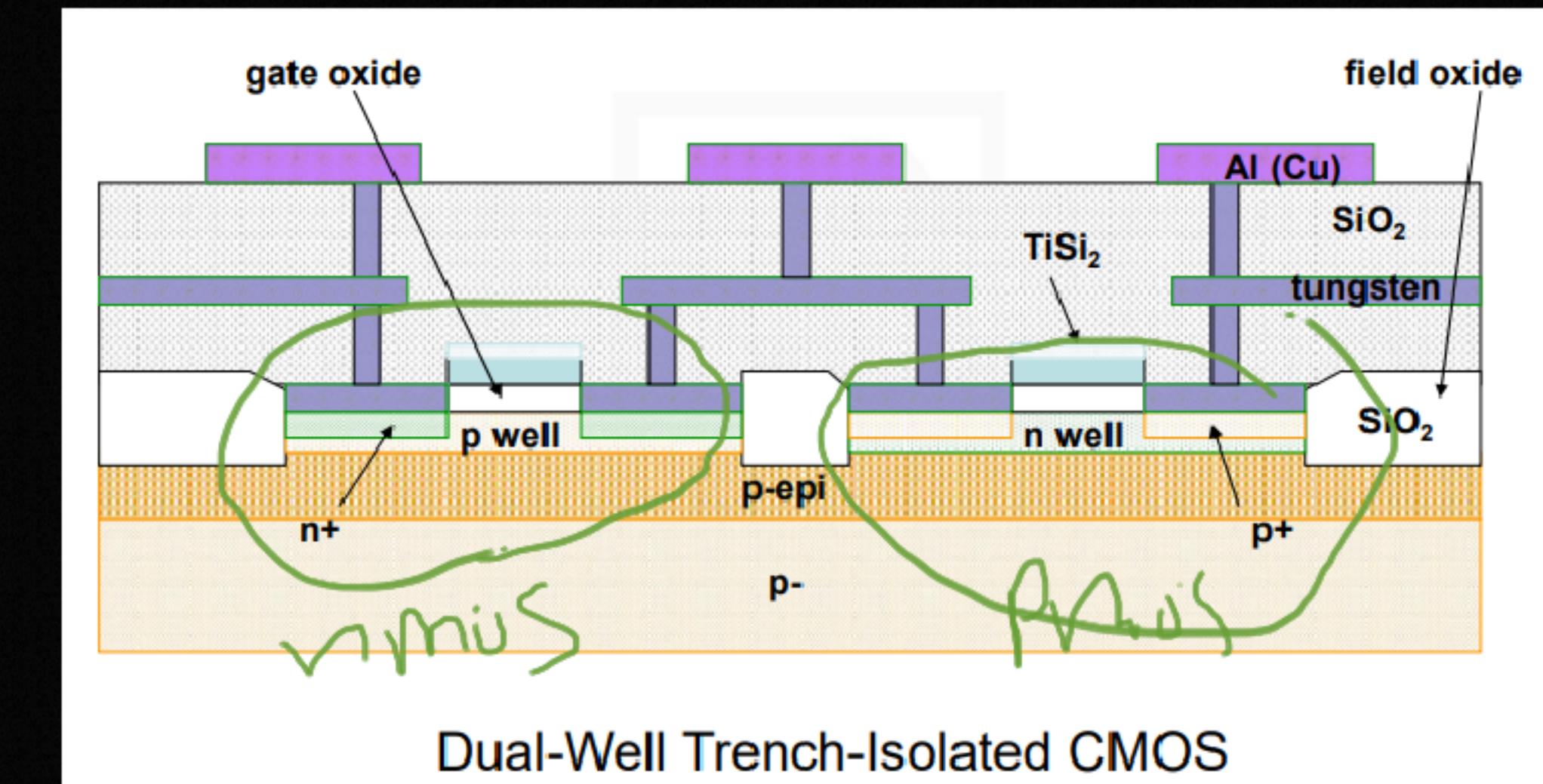


- Full rail-to-rail swing \Rightarrow high noise margins
 - Logic levels not dependent upon the relative device sizes \Rightarrow transistors can be minimum size \Rightarrow ratioless
- Always a path to V_{dd} or GND in steady state \Rightarrow low output impedance (output resistance in $k\Omega$ range) \Rightarrow large fan-out (albeit with degraded performance)
- Extremely high input resistance (gate of MOS transistor is near perfect insulator) \Rightarrow nearly zero steady-state input current
- No direct path steady-state between power and ground \Rightarrow no static power dissipation
- Propagation delay function of load capacitance and resistance of transistors.

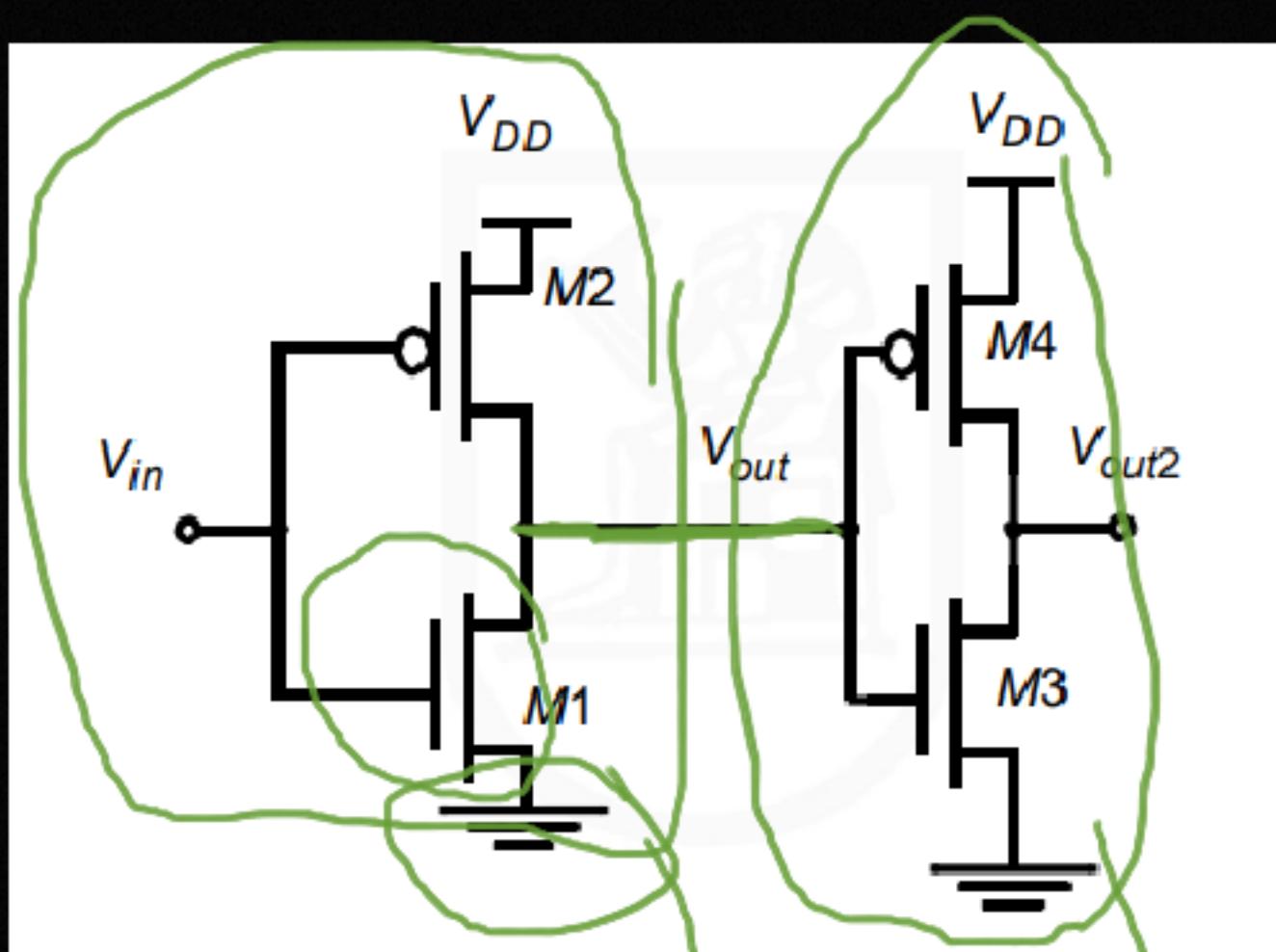
Inverter in CMOS process



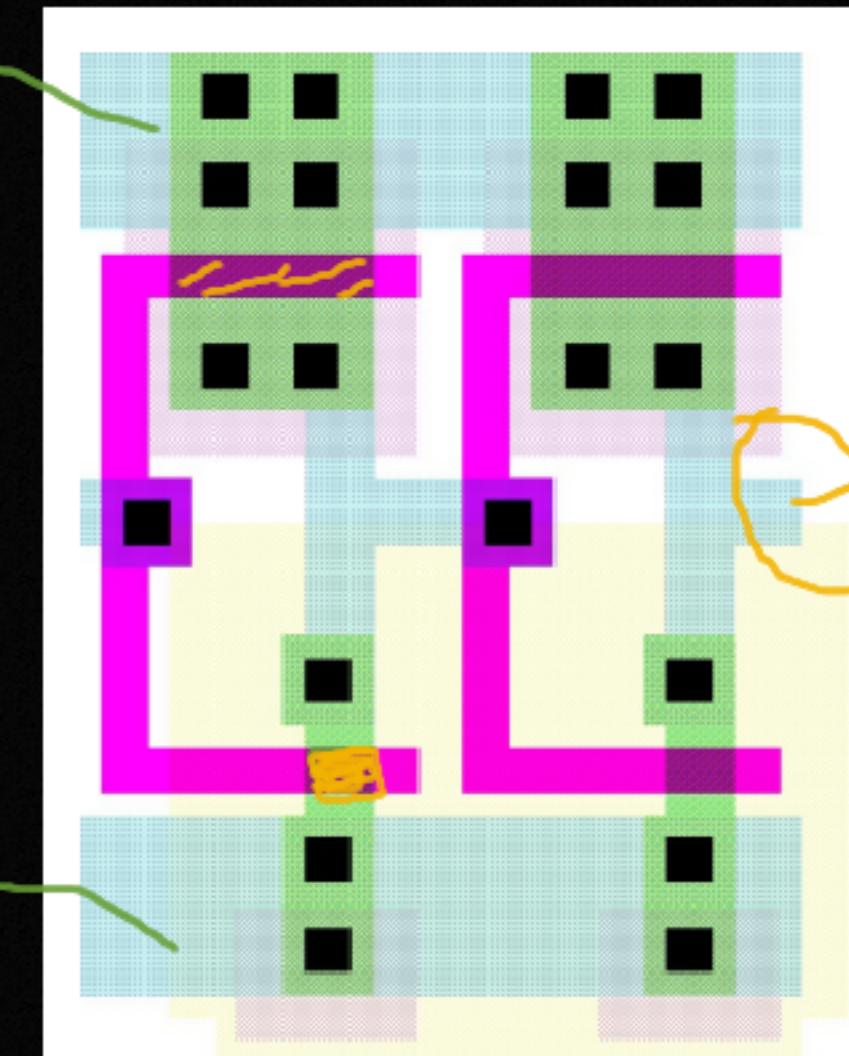
A modern CMOS process



CMOS Buffer



Layout view



Go to Slides 3, Then Return Back

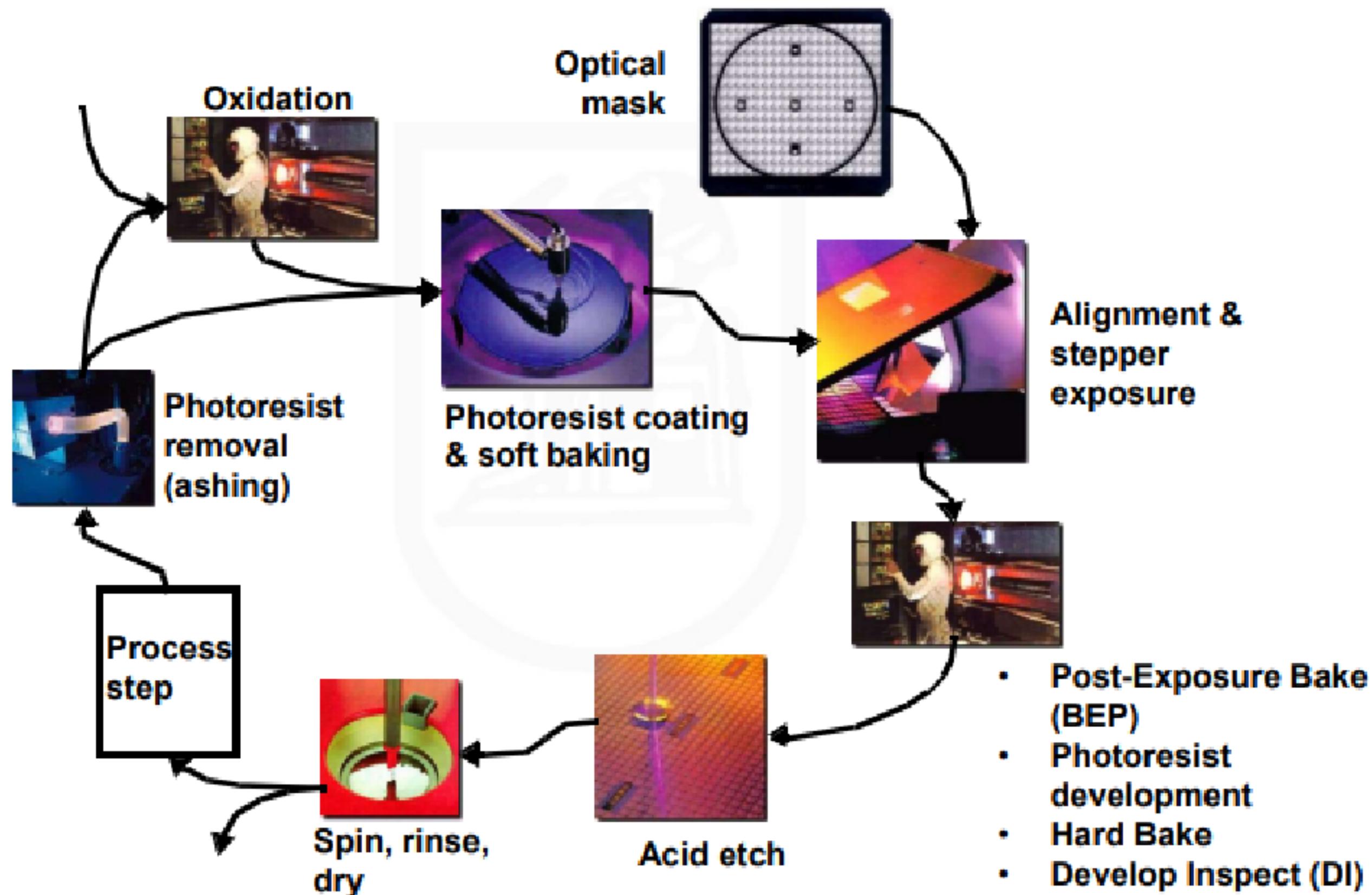
Growing the Silicon Ingot

- Start with clean sand, melt into liquid
- Grown as a high purity crystal: “boule”
- Sliced into wafers which are polished
- Notch or flat indicates crystal orientation
- 200 mm \$30-\$100/wafer
- 300 mm \$50-\$300/wafer



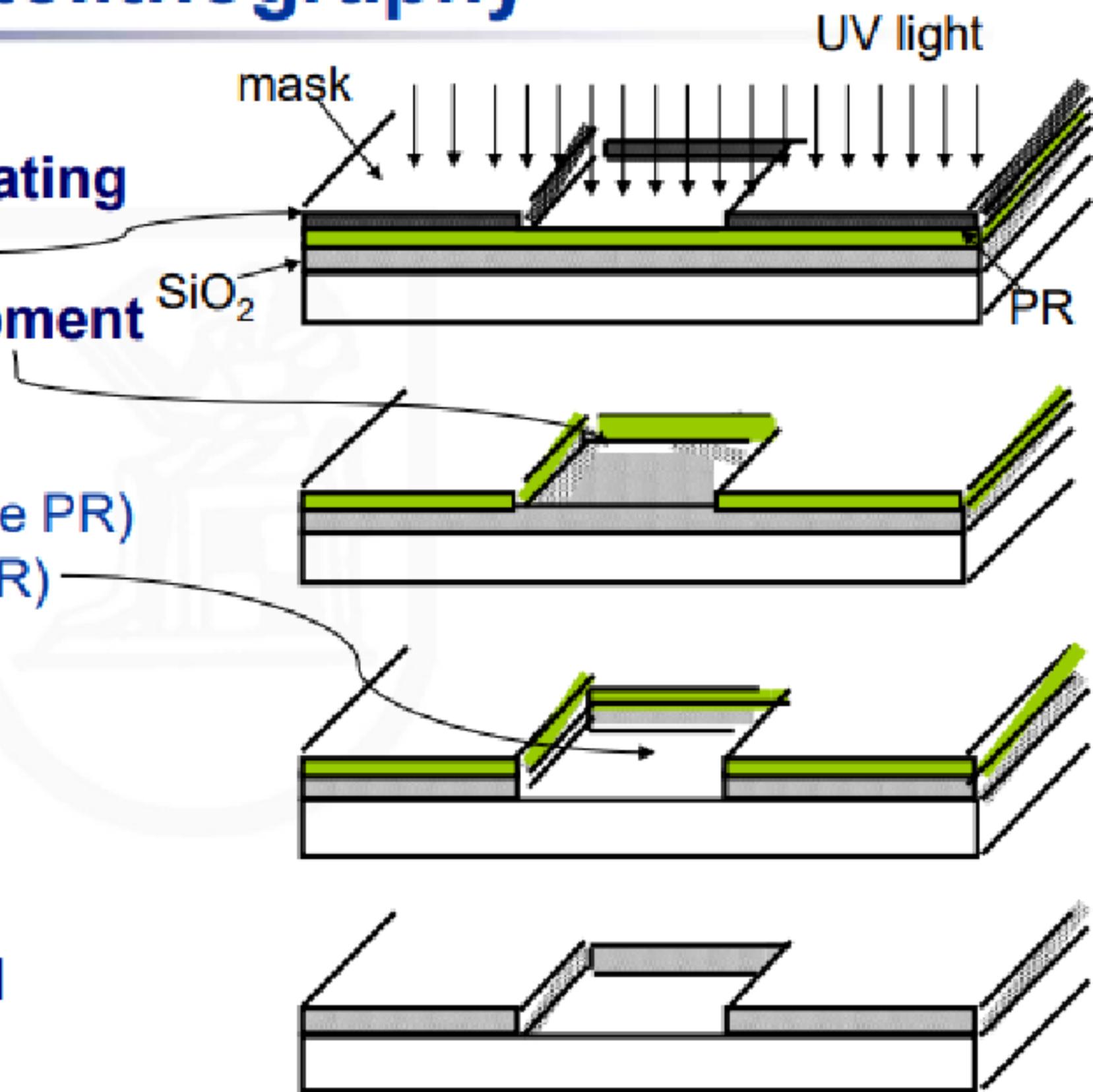
From Smithsonian, 2000

Photolithographic Process

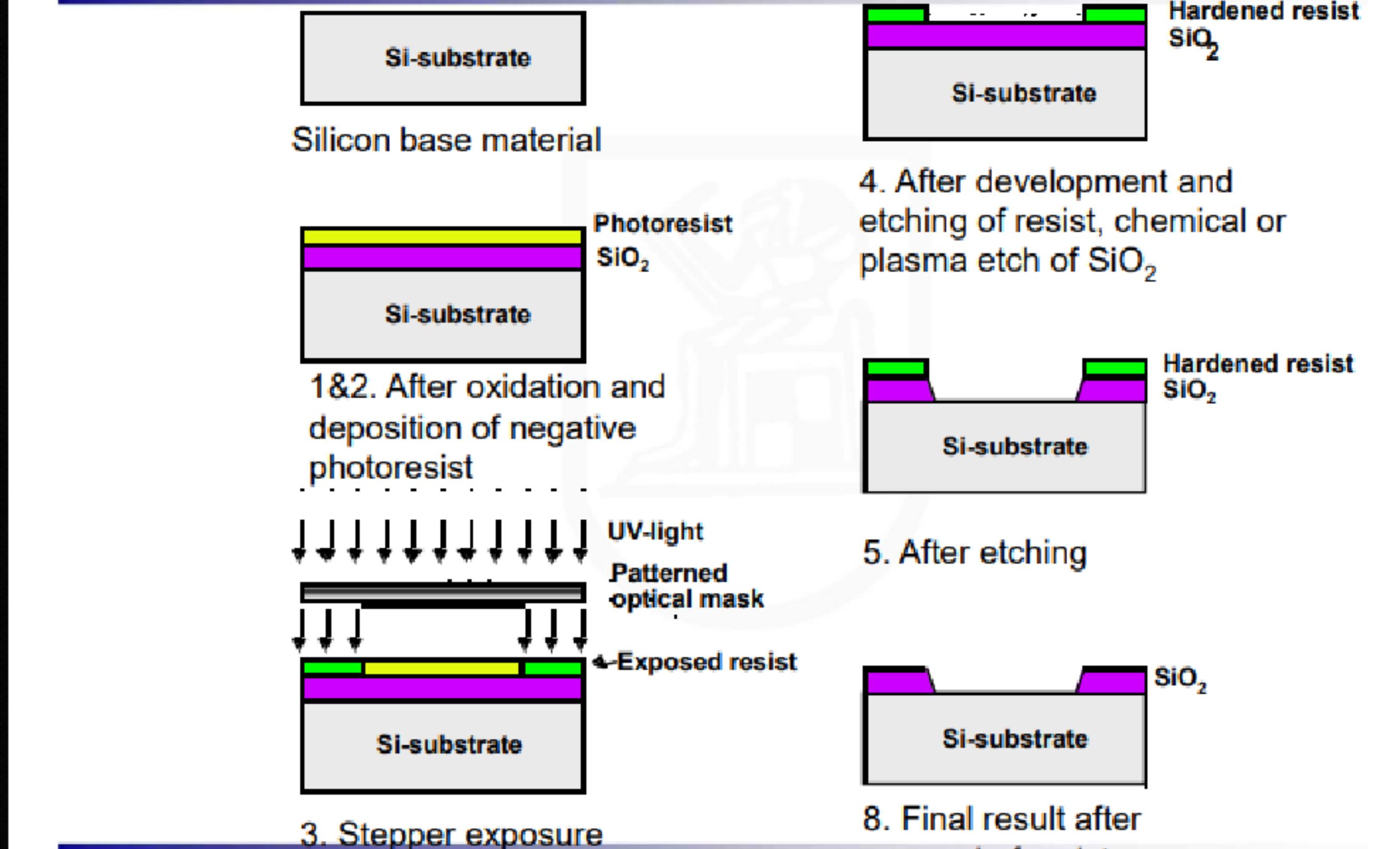


Patterning - Photolithography

1. **Oxidation**
2. **Photoresist (PR) coating**
3. **Stepper exposure**
4. **Photoresist development and bake**
5. **Acid etching**
 - Unexposed (negative PR)
 - Exposed (positive PR)
6. **Spin, rinse, and dry**
7. **Processing step**
 - Ion implantation
 - Plasma etching
 - Metal deposition
8. **Photoresist removal (ashing)**

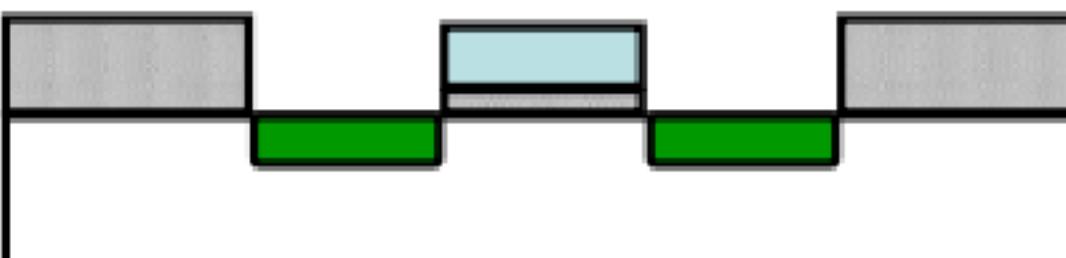
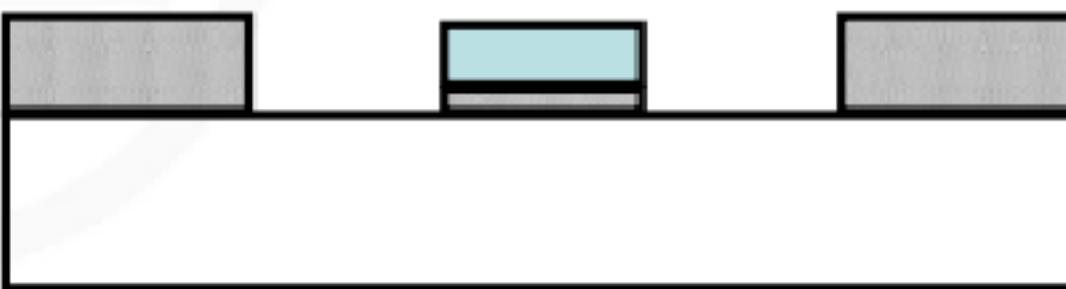
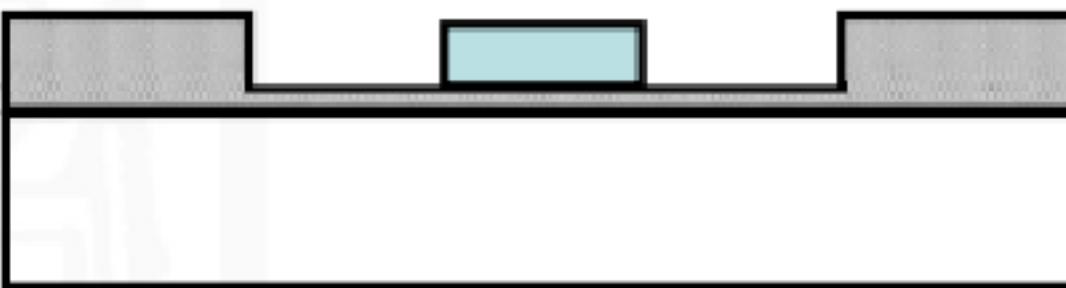


Example of Patterning of SiO₂

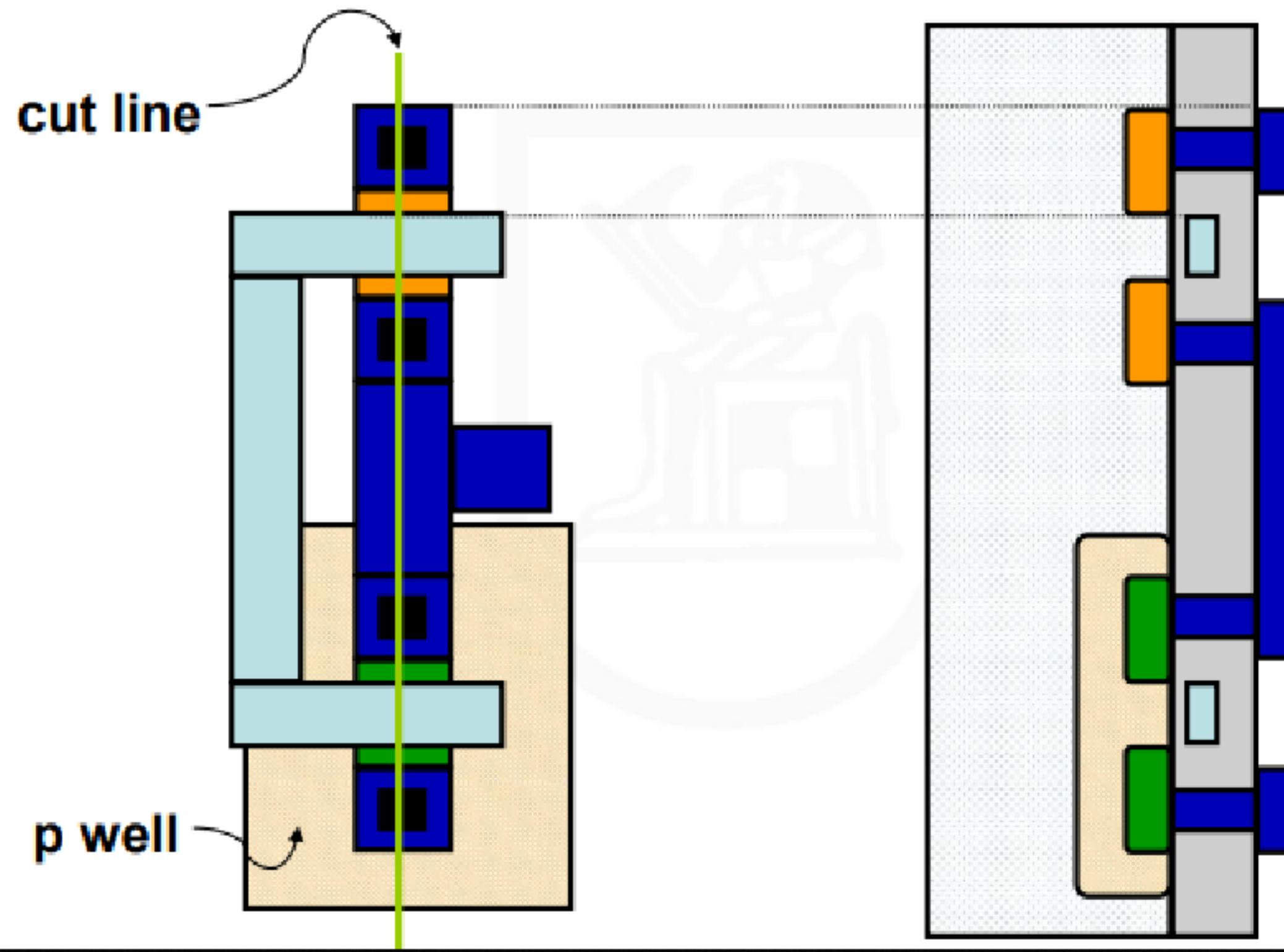


Self-Aligned Gates

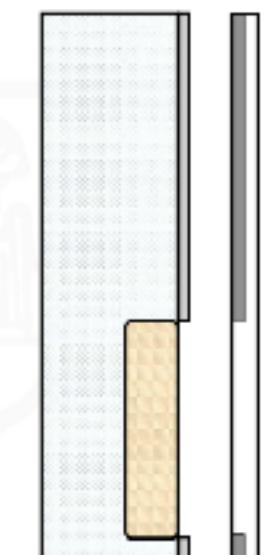
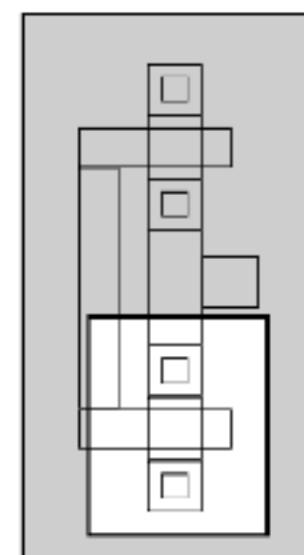
1. Create thin oxide in the “active” regions, thick elsewhere
2. Deposit polysilicon
3. Etch thin oxide from active region (poly acts as a mask for the diffusion)
4. Implant dopant



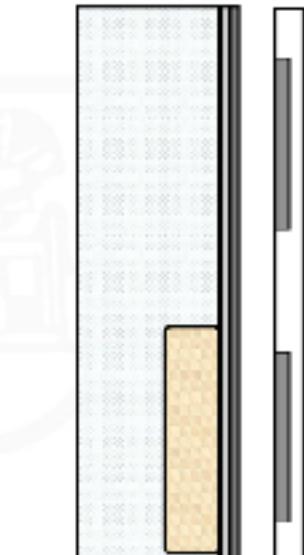
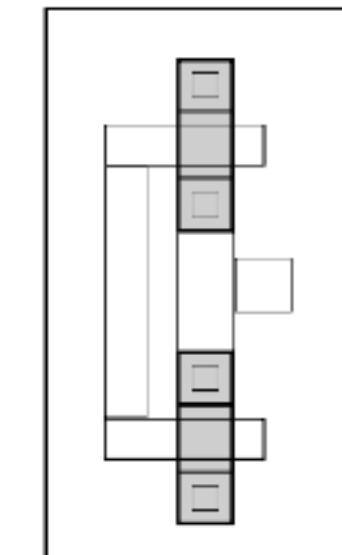
Simplified CMOS Inverter Process



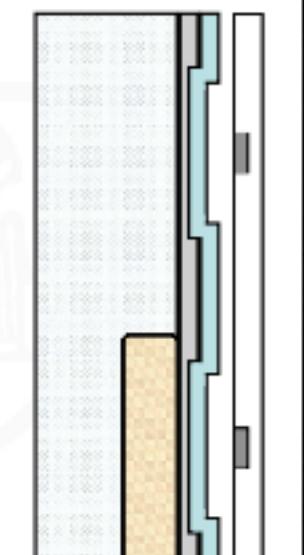
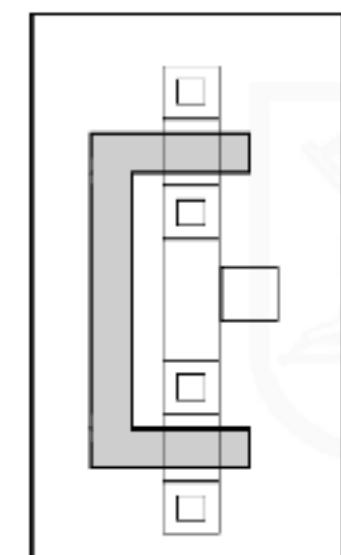
P-Well Mask



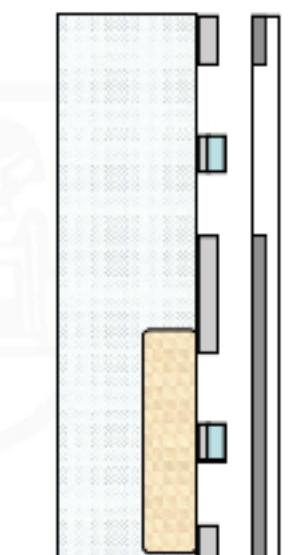
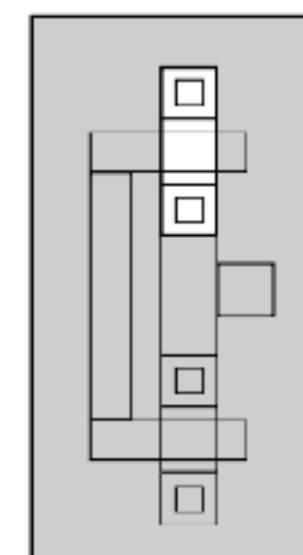
Active Mask



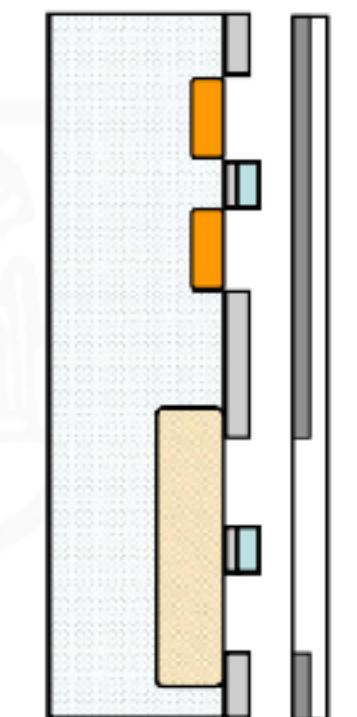
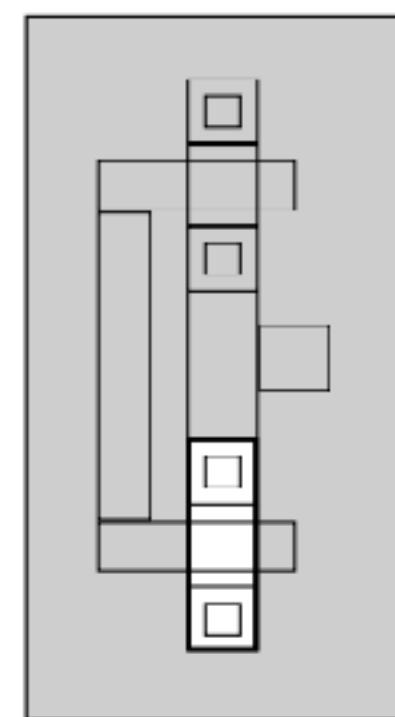
Poly Mask



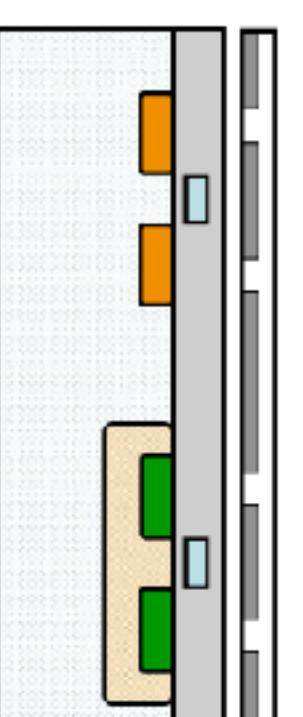
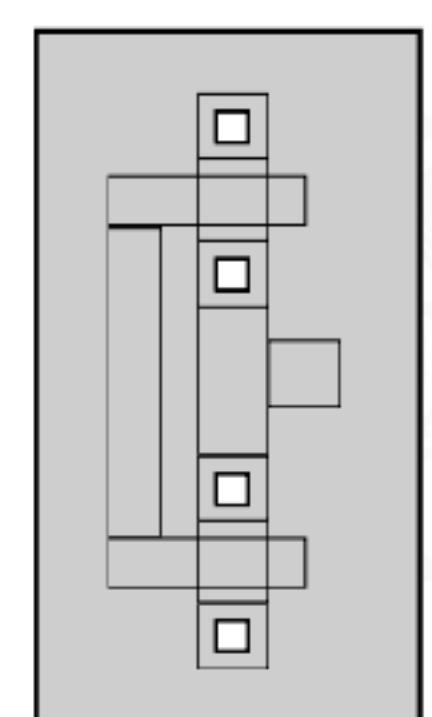
P+ Select Mask



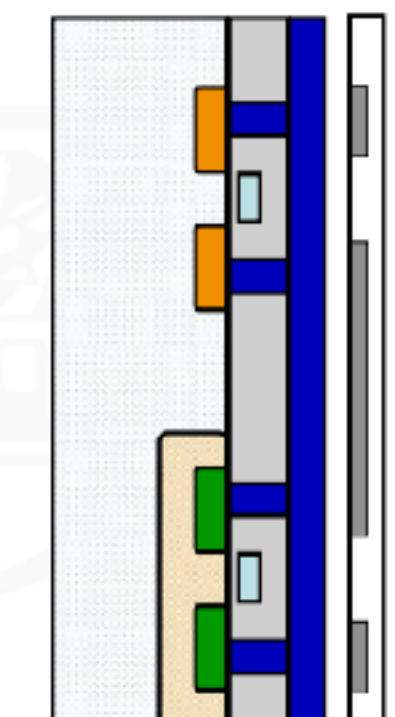
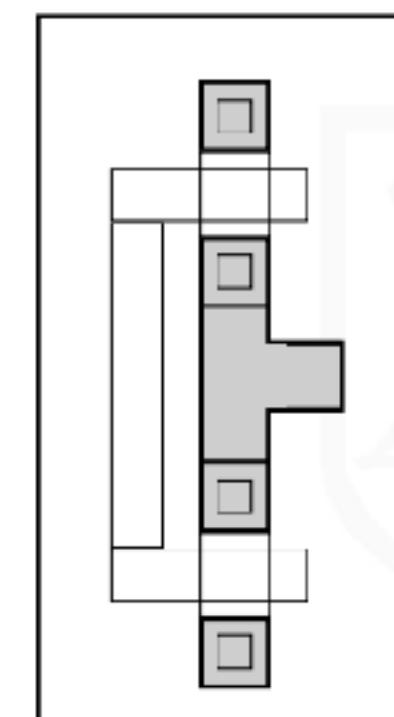
N+ Select Mask



Contact Mask

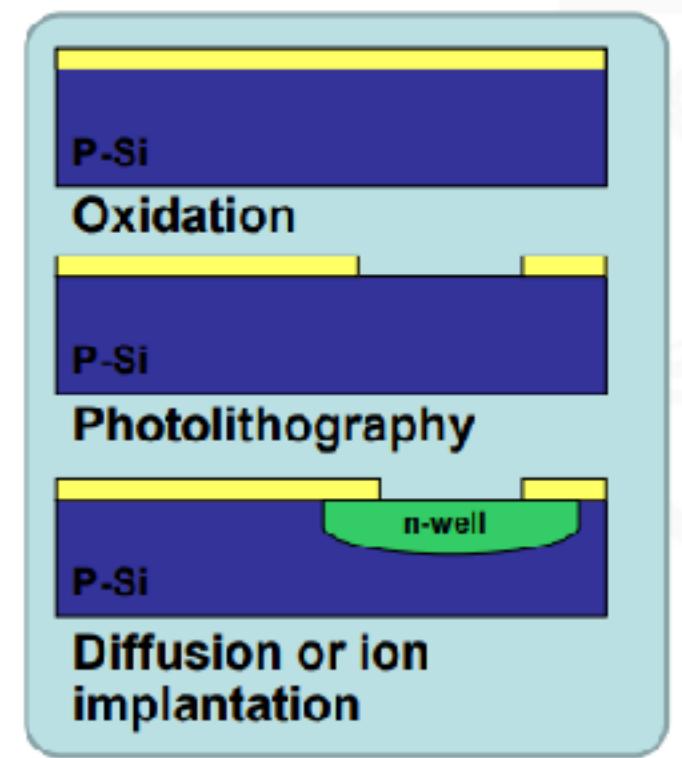


Metal Mask



Mask Example (1)

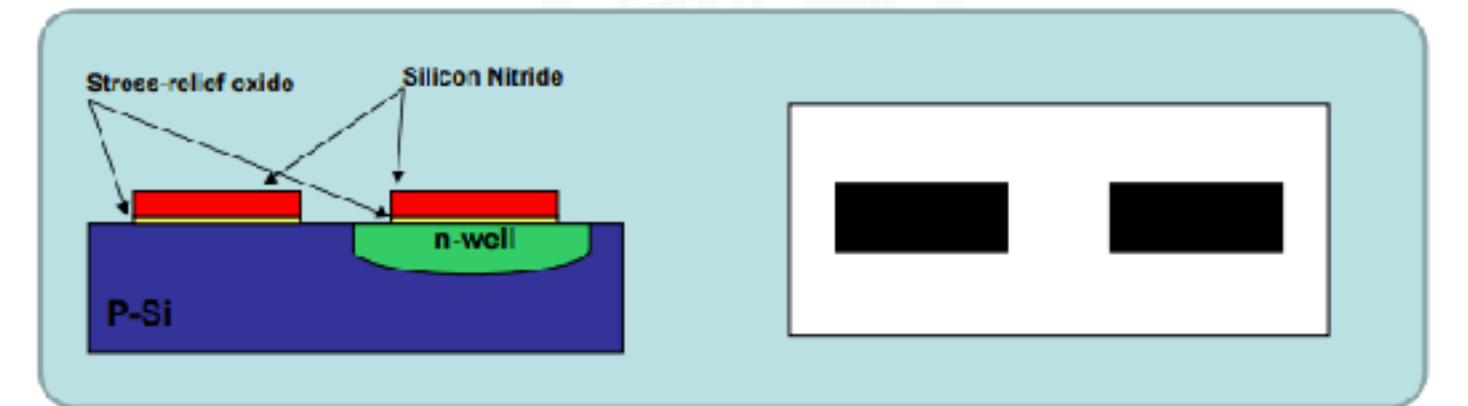
N-well Process mask



CMOS Fabrication Sequence (2)

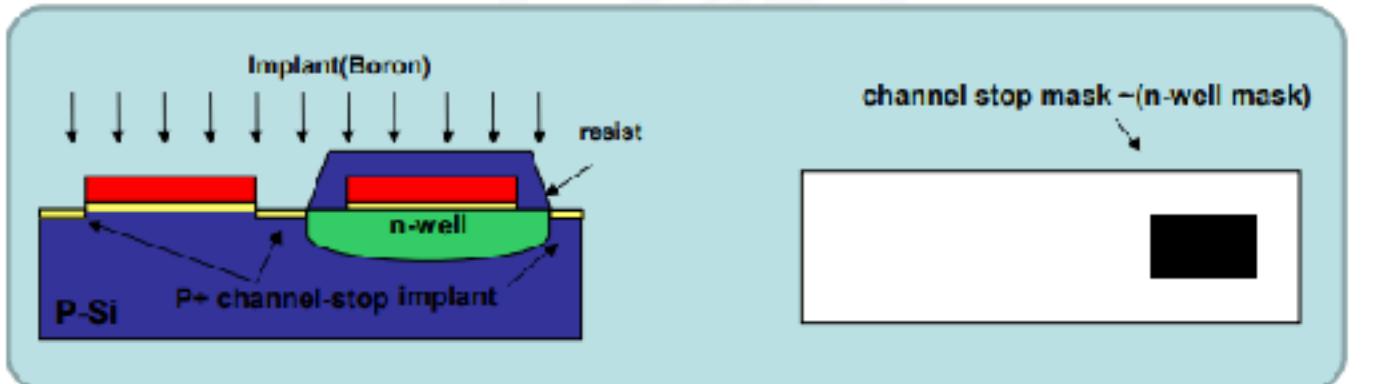
• Active area definition

- active area is a planar section of the surface
- defines transistors regions
- defines the n+ and p+ regions
- defines the gate region



CMOS Fabrication Sequence (3)

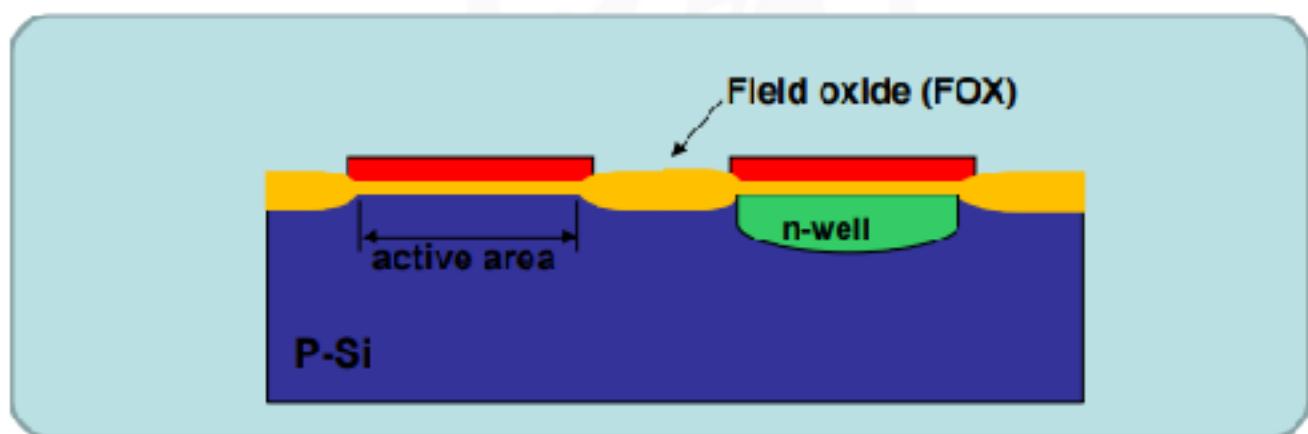
Channel-stop implant



Ion implantation

CMOS Fabrication Sequence (4)

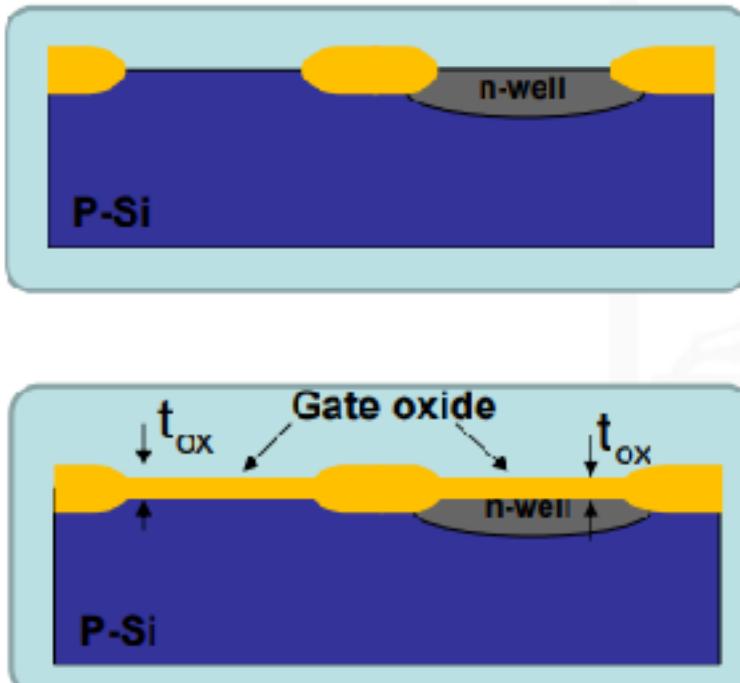
LOCOS (Local oxidation of silicon)



Field oxide formation

CMOS Fabrication Sequence (5)

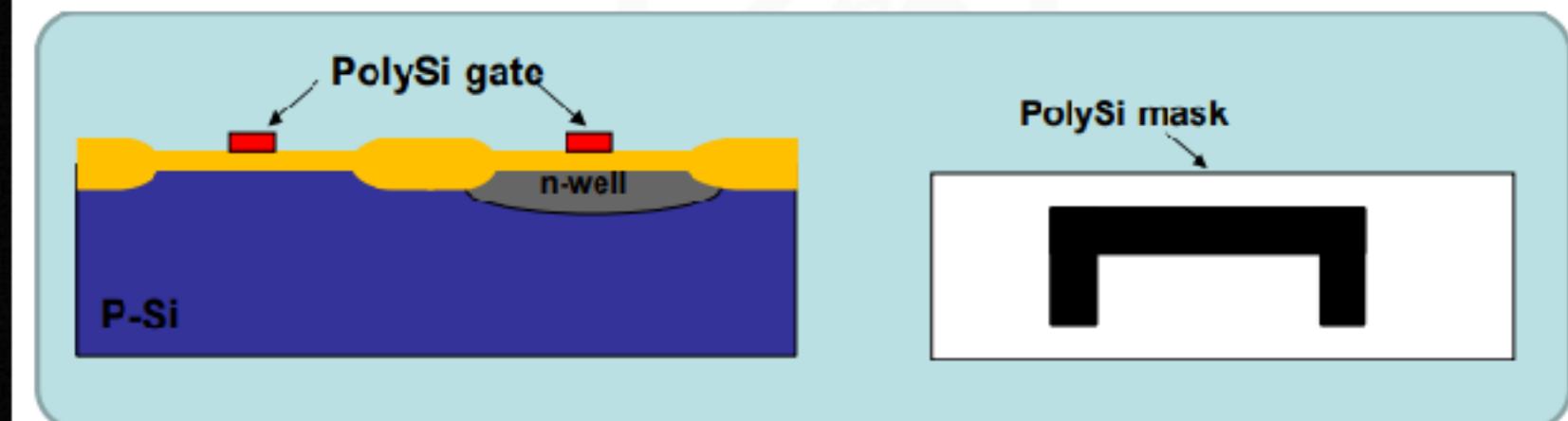
Thin Gate Oxide Growth



- The nitride and stress-relief oxide is removed.
- The threshold voltage is adjusted by ion implantation.
- Gate oxide growth, $t_{ox} = 50 \dots 2\text{nm}$
- Thermal oxidation

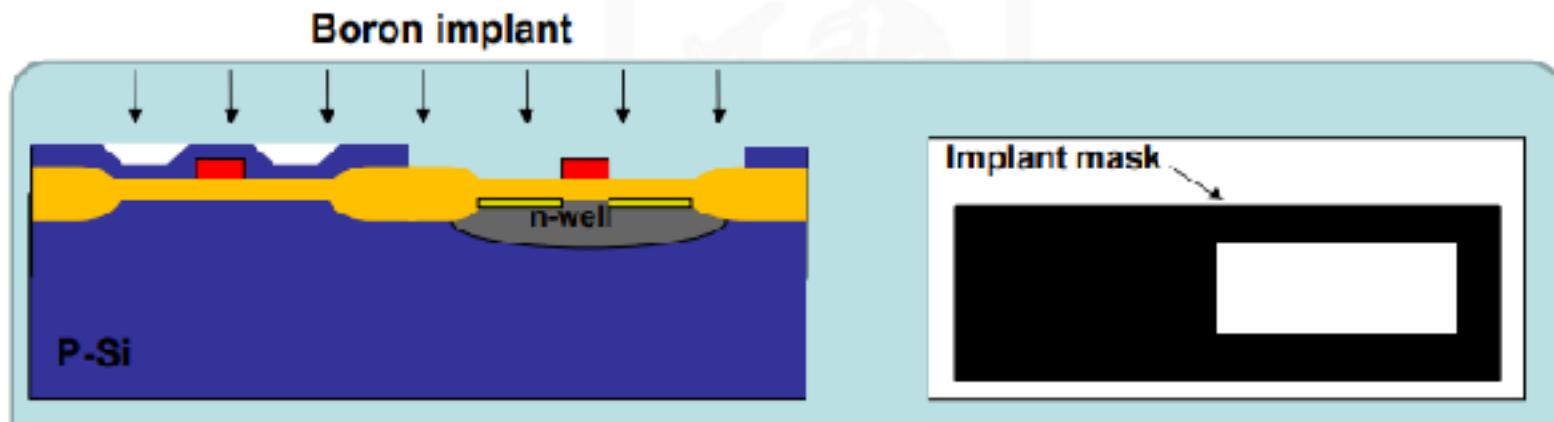
CMOS Fabrication Sequence (6)

Polysilicon deposition and photolithography



All the gates are formed and doped (n^+) by CVD technique in the single step.

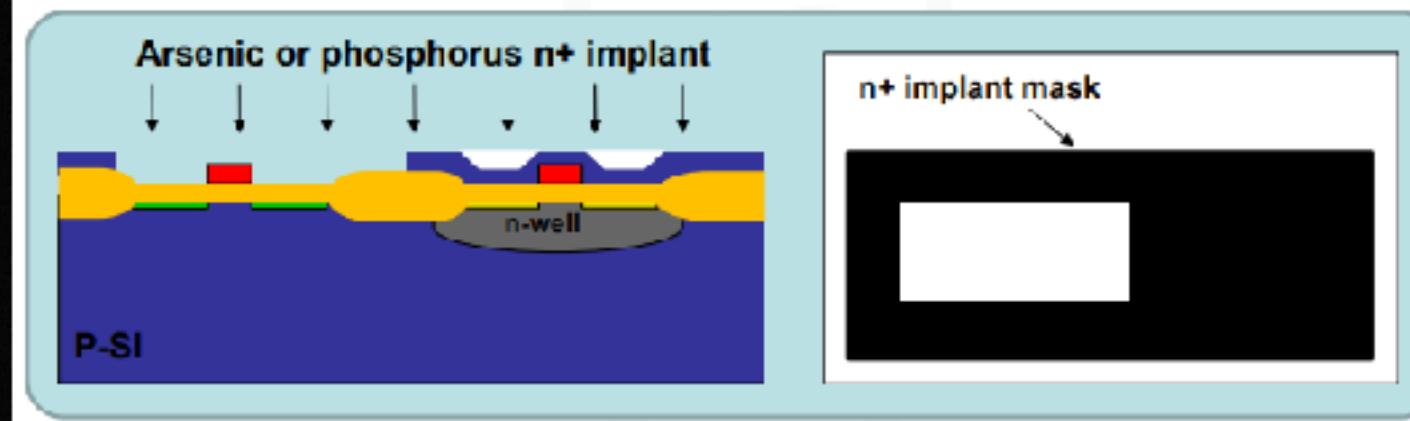
P-MOS Formation



Photolithography and boron ion implantation – Self aligned process

CMOS Fabrication Sequence (8)

N-MOS Formation

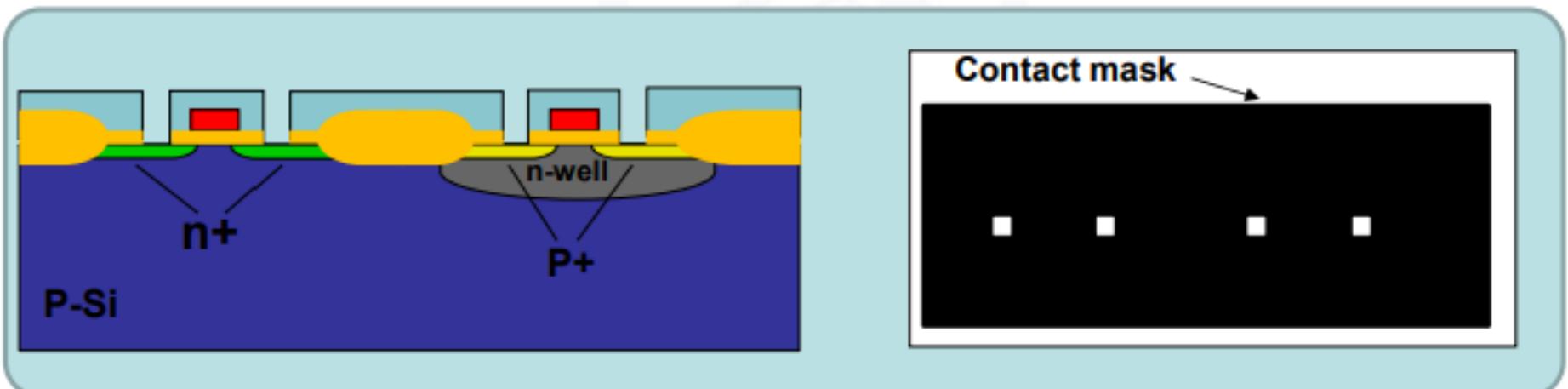


Photolithography and ion implantation – Self aligned process (n^+ doped gate)

Thermal annealing cycle is performed.

CMOS Fabrication Sequence (9)

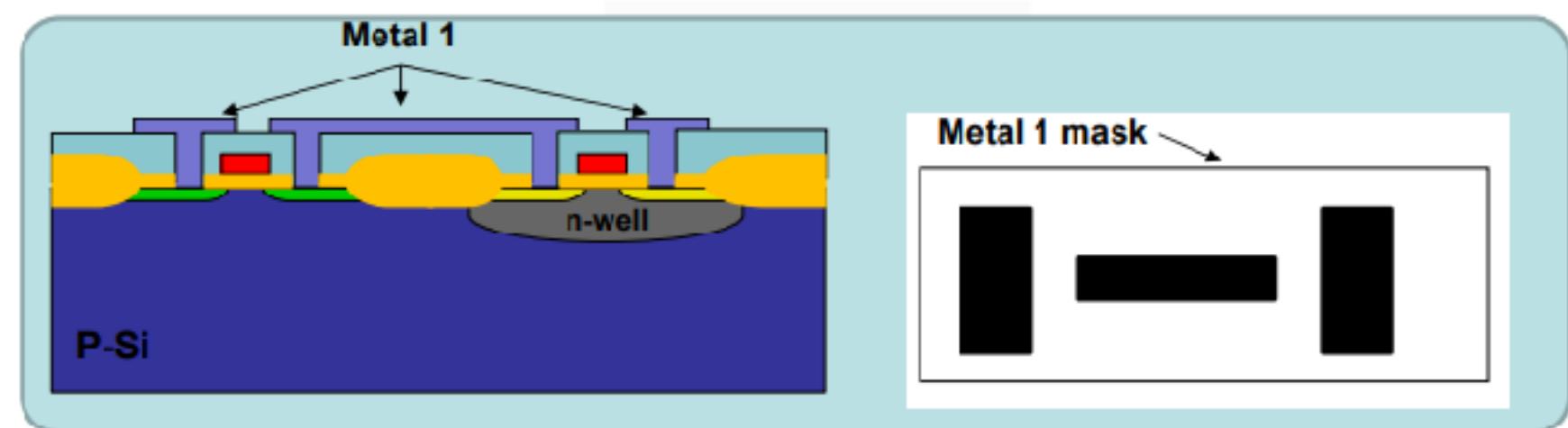
Contact cut formation



- Oxide deposition by low temperature CVD process.
- Photolithography and SiO_2 etching.

CMOS Fabrication Sequence (10)

Contact formation



- Metal (Al or Cu) deposition and photolithography.
- Contacts and interconnects are formed.
- In just the same way the other metal layers are formed.
- After surface glass passivation and pad opening, the chips pass to the next step according to general IC fabrication flow.

Other CMOS Processes

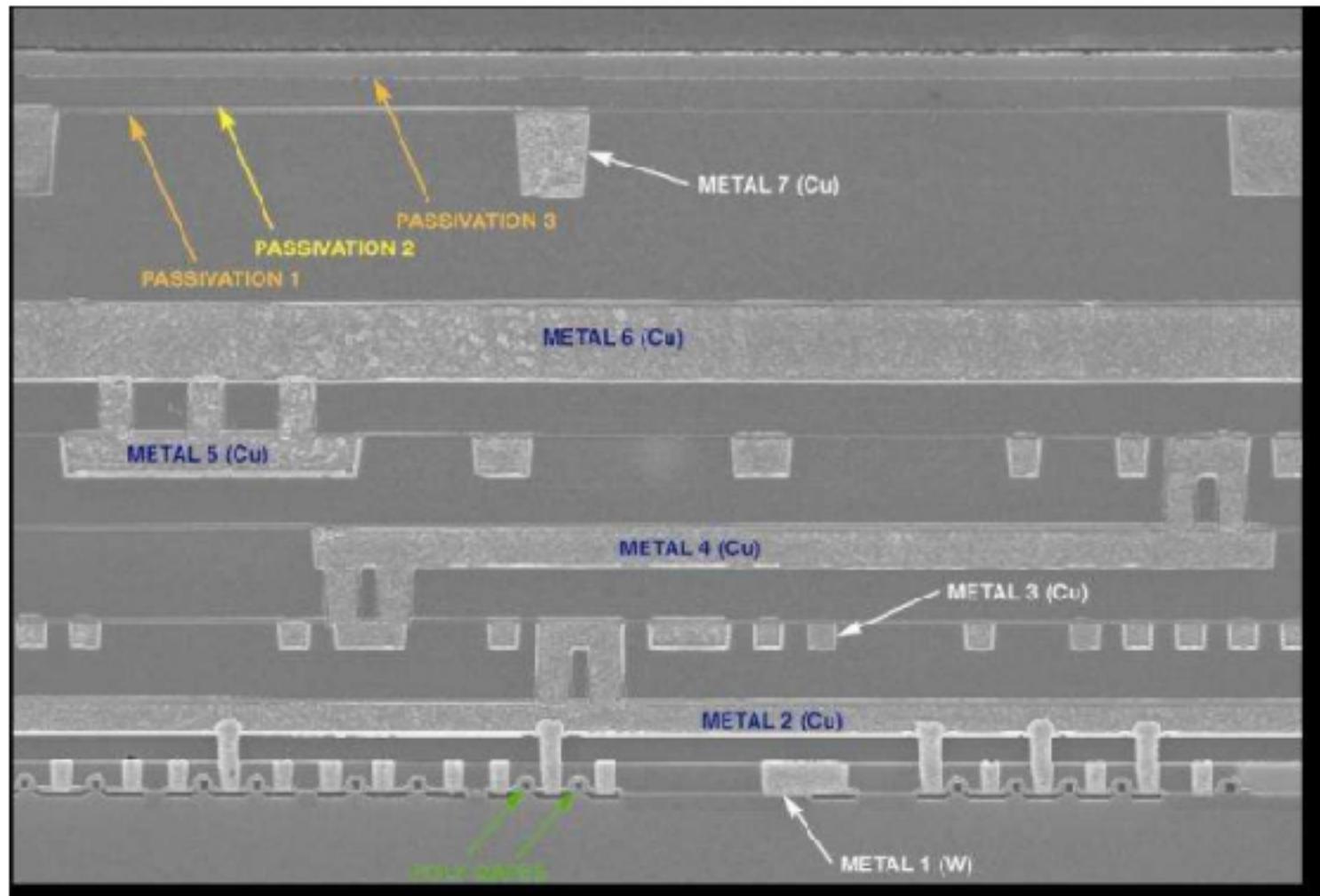
- **Other CMOS Processes**

- P-well
- Twin-well
- Silicon on insulator (SOI-SIMOX)
- Shallow trench isolation (STI)

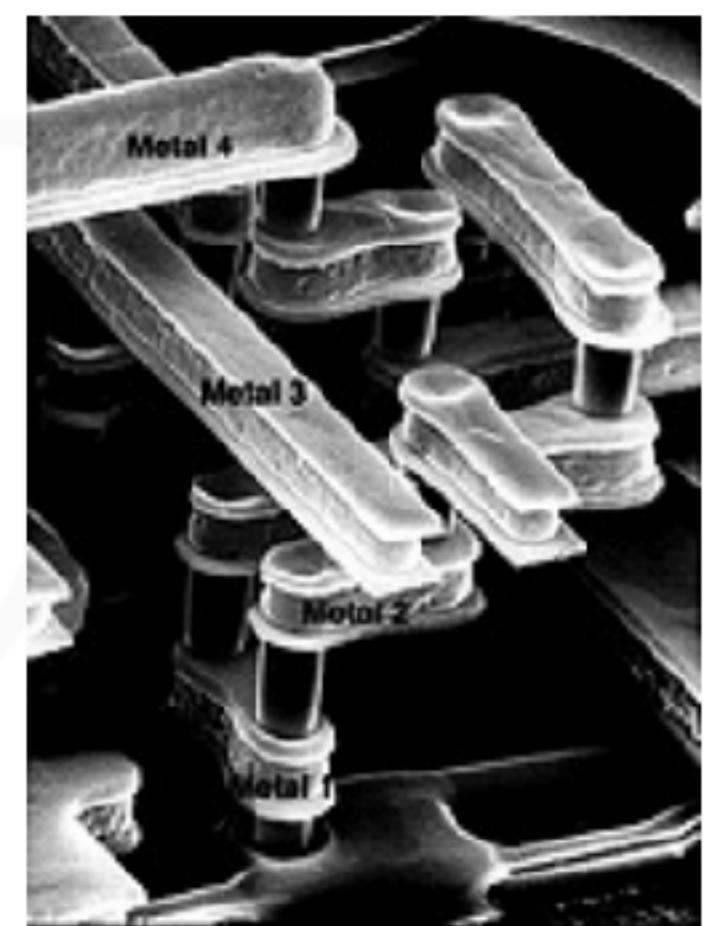
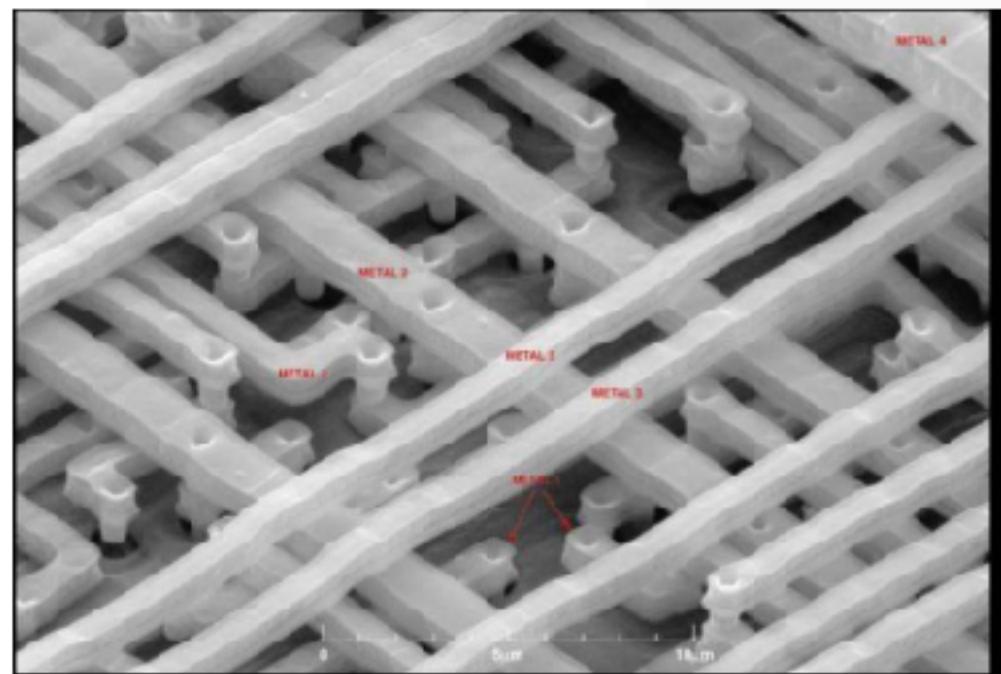
- **Process enhancements**

- Increase of metal levels
- Copper for interconnects and vias
- Very thin oxide layers(1,0...2nm), stacked contacts and vias
- Chemical and Mechanical Polishing (CMP)

Copper Metallization

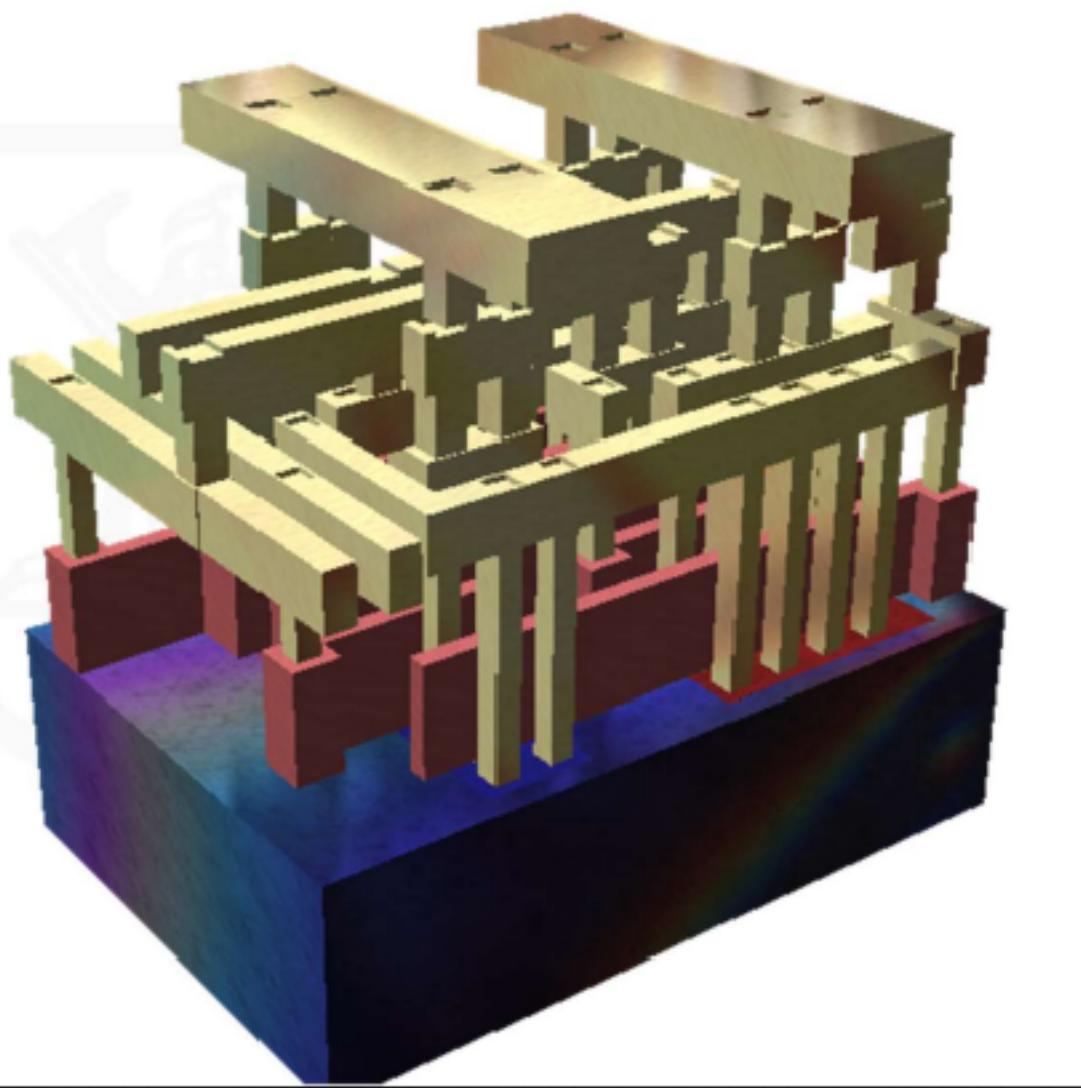


Advanced Metallization



Advanced Metallization (cont.)

- 3D view of a modern standard cell



GO TO Manufacturing CMOS ICs
Slides, Then Continue