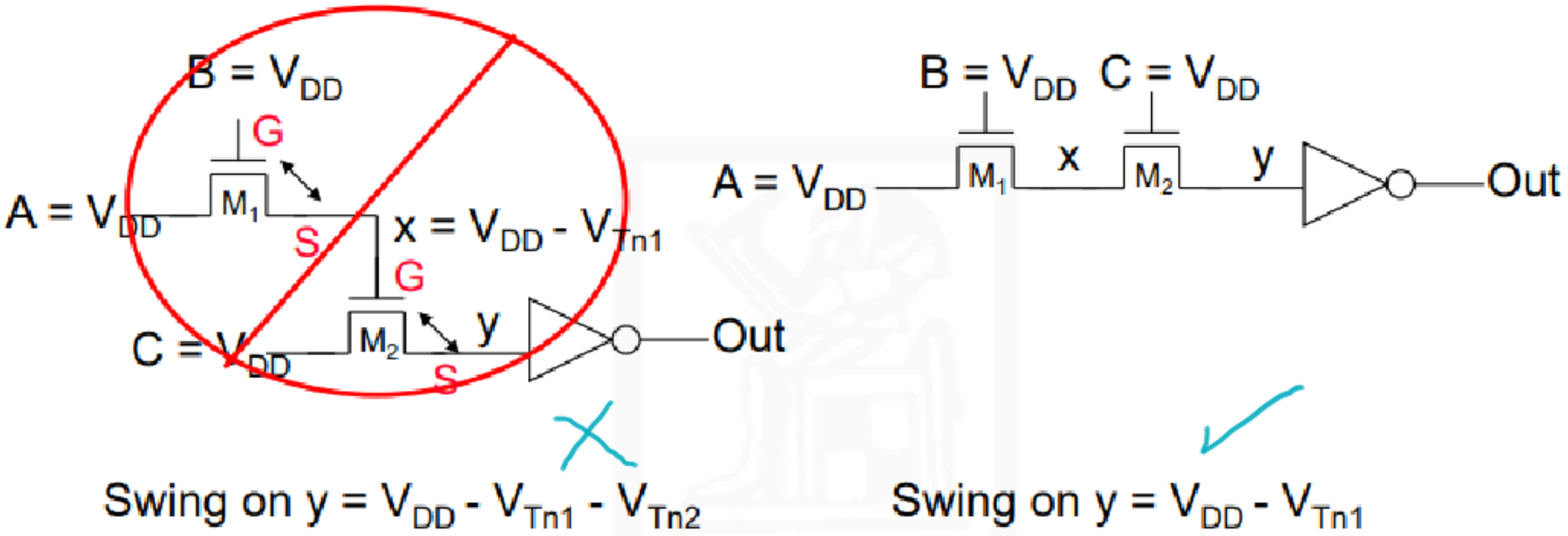
Cascaded NMOS Only PTs

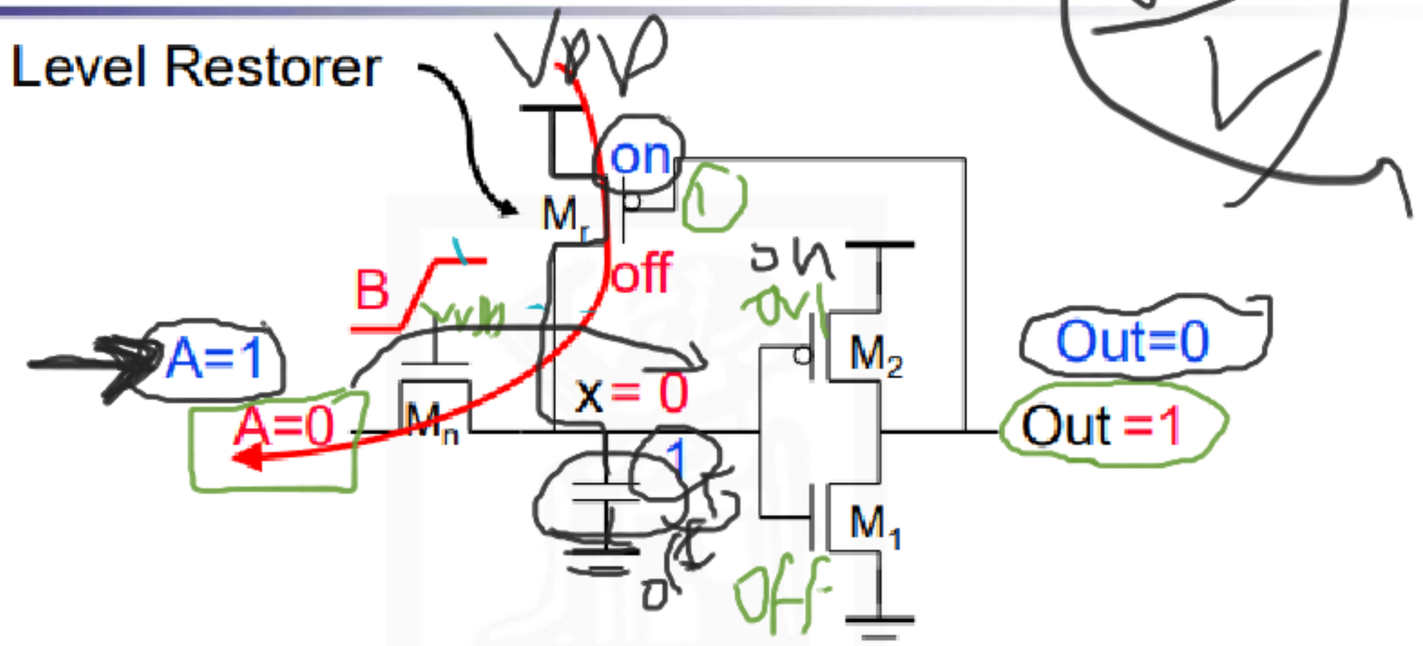


Swing on y = $V_{DD} - V_{Tn1} - V_{Tn2}$

Swing on y = $V_{DD} - V_{Tn1}$

- Pass transistor gates should never be cascaded as on the left
- Logic on the right suffers from static power dissipation and reduced noise margins

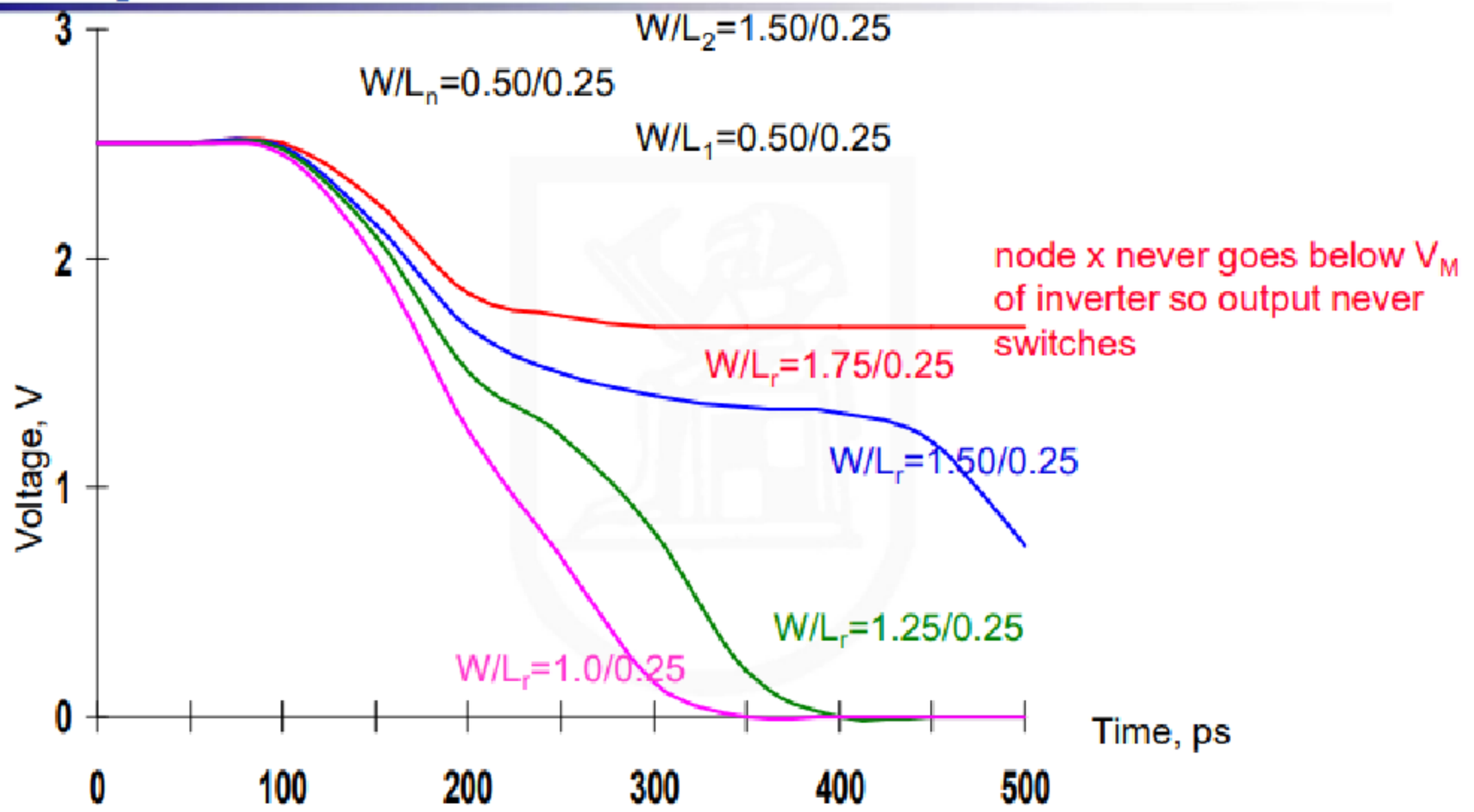
Solution 1: Level Restorer



- Full swing on x (due to Level Restorer) so no static power consumption by inverter
- No static backward current path through Level Restorer and PT since Restorer is only active when A is high

- **For correct operation M_r must be sized correctly (ratioed)**

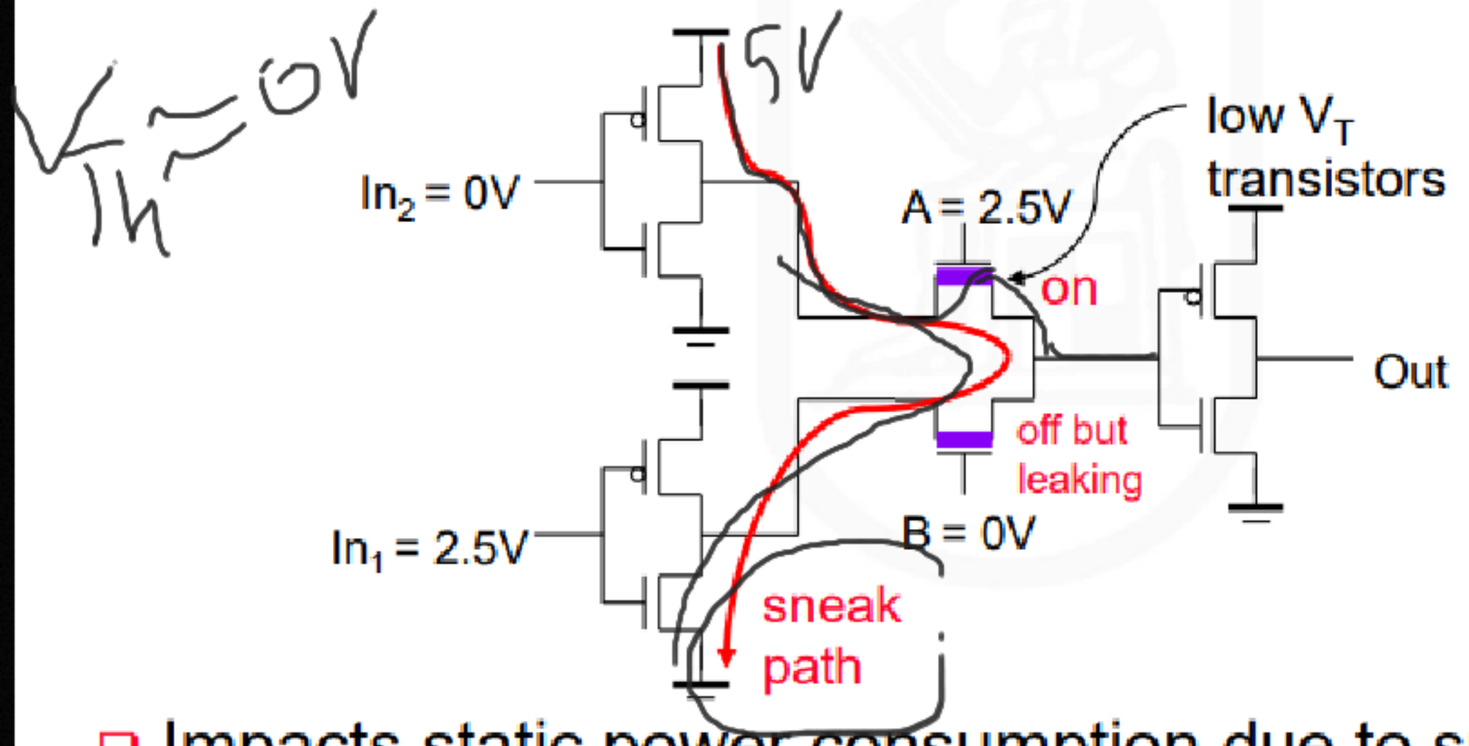
Transient Level Restorer Circuit Response



- Restorer has speed and power impacts: increases the cap at x, slowing down the gate; increases t_r (but decreases t_f)

Solution 2: Multiple V_T Transistors

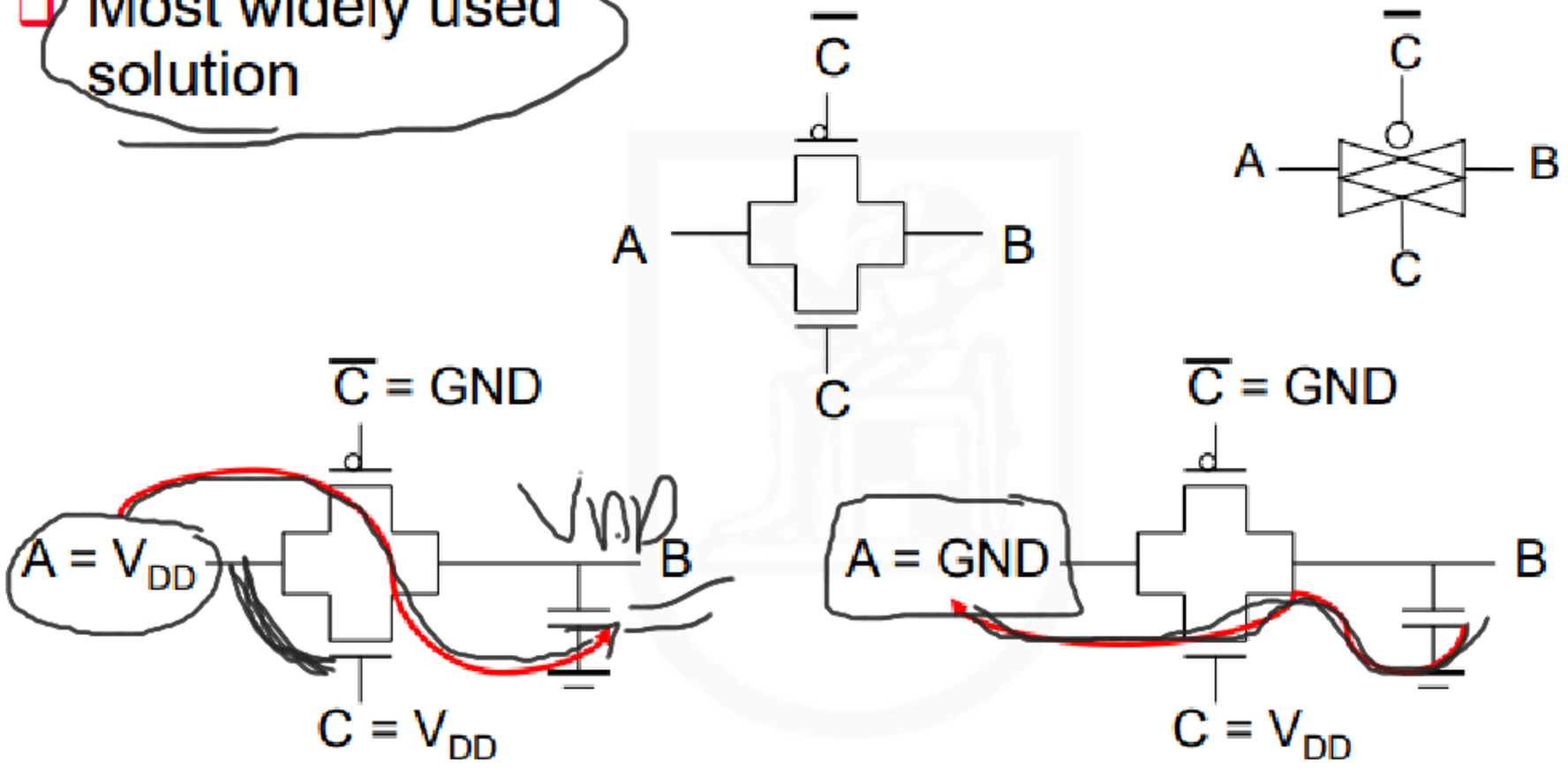
- Technology solution: Use (near) zero V_T devices for the NMOS PTs to eliminate *most* of the threshold drop (body effect still in force preventing full swing to V_{DD})



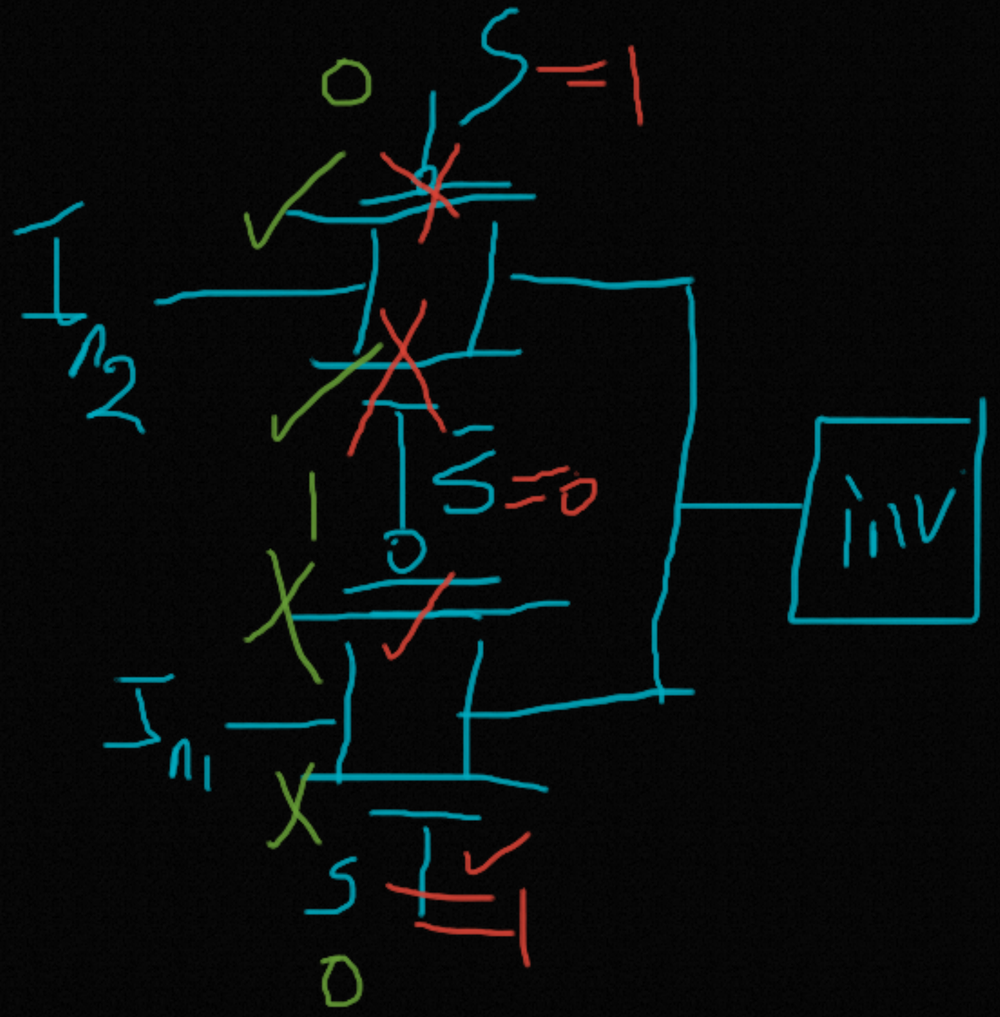
- Impacts static power consumption due to subthreshold currents flowing through the PTs (even if V_{GS} is below V_T)

Solution 3: Transmission Gates (TGs)

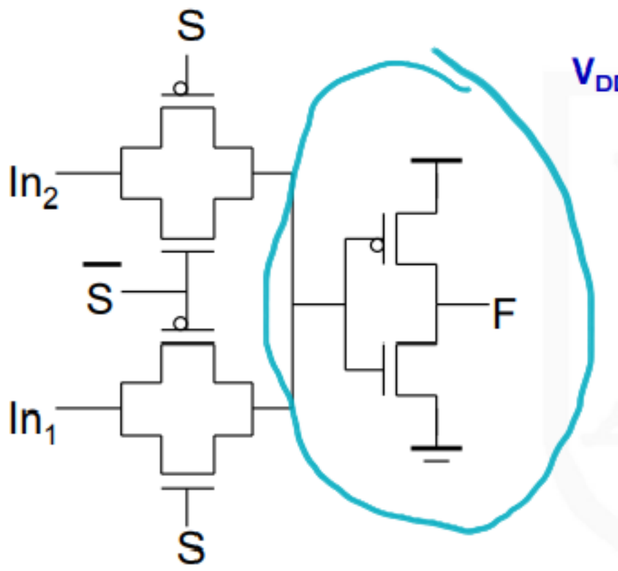
- Most widely used solution



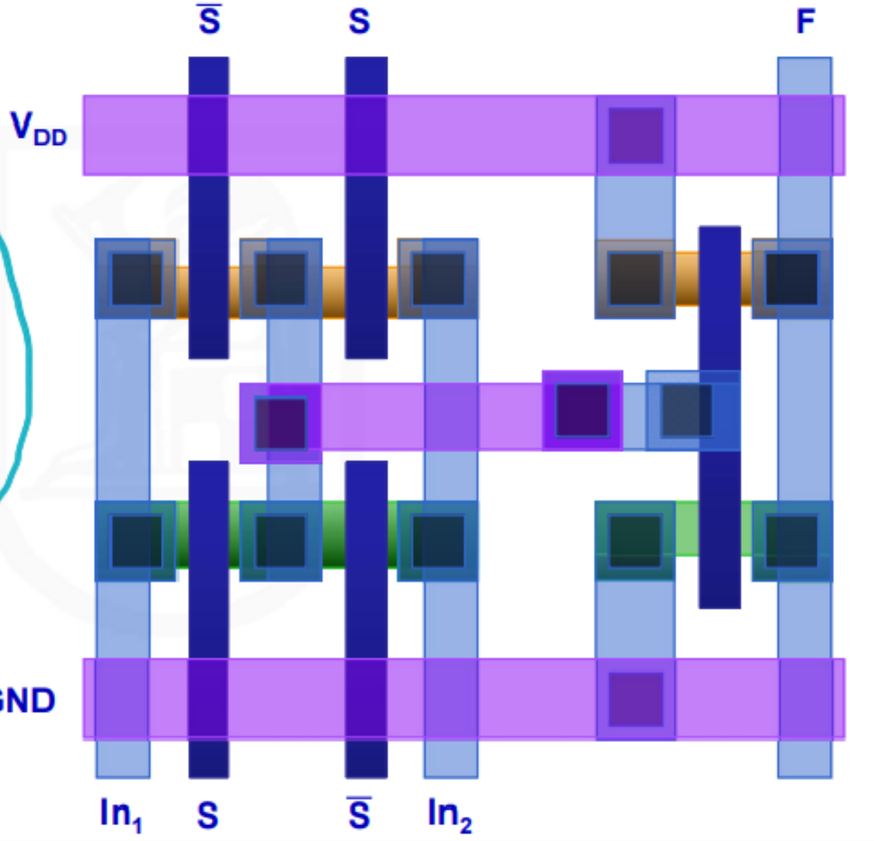
- **Full swing *bidirectional* switch controlled by the gate signal C, A = B if C = 1**

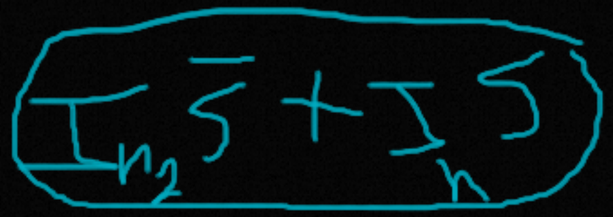


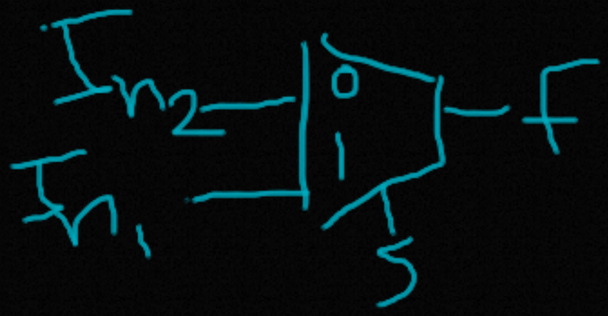
TG Multiplexer



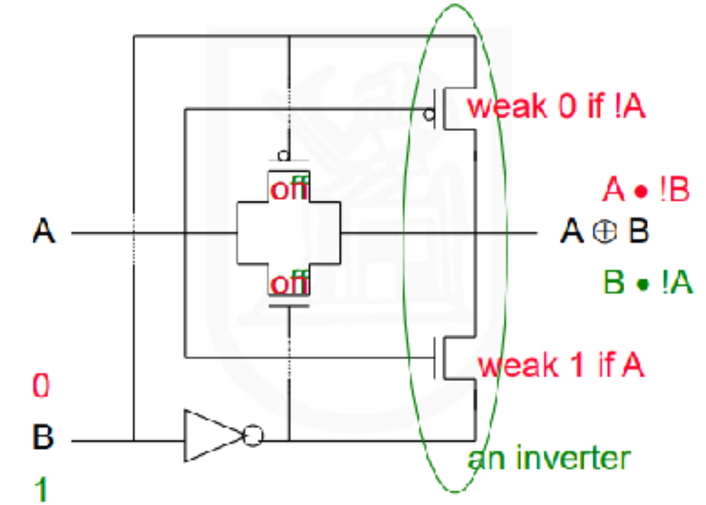
$F = !(In_1 \bullet S + In_2 \bullet \overline{S})$







Transmission Gate XOR



TG Full Adder