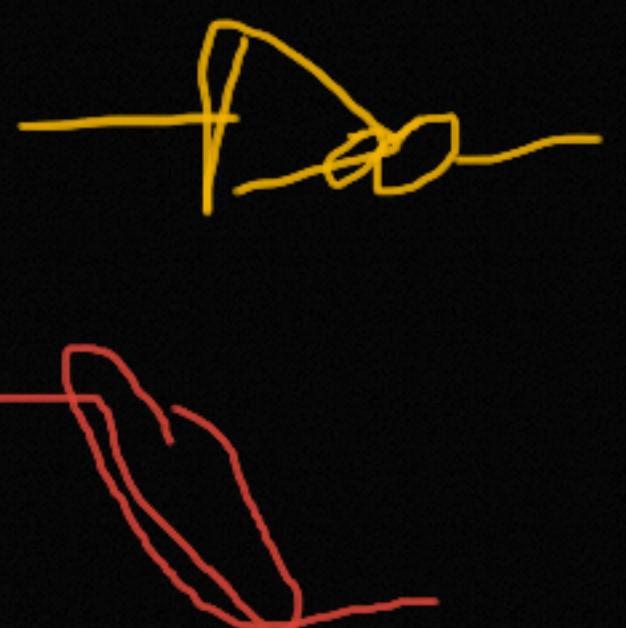
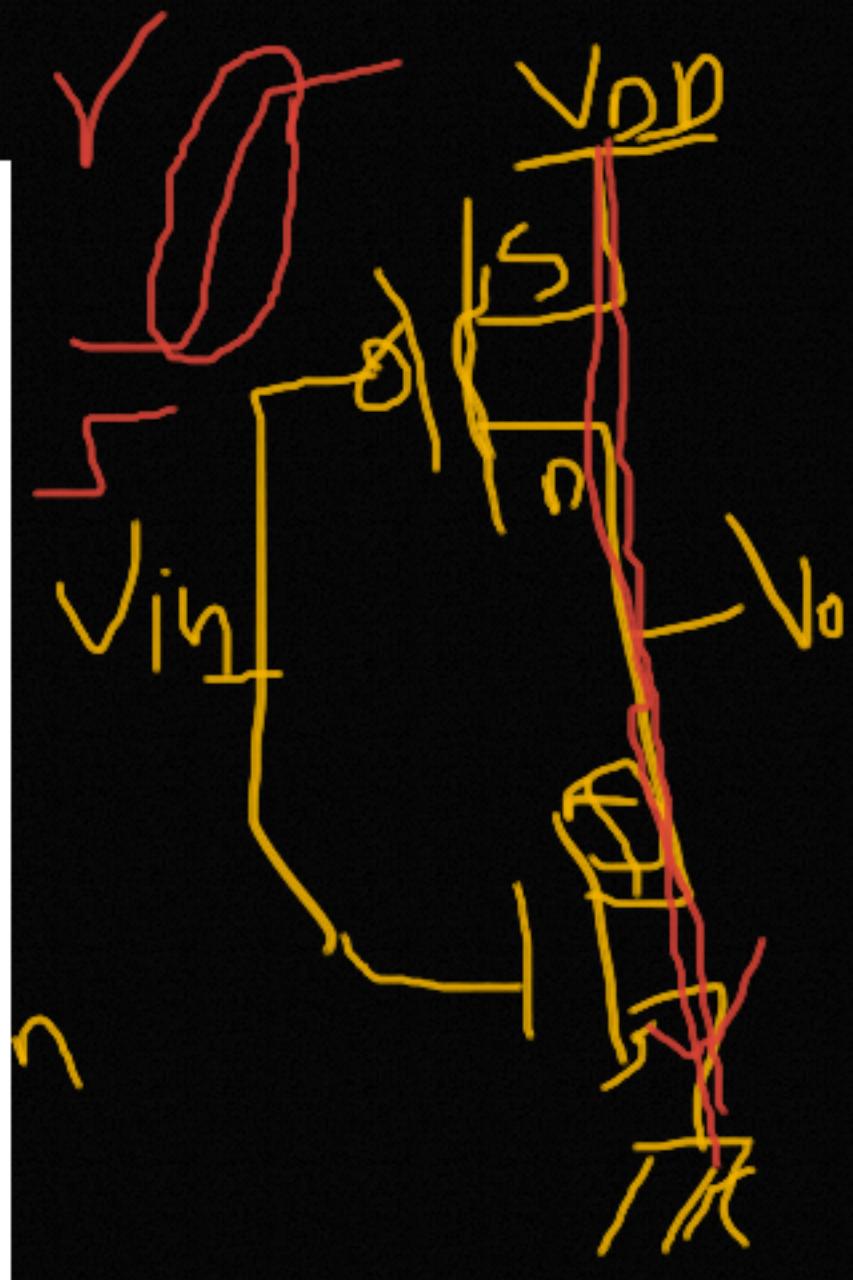


Digital Logic Families

CMOS Circuit Styles

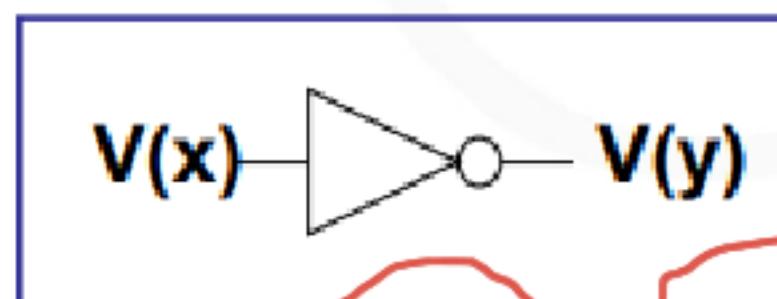
- **Static complementary CMOS** - except during switching, output connected to either V_{DD} or GND via a low-resistance path
 - high noise margins
 - full rail to rail swing
 - V_{OH} and V_{OL} are at V_{DD} and GND, respectively
 - low output impedance, high input impedance
 - no steady state path between V_{DD} and GND (no static power consumption)
 - delay a function of load capacitance and transistor resistance
 - comparable rise and fall times (under the appropriate transistor sizing conditions)
- **Dynamic CMOS** - relies on temporary storage of signal values on the capacitance of high-impedance circuit nodes
 - simpler, faster gates, cycle has pre-charge and evaluation phases
 - increased sensitivity to noise



Static Inverter Behavior

- Steady-state parameters of a gate – *static behavior* – tell how robust a circuit is with respect to both variations in the manufacturing process and to noise disturbances.
- Digital circuits perform operations on Boolean variables $x \in \{0,1\}$
- A logical variable is associated with a *nominal voltage level* for each logic state

$$1 \Leftrightarrow V_{OH} \text{ and } 0 \Leftrightarrow V_{OL}$$



$$V_{OH} = ! (V_{OL})$$

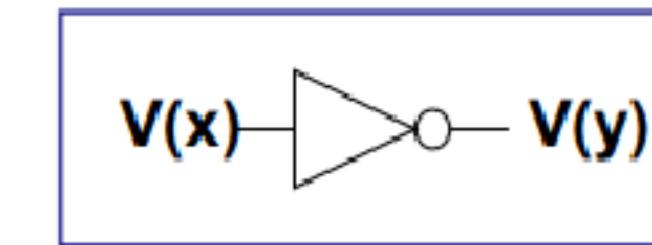
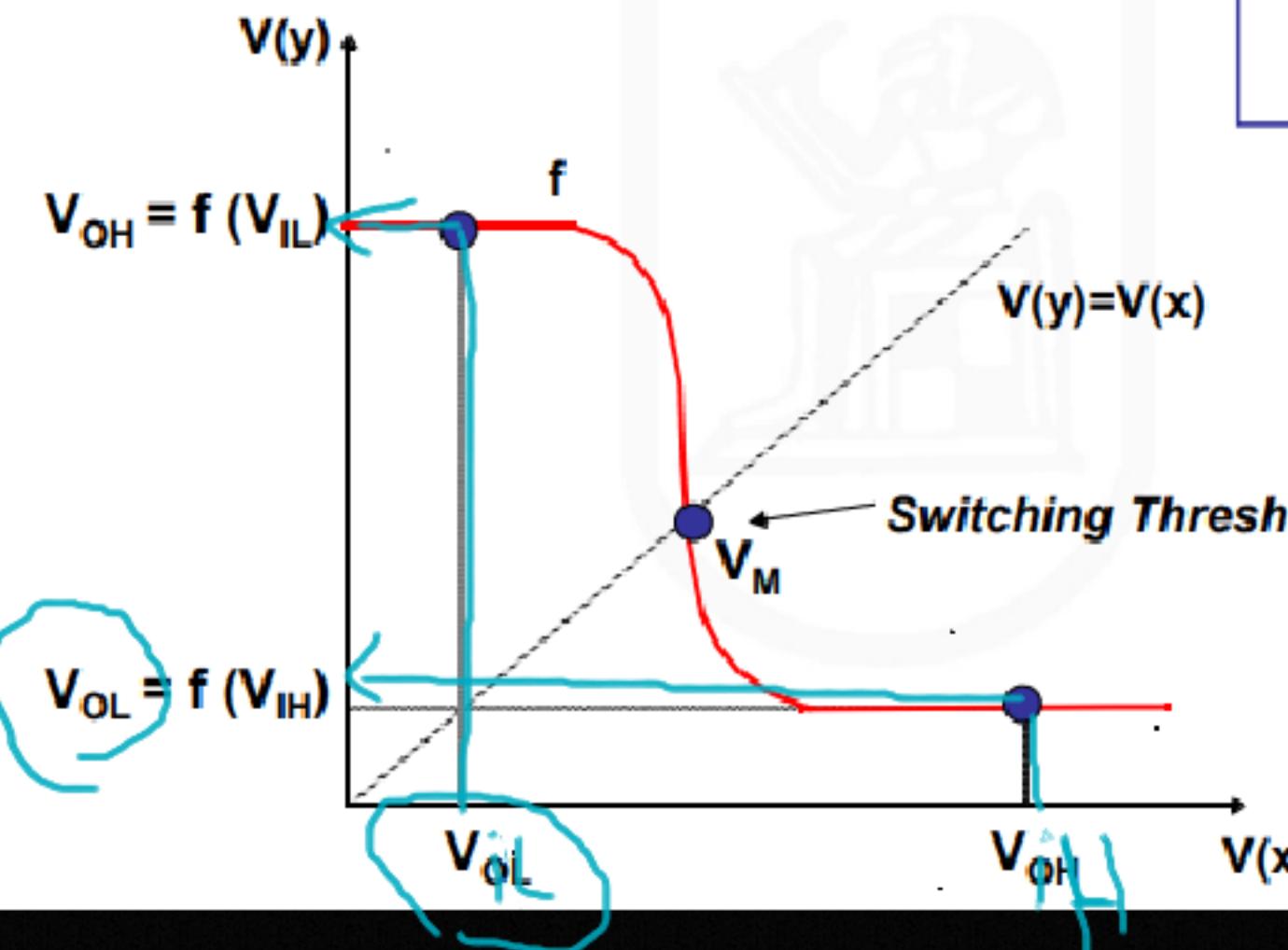
$$V_{OL} = ! (V_{OH})$$

- Difference between V_{OH} and V_{OL} is the logic or signal swing V_{sw}

DC Operation

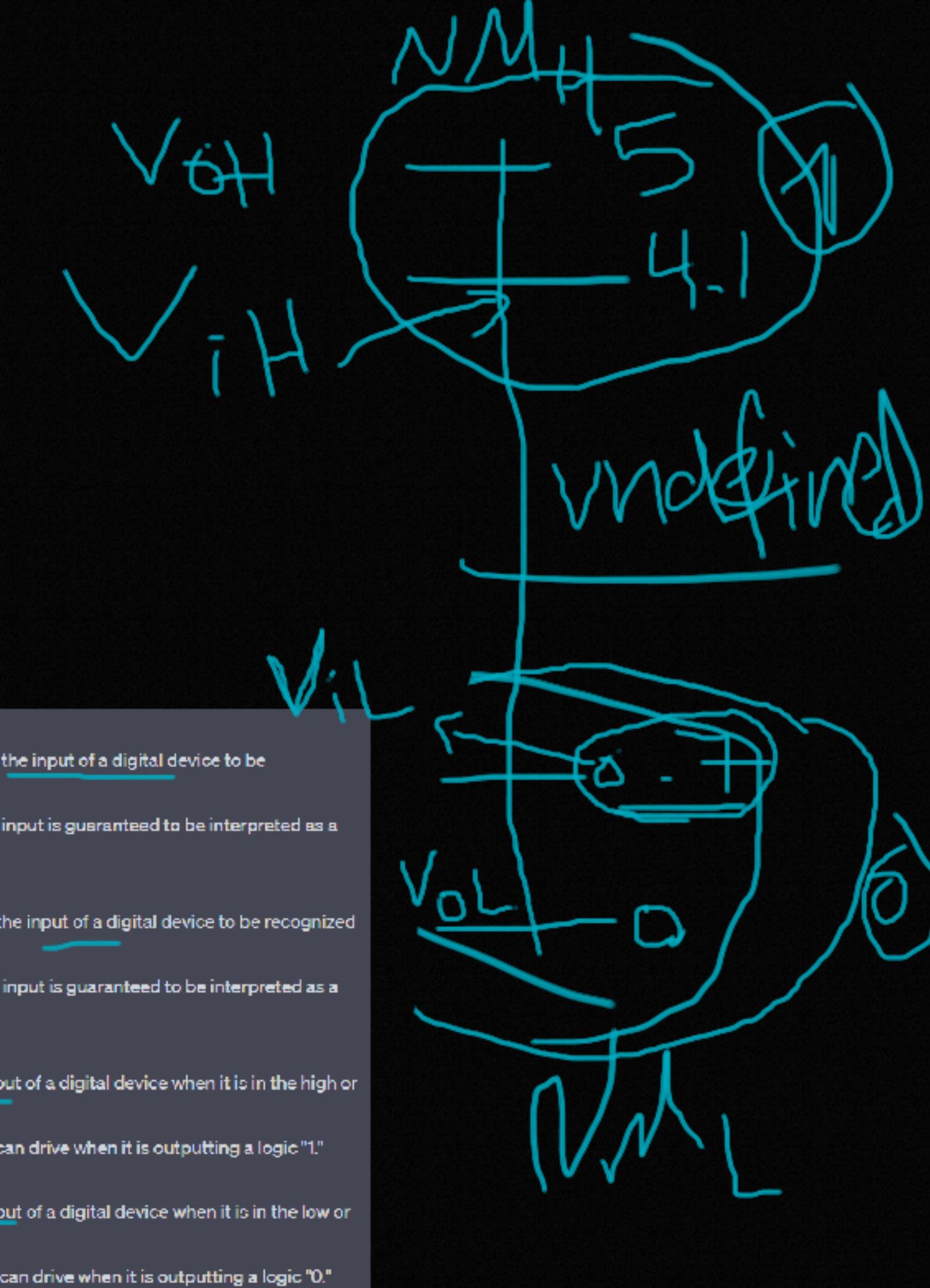
Voltage Transfer Characteristics (VTC)

- Plot of output voltage as a function of the input voltage



1. VIH (Voltage Input High):
 - VIH is the minimum voltage level required at the input of a digital device to be recognized as a high or logic "1."
 - It specifies the voltage level below which the input is guaranteed to be interpreted as a logic "0."
2. VIL (Voltage Input Low):
 - VIL is the maximum voltage level allowed at the input of a digital device to be recognized as a low or logic "0."
 - It specifies the voltage level above which the input is guaranteed to be interpreted as a logic "1."
3. VOH (Voltage Output High):
 - VOH is the minimum voltage level at the output of a digital device when it is in the high or logic "1" state.
 - It specifies the minimum voltage the device can drive when it is outputting a logic "1."
4. VOL (Voltage Output Low):
 - VOL is the maximum voltage level at the output of a digital device when it is in the low or logic "0" state.
 - It specifies the maximum voltage the device can drive when it is outputting a logic "0."

$$NMH = V_{OH} - V_{IH}$$
$$NML = V_{IL} - V_{OL}$$



The Inverter's VTC

- To construct the *VTC* of the CMOS inverter, we need to graphically superimpose the *I-V curves* of the *nMOS* and *pMOS* onto a common coordinate set.
- We can see that:

$$I_{SDp} = I_{DSn}$$

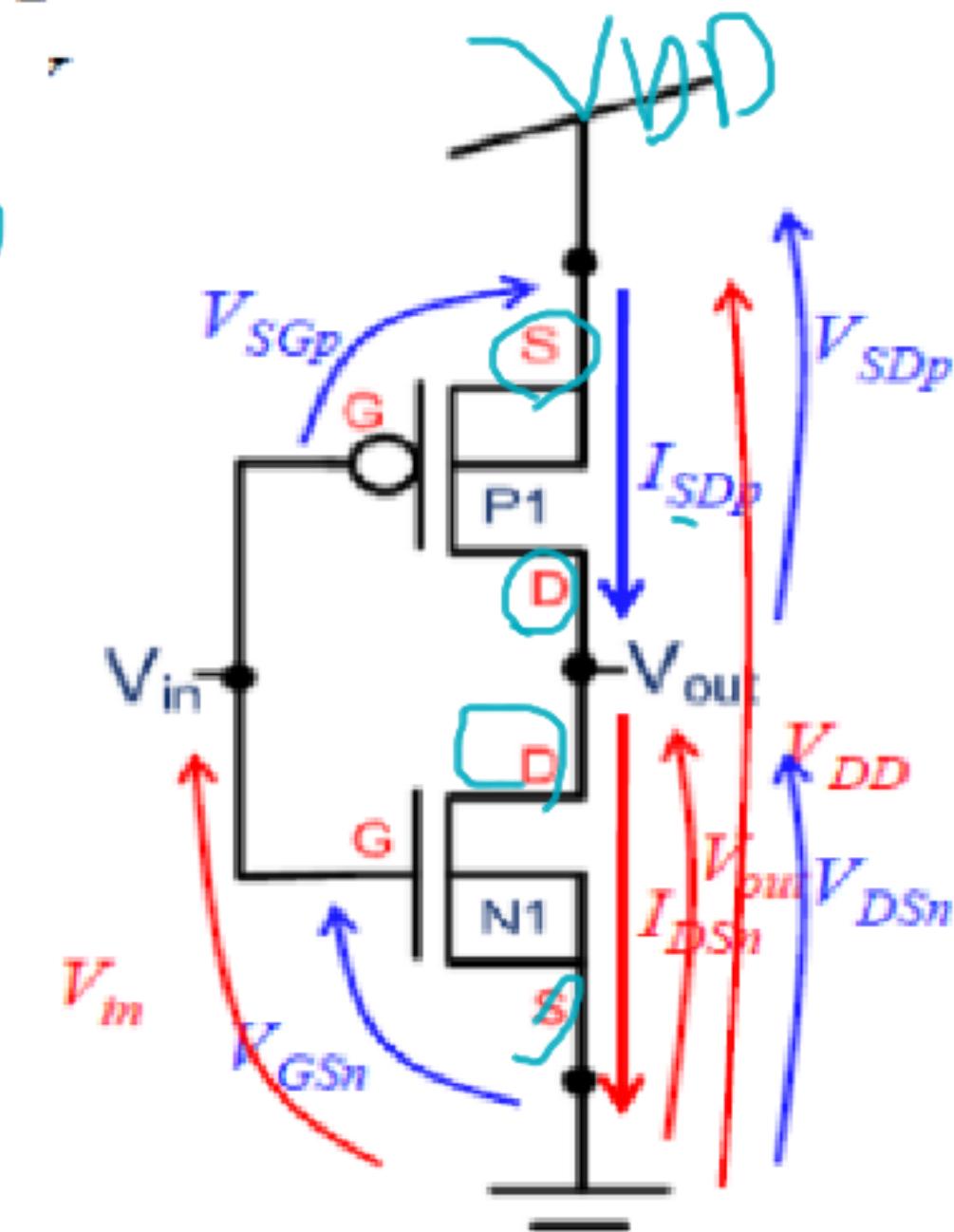
$$V_{SGp} = V_{DD} - V_{in}$$

$$V_{GSn} = V_{in}$$

$$V_{SDp} = V_{DD} - V_{out}$$

$$V_{DSn} = V_{out}$$

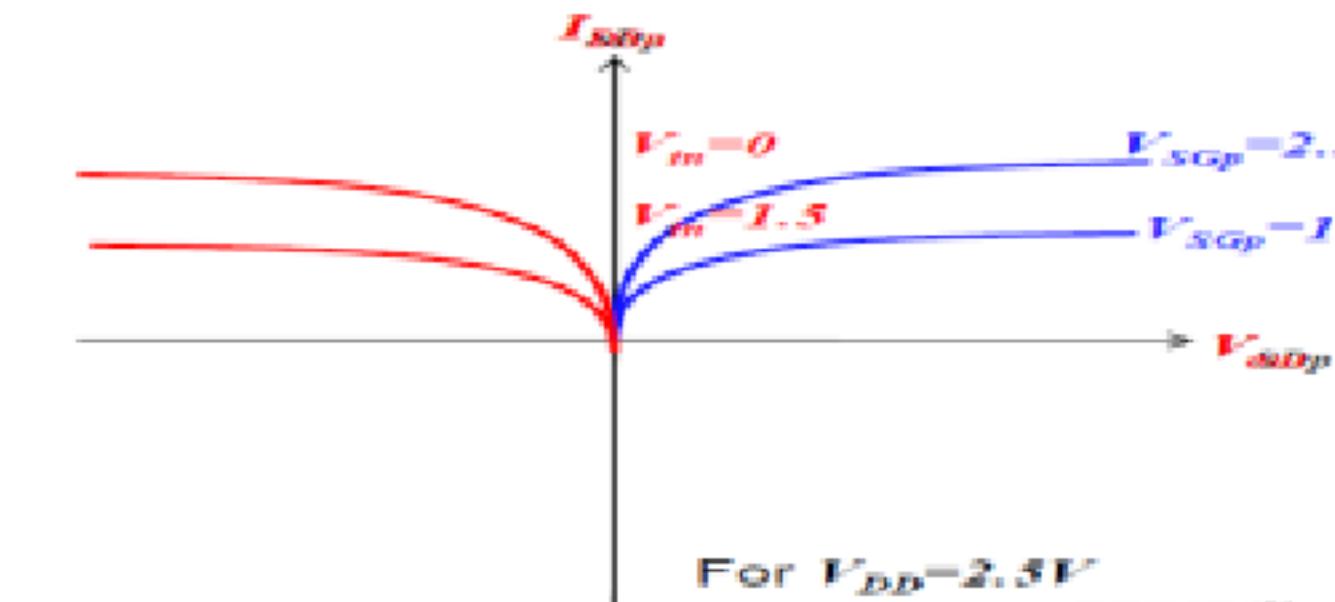
$$V_o = V_{DD} - V_{SGp}$$



The Inverter's VTC

- Since V_{in} and V_{out} are the input and output voltages of the **nMOS** transistor, we will change the coordinates of the **pMOS**.

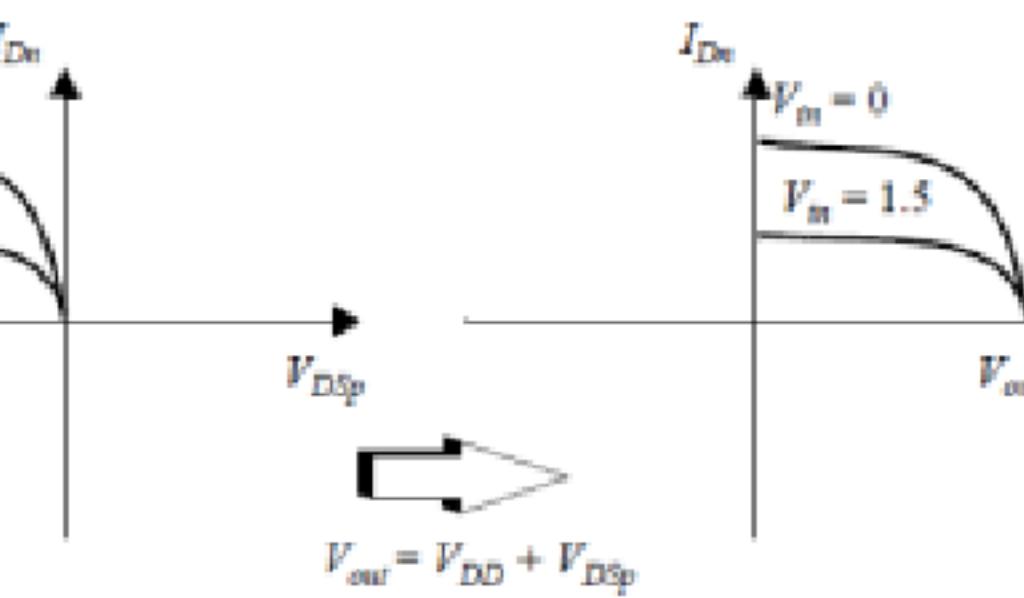
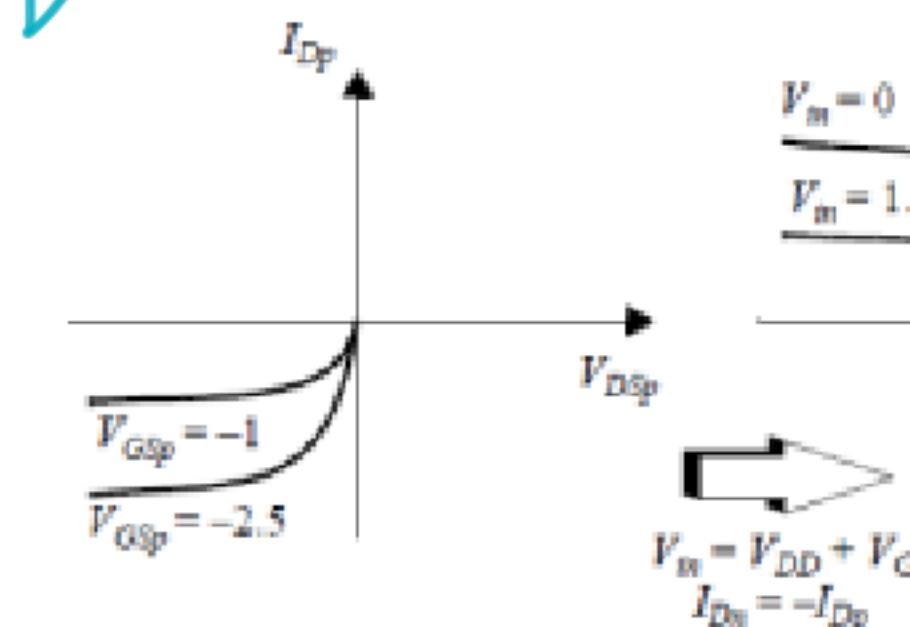
$$V_{out} = V_{DD} - V_{SDp}$$



$$V_{in} = V_{DD} - V_{SGp}$$



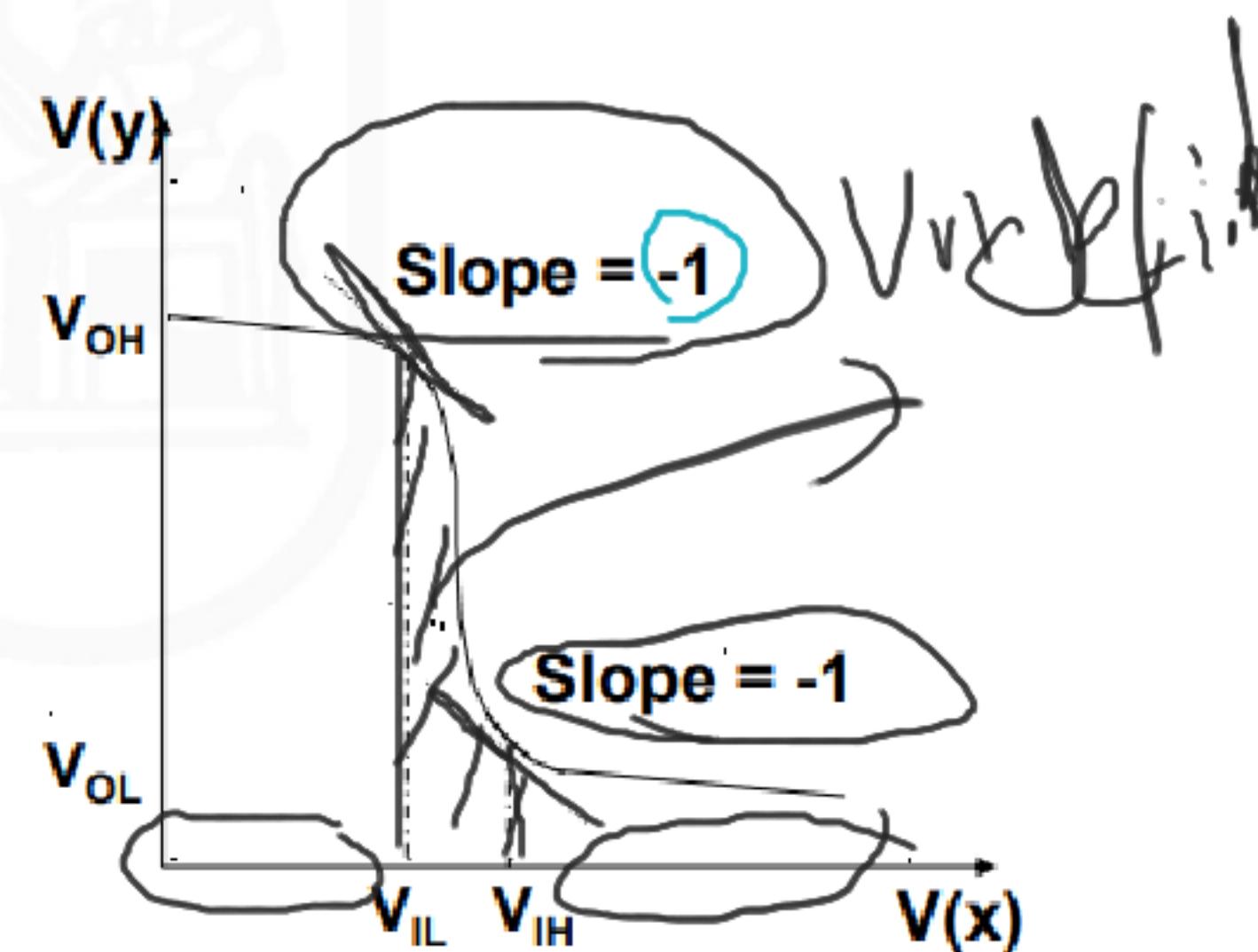
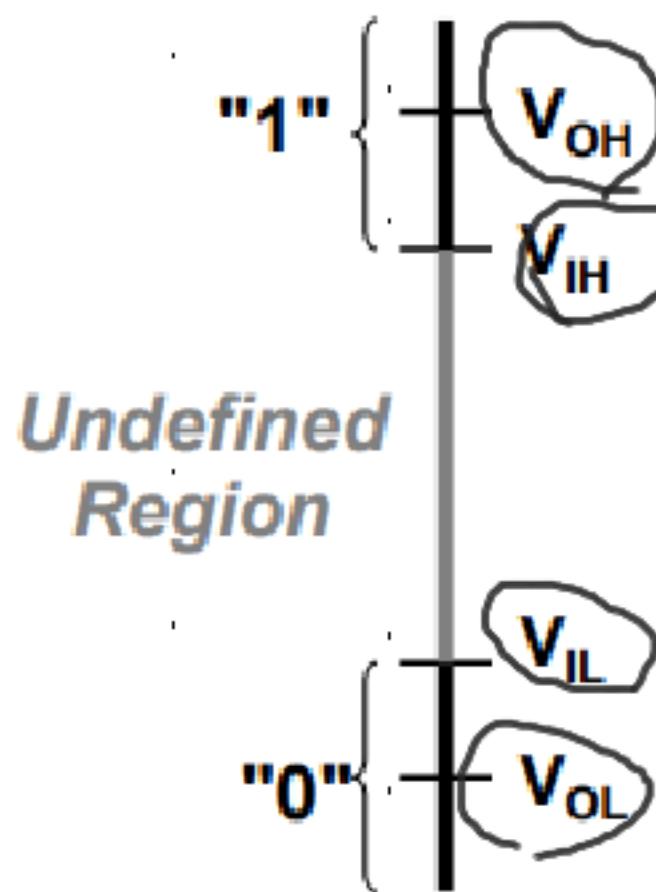
$$I_{DSn} = I_{SDp}$$



Switch to Operating Regions Slides,
Then Return Back

Mapping Logic Levels to the Voltage Domain

- The regions of acceptable high and low voltages are delimited by V_{IH} and V_{IL} that represent the points on the VTC curve where the gain = -1



The major difference between both signals is that the analog signals have continuous electrical signals, while digital signals have non-continuous electrical signals.

With a digital signal, we are using an analog signal to transmit numbers, which we convert into bits and then transmit the bits. A digital signal uses some physical property, such as voltage, to transmit a single bit of information.

=> The noise margin in VLSI is the amount of noise that a CMOS circuit can endure without interfering with its function.

=> The noise margin ensures that any logic '1' signal with finite noise added to it is still identified as logic '1' and not logic '0'.

Noise Margins

- Let's calculate V_{IH} :

$$I_{DSn} (res) = k_n \left[(V_{GSn} - V_T) V_{DSn} - \frac{V_{DSn}^2}{2} \right] = I_{DSp} (sat) = \frac{k_p}{2} (V_{GSp} - V_T)^2$$

- Assuming matching devices ($k_n = k_p$, $V_{Tn} = V_{Tp}$):

$$(V_{IN} - V_T) V_{out} - \frac{V_{out}^2}{2} = \frac{1}{2} (V_{DD} - V_{IN} - V_T)^2$$

- Differentiating and equating -1, we reach:

$$V_{IH} - \frac{1}{8} (5V_{DD} - 2V_T)$$

- Doing the same for V_{IL} or using symmetry, we reach:

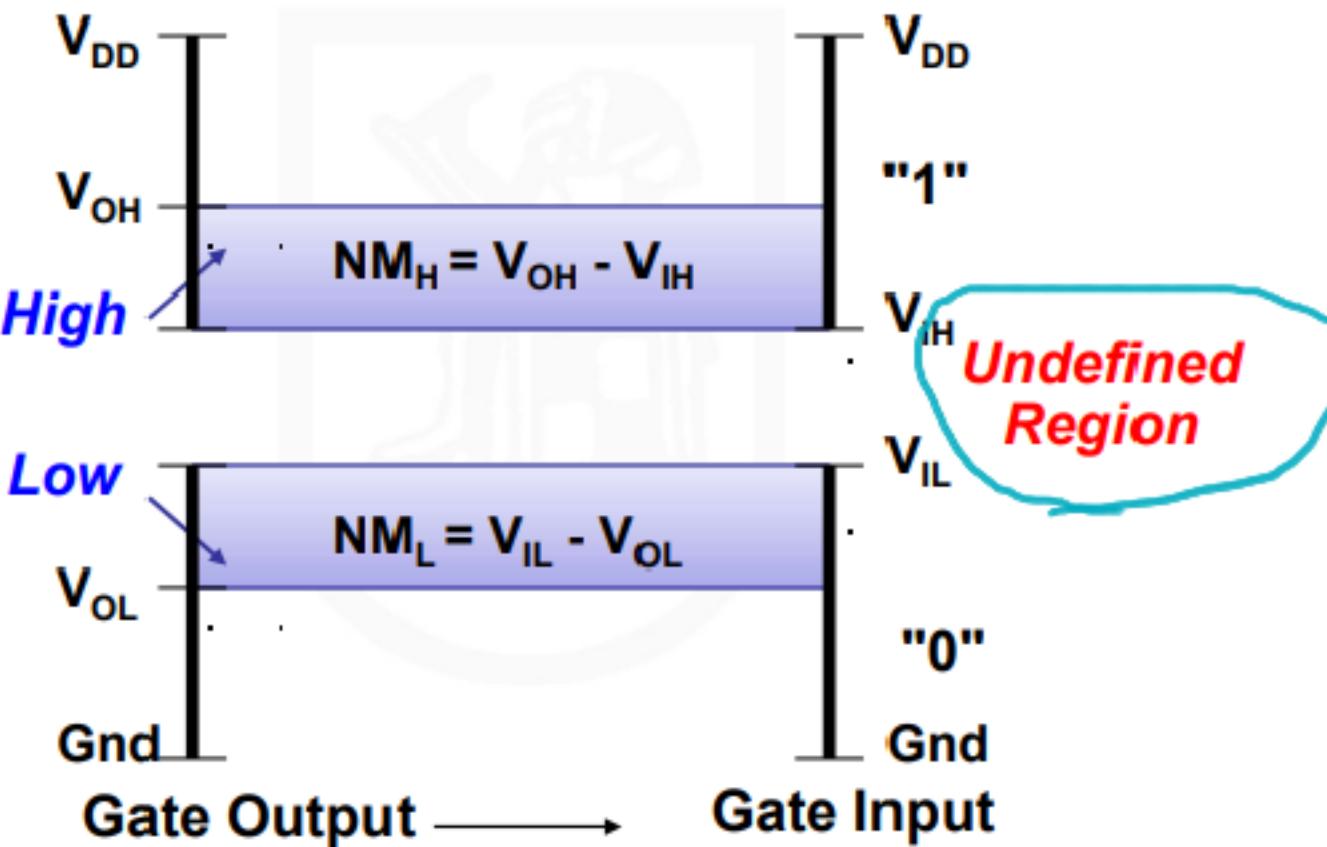
$$V_{IL} = \frac{1}{8} (3V_{DD} + 2V_T)$$

- Accordingly, for a matched *long-channel* device, and assuming $V_{OHmin} \rightarrow V_{OHmax}$ and $V_{OLmax} \rightarrow V_{OLmin}$ in CMOS, we get:

$$NM_H = NM_L \approx V_{DD} - V_{IH} = V_{IL} - 0 = \frac{1}{8} (3V_{DD} + 2V_T)$$

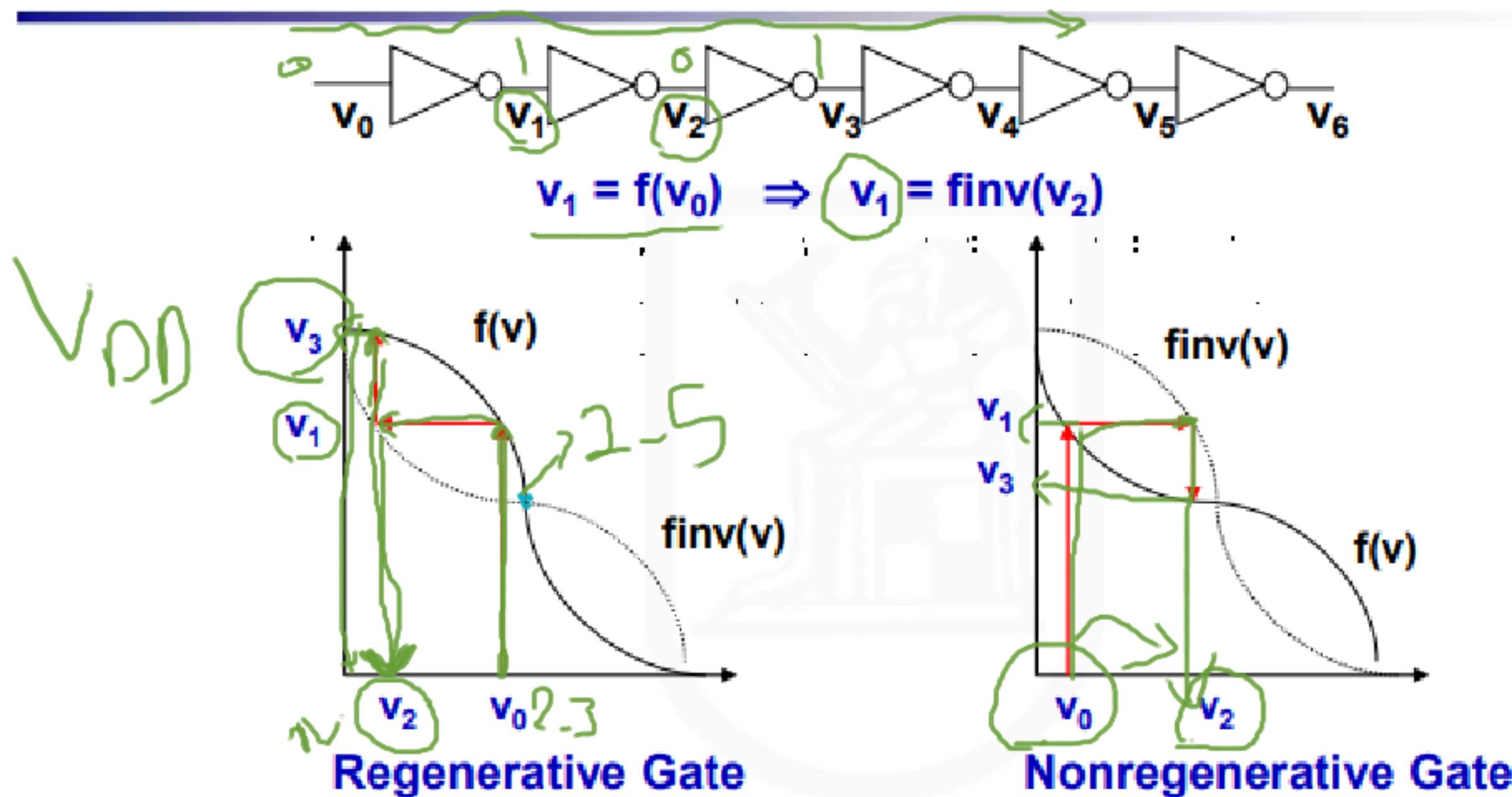
Noise Margins

- For robust circuits, want the "0" and "1" intervals to be as large as possible



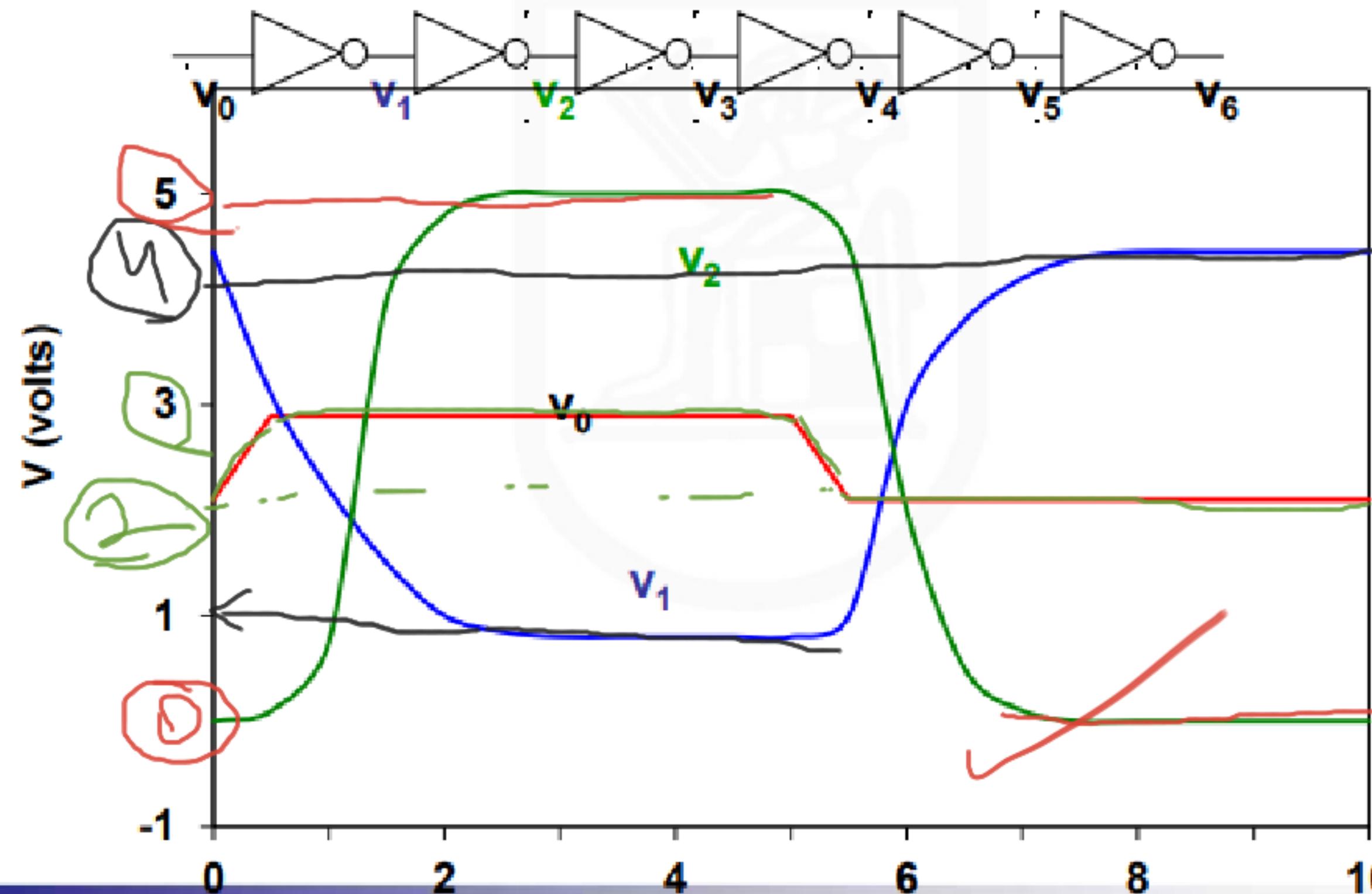
- Large noise margins are desirable, but not sufficient

The Regenerative Property



- The VTC must have a transient region with a gain greater than 1 (in absolute value) bordered by two valid zones where the gain is smaller than 1. Such a gate has two stable operating points.

- A gate with regenerative property ensures that a disturbed signal converges back to a nominal voltage level



Noise Immunity

- Noise margin expresses the ability of a circuit to overpower a noise source
 - noise sources: supply noise, cross talk, interference, offset
- Absolute noise margin values are deceptive
 - a floating node is more easily disturbed than a node driven by a low impedance (in terms of voltage)
- **Noise immunity** expresses the ability of the system to process and transmit information correctly in the presence of noise
- For good noise immunity, the signal swing (i.e., the difference between V_{OH} and V_{OL}) and the noise margin have to be large enough to overpower the impact of fixed sources of noise

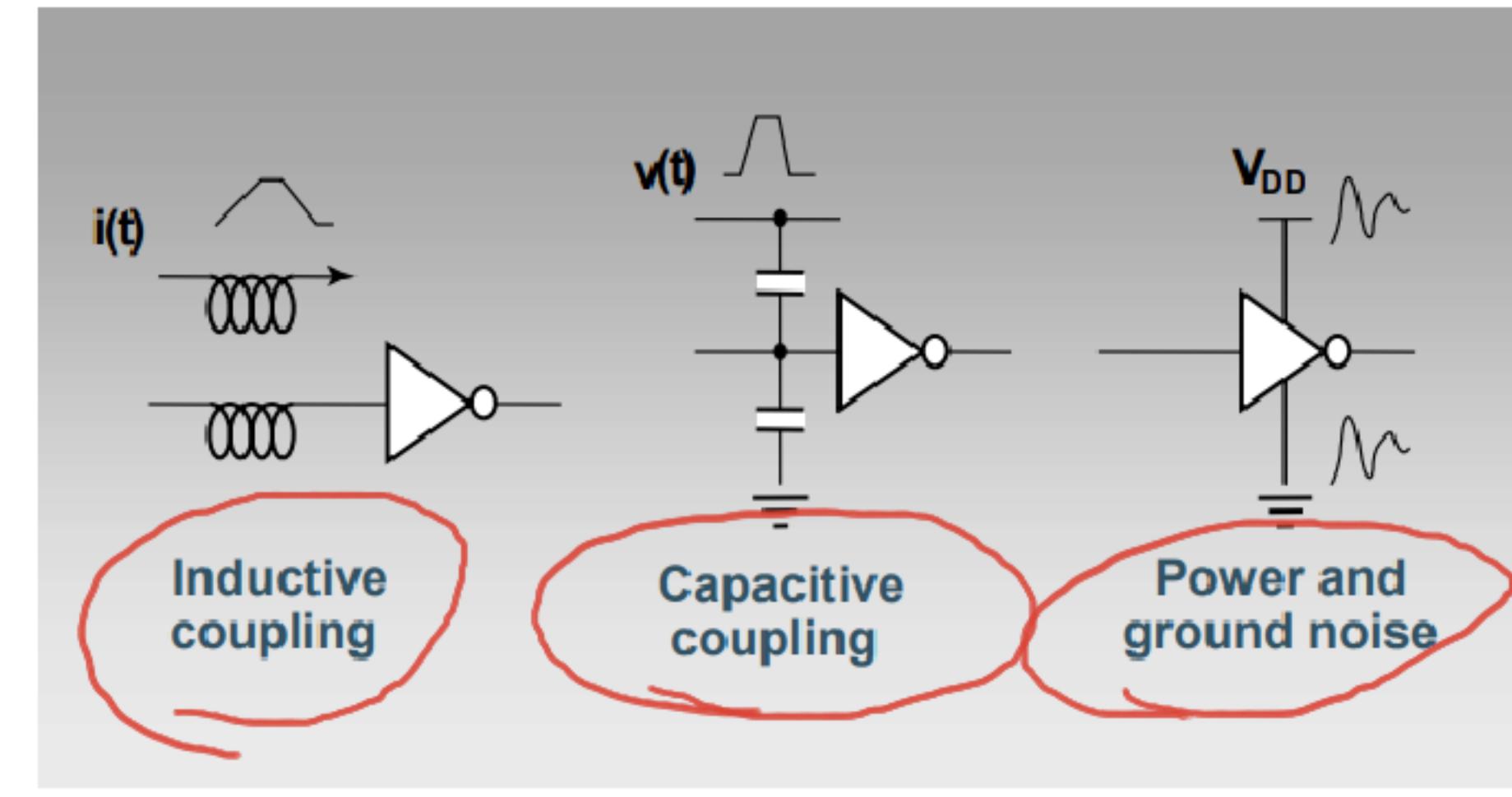
Reliability:

=> is the probability that a system performs correctly during a specific time duration.

=> During this correct operation: No repair is required or performed.

=> The system follows the defined performance specifications.

Noise in Digital Integrated Circuits



Noise:

=> is one of the biggest challenges in IC design, especially for applications that require high performance, precision, and reliability

=> Noise can degrade the signal quality, increase the power consumption, and cause errors or failures in the IC.

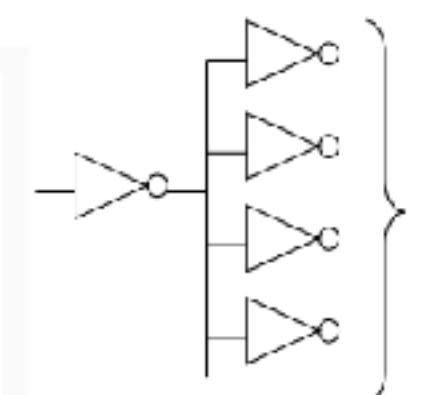
Directivity

- A gate must be **unidirectional**: changes in an output level should not appear at any unchanging input of the same circuit
 - In real circuits, full directivity is an illusion (e.g., due to capacitive coupling between inputs and outputs)
- Key metrics: **output impedance** of the driver and **input impedance** of the receiver
 - ideally, the output impedance of the driver should be zero and
 - input impedance of the receiver should be infinity

Fan-In and Fan-Out

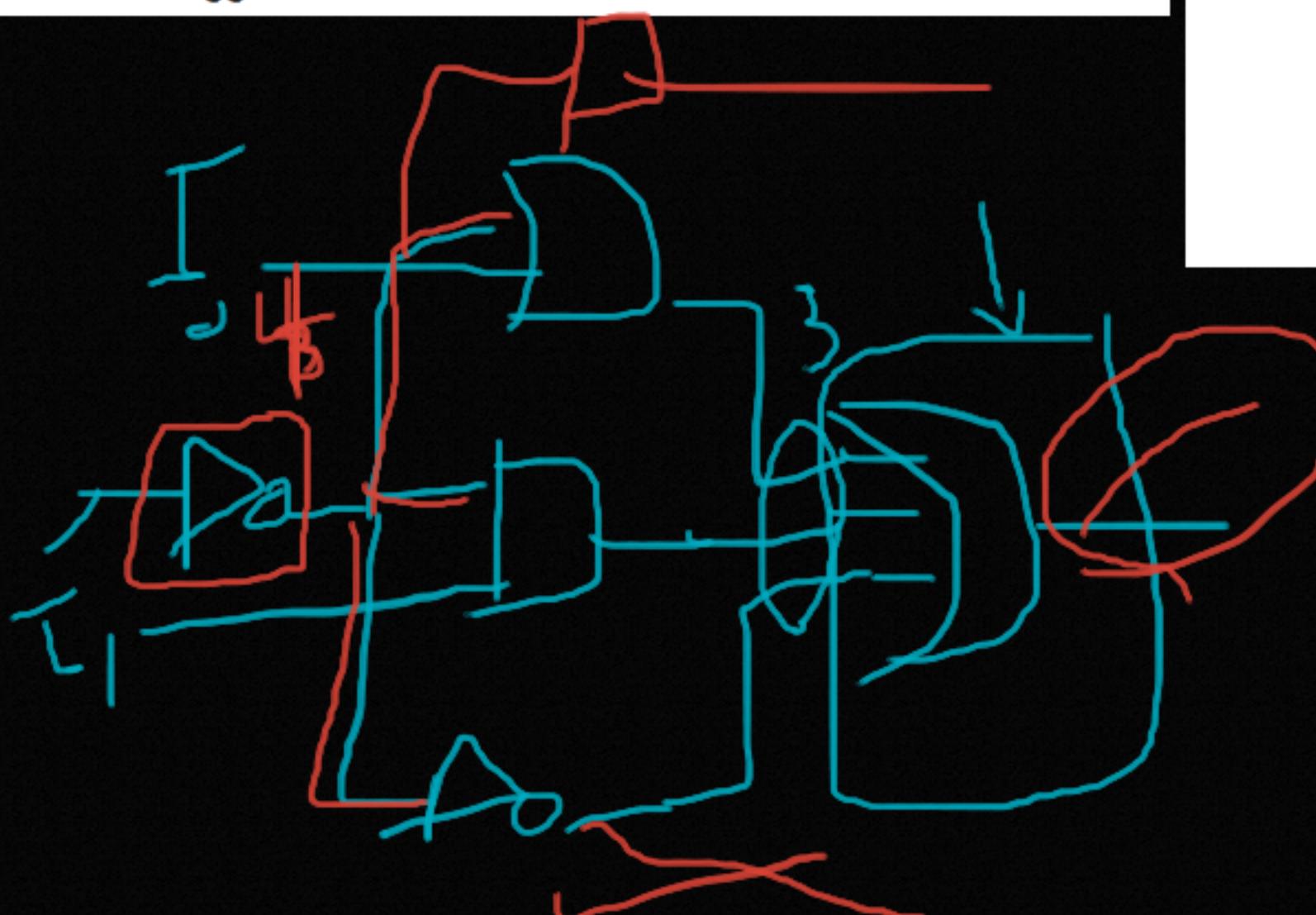
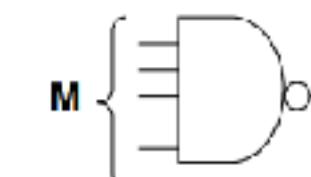
- Fan-out – number of load gates connected to the output of the driving gate

- gates with large fan-out are slower



- Fan-in – the number of inputs to the gate

- gates with large fan-in are bigger and slower



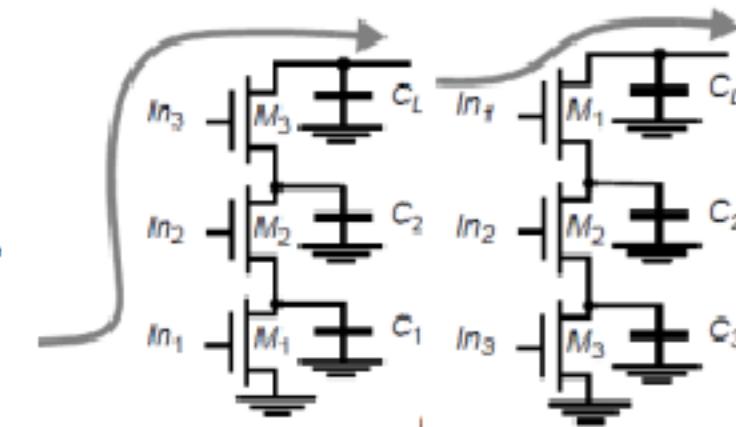
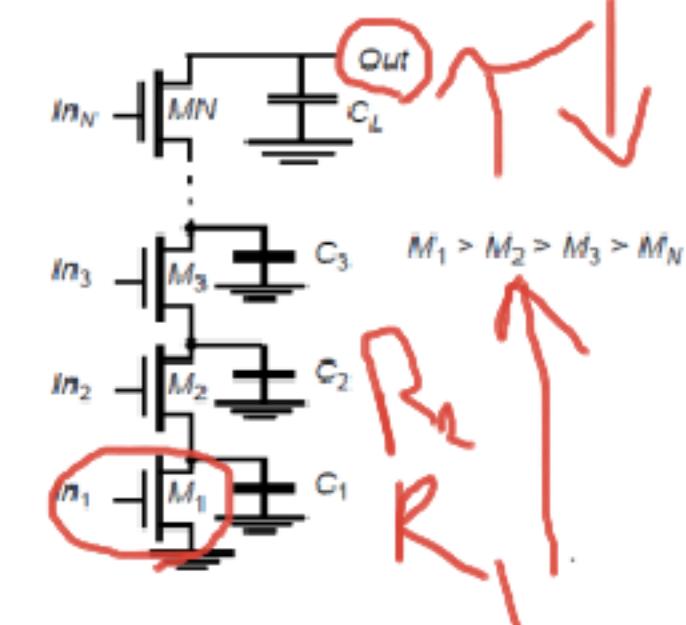
Design Techniques for Large Fan-in

1. **Transistor Sizing:** This lowers the resistance of devices in series and lowers the time constant.

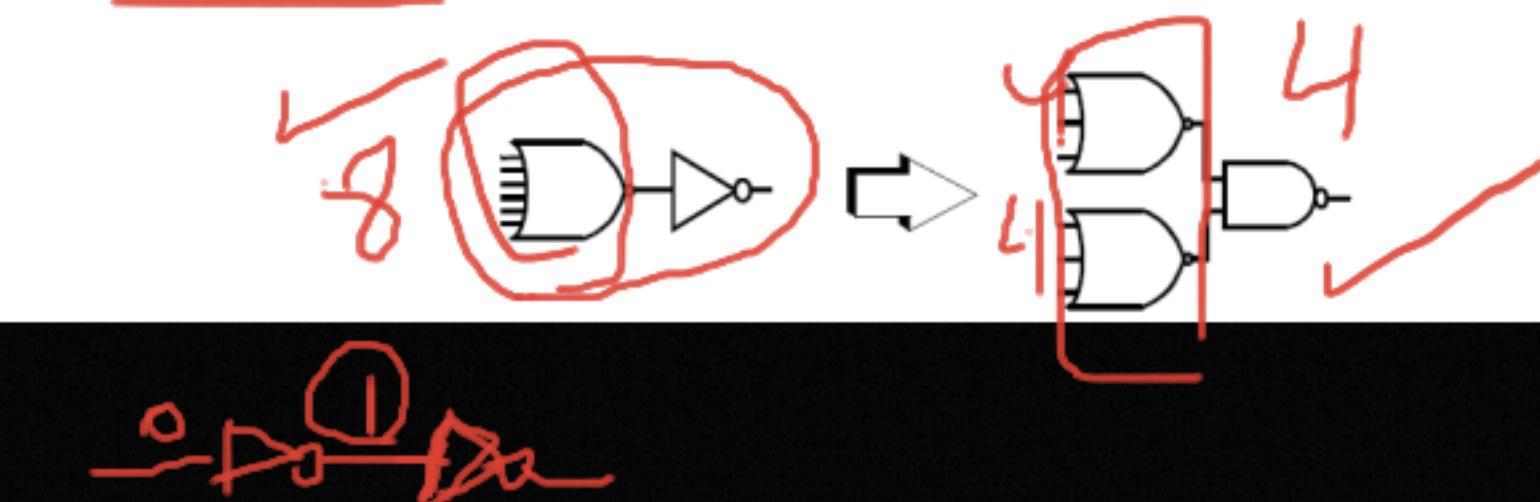
2. **Progressive Transistor Sizing:** in which each transistor is scaled up uniformly, that R_1 should be made the smallest, R_2 the next smallest, etc.

3. **Input Re-Ordering:** An input signal to a gate is called critical if it is the last signal of

4. **All inputs to assume a stable value.** The path through the logic which determines the ultimate speed of the structure is called the **critical path**. Putting the critical-path transistors closer to the output of the gate can result in a speedup.



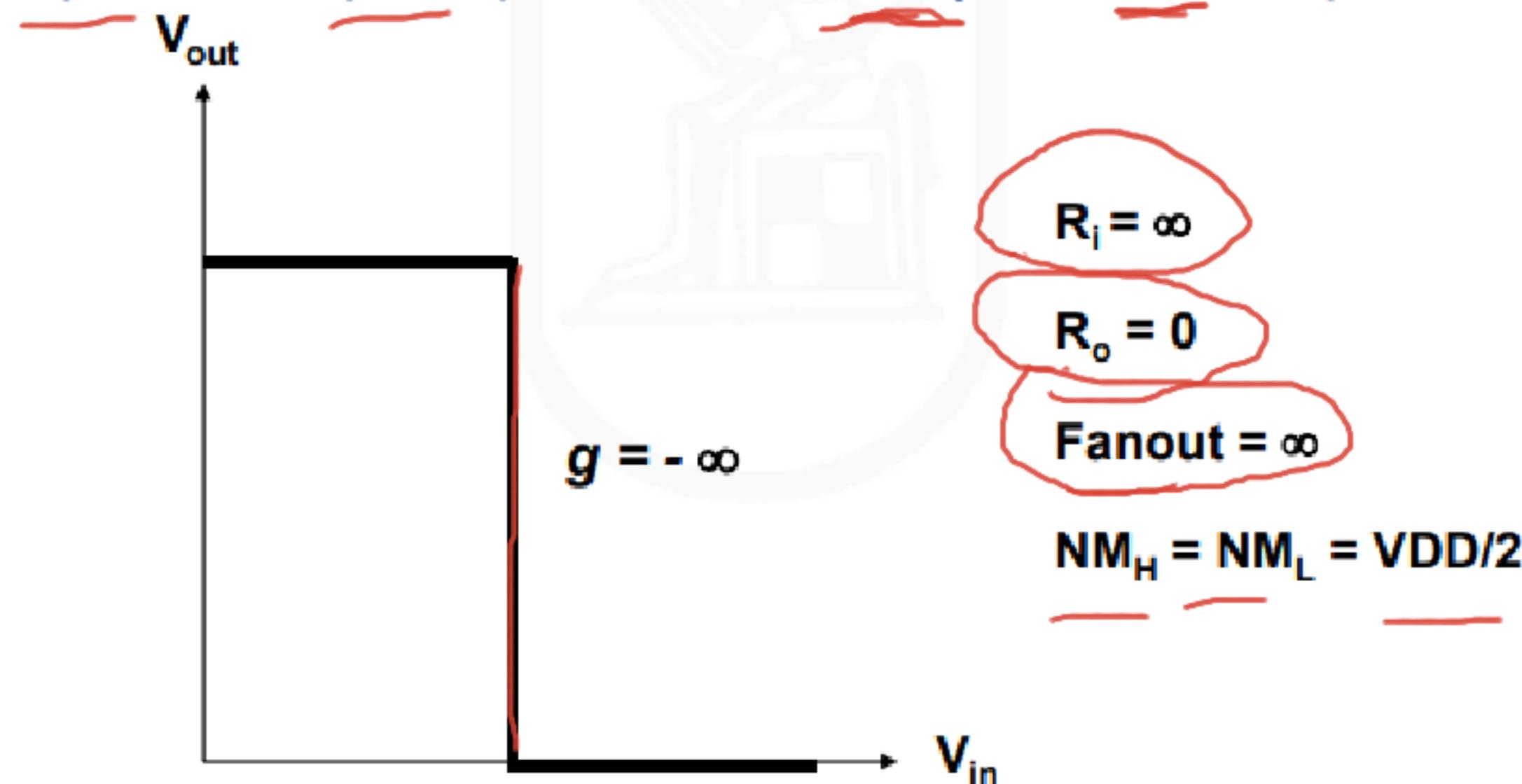
- Logic Restructuring: Manipulating the logic equations can reduce the fan-in requirements and hence reduce the gate delay



The Ideal Inverter



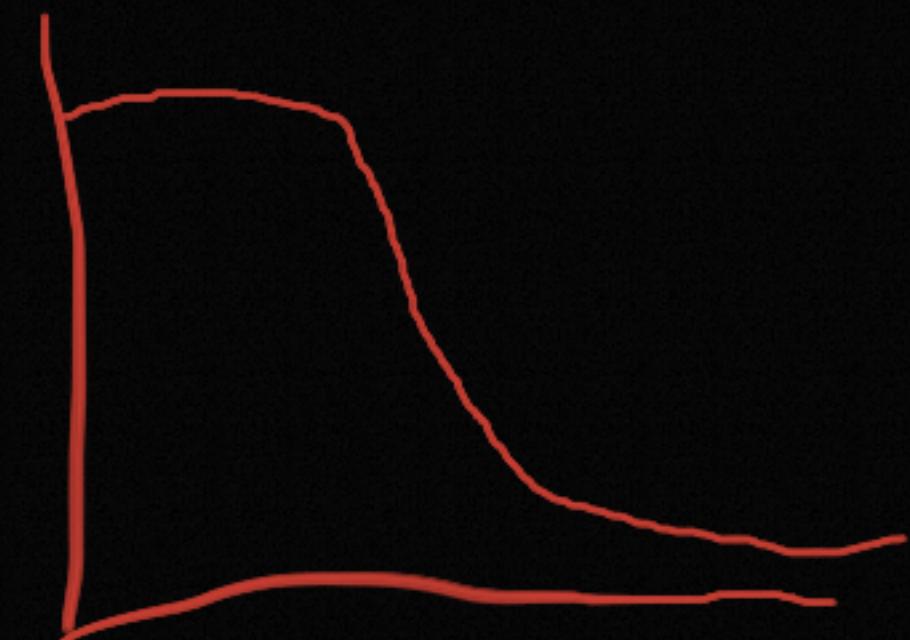
- The ideal gate should have
 - infinite gain in the transition region
 - a gate threshold located in the middle of the logic swing
 - high and low noise margins equal to half the swing
 - input and output impedances of infinity and zero, resp.



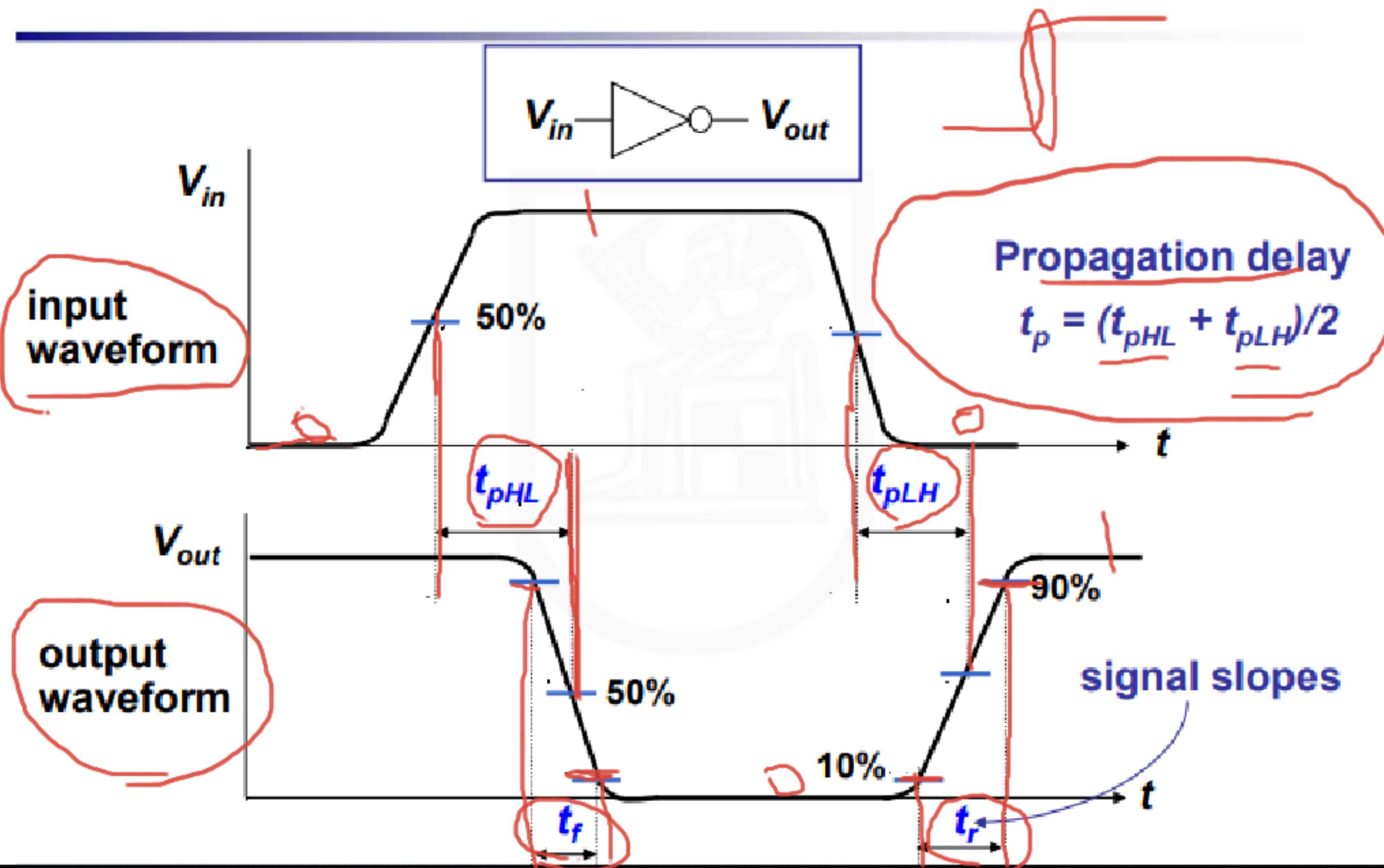
It should:

- 1- dissipate no power
- 2- have zero propagation delay
- 3- controlled rise and fall times
- 4- have noise immunity equal to 50% of the logic swing.

==> The properties of CMOS (complementary MOS) begin to approach these ideal characteristics.



Delay Definitions



Gate delay is the time taken for a signal at the output of a gate to reach 50% of (logic 1 level) after the signal at the input of the gate has reached 50% of .

$$T_p = (t_{phl} + t_{plh}) / 2$$

t_pH: propagation delay (High to low)

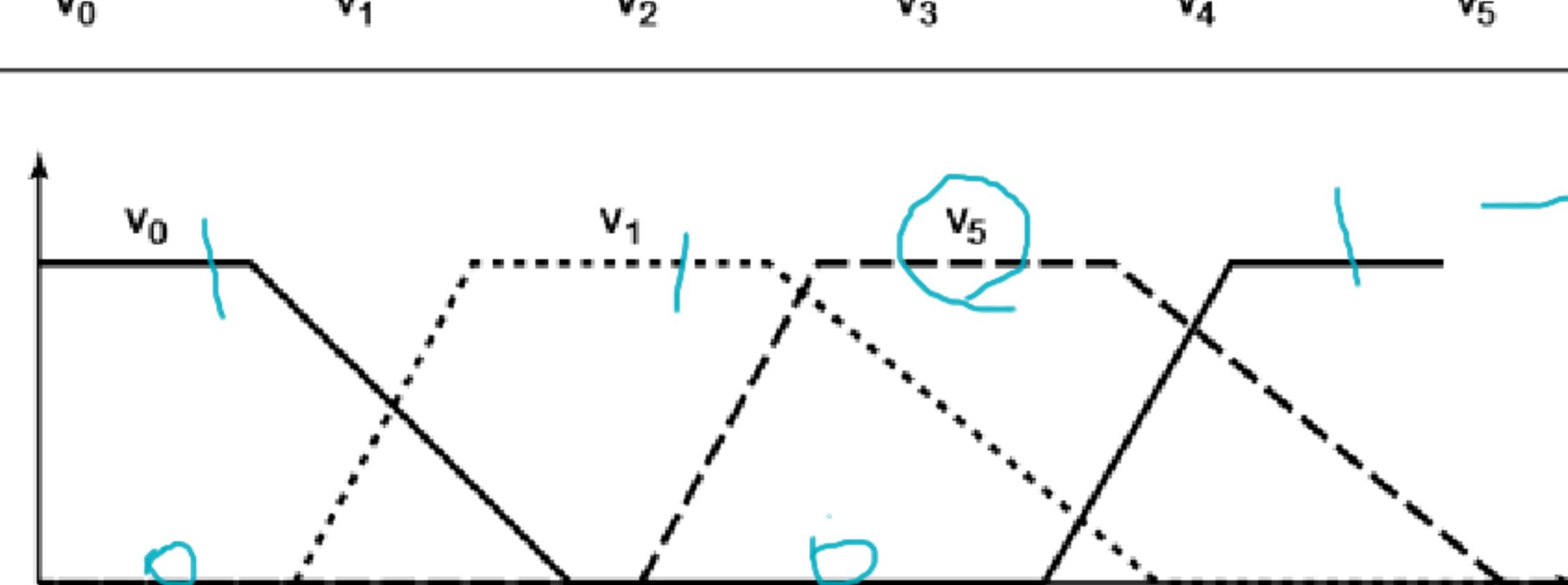
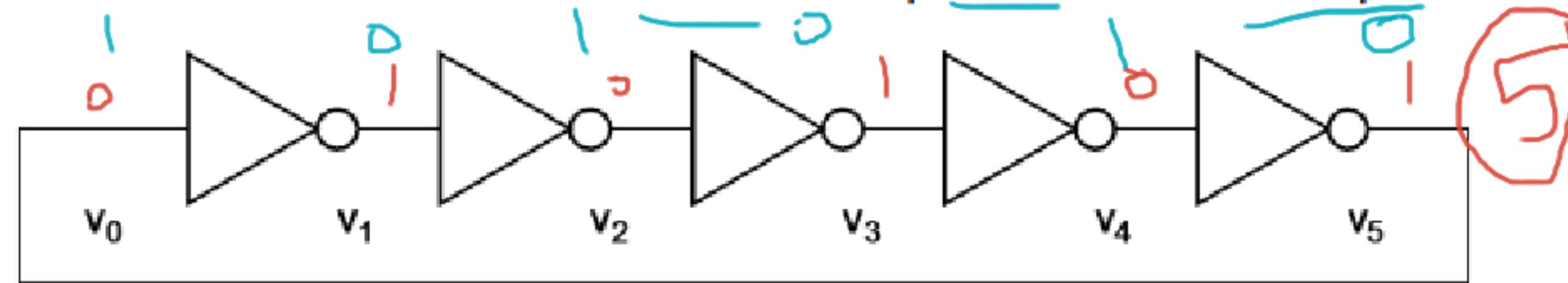
t_pL: propagation delay (low to high)

T_f: fall time.

T_r: rise time.

Ring Oscillator

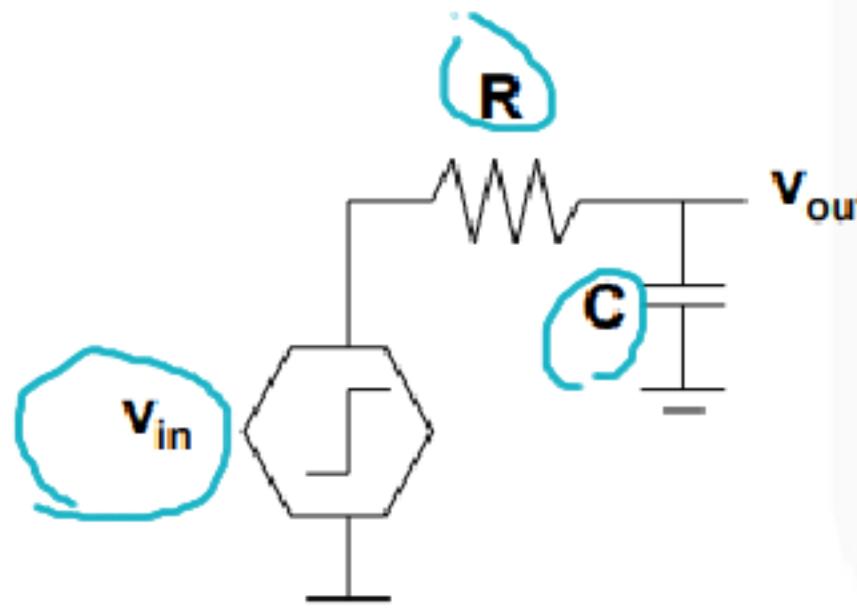
Gate delay is a function of the amount of resistance and capacitance in the current path.



$$T = 2 \times t_p \times N$$

Modeling Propagation Delay

- Model circuit as first-order RC network



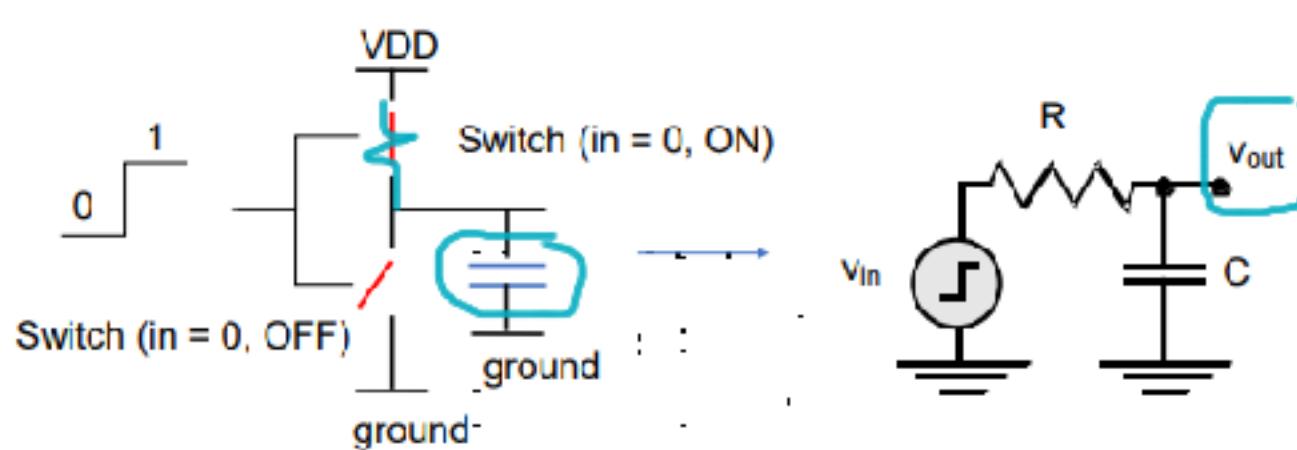
$$V_{out}(t) = (1 - e^{-t/\tau})V$$

where $\tau = RC$

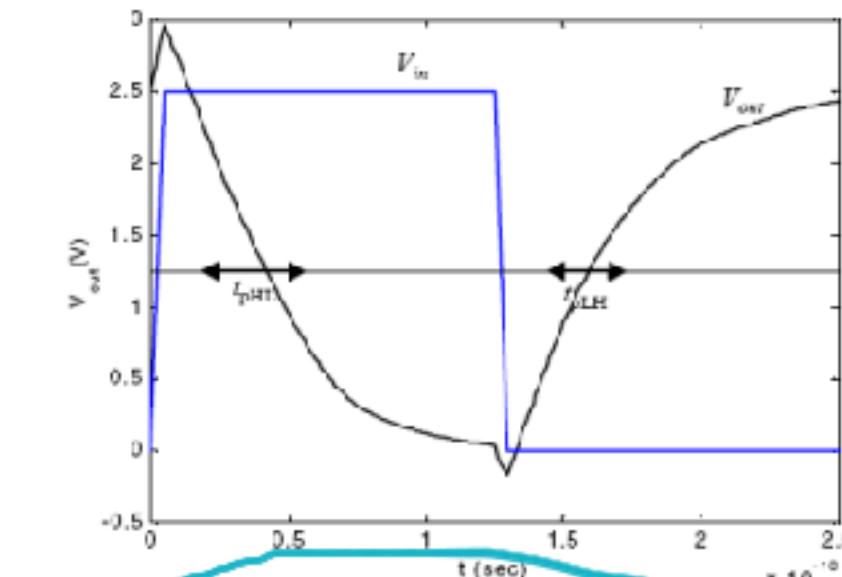
Time to reach 50% point
 $t = \ln(2) \tau = 0.69 \tau$

Time to reach 90% point is
 $t = \ln(9) \tau = 2.2 \tau$

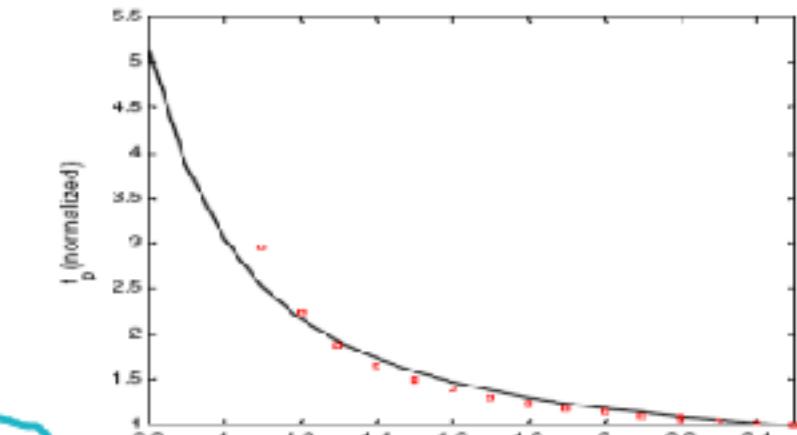
□ Matches the delay of an inverter gate



Transient Response

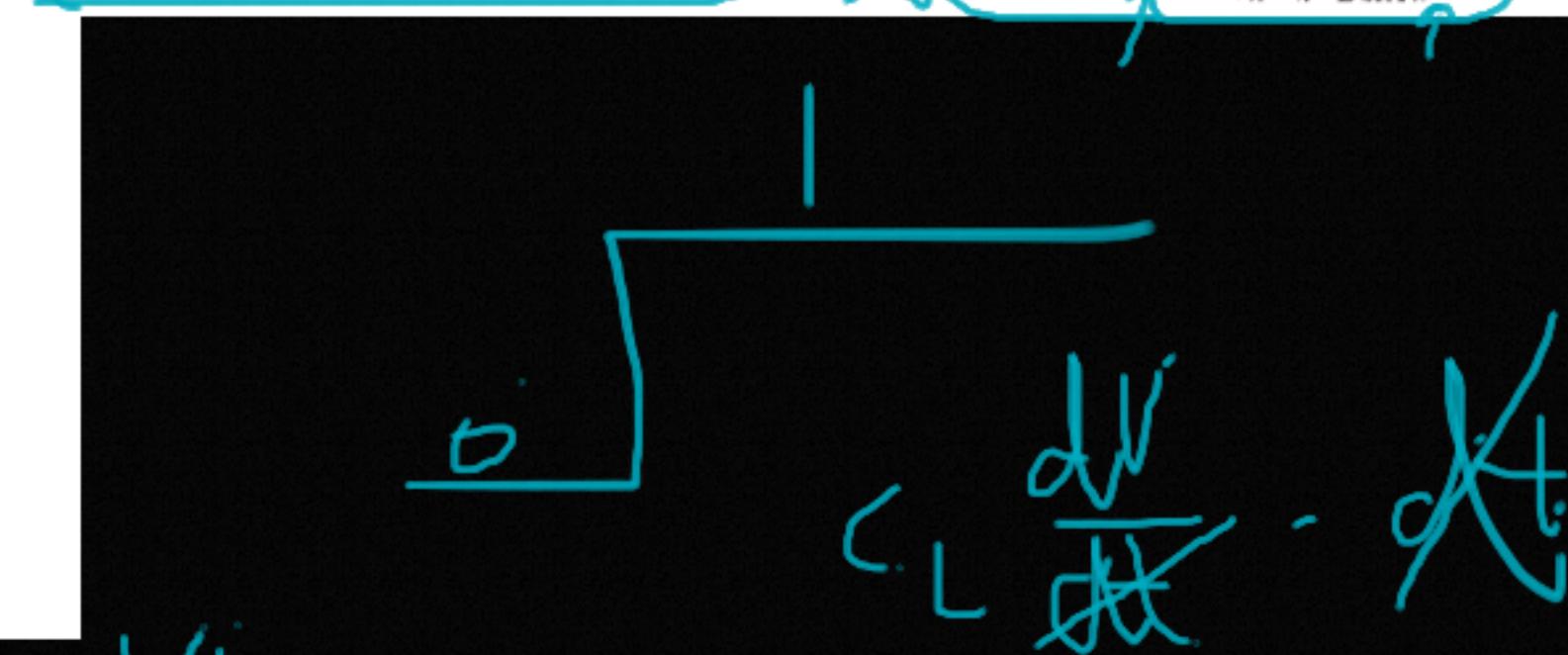


Hand calculated
 $t_{pHL} = 0.69 \times (13\text{Kohm}/1.5) \times 6.1\text{fF} = 36\text{psec}$
 $t_{pLH} = 0.69 \times (31\text{kohm}/4.5) \times 6.1\text{fF} = 29\text{psec}$
 Thus, $t_p = 32.5\text{psec}$



Reduce C_L .
 Increase the W/L ratio of the transistors.
 Increase V_{DD} .

$$t_{pHL} \approx 0.52 \frac{C_L}{(W/L)_n k'_n V_{DSATn}}$$



$$E_{0 \rightarrow 1} = \int_0^T P(t) dt = V_{dd} \int_0^T i_{supply}(t) dt = V_{dd} \int_0^T C_L dV_{out} = C_L \cdot V_{dd}^2$$

$$E_{cap} = \int_0^T P_{cap}(t) dt = \int_0^T V_{out} i_{cap}(t) dt = \int_0^T C_L V_{out} dV_{out} = \frac{1}{2} C_L \cdot V_{dd}^2$$

Power and Energy Dissipation

- Power consumption: how much energy is consumed per operation and how much heat the circuit dissipates
 - supply line sizing (determined by peak power)
$$P_{\text{peak}} = V_{dd} i_{\text{peak}}$$
 - battery lifetime (determined by average power dissipation)
$$p(t) = v(t)i(t) = V_{dd}i(t)$$
$$P_{\text{avg}} = 1/T \int p(t) dt = V_{dd}/T \int i_{dd}(t) dt$$
 - packaging and cooling requirements
- Two important components: static and dynamic

$$P (\text{watts}) = C_L V_{dd}^2 f_{0 \rightarrow 1} + t_{sc} V_{dd} I_{\text{peak}} f_{0 \rightarrow 1} + V_{dd} I_{\text{leakage}}$$

Short Circuit

Power and Energy Dissipation

- Propagation delay and the power consumption of a gate are related
- Propagation delay is (mostly) determined by the speed at which a given amount of energy can be stored on the gate capacitors
 - the faster the energy transfer (higher power dissipation) the faster the gate
- For a given technology and gate topology, the product of the power consumption and the propagation delay is a constant
 - **Power-delay product (PDP)** – energy consumed by the gate per switching event = $P_{av} \times t_p$
 - An ideal gate is one that is fast and consumes little energy, so the ultimate quality metric is
 - **Energy-delay product (EDP)** = $E \times t_p$ = power × delay²

$P \uparrow$
 $P_{delay} \downarrow$