

Lab 5: INVERTER LAYOUT SETUP

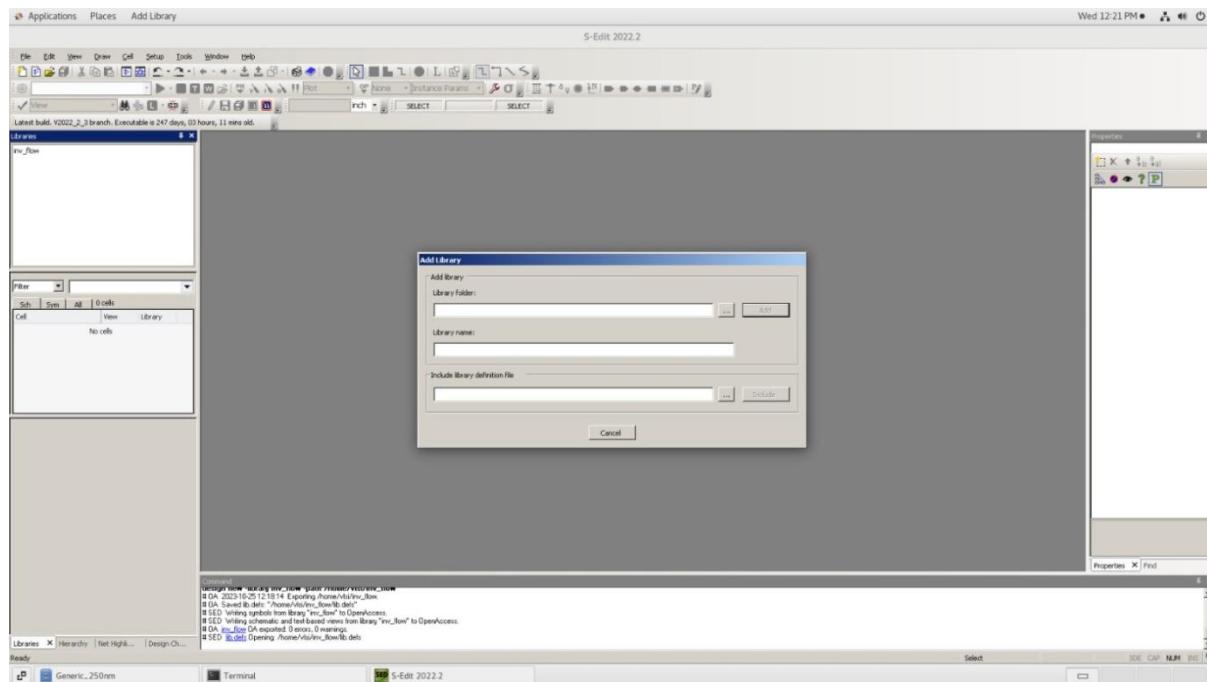
Objective

The objective of this lab is to go through the full design flow of inverter, including frontend and backend flow (Design, Simulation, layout, DRC, LVS, Parasitic extraction and post layout simulation).

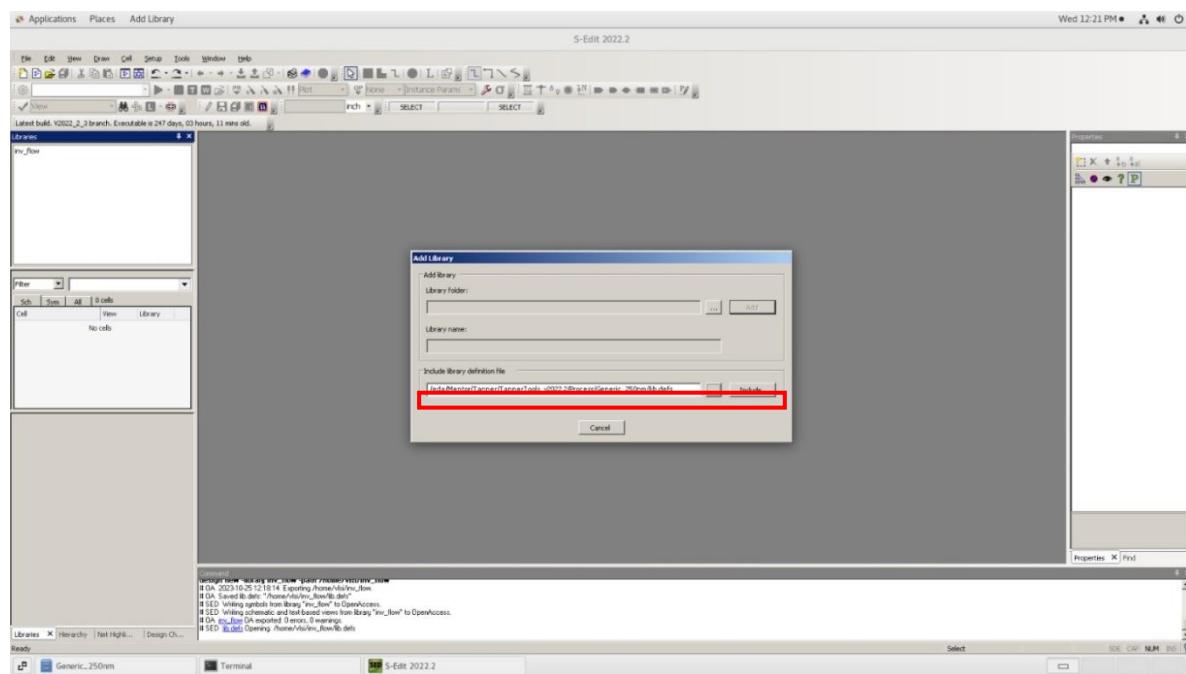
Frontend Flow

1. Include libraries

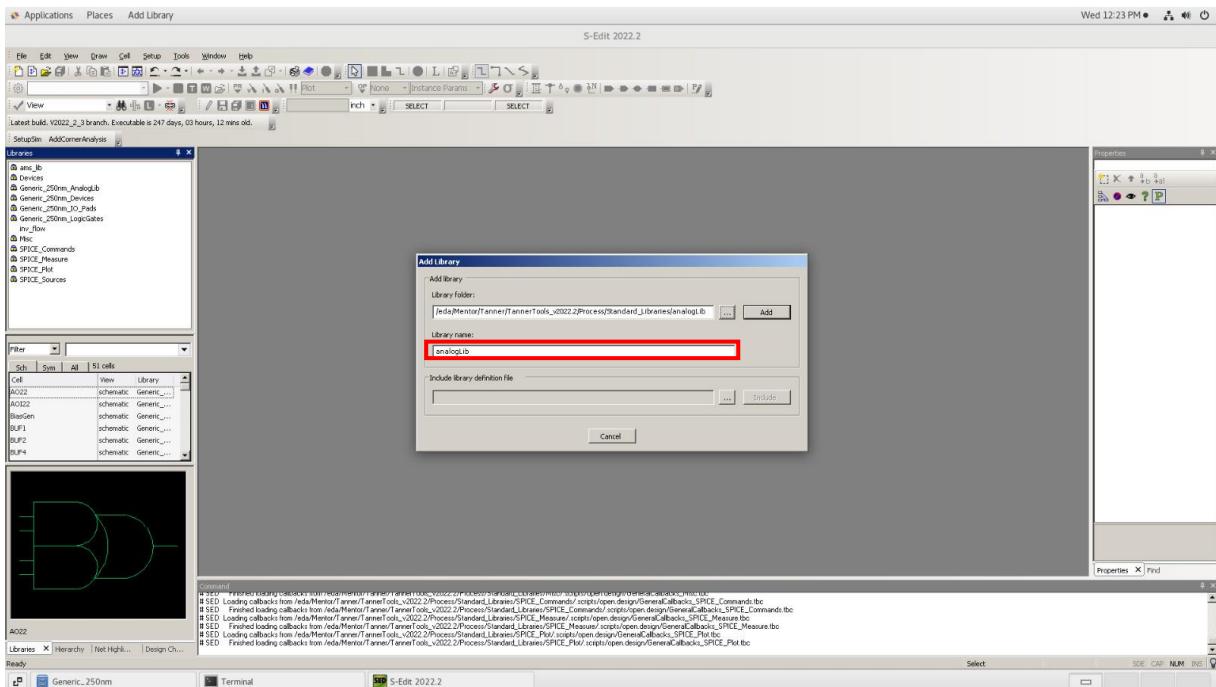
Note: All Libraries used are from technology 2022.



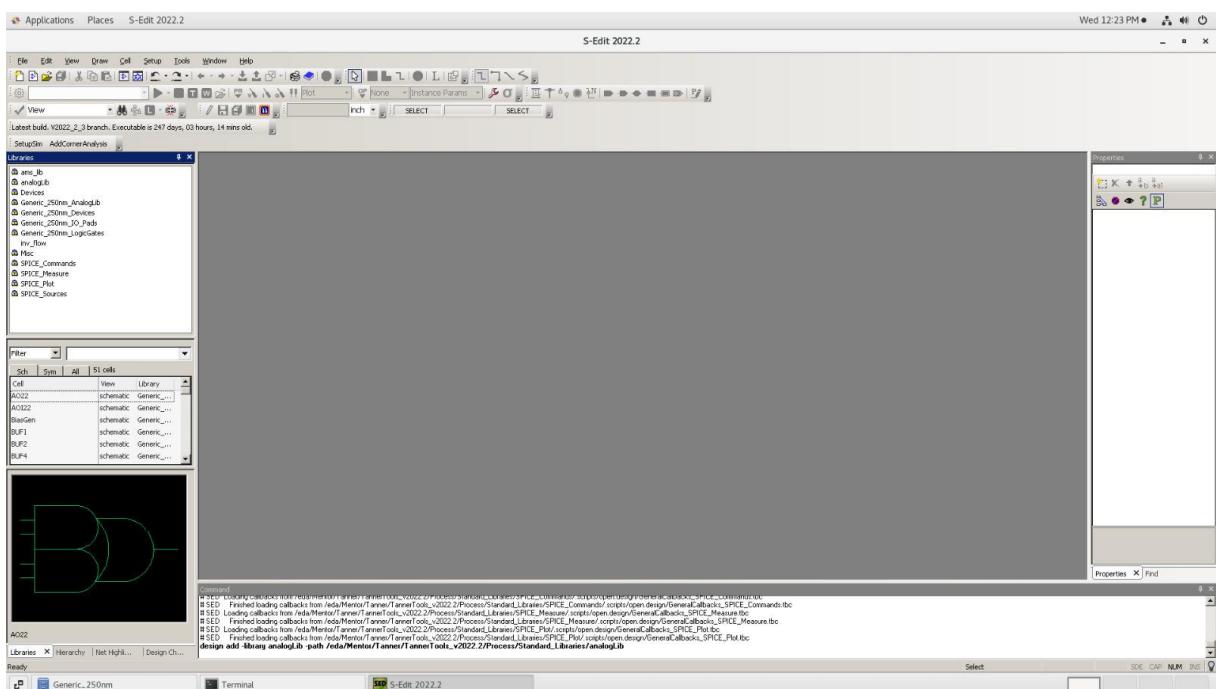
Include all libraries in one step 😊



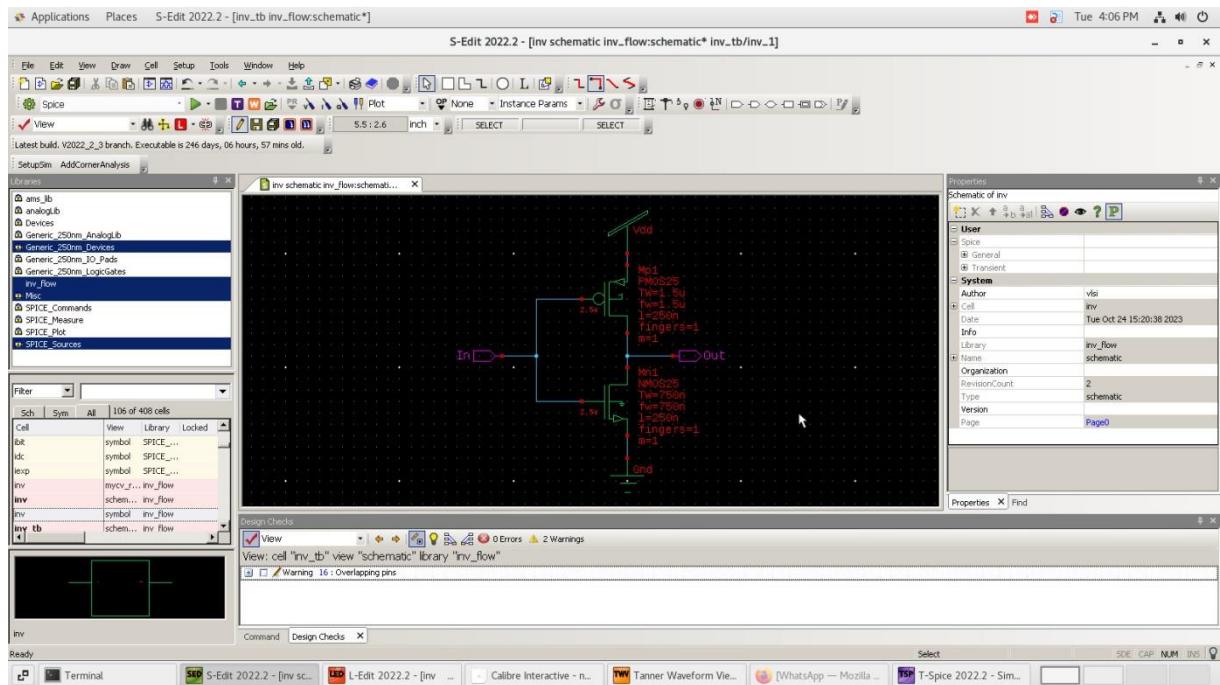
You also need to add **analog-lib** from standard libraries.



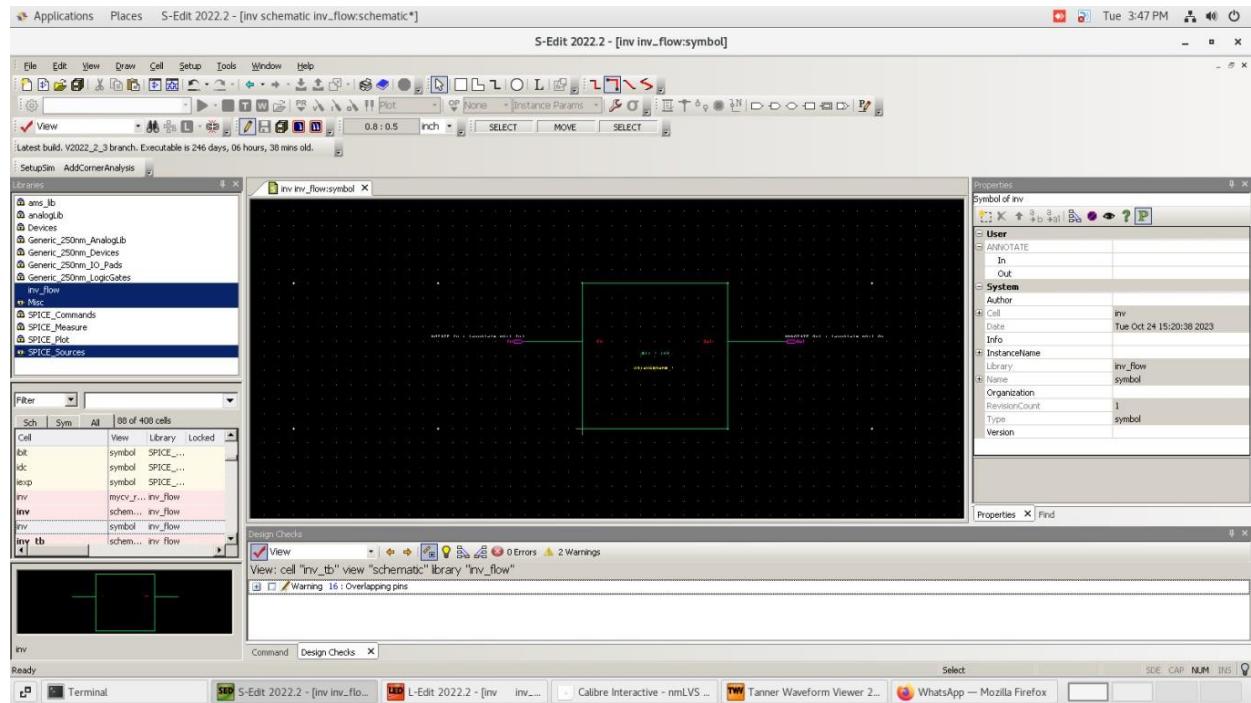
Now all done 😊



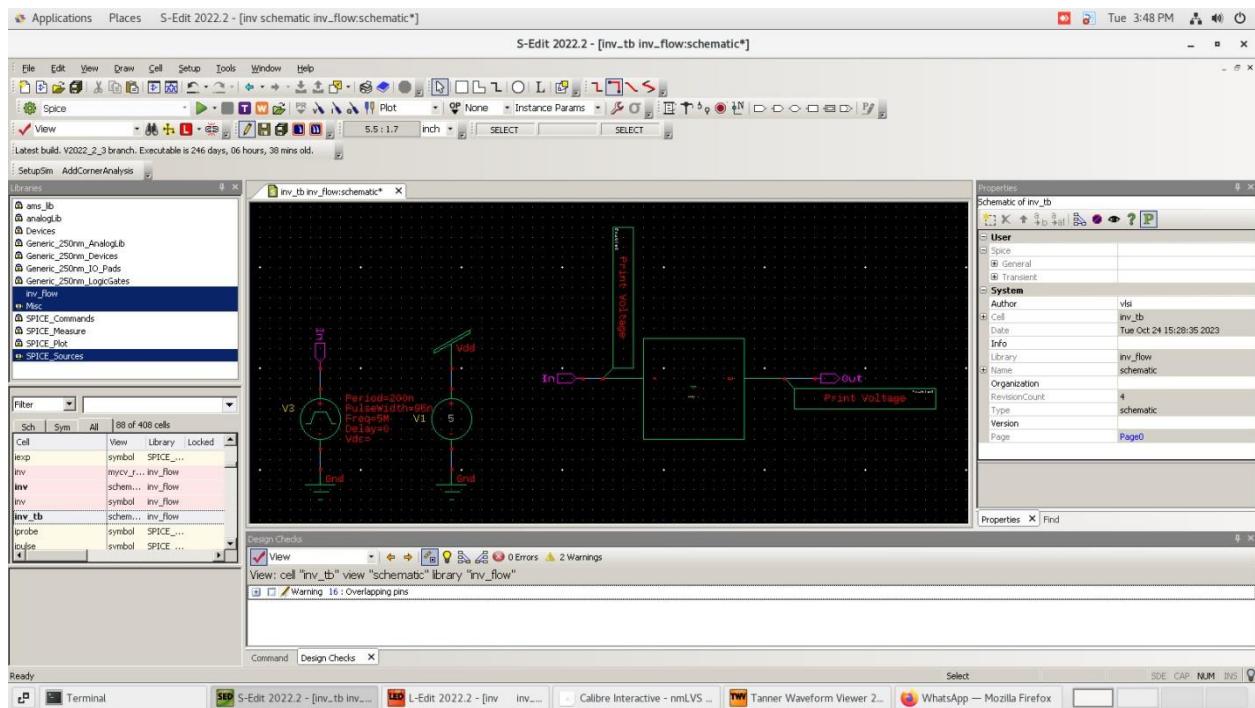
2. Design an inverter from scratch (don't use generic gates)



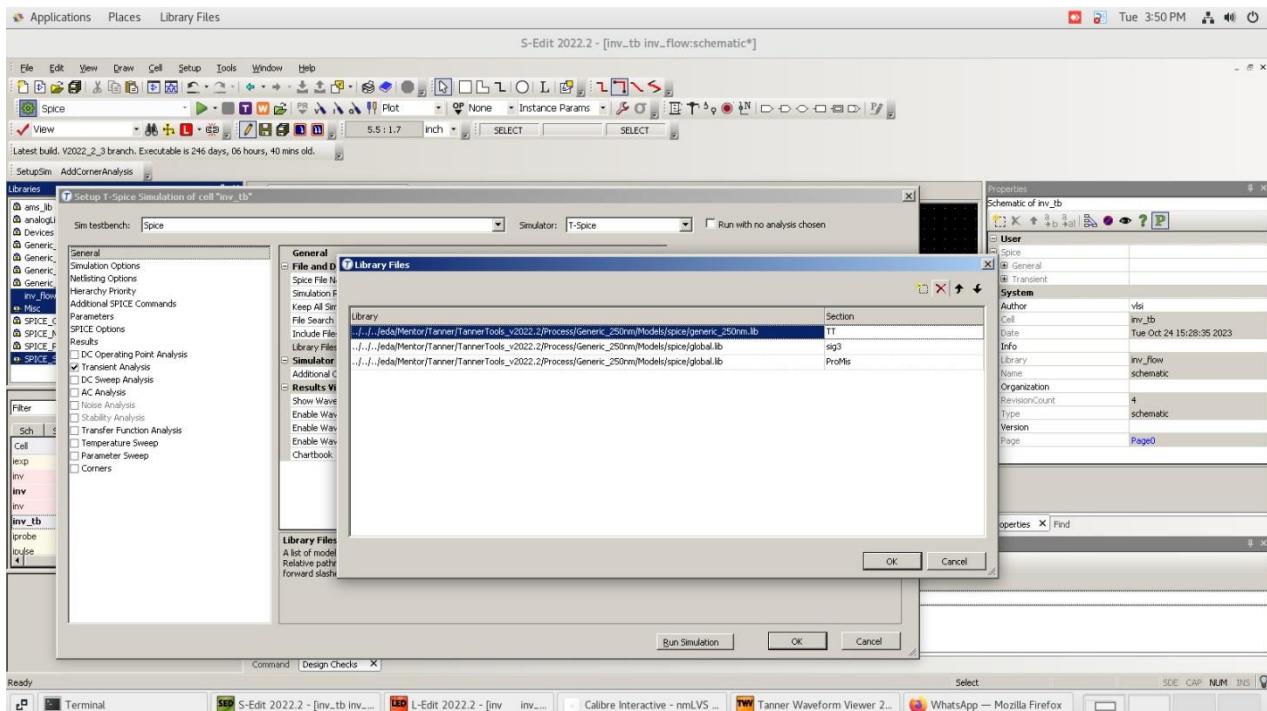
3. Create a symbol from your schematic.

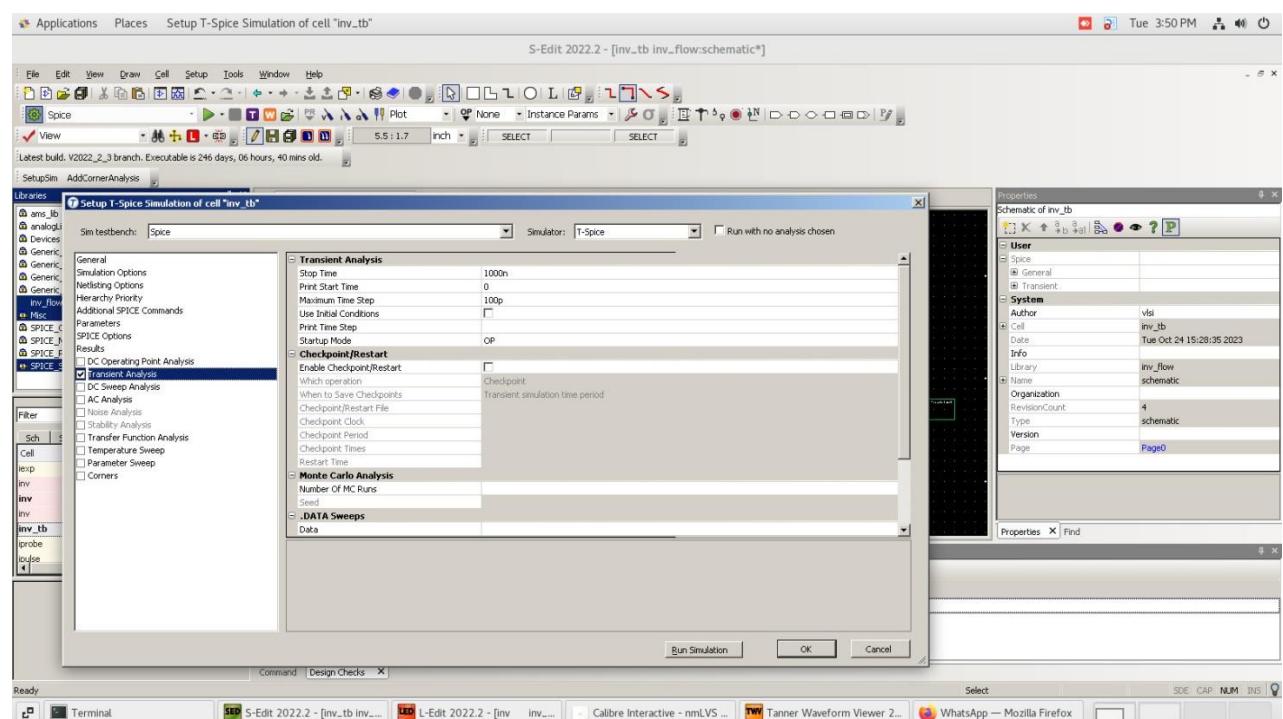
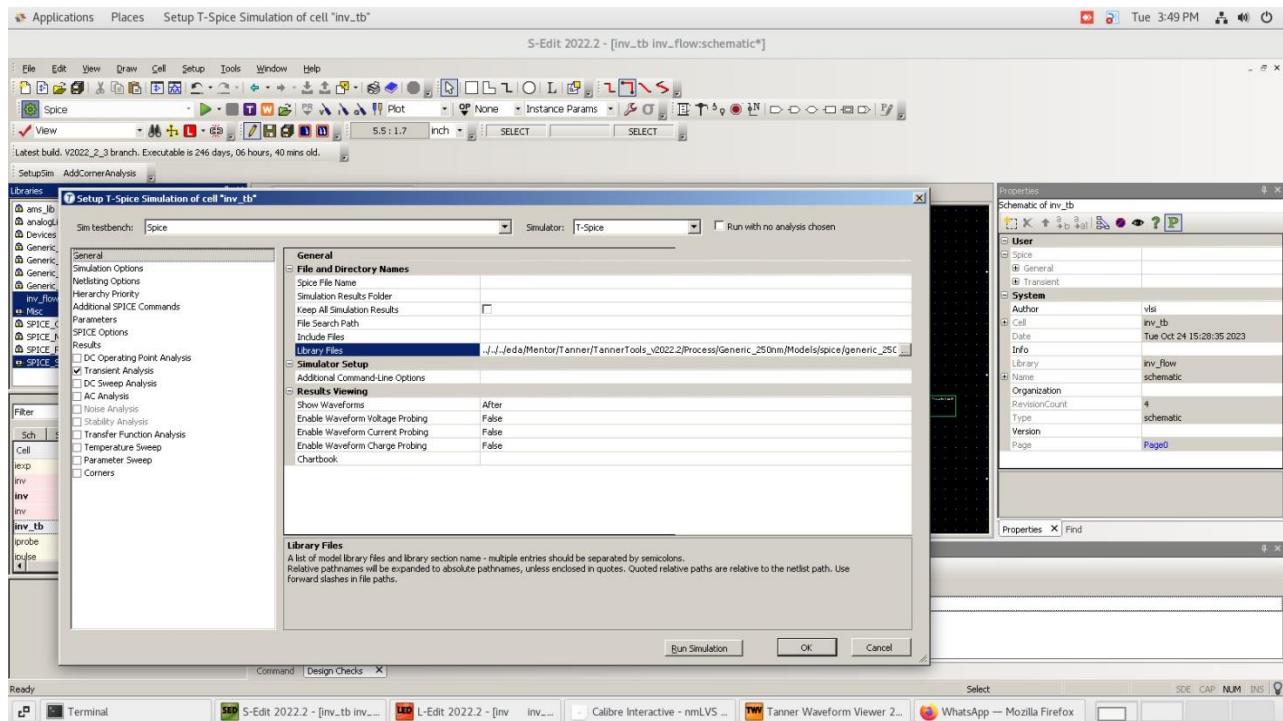


4. Test your design.



5. Simulate





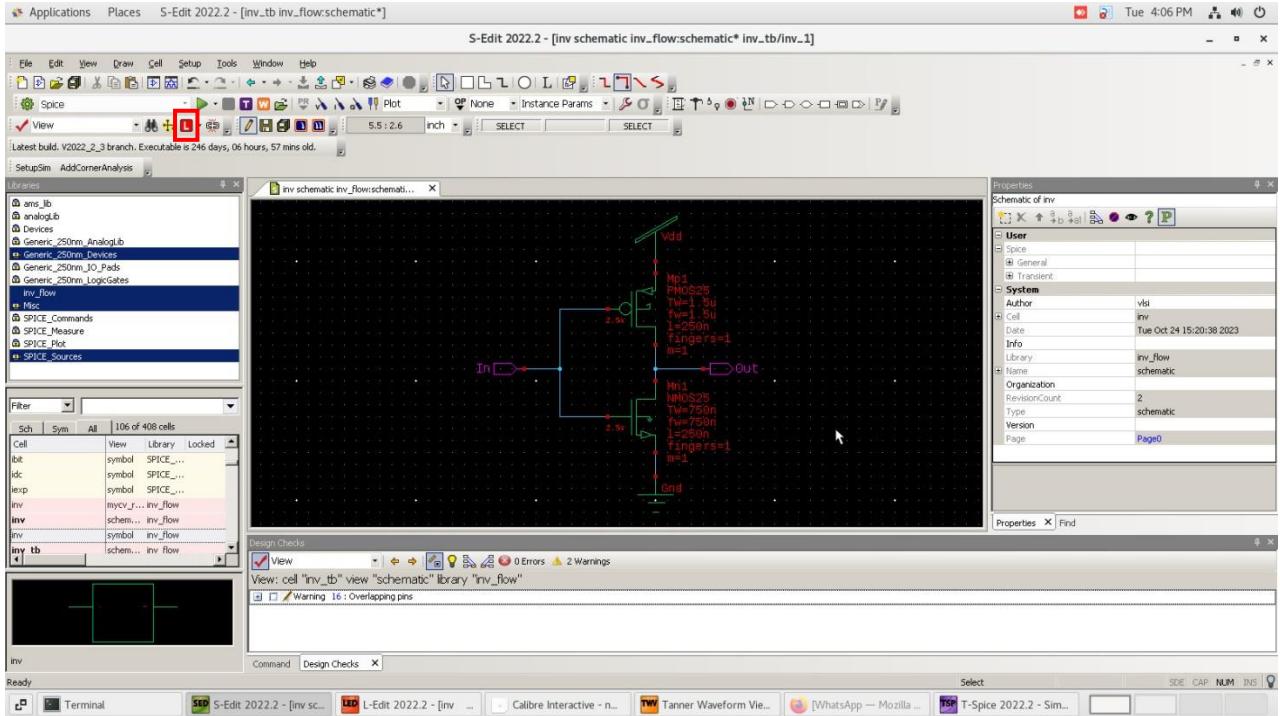
6. Calculate the propagation delay= 201.5psec

“.measure tran tdelay trig v(ln) val=2.5 fall=1 targ v(Out) val=2.5 rise=1”

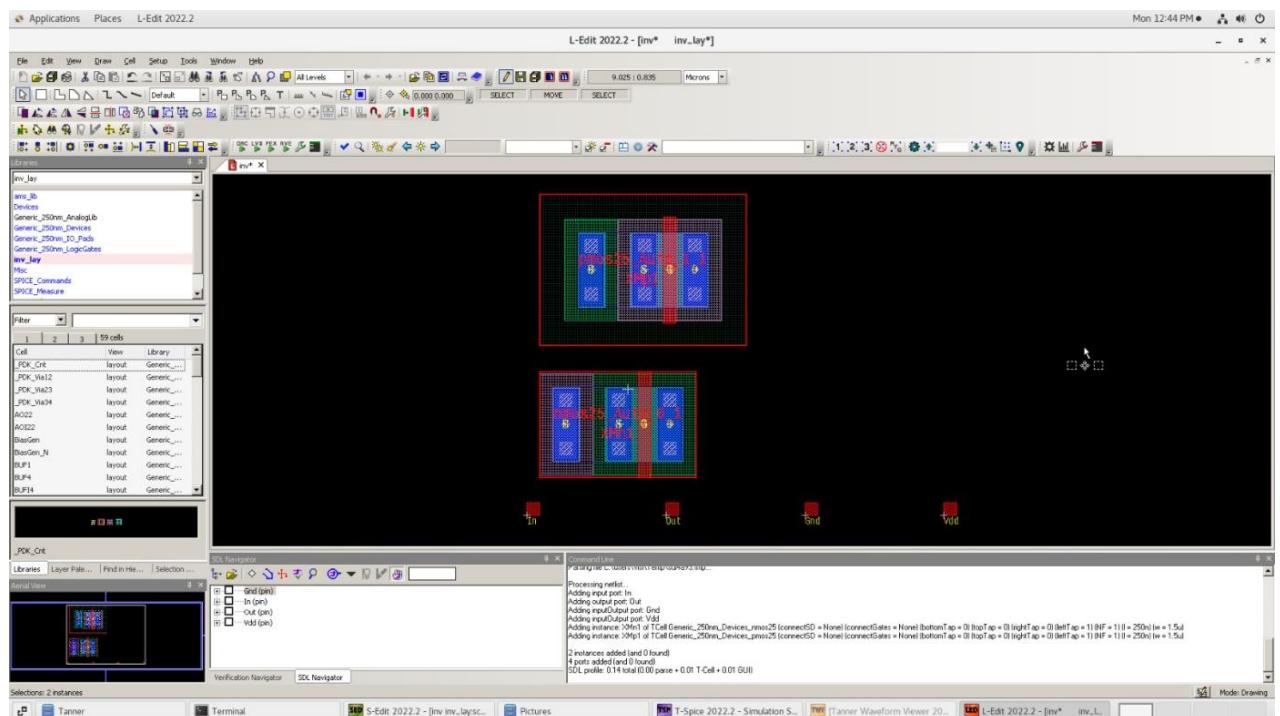
Backend Flow

1. After Finishing your Schematic, now it is time to setup your Layout. The next step is to publish to **SDL** (schematic driven layout).

Note: Or simply you can load the SPICE netlist that was extracted from S-Edit by going to **SDL Navigator** and choose the **Load Netlist** icon.



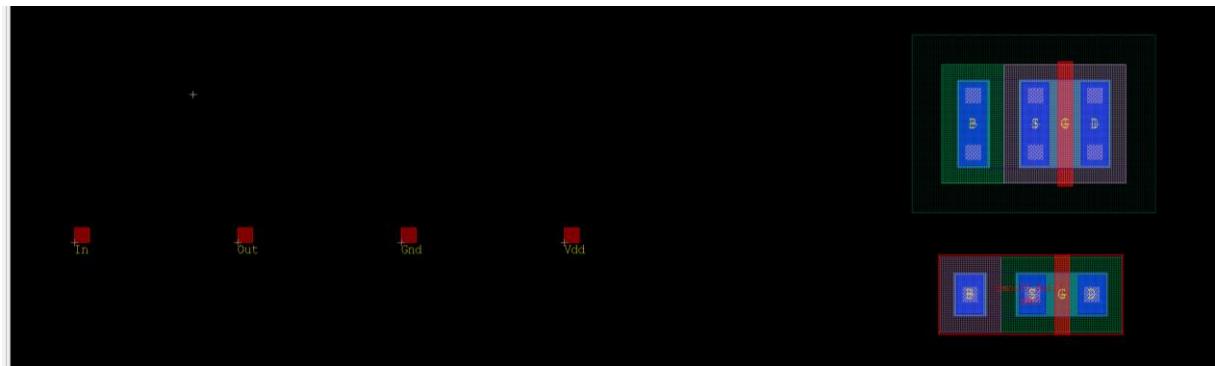
L-edit will be updated with the generated layout, all you should do now is to route it.



2. Now, st1+art the routing step.

First: align the NMOS and PMOS vertically, by moving anyone of them and make it under the other and not behind it.

(Remember that to move the NMOS for example, then select it and move it by pressing the Alt key on the keyboard then drag it with the mouse)



Note: NMOS can't be very close to PMOS according to DRC. DRC specifies a minimum width between the NMOS and PMOS. So, need to be adjusted.

press **AlignHorizontalCenter** icon while selecting both of them:



Second, connect the gates of NMOS and PMOS with poly.

Layer Palette

Layer	Purpose		
P_Well	drawing	<input type="checkbox"/>	<input type="checkbox"/>
N_Well	drawing	<input type="checkbox"/>	<input type="checkbox"/>
Active	drawing	<input type="checkbox"/>	<input type="checkbox"/>
ThickActive	drawing	<input type="checkbox"/>	<input type="checkbox"/>
N_Implant	drawing	<input type="checkbox"/>	<input type="checkbox"/>
P_Implant	drawing	<input type="checkbox"/>	<input type="checkbox"/>
Poly	drawing	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
SilicideBlock	drawing	<input type="checkbox"/>	<input type="checkbox"/>
Resistor	Im	<input type="checkbox"/>	<input type="checkbox"/>
Poly2	drawing	<input type="checkbox"/>	<input type="checkbox"/>

Libraries Layer Palette Find in Hierarchy

Aerial View

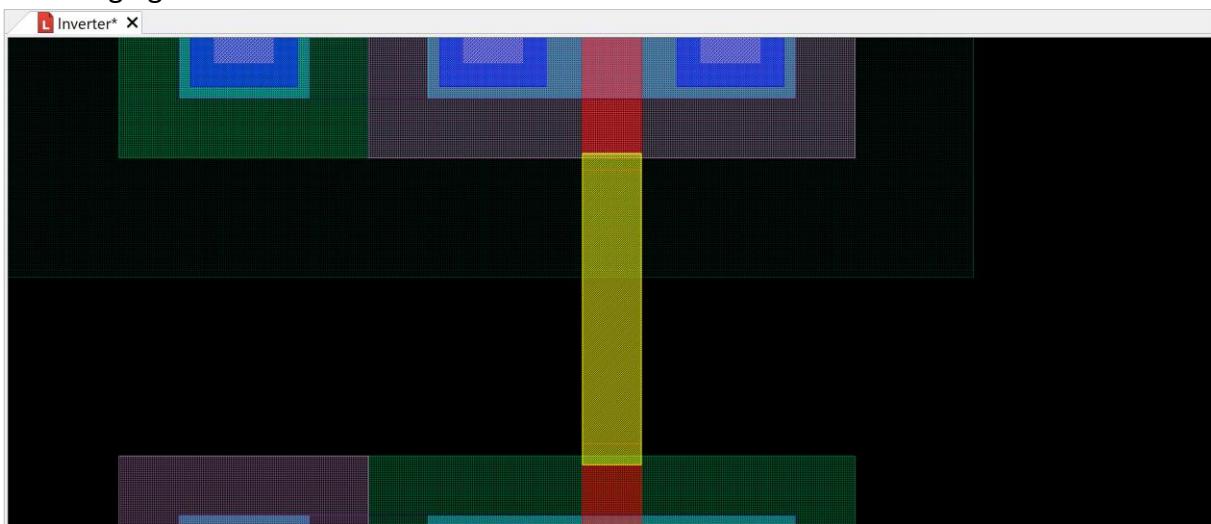
To do so:

- (1) Choose Layer Palette window.
- (2) Then Choose Poly from it.

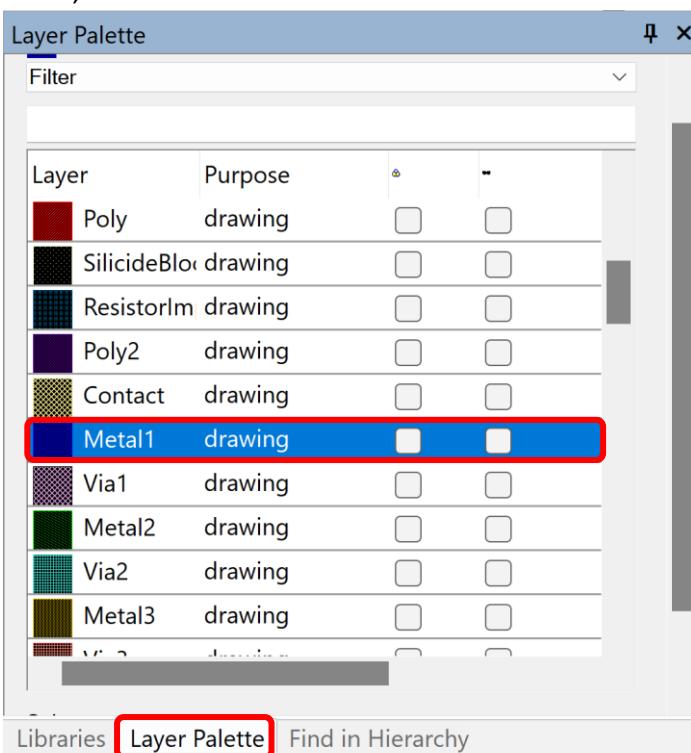
Then press **Box** icon.



Then start drawing a rectangle (connection) between the gates of NMOS and PMOS as shown in the following figure:

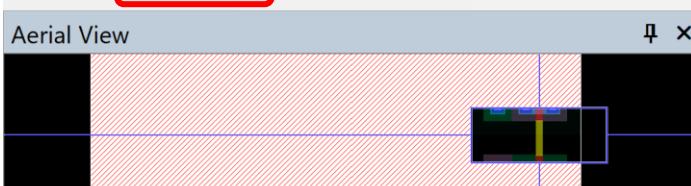


Third, connect the drains of NMOS and PMOS with Metal1.



To do so:

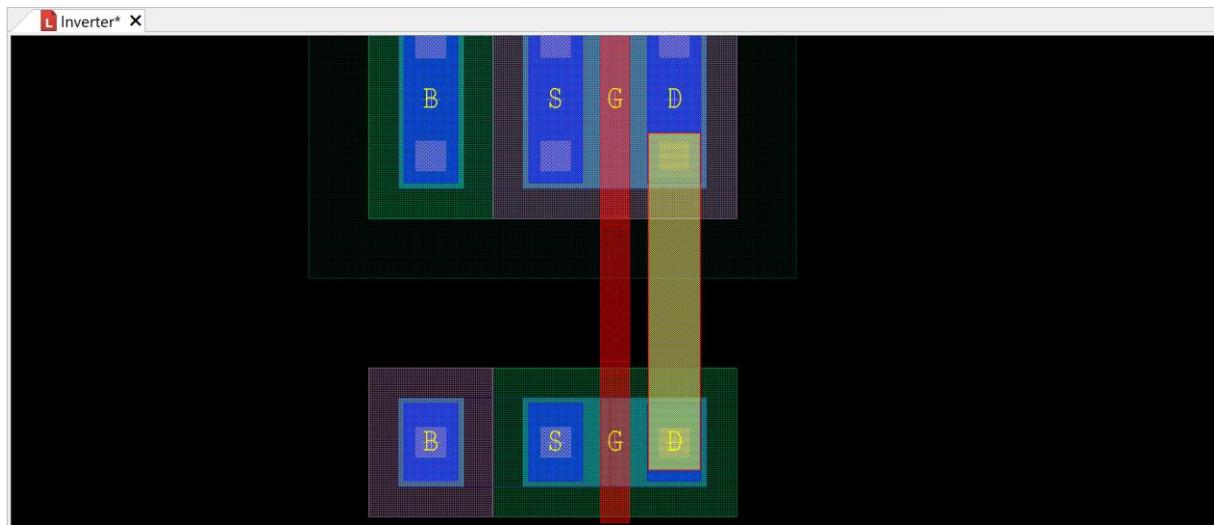
- (1) Choose Layer Palette window.
- (2) Then Choose Metal1 from it.



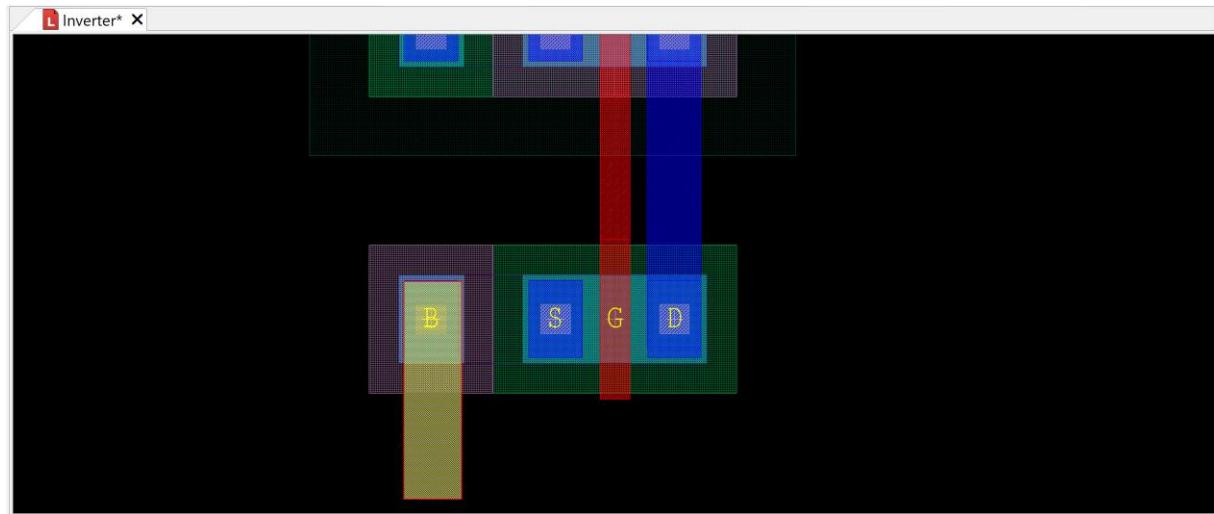
Then press **Box** icon.



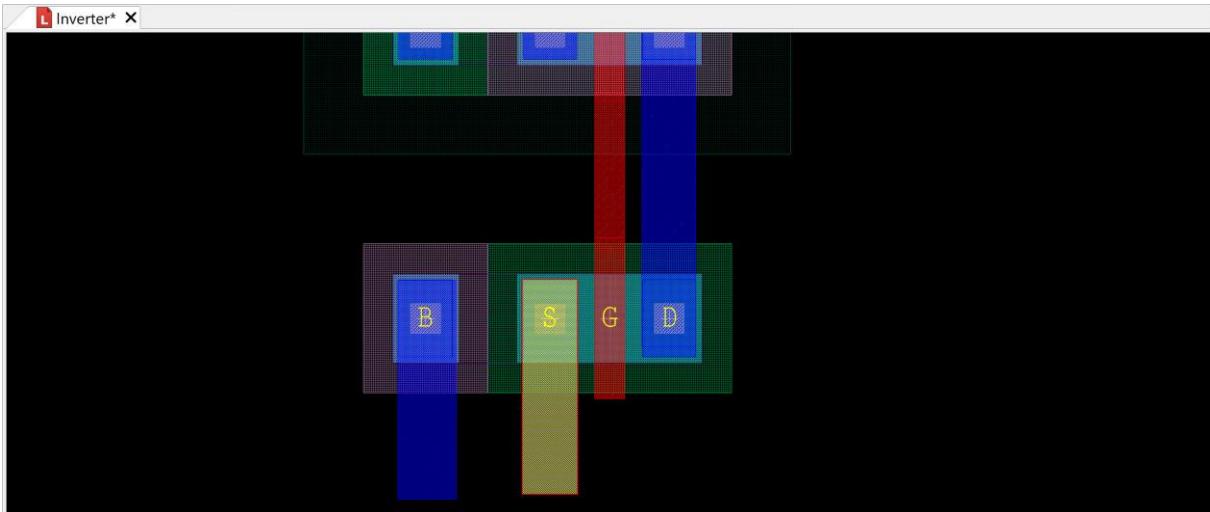
Then start drawing a rectangle (connection) between the drains of NMOS and PMOS as shown in the following figure:



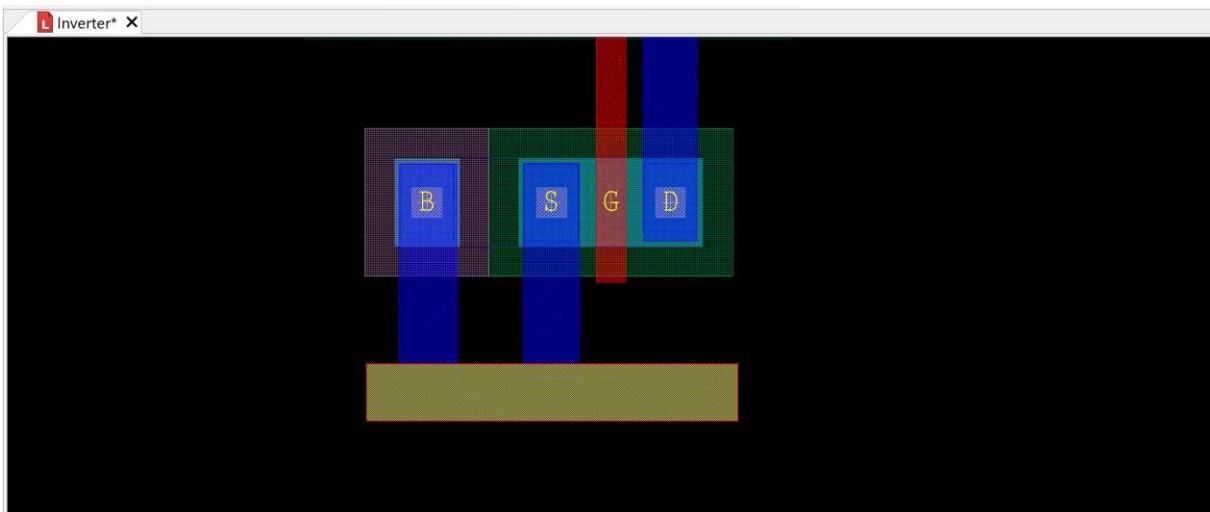
- Fourth, connect the Gnd. Use Metal1 to connect the Bulk and Source of NMOS with Gnd.
(1) Extend the bulk (B).



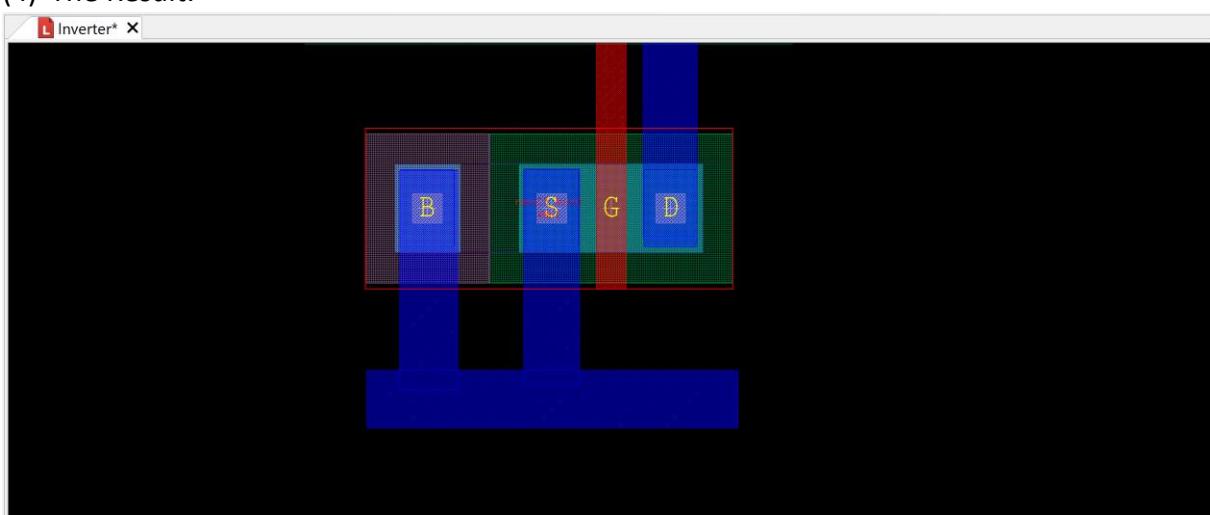
(2) Extend the source (S).



(3) Connect between B and S.

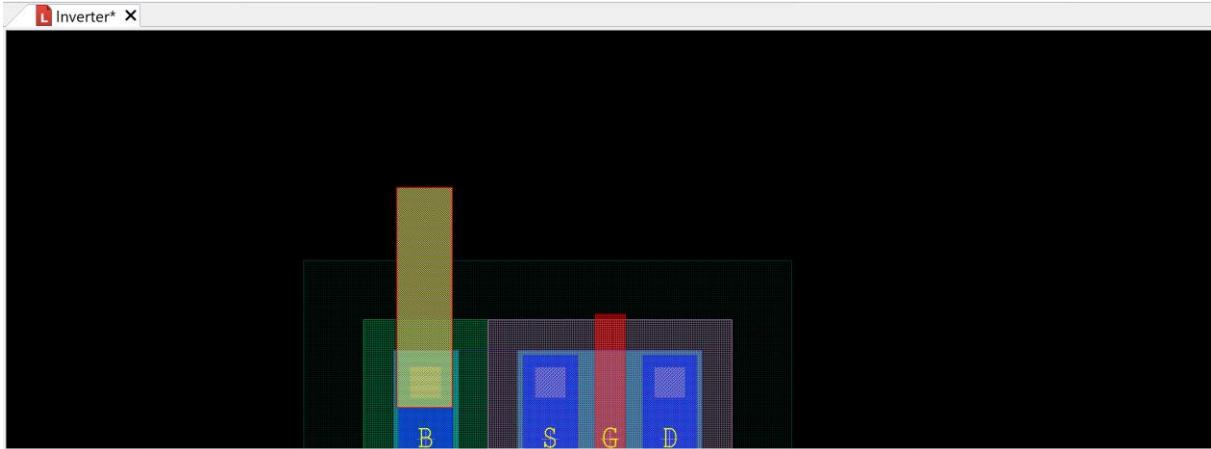


(4) The Result.

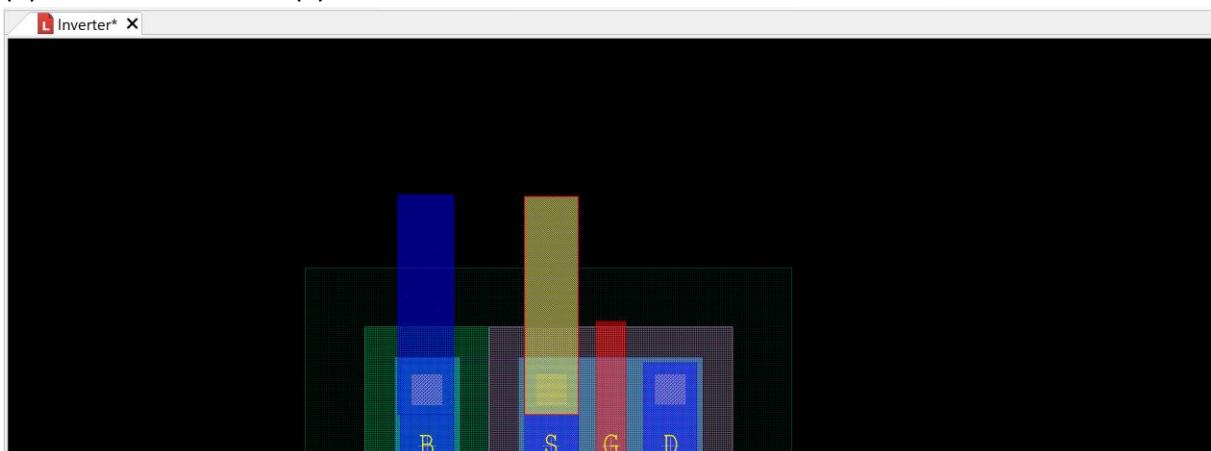


Fifth, connect the Vdd. Use Metal1 to connect the Bulk and Source of PMOS with Vdd.

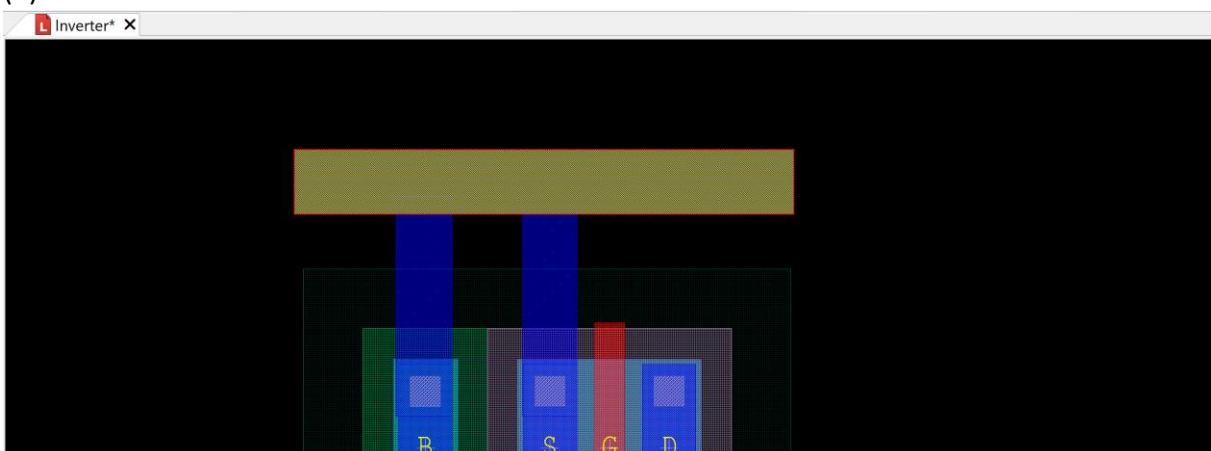
(1) Extend the bulk (B).



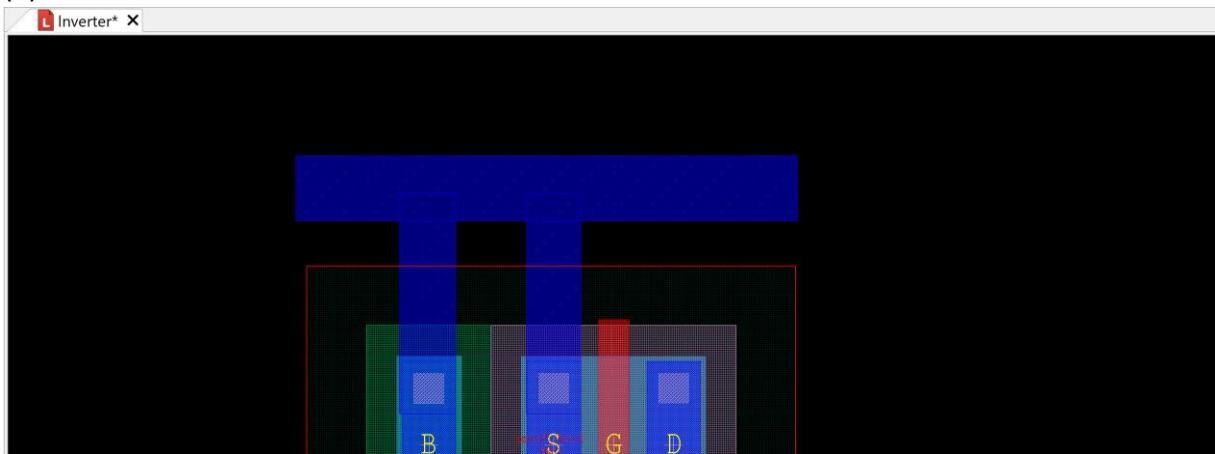
(2) Extend the source (S).



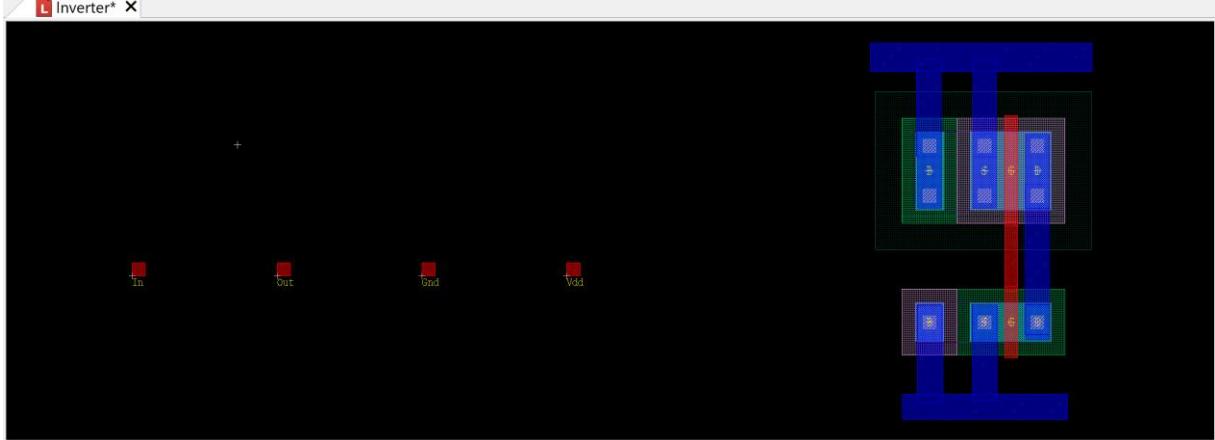
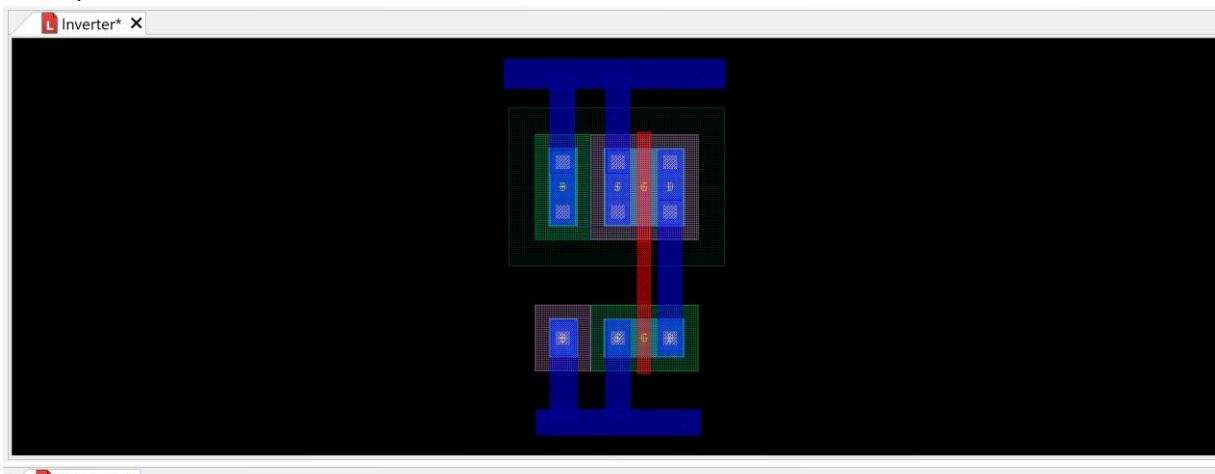
(3) Connect between B and S.



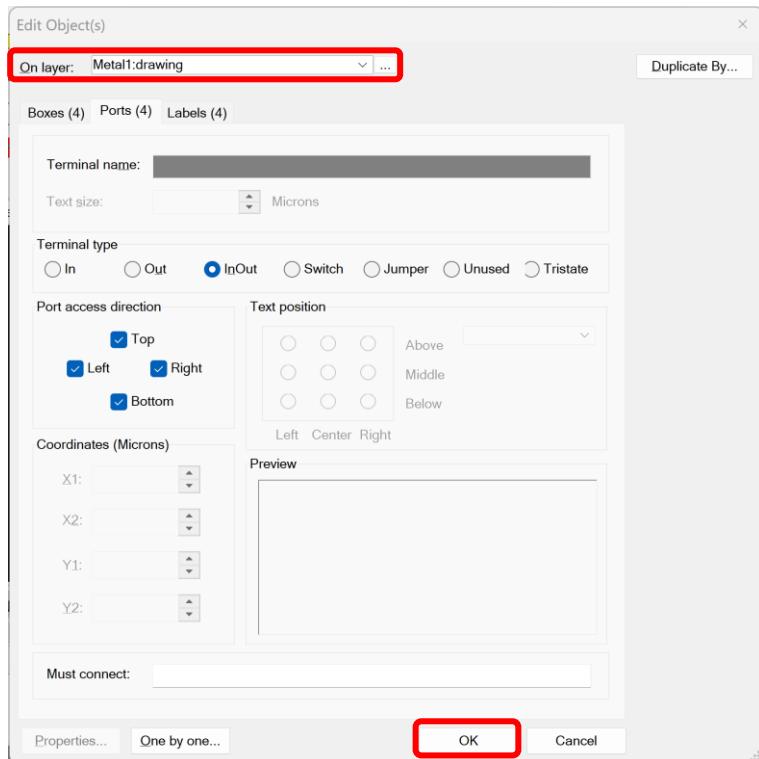
(4) The Result.



The update until now:



Sixth, select In, Out, Gnd and Vdd ports, then press **(Ctrl + E)** on keyboard. A new window is opened.



(1) Change from “Metal1: drawing”

On **layer** menu to “Metal1: pin”

for Vdd & Gnd & Out.

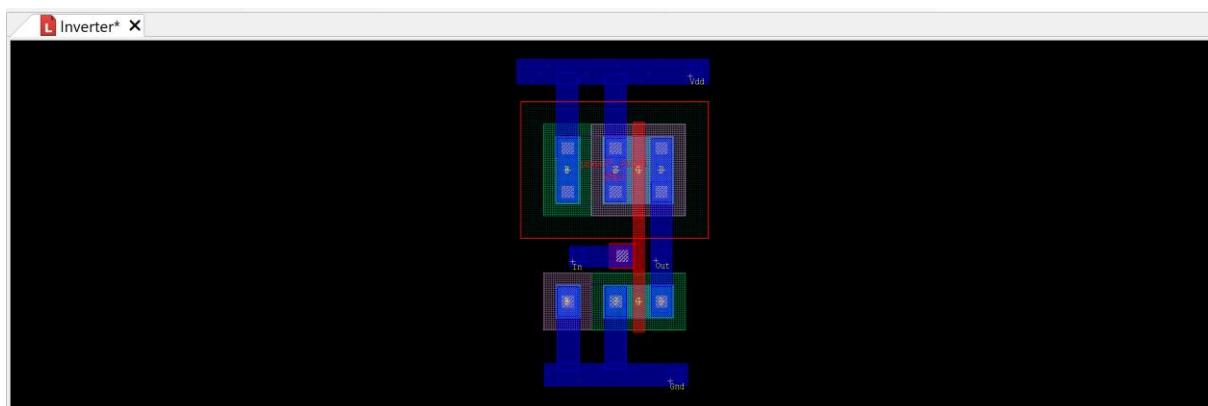
(2) Change from “poly: drawing” On **layer** menu to “poly: pin” for In.

(3) Then press **OK**.

Seventh, connect the ports with the inverter layout:

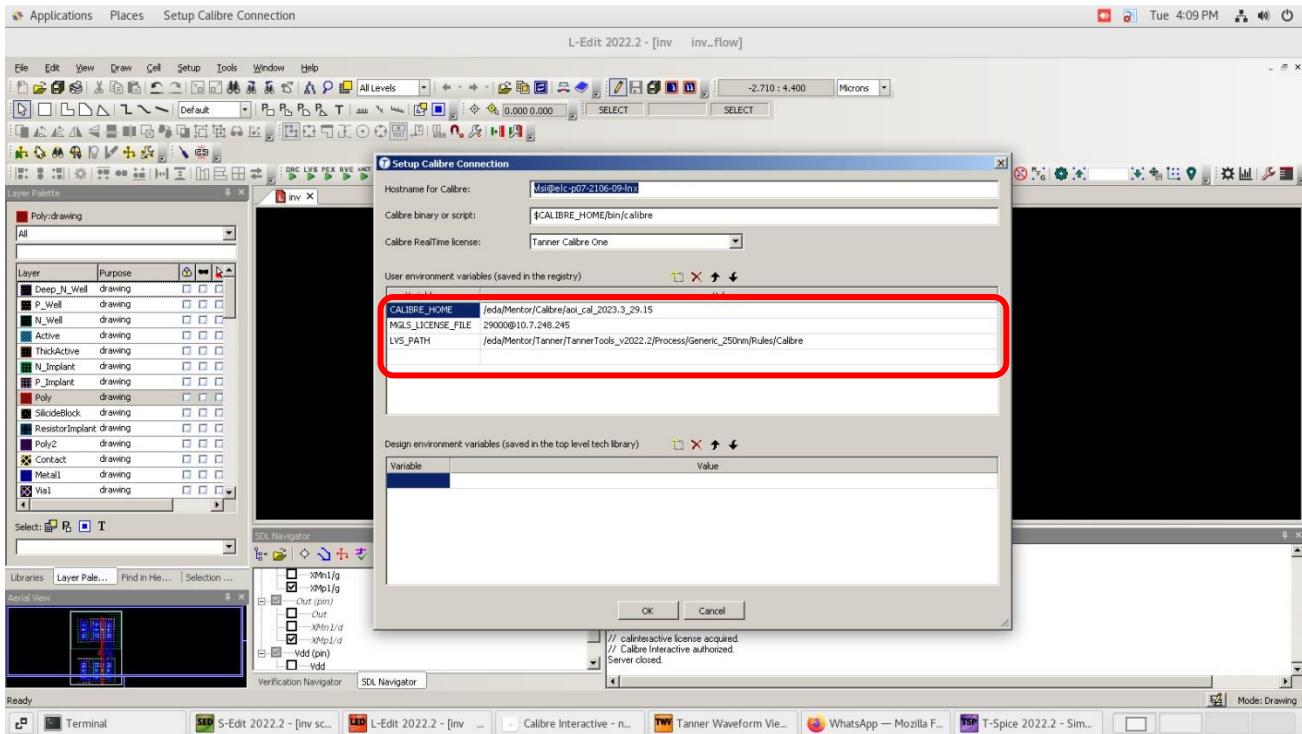
- (1) Select and move the Out port and put it on Metal1 that connects the drains of NMOS and PMOS.
- (2) Select and move the In port and put it on poly that connects the gates of NMOS and PMOS.
- (3) Select and move the Gnd port and put it on Metal1 that connects the B and S of NMOS.
- (4) Select and move the Vdd port and put it on Metal1 that connects the B and S of PMOS.

As shown in the following figure:

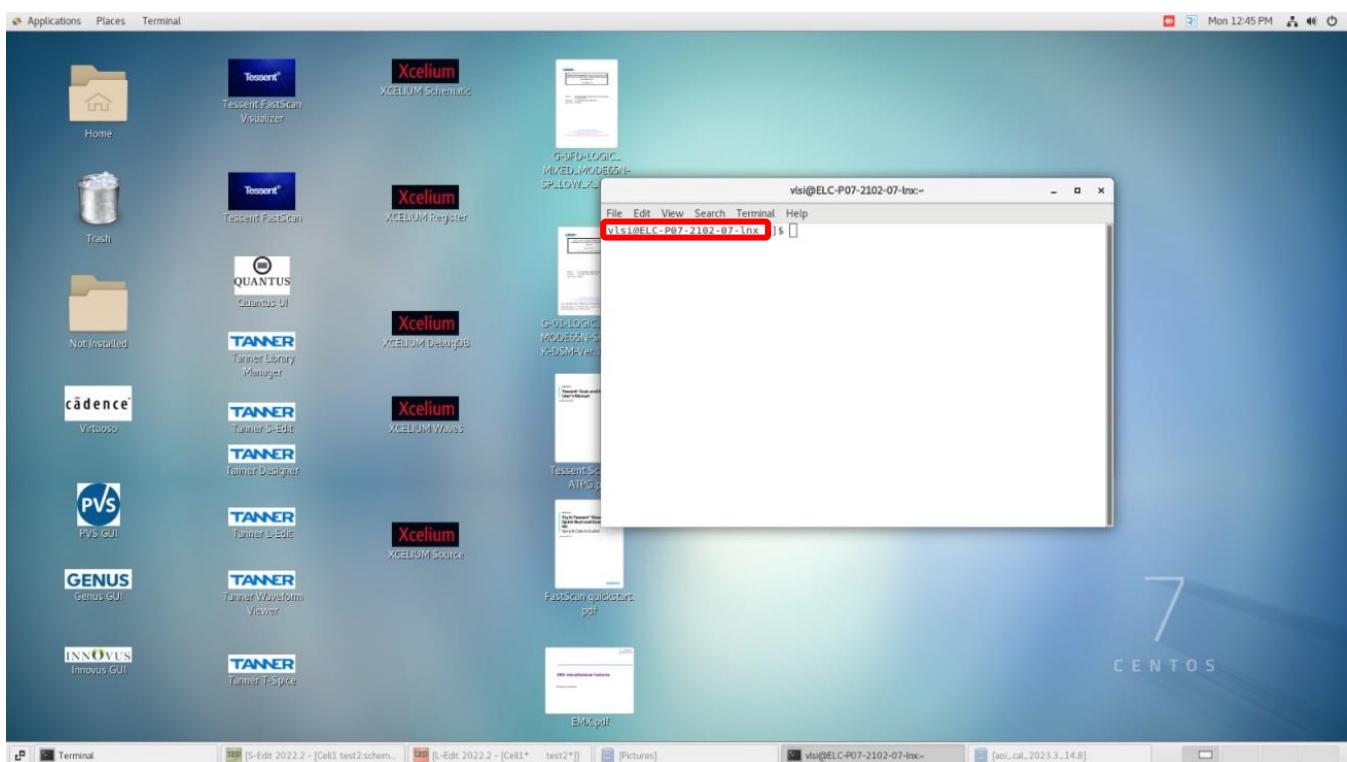


Calibre Setup

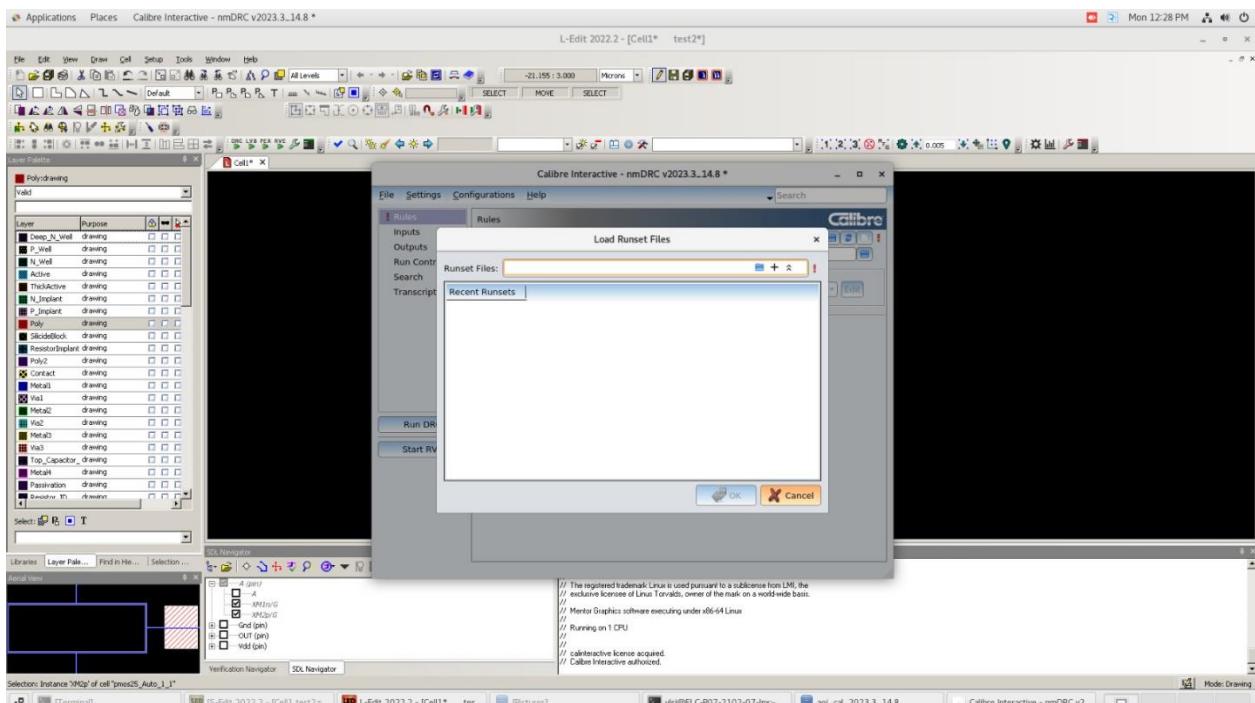
Setup Calibre connection **VERY IMPORTANT STEP:**



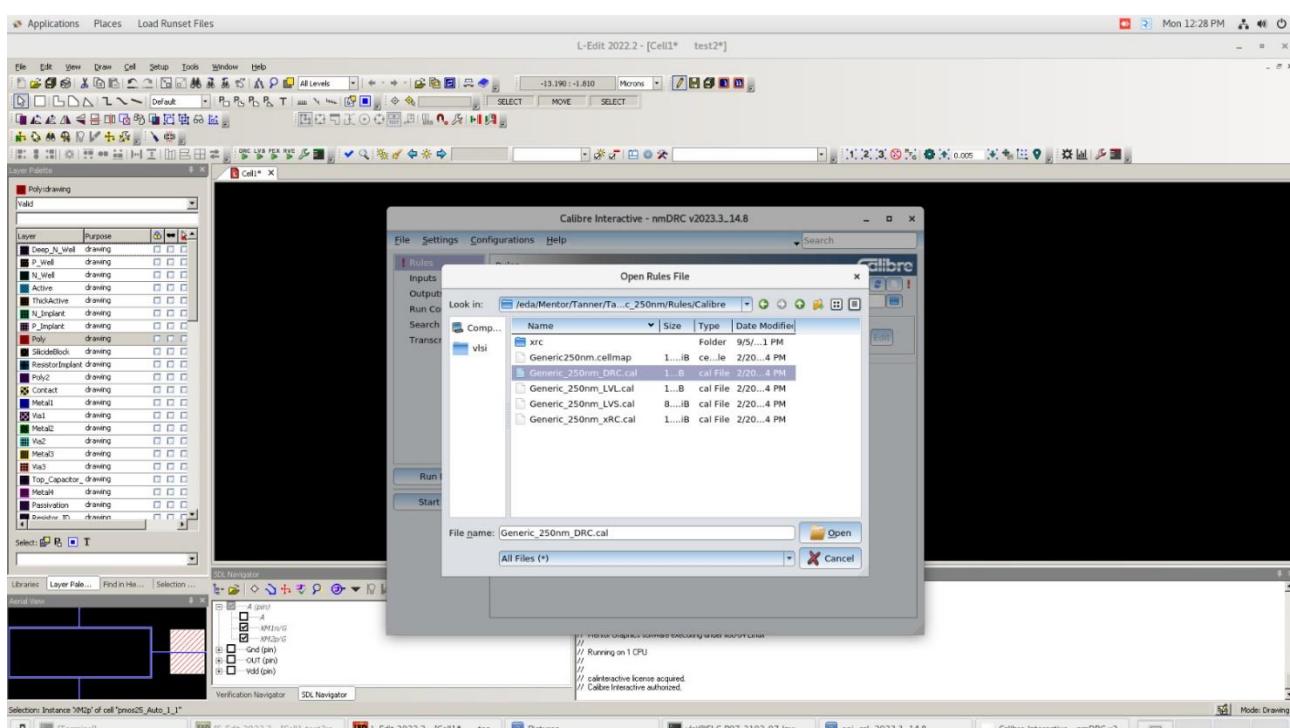
- Note: write **MGLS_LISENCE_FILE** instead of **MGLS_LICENSE_FILE**.
- Note: you can find Hostname for Calibre from your tanner location just open it in the terminal of the device.



DRC Setup



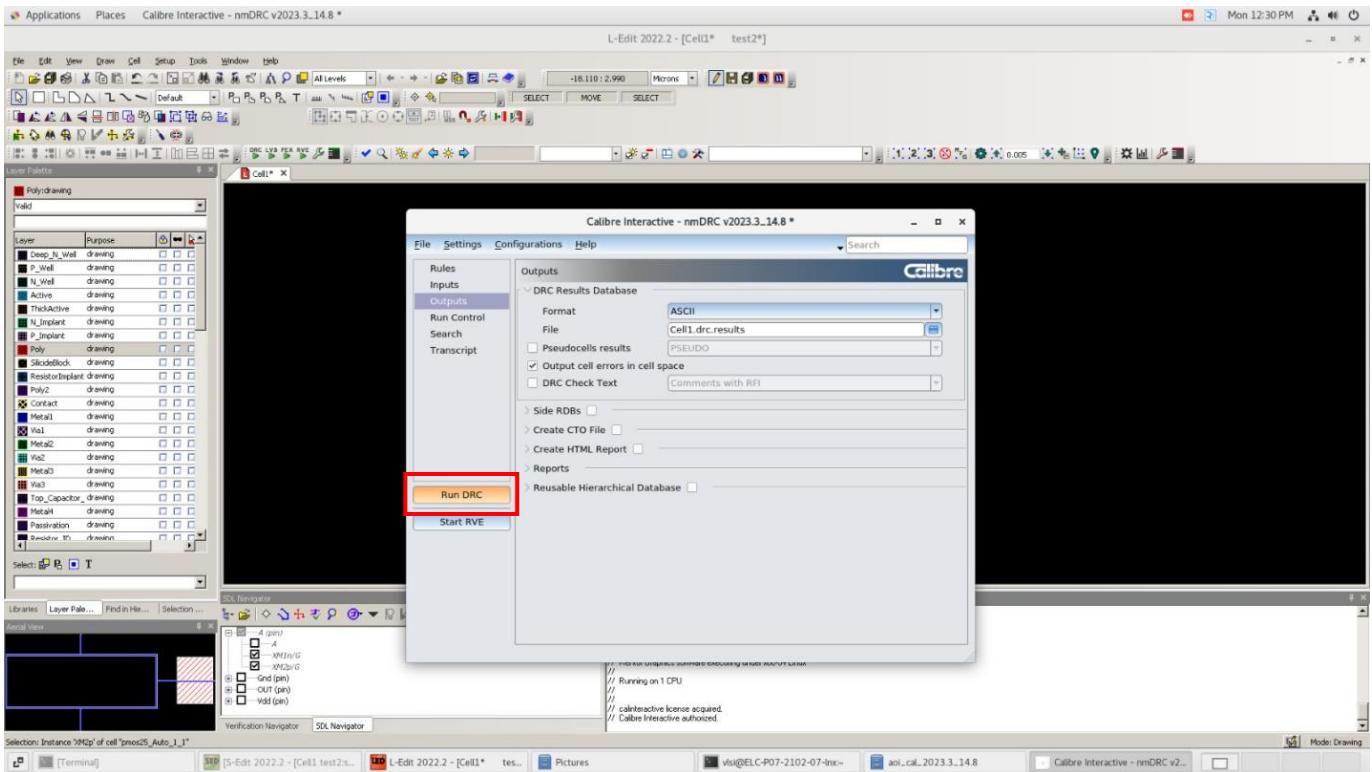
Cancel the first window appears.



Add DRC library from Process file.

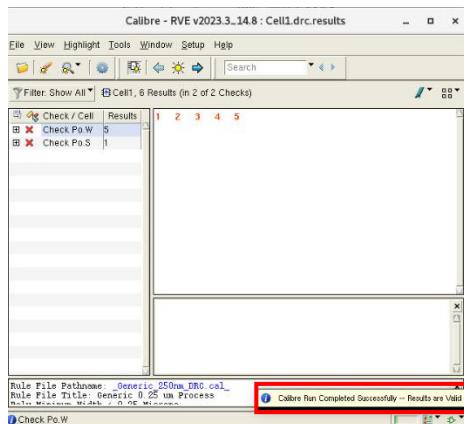
["/eda/Mentor/Tanner/TannerTools_v2022.2/Process/Generic_250nm/Rules/Calibre/Generic_250nm_DRC.cal"](file:///eda/Mentor/Tanner/TannerTools_v2022.2/Process/Generic_250nm/Rules/Calibre/Generic_250nm_DRC.cal)

Use default setting



Run DRC

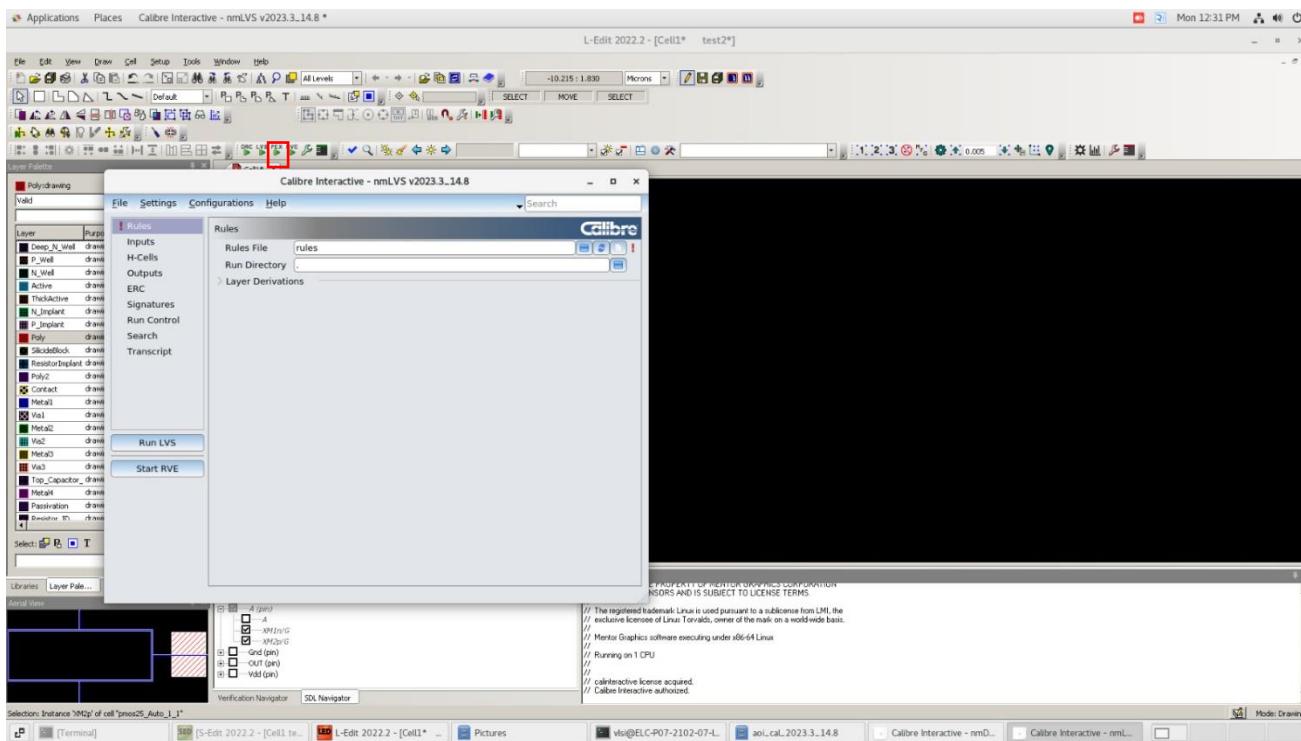
Result view (RVE) window will open



Fix all errors & **DRC** is Done Now 😊

LVS SETUP

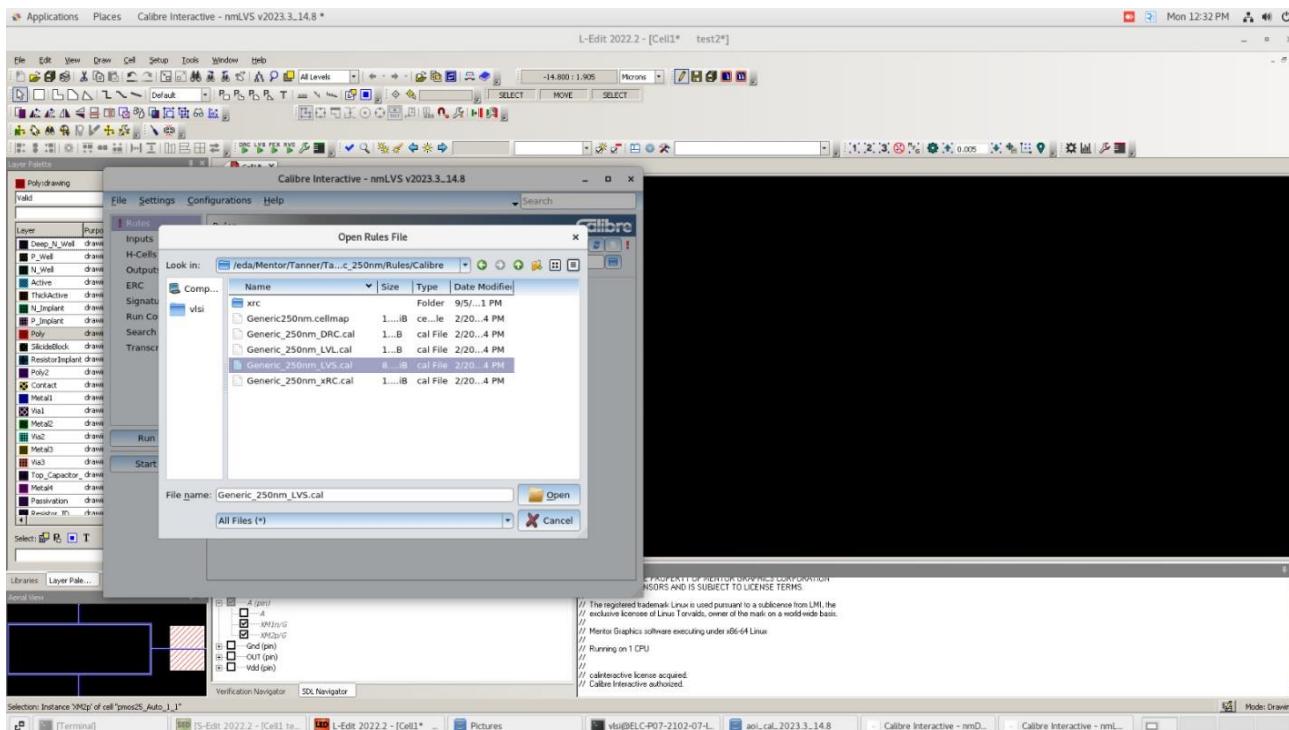
Run LVS

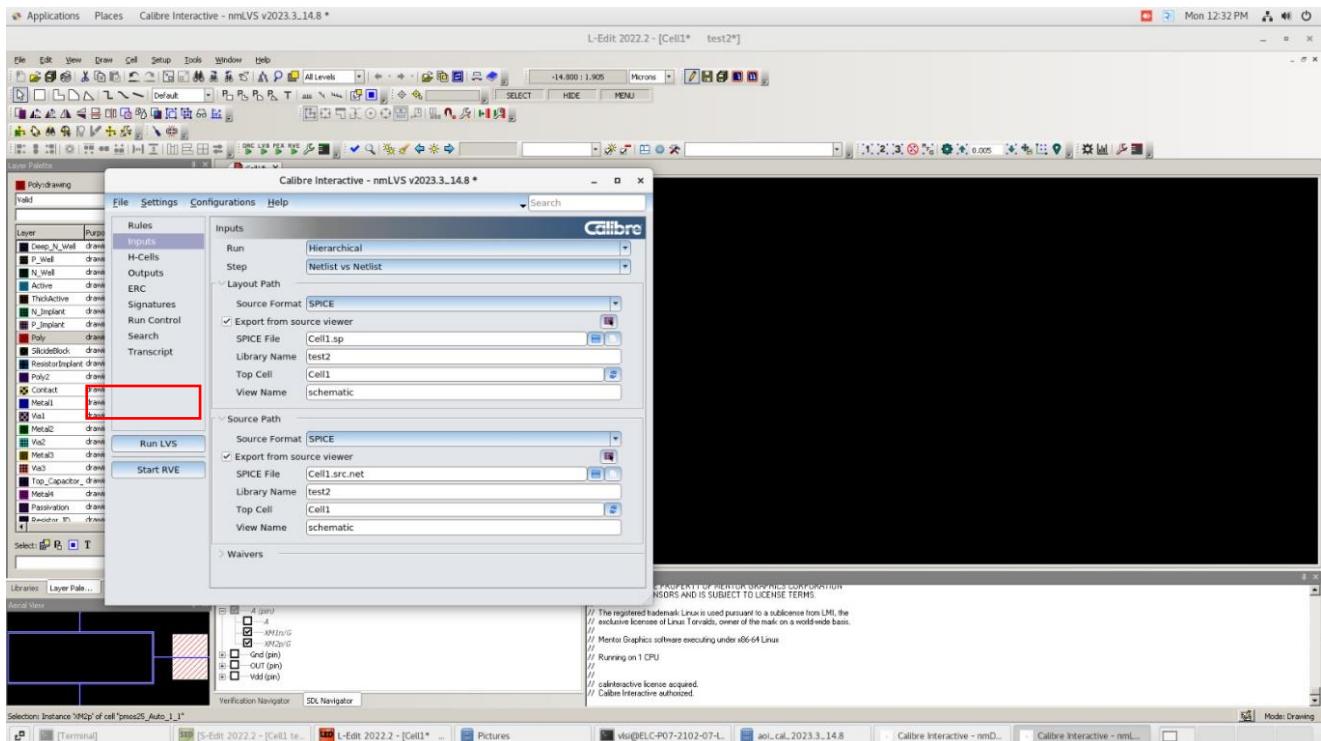


Cancel the first window appears.

Then add LVS library from Process file:

`"/eda/Mentor/Tanner/TannerTools_v2022.2/Process/Generic_250nm/Rules/Calibre/Generic_250nm_LVS.cal"`



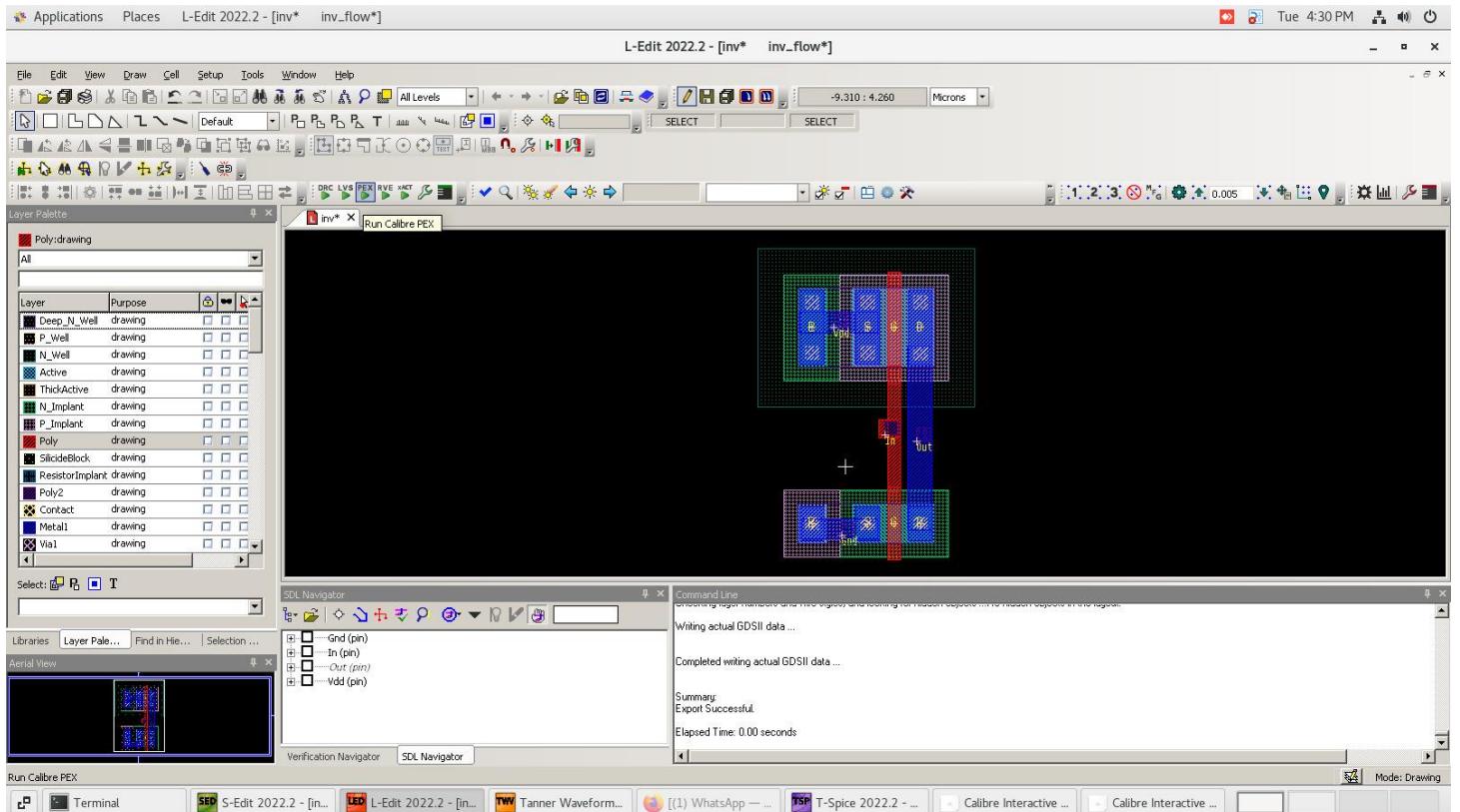


Run LVS

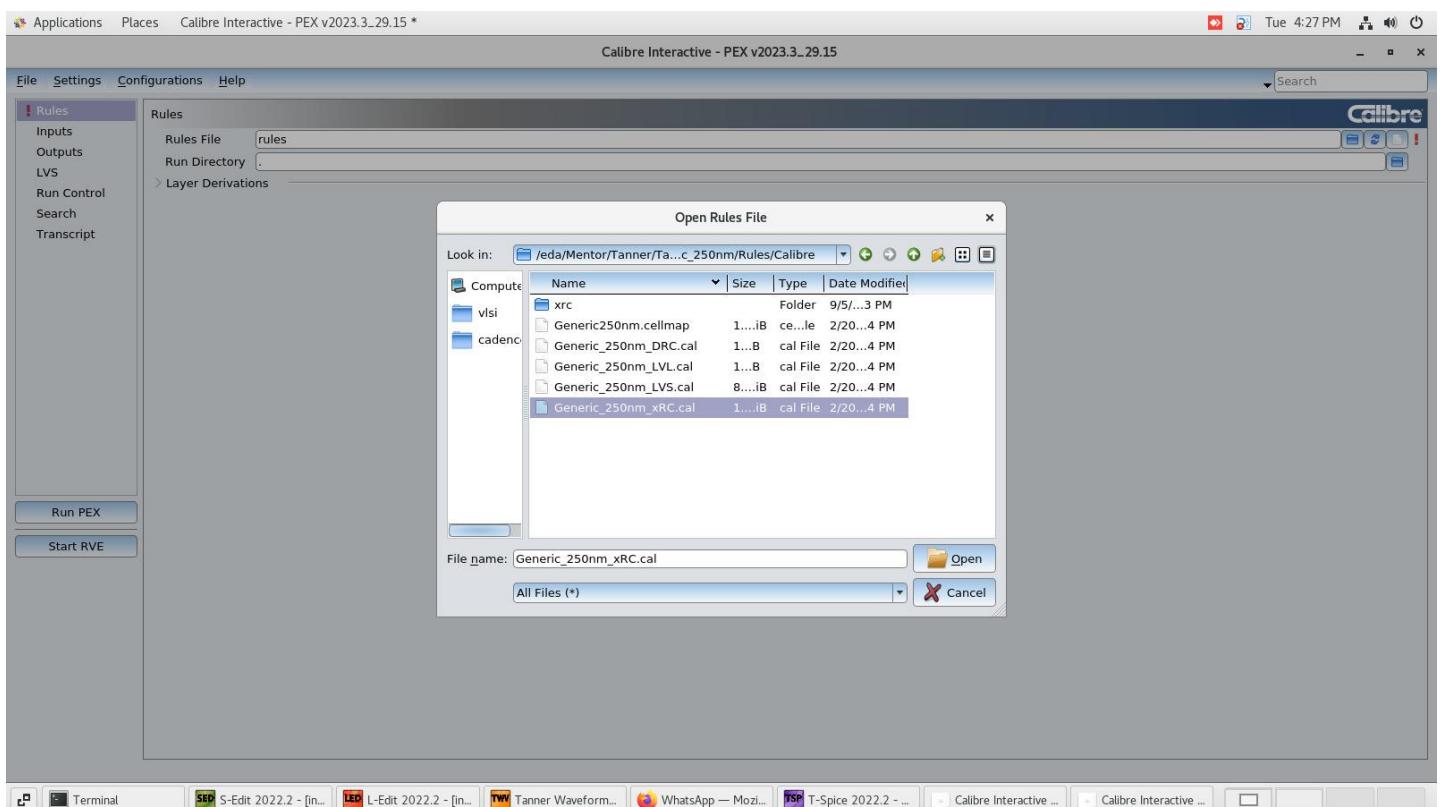
Fix all errors & LVS is Done Now 😊

Extraction SETUP

Run PEX

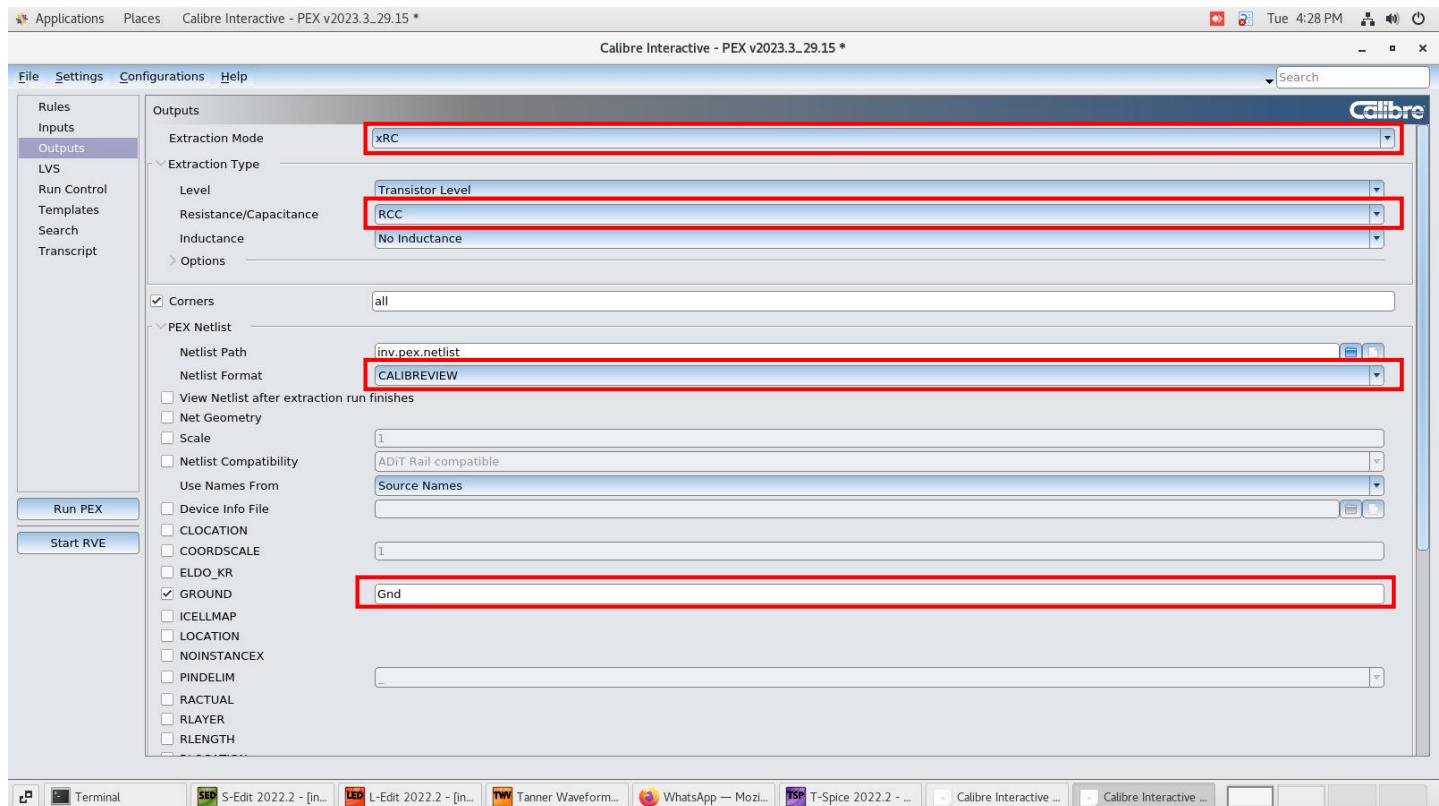


Cancel the first window appears.

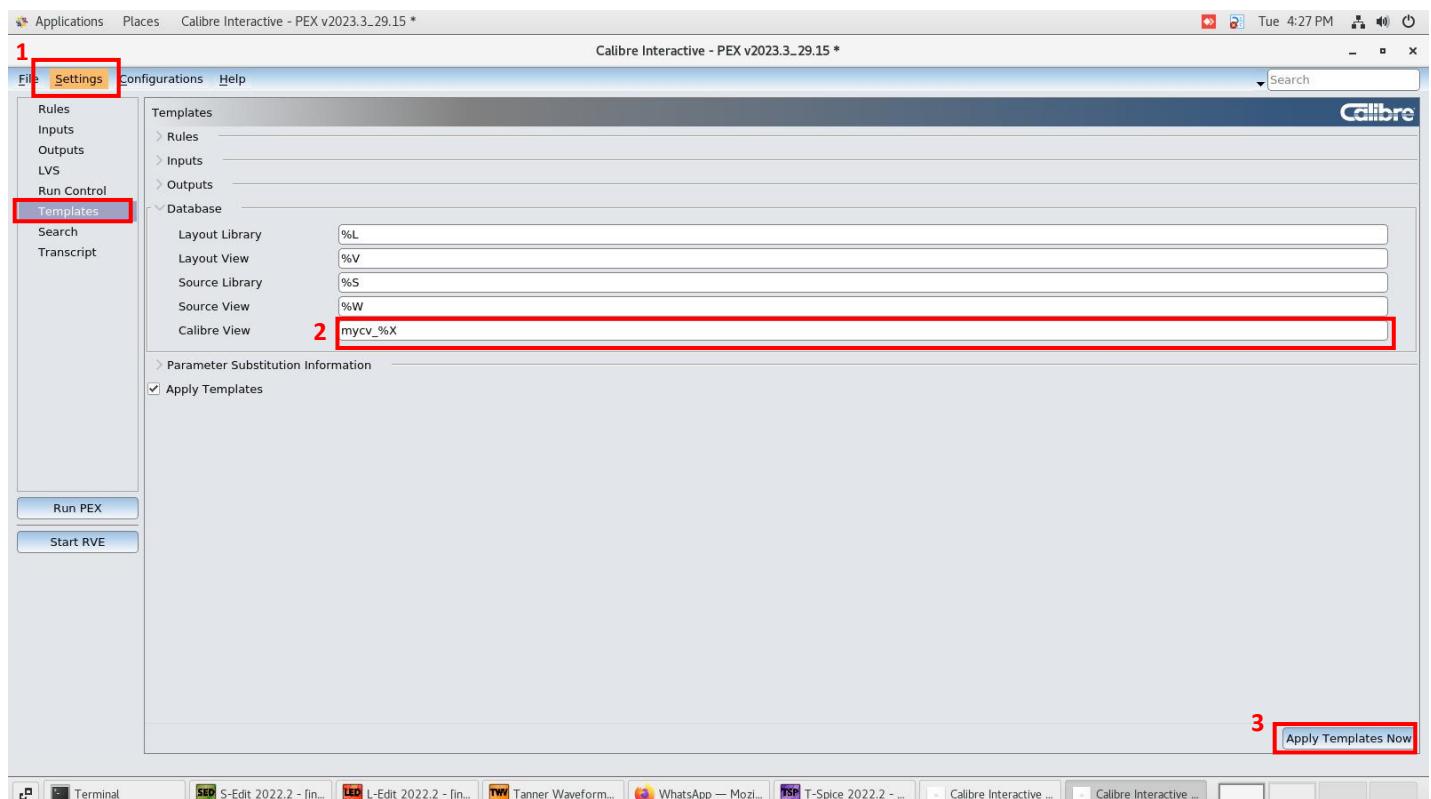


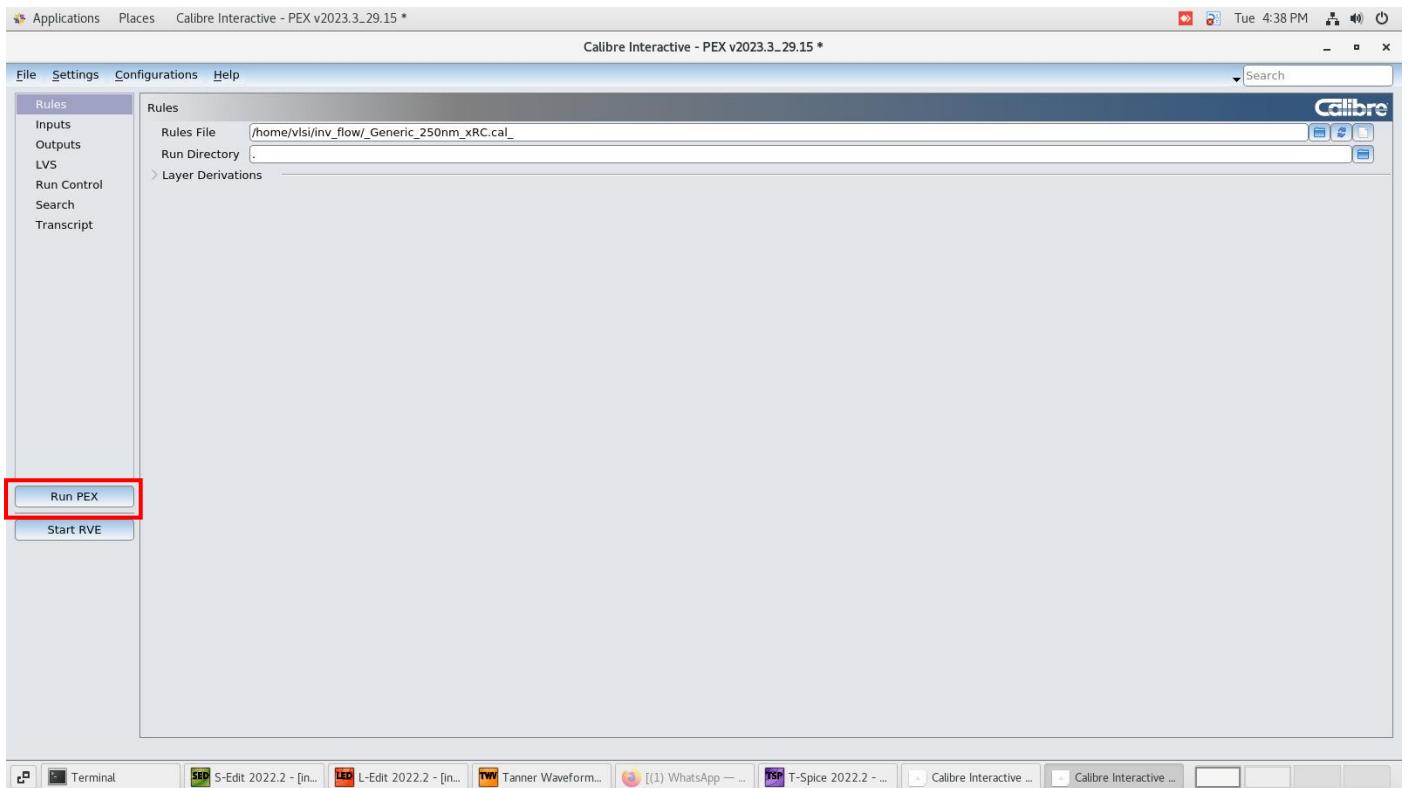
Then add PEX library from Process file.

`"/eda/Mentor/Tanner/TannerTools_v2022.2/Process/Generic_250nm/Rules/Calibre/Generic_250nm_xRC.cal"`



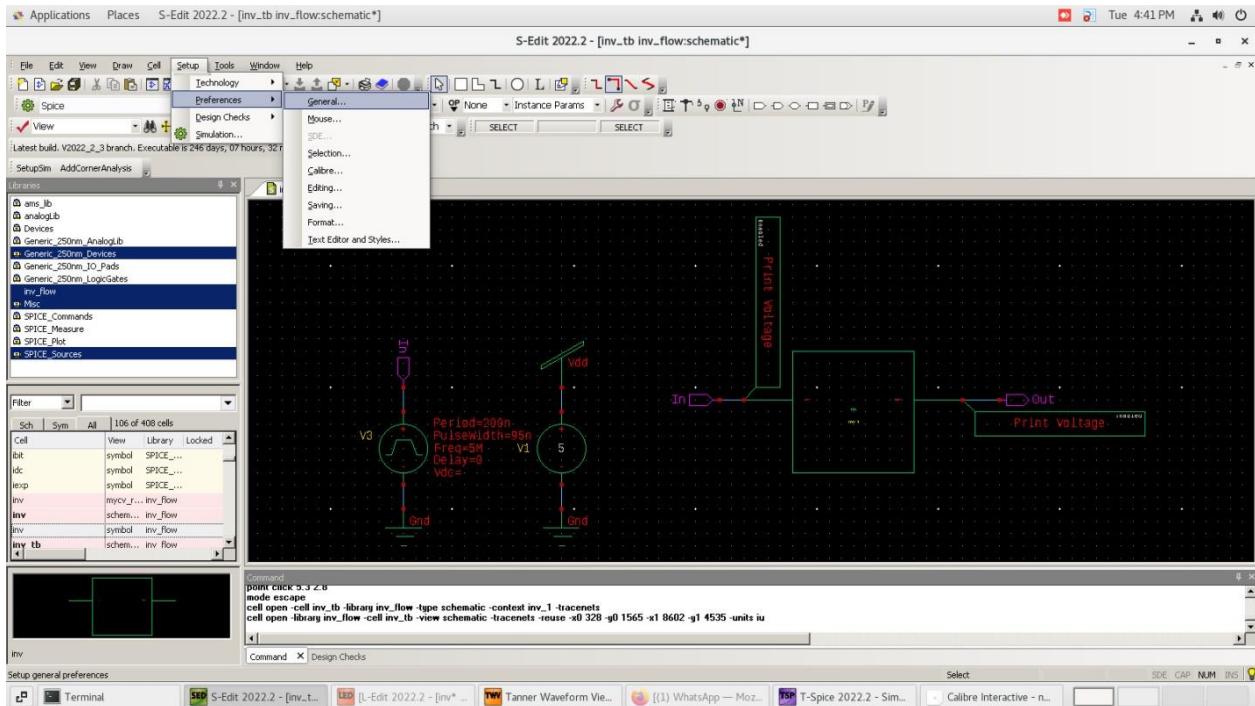
If Templates not appears show it from setting >> show pages



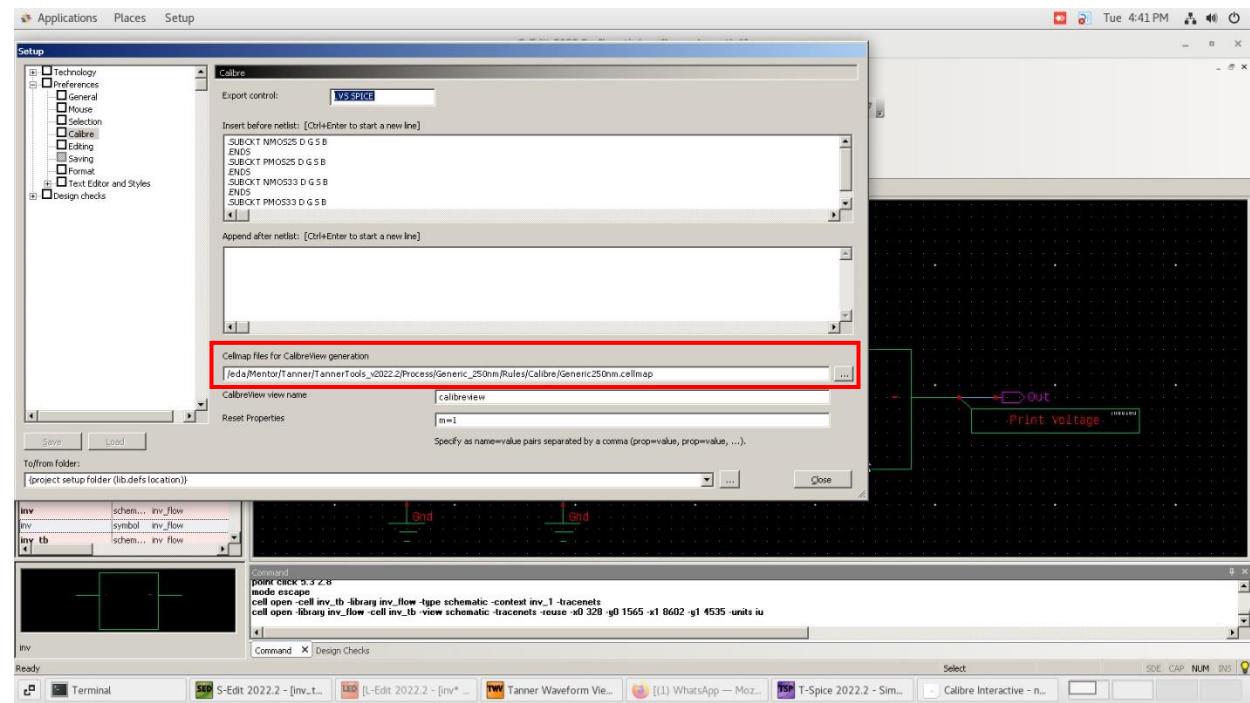


Post Layout Simulation

Open S>Edit



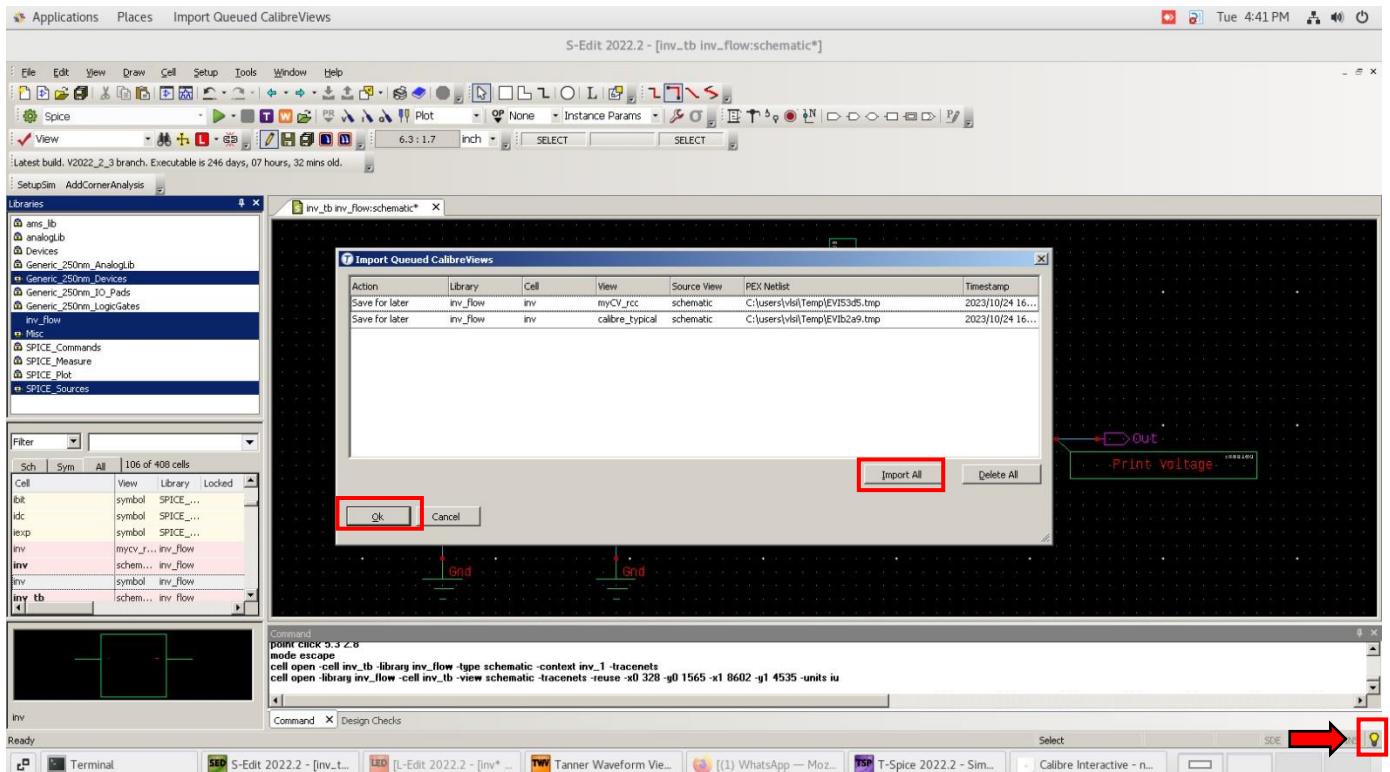
Setup >> Preferences >> General >> Calibre



Remove the old cellmap file and add the new path:

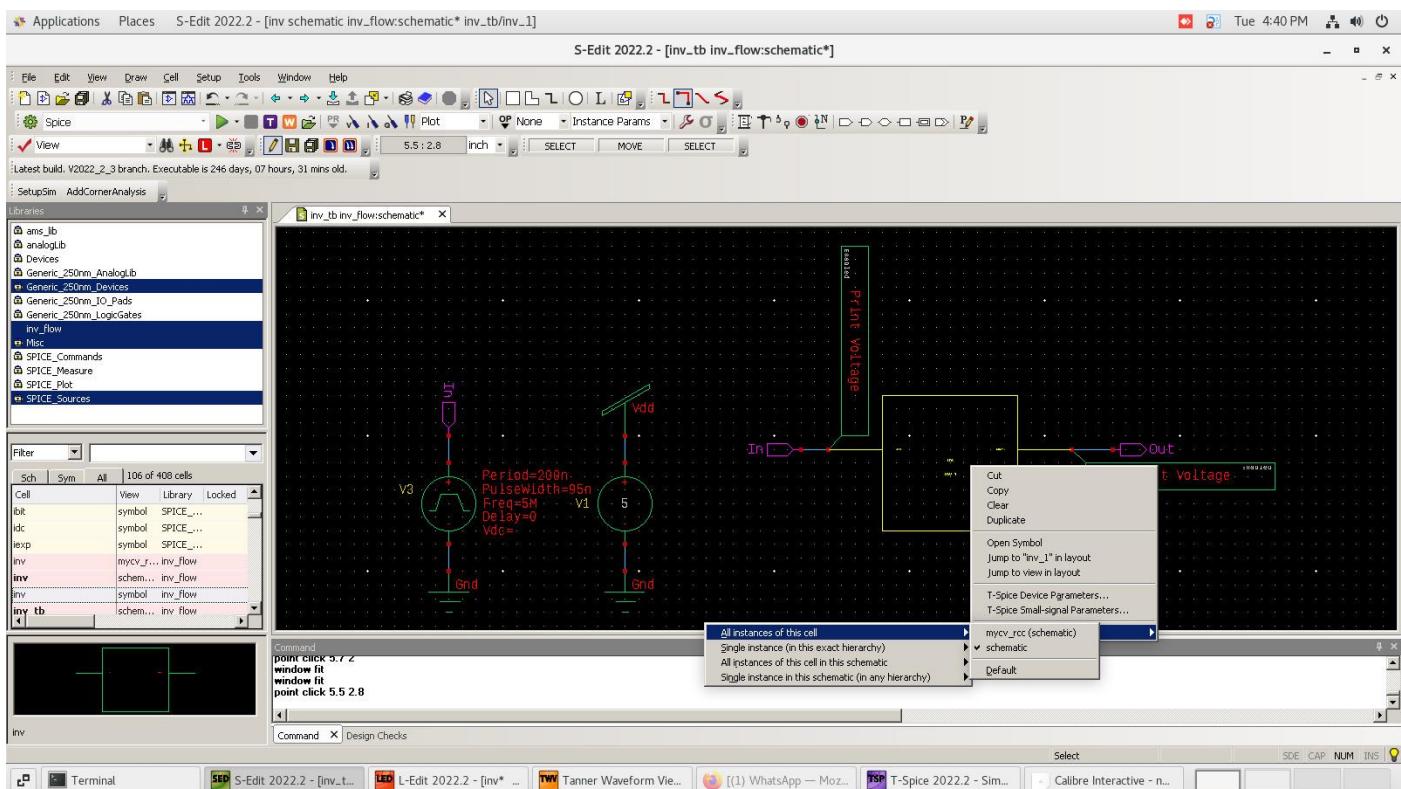
"/eda/Mentor/Tanner/TannerTools_v2022.2/Process/Generic_250nm/Rules/Calibre/Generic_250nm.cellmap"

Press the lamp in the bottom right, import calibre view and press ok



Now right click in your symbol (long click) and choose....

Netlist >> All instance of this cell >> Choose schematic or mycv_rcc.



Now you can decide whether you want to simulate your schematic or the extracted one. Re calculate the propagation delay and analyze the difference.