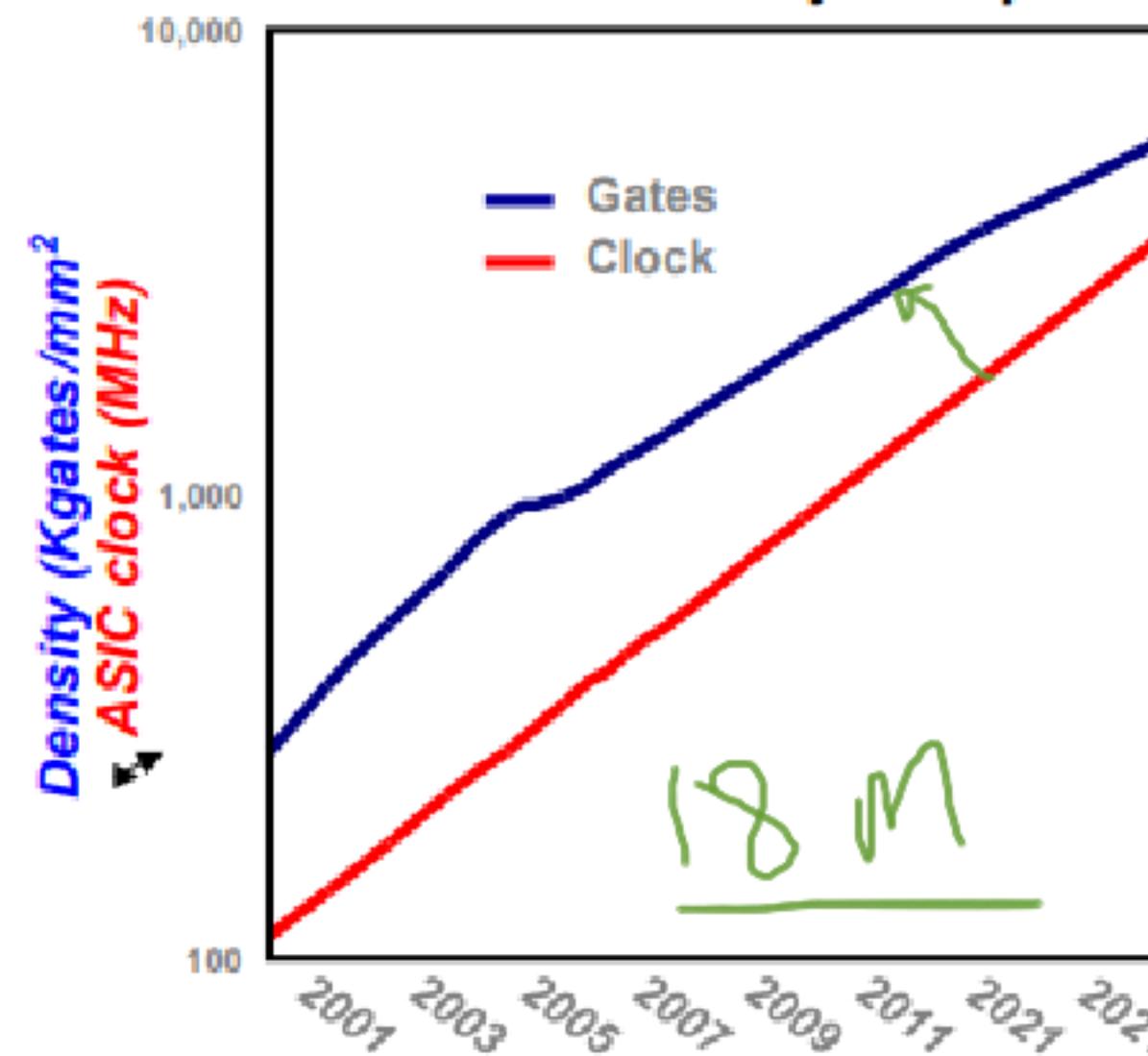


Growing Design-Productivity Gap

Moore's Law:

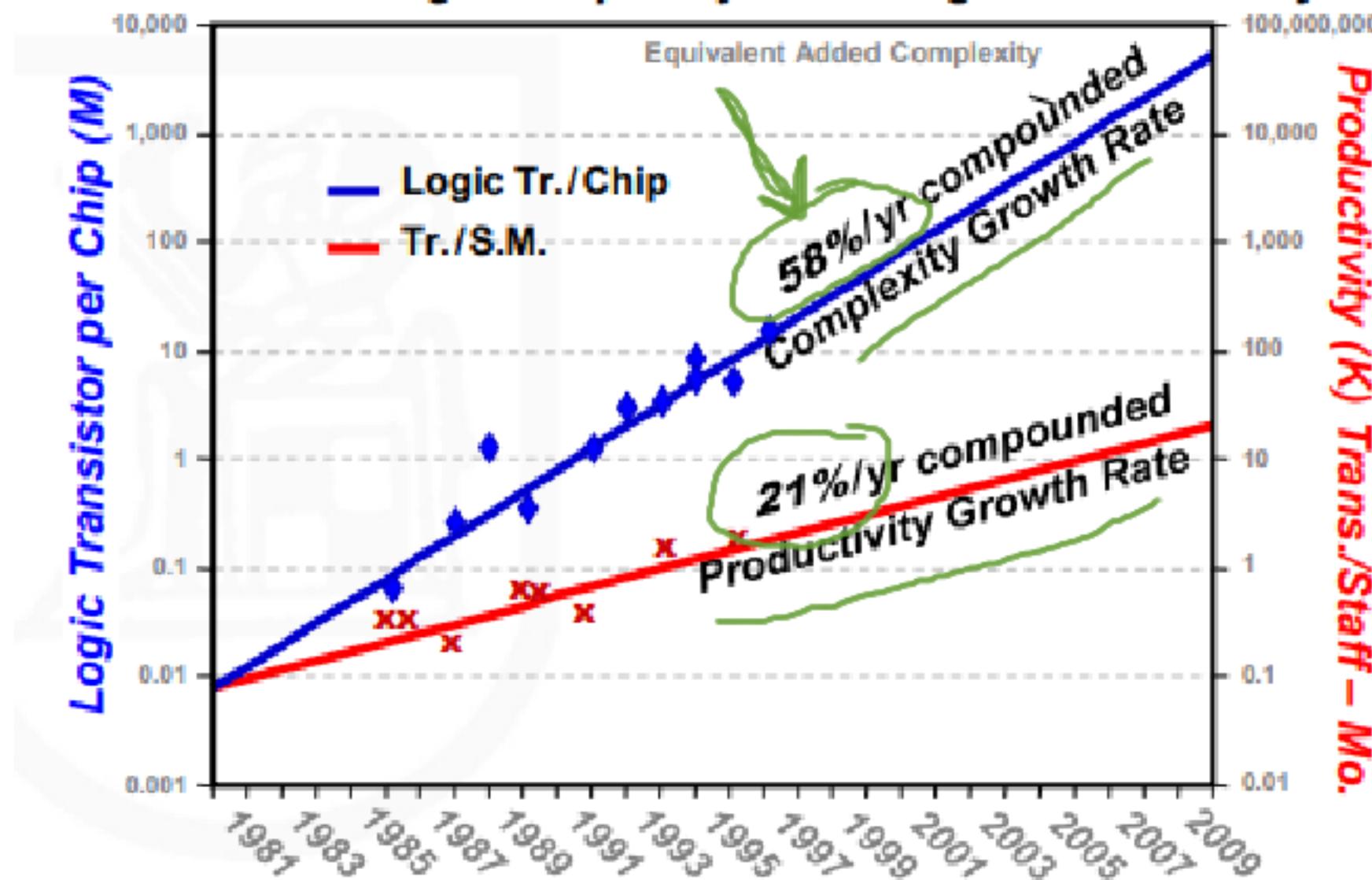
Standard cell density and speed



Source: (SRC 1997)

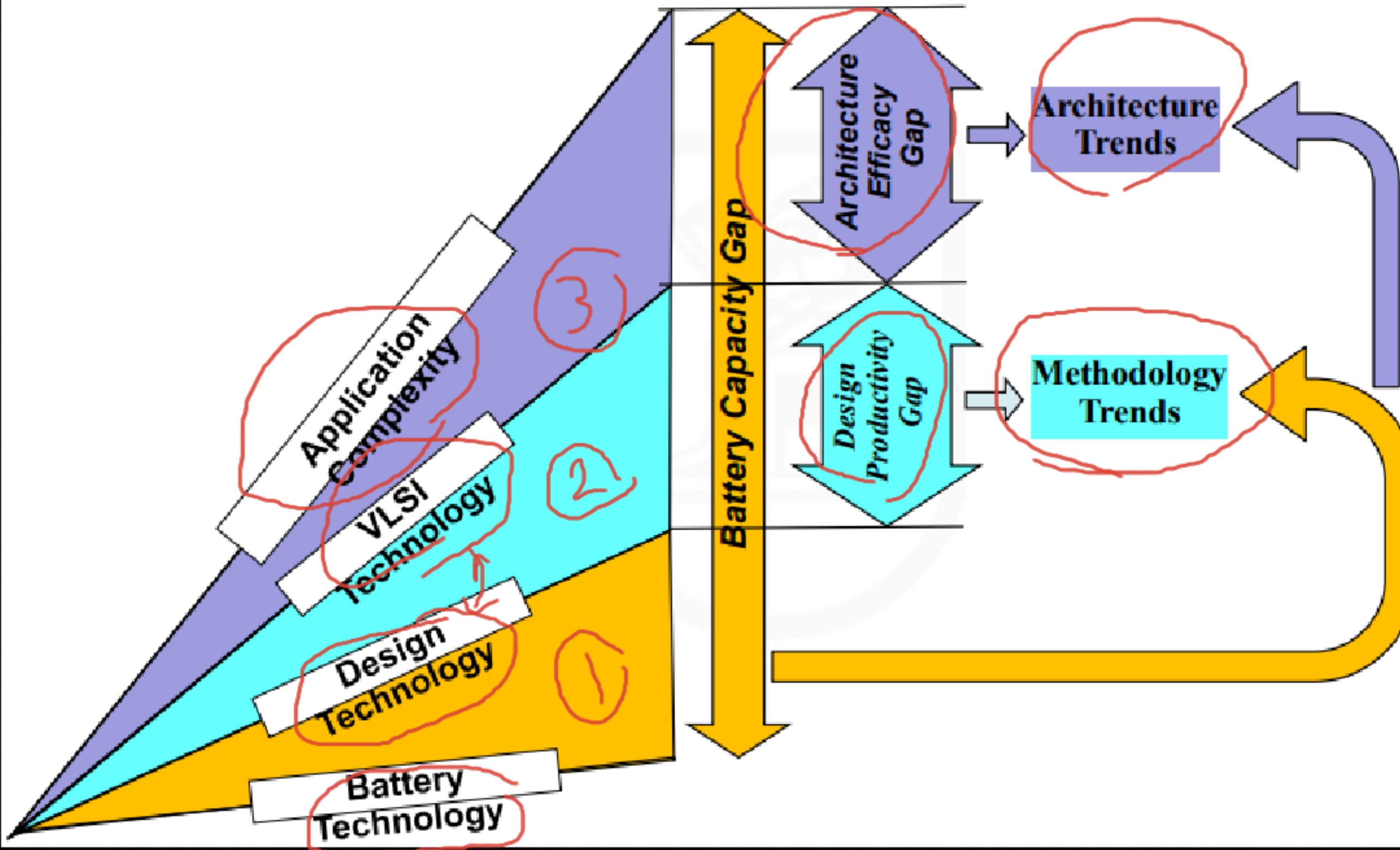
Design Productivity Crisis

Potential Design Complexity and Designer Productivity

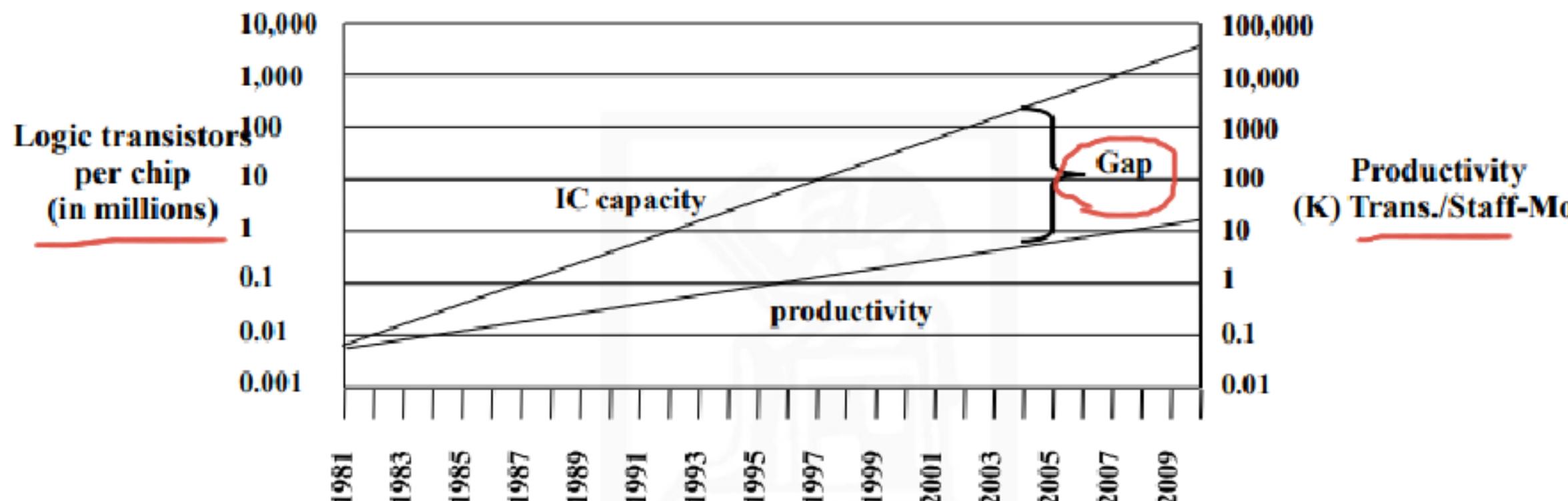


Designs do not only get more complex, but also much more expensive!

Trends that Shape the Gap



Design Productivity

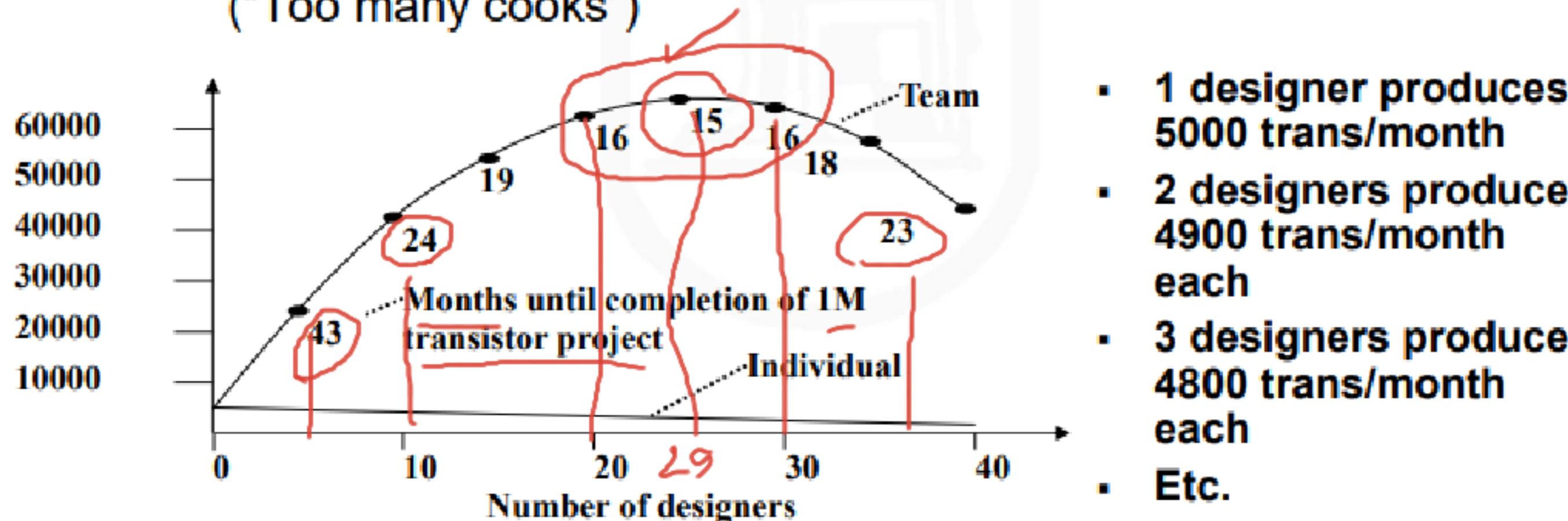


- **Design productivity gap:**
 - Productivity grew at an impressive rate over the past decades
 - Yet, the rate of improvement has not kept pace with chip capacity

- 1981 leading edge chip required 100 designer months
 - 10,000 transistors / 100 transistors/month
- 2002 leading edge chip requires 30,000 designer months
 - 150,000,000 / 5000 transistors/month

Design Productivity

- The situation is even worse:
 - In theory, adding designers reduces project completion time
 - In reality, productivity per designer decreases due to complexities of team management and communication
 - At some point, can actually lengthen project completion time! (“Too many cooks”)



Optimizing Design Metrics

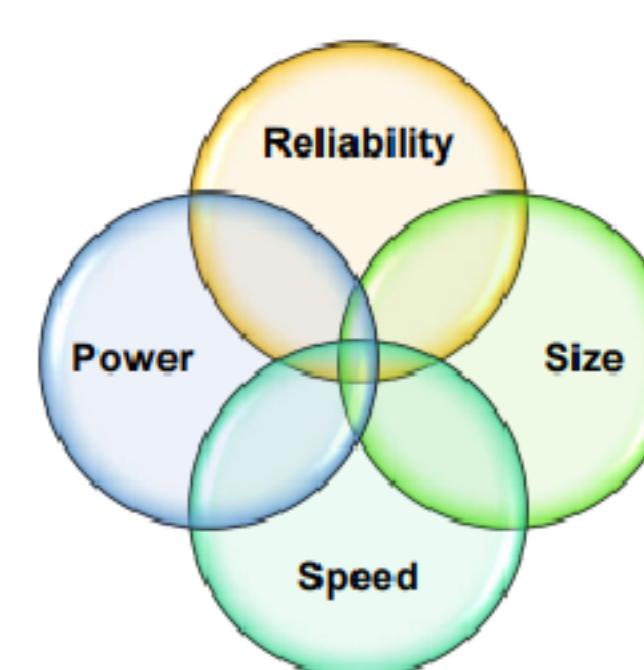
- **Obvious system design goal:**
 - Construct an implementation of an electronic system with desired functionality
- **Key design challenge:**
 - Simultaneously optimize numerous design metrics
- **Design metric**
 - A measurable feature of a system's implementation
 - Optimizing design metrics is a key challenge

Optimizing Design Metrics

- **Common metrics**

1.
 - **Size**: the physical space required by the system (Area)
2.
 - **Performance**: the execution time or throughput of the system
3.
 - **Power**: the amount of power consumed by the system
- **NRE (Non-Recurring Engineering) cost**:
The one-time monetary cost of designing the system

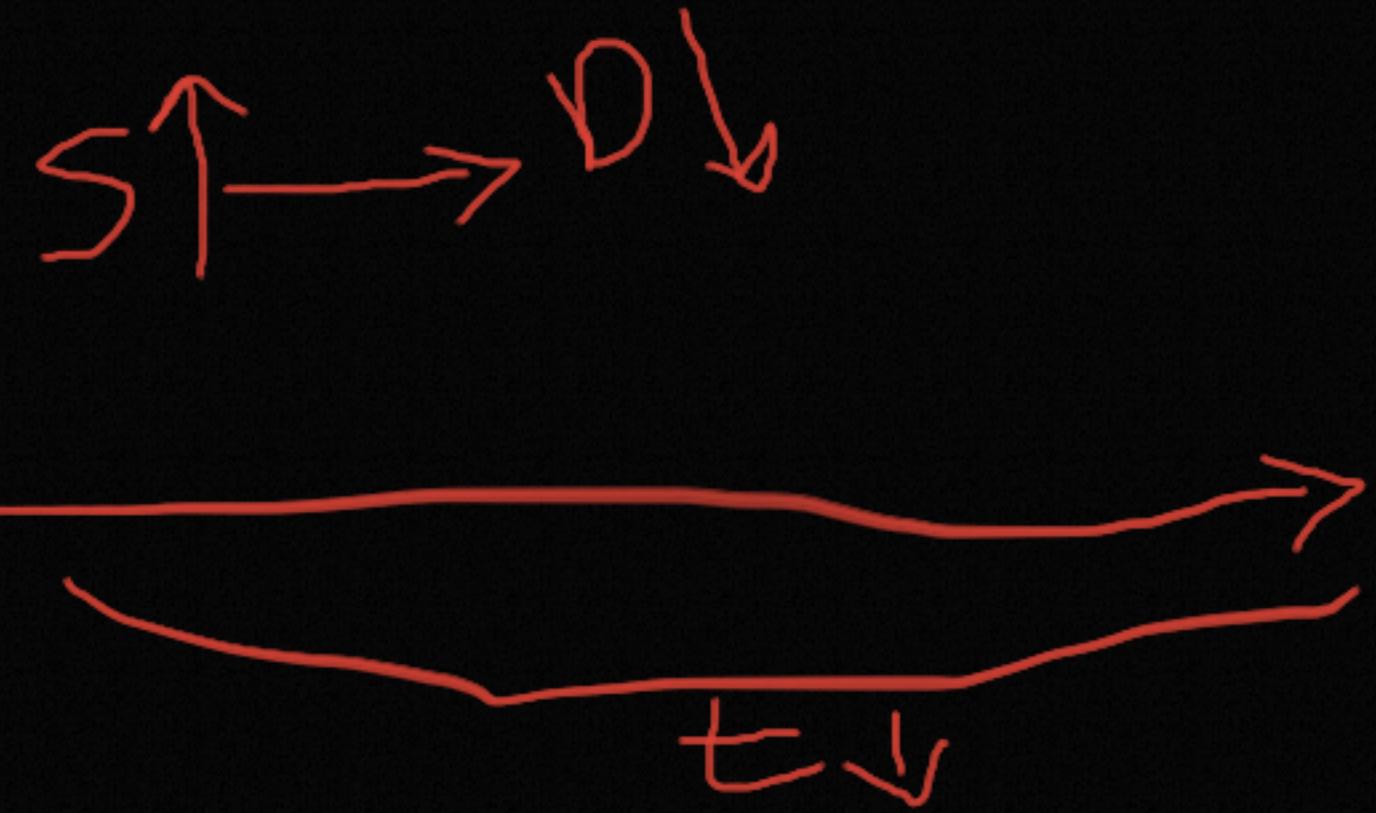
NRE cost refers to:
the one-time cost to
research, design, develop
and test a new product or
product enhancement.



- **Unit cost**: the monetary cost of manufacturing each copy of the system, excluding NRE cost
- **Flexibility**: the ability to change the functionality of the system without incurring heavy NRE cost
- **Time-to-prototype**: the time needed to build a working version of the system
- **Time-to-market**: the time required to develop a system to the point that it can be released and sold to customers
- **Maintainability**: the ability to modify the system after its initial release
- **Correctness**
- **Safety**
- **Many more...**

- **Performance:** typically refers to speed
 - Increasing the speed of a circuit is equivalent to reducing signal delays
- **Widely-used measure of a system, widely-abused**
 - Clock frequency, instructions per second – not good measures
 - Digital camera example: a user cares about how fast it processes images, not clock speed or instructions per second

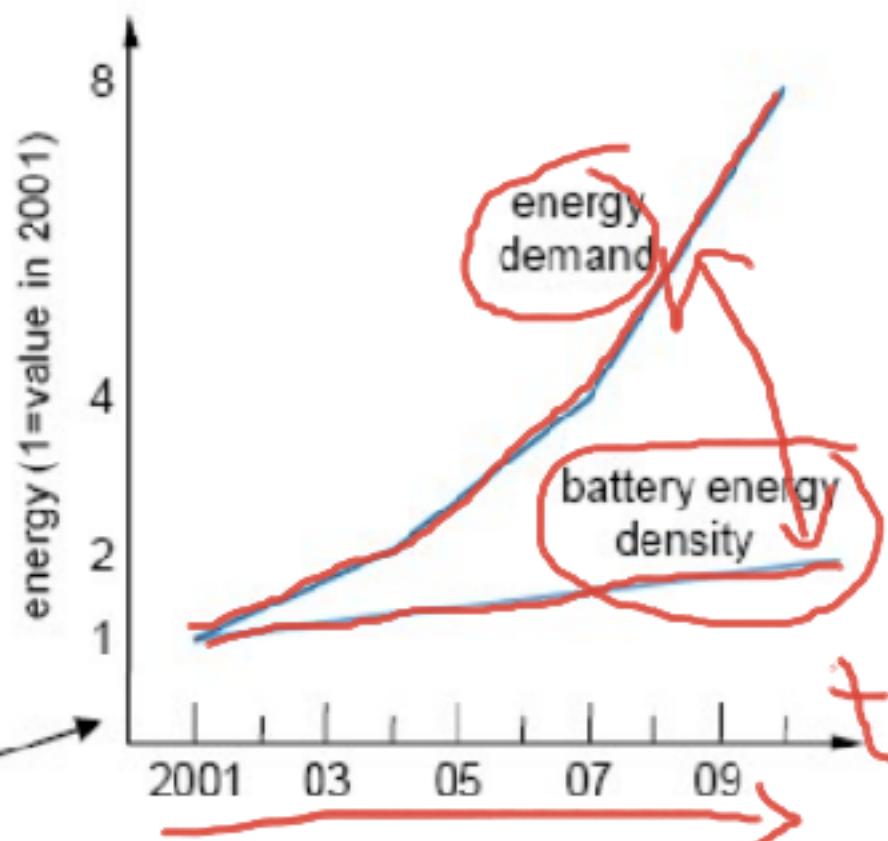
Start = 10
End = 30
Latency = 20 sec



- **Other measures of performance:**
 - Latency (response time)
 - Time between task start and end
 - e.g. Cameras A and B process images in 0.25 seconds
 - Throughput
 - Tasks per second
 - e.g. Camera A processes 4 images per second
 - Throughput can be more than latency (seems to imply concurrency)
 - e.g. Camera B may process 8 images per second (by capturing a new image while previous image is being stored)

• Power Consumption:

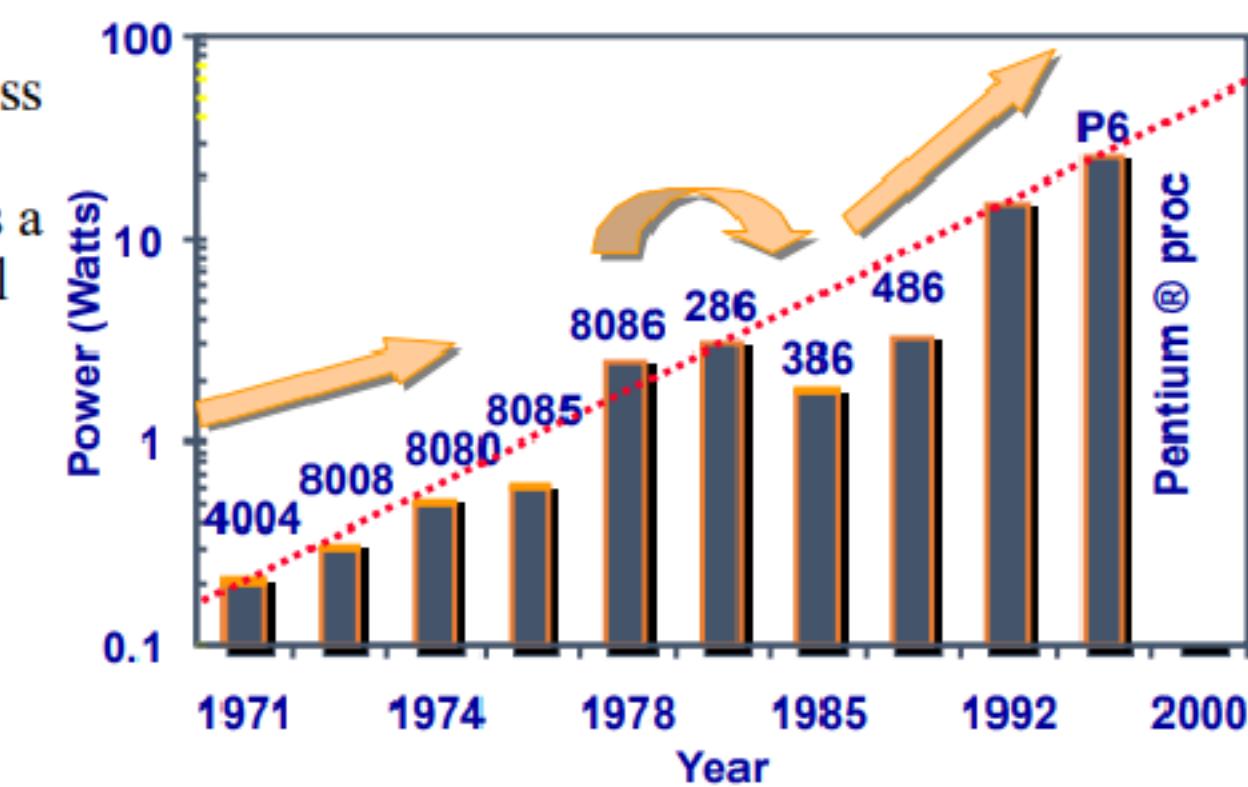
- Increasingly important as more transistors fit on a chip
- Power not scaling down at same rate as size
 - Means more heat per unit area – cooling is difficult
 - Batteries are not improving at the same rate



Power Dissipation



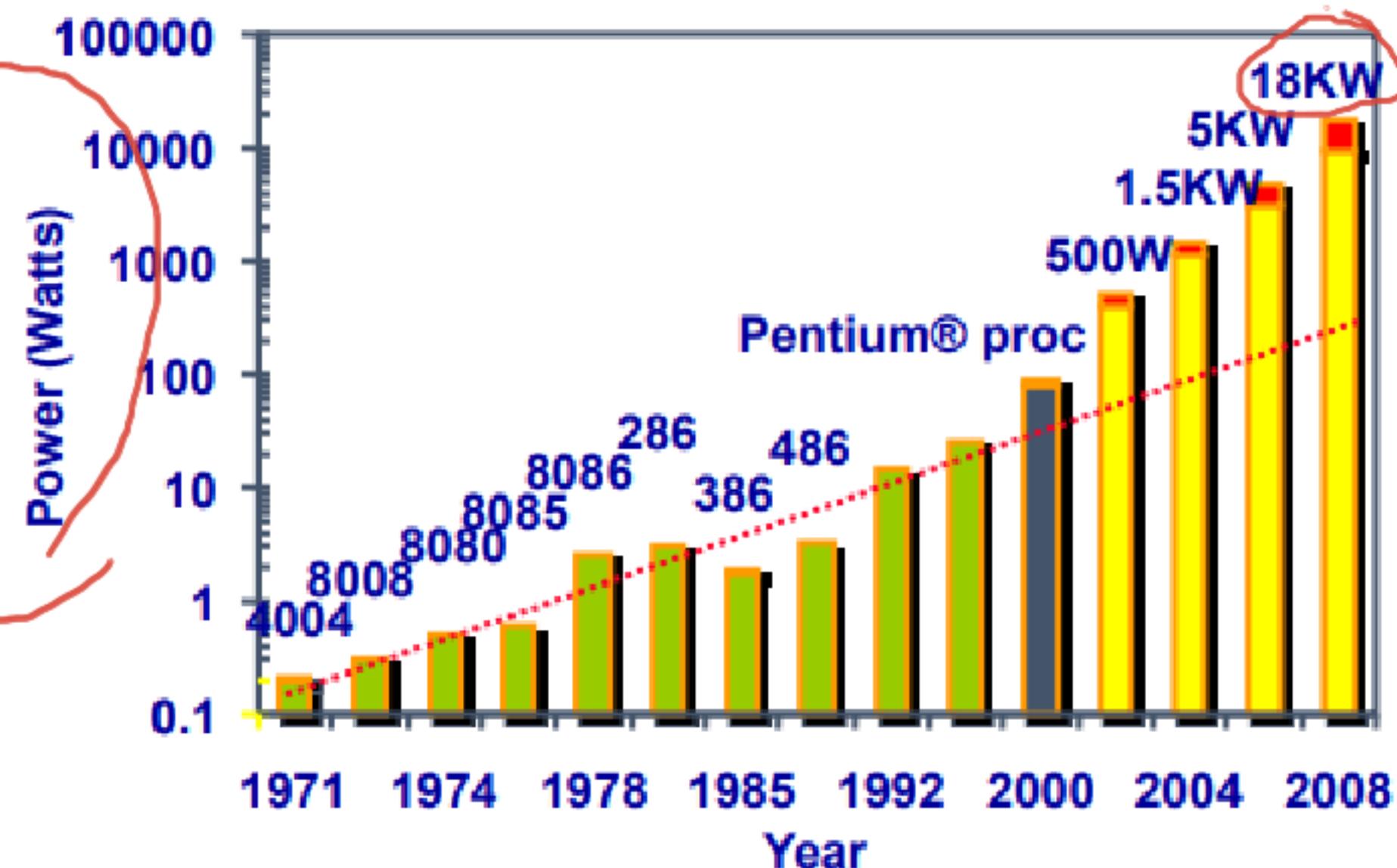
- **Power dissipation** is the process of loss of power in the form of heat due to primary action. It is a naturally occurring process. All the resistors that are part of the circuit and have a voltage drop across them will dissipate power.
- A VLSI circuit's power consumption may be divided into two categories: **static power dissipation** and **dynamic power dissipation**.



Lead Microprocessors power continues to increase

Power will be a Major Problem

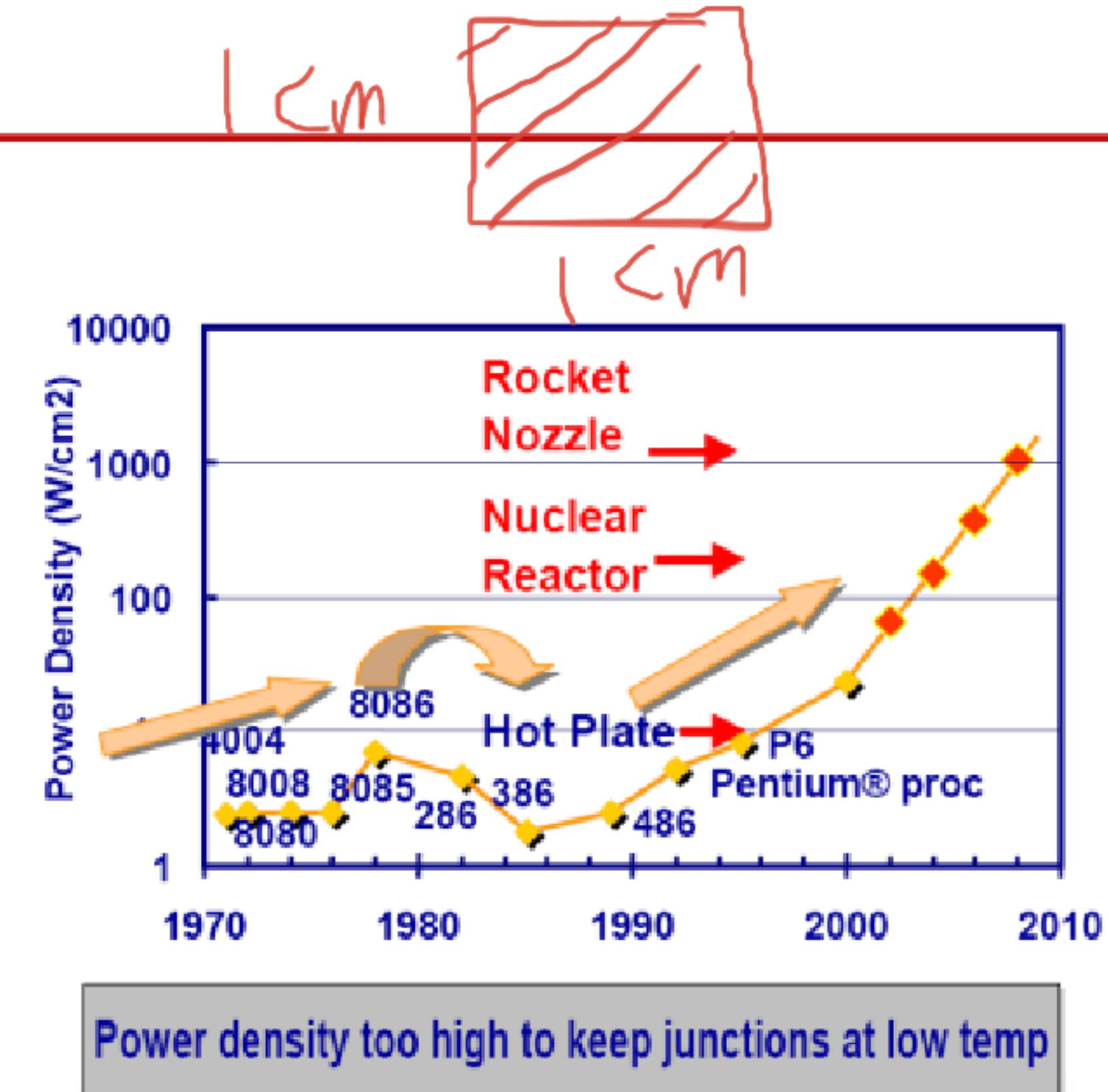
- **Static power** is the power consumed when there is no circuit activity or you can say, when the circuit is in quiescent mode.
- **Dynamic power** is the power consumed when the circuit is in operation, which means we have applied supply voltage, applied clock and changing the inputs. It is mainly due to the **dynamic currents**, such as capacitance currents (switching power) and short-circuit currents (short-circuit power).



Power delivery and dissipation will be prohibitive

Power density

- The concept of power density in VLSI circuits was first introduced by Najim et al.
- The authors define transition density to be **the average switching rate** and develop a technique for computing average switching rate based on stochastic models of logic signals.



• NRE cost (Non-Recurring Engineering cost):

- The one-time monetary cost of designing the system
- Includes:
 - Design cost (CAD tools + designers)
 - Masks
 - Any other one time cost (prototyping, false runs, ...)

NRE cost ==> the one-time cost to research, design, develop and test a new product or product enhancement.

When budgeting for a new product, NRE must be considered to analyze if a new product will be profitable.

- Mask cost per process:

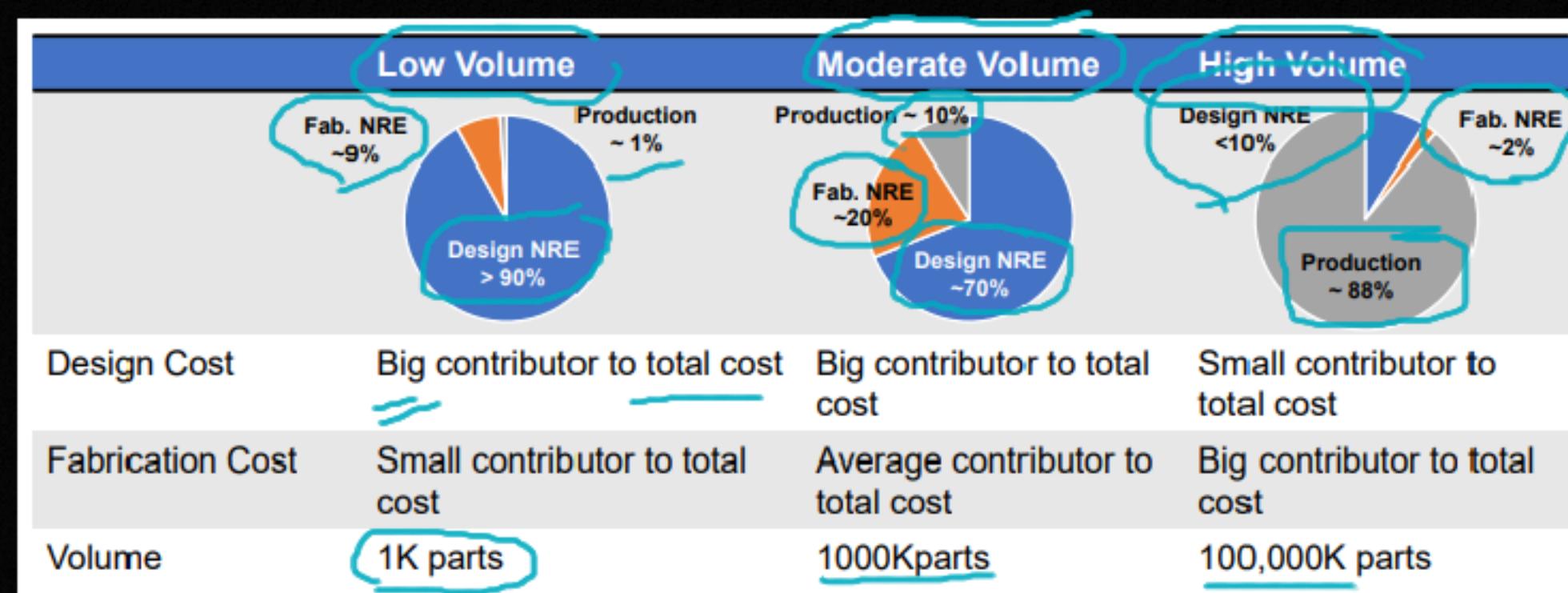
| Process(μ) | 2.0 | ... | 0.8 | 0.6 | 0.35 | 0.25 | 0.18 | 0.13 | 0.09 |
|------------------------|-----|-----|-----|-----|------|------|------|-------|-------|
| Single Mask cost (\$K) | 1.5 | | 1.5 | 2.5 | 4.5 | 7.5 | 12 | 40 | 60 |
| # of Masks | 12 | | 12 | 12 | 16 | 20 | 26 | 30 | 34 |
| Mask Set cost (\$K) | 18 | | 18 | 30 | 72 | 150 | 312 | 1,000 | 2,000 |

▪ Design cost:

- Can reach \$10s to \$100s of million for high-performance ICs

▪ Mask costs:

- Before 0.65 μm, mask costs were stable at around \$18K/set
- Since then they have approximately doubled every process node
 - Caused by sub wavelength feature sizes,
 - more metal layers due to interconnect dominance,
 - reduced mask yields, mask inspection and repair costs,
 - ...



- **Unit cost:**

- The monetary cost of manufacturing each copy of the system, excluding NRE cost

- **Includes:**

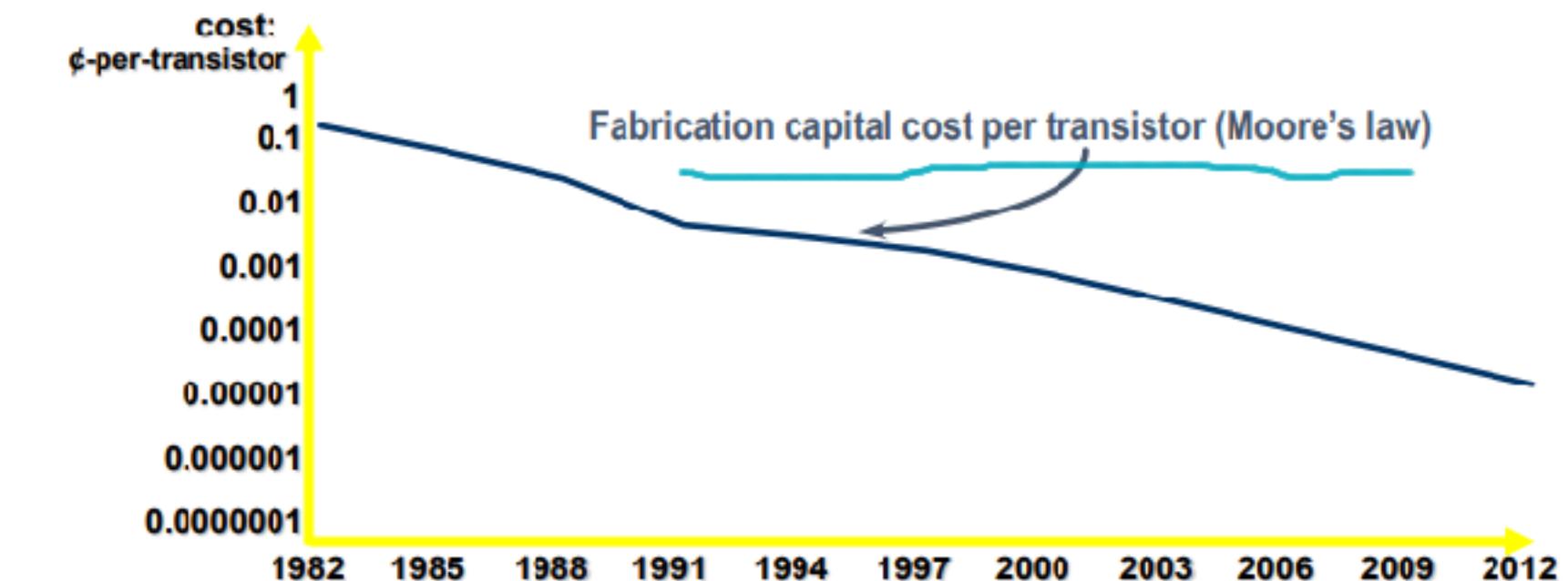
- Fabrication
- Packaging
- Testing

- Total cost = NRE cost + unit cost X # of units

- Per-product cost = total cost / # of units

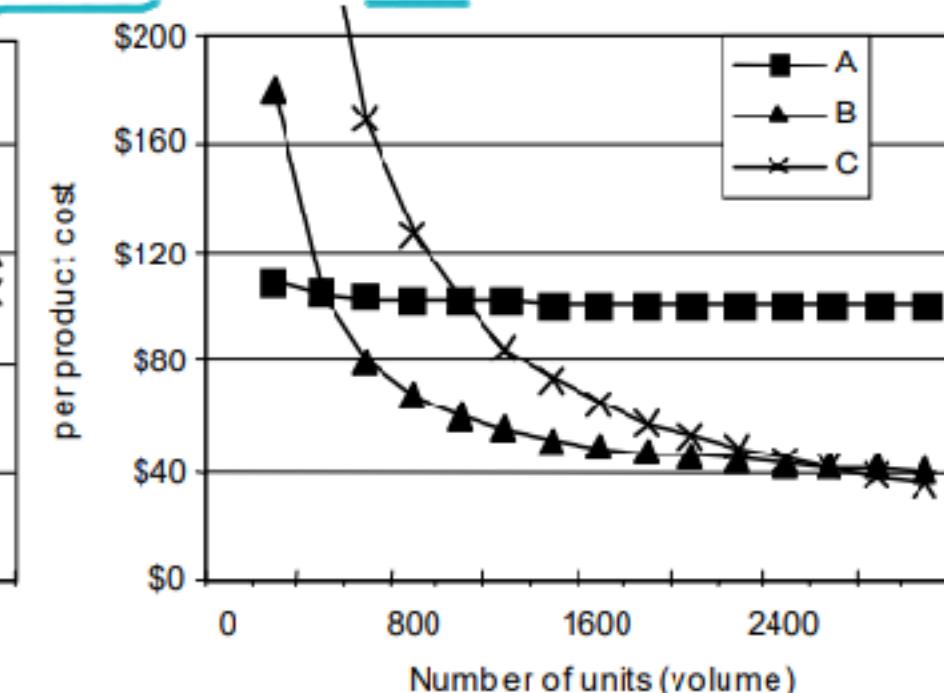
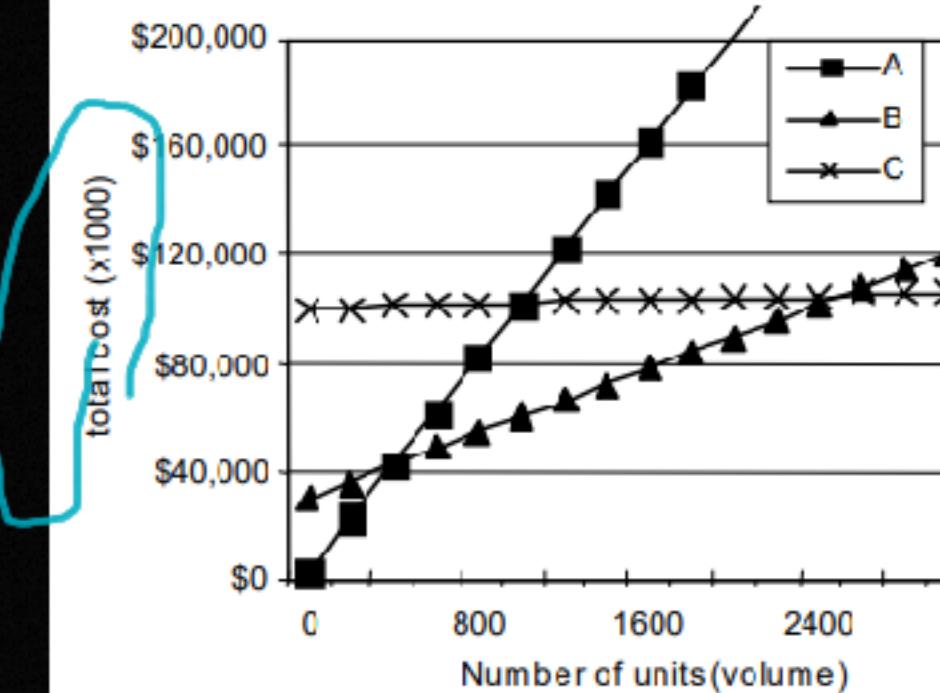
$$= (\text{NRE cost} / \# \text{ of units}) + \text{unit cost}$$

Cost per Transistor



- Compare technologies by costs – best depends on quantity

- Technology A: NRE=\$2,000, unit=\$100
- Technology B: NRE=\$30,000, unit=\$30
- Technology C: NRE=\$100,000, unit=\$2



- **Time-to-market:**

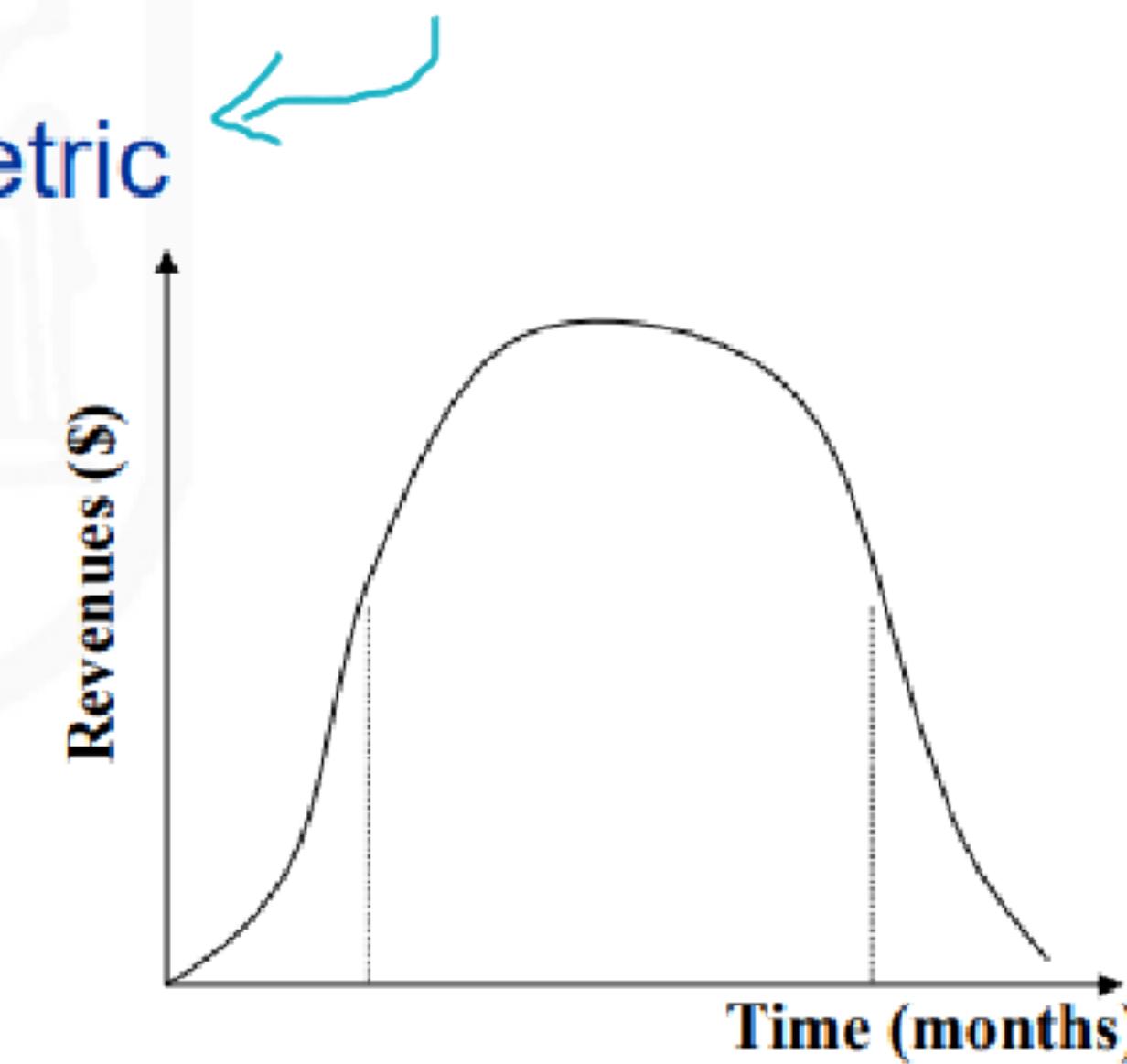
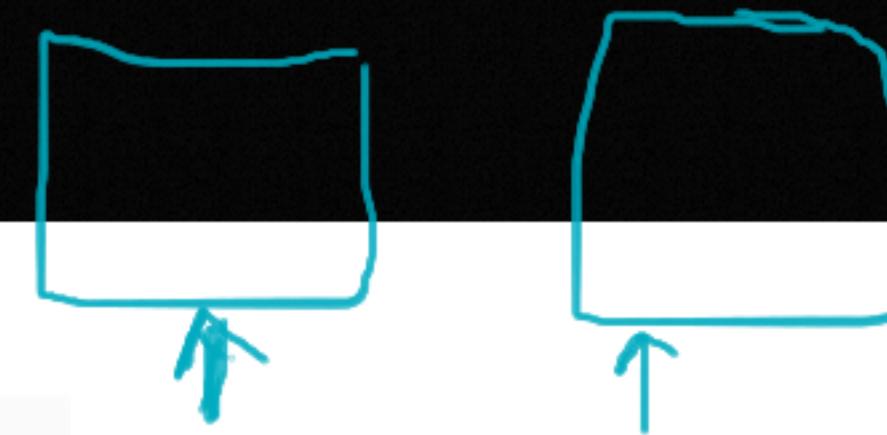
- Time required to develop a product to the point it can be sold to customers

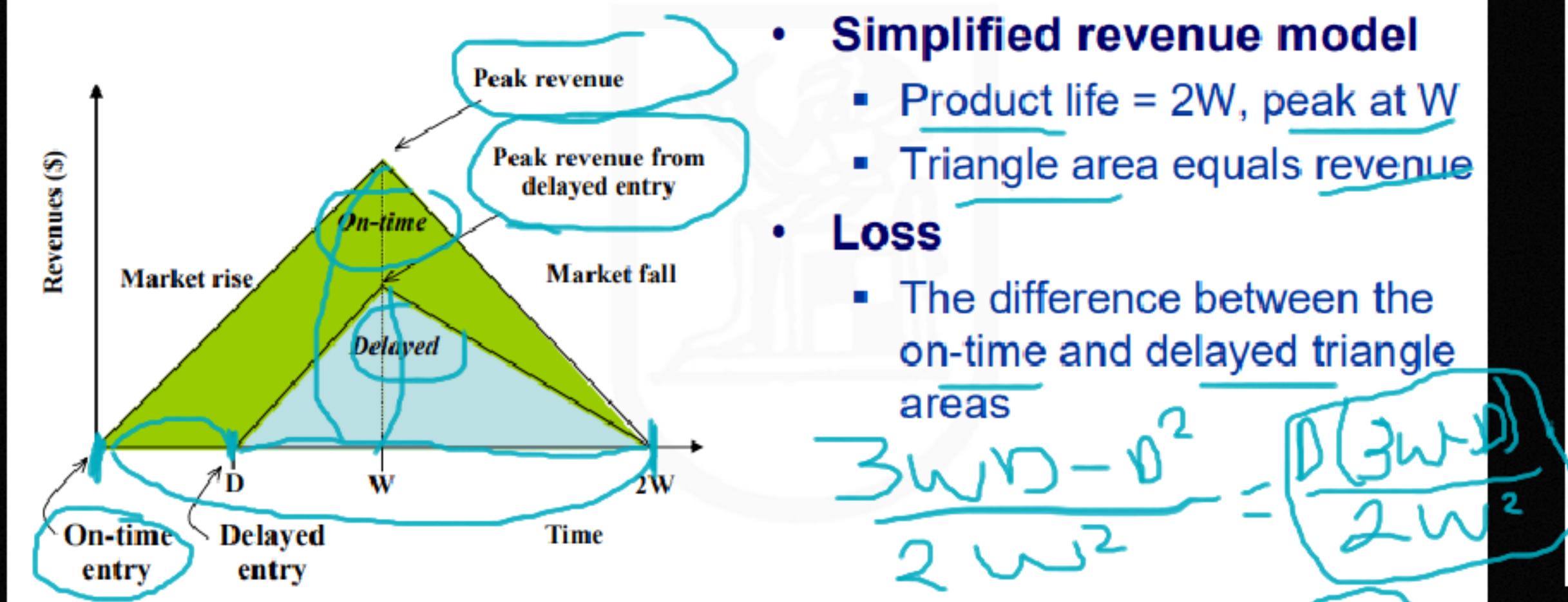
- Very demanding design metric

- Market window

- Period during which the product would have highest sales

- **Delays can be costly**





- Area:**
 - On-time = $\frac{1}{2} * 2W * W$
 - Delayed = $\frac{1}{2} * (W-D+W) * (W-D)$
 - Percentage revenue loss = $(D(3W-D)/2W^2) * 100\%$
- Some examples:**
 - Lifetime = 52 wks, delay = 4 wks
 $- (4*(3*26 - 4)/2*26^2)*100\% = 22\%$
 - Lifetime = 52 wks, delay = 10 wks
 $- (10*(3*26 - 10)/2*26^2)*100\% = 50\%$

Delays are Costly!!!

$$\text{On-time} = \frac{1}{2} 2W * W = \frac{W^2}{2}$$

$$\text{Delayed} = \frac{1}{2} (2W - D)(W - D) = \frac{1}{2} [2W^2 - 3WD + D^2]$$

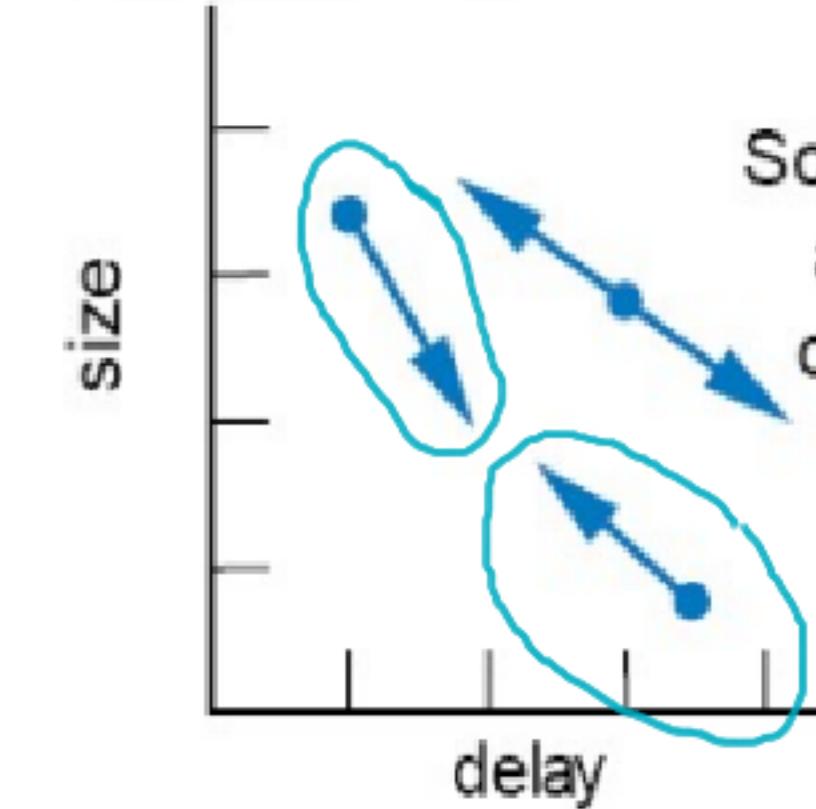
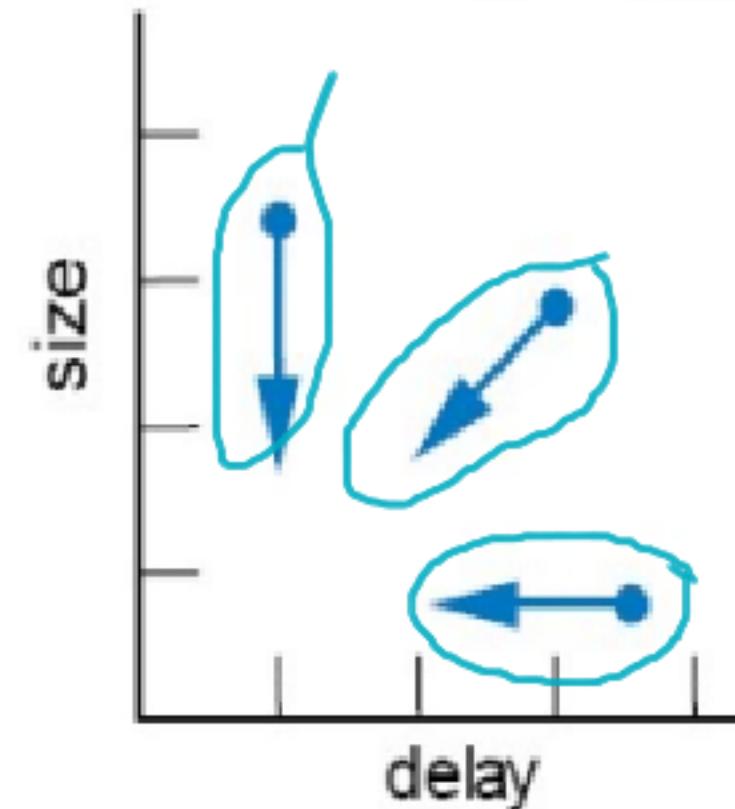
$$\% \text{ Rev. loss} = \frac{\text{On-time} - \text{Delayed}}{\text{on-time}} = \frac{\frac{W^2}{2} - \frac{2W^2 - 3WD + D^2}{2}}{\frac{W^2}{2}} = \frac{-W^2 + 3WD - D^2}{W^2}$$

• Optimization vs. Tradeoffs

Optimizations

All criteria of interest are improved (or at least kept the same)

$S \uparrow \rightarrow P \uparrow$



Tradeoffs

Some criteria of interest are improved, while others are worsened

- We obviously prefer optimizations, but often must accept tradeoffs

