Lab 1: NMOS VI CHARACTERISTICS

OBJECTIVE

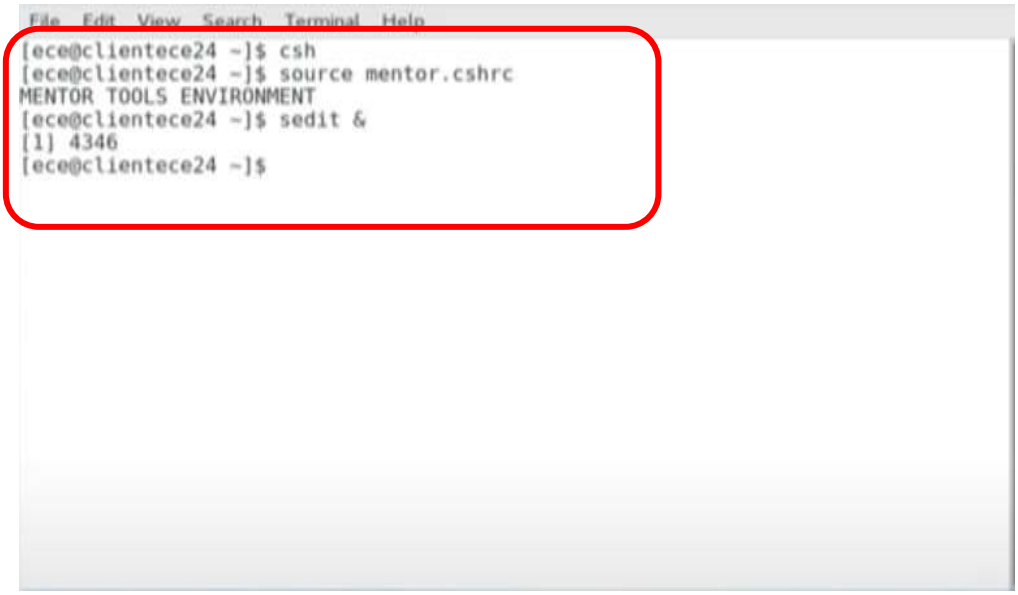
The objective of this lab is to characterize the NMOS transistor as the following:

- Characterize the NMOS & PMOS transistor by examine the “DC Sweep Analysis”.
- I-V behavior Simulatation of NMOS & PMOS transistor.

SCHEMATIC ENTRY

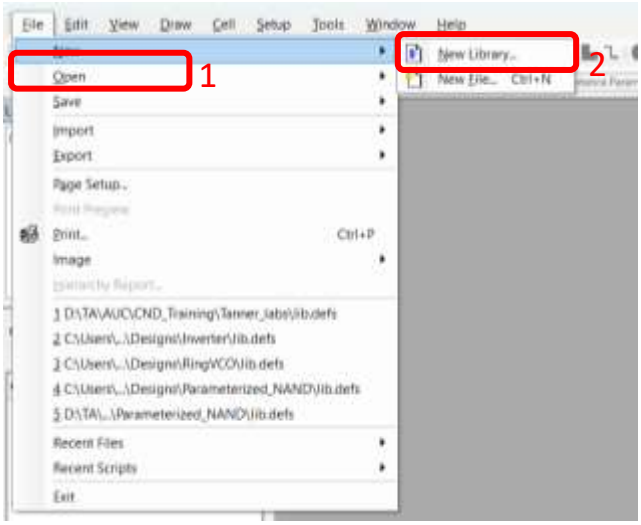
1. To build a schematic you will use S-Edit, so start it on desktop for windows or on Linux terminal write:

   csh
   source mentor.cshrc
   sedit &



2. To begin, Create new library for your design by simply choosing:
   File >> New >> New Library.
   Now choose you library name and create a new folder with the library name to add it on. You will see that the library you created is added in the **Libraries section on the left of the screen.**

   Remember to name the folder the same name as your Library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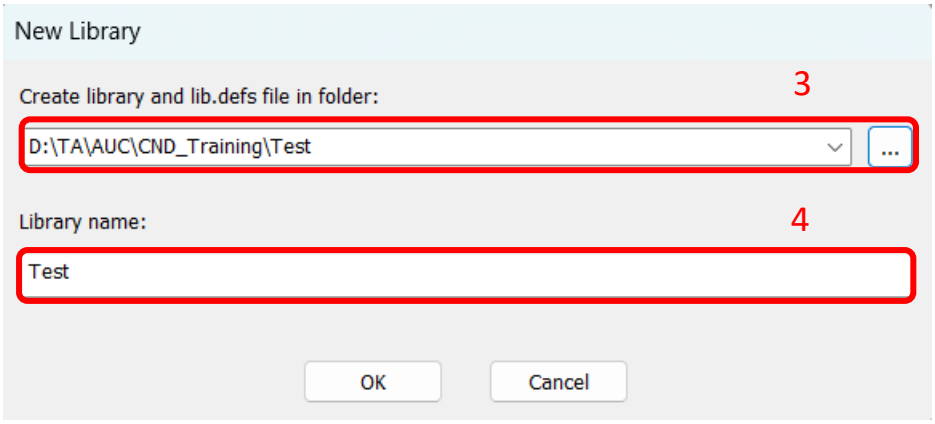
New Library
Create library and lib.defs file in folder:
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D:\TA\AUC\CND_Training\Test
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Library name:
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Test
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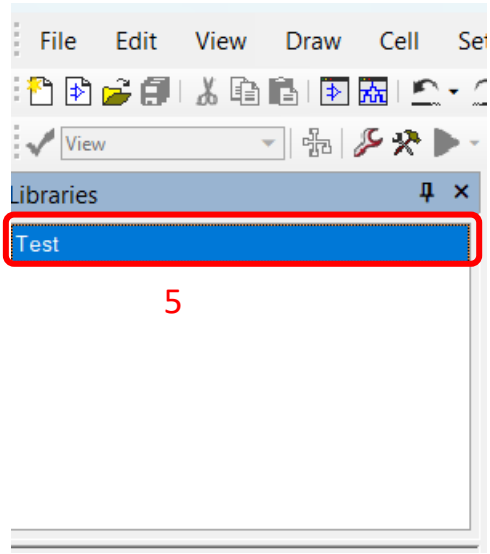
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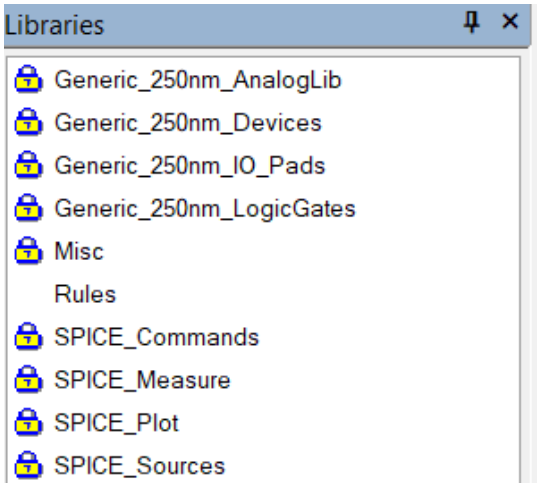
3. You will need to include Libraries of the technology and libraries for basic circuits, which contain the symbols for all basic circuit elements such as resistors, NMOS, capacitors, etc… The libraries for all the basic symbols and technology are in the TannerEDA folder in documents.

   On the left side of the S-edit screen, you will see a Libraries window, **Right-click and choose Add Library**. Browse to: "C:\Documents\TannerEDA\TannerTools_v2019.2\Process\Generic_250nm" and **add all libraries in this folder**. Then browse to: C:\Users\mosta\Documents\TannerEDA\TannerTools_v2019.2\Process\Standard_Libraries **and add all of them.**

   At the end, you should have included all that...



Remember to include the libraries ONE BY ONE

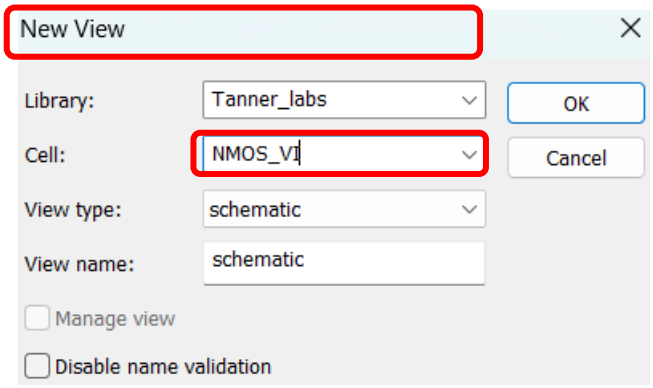
4. Create a new Cell

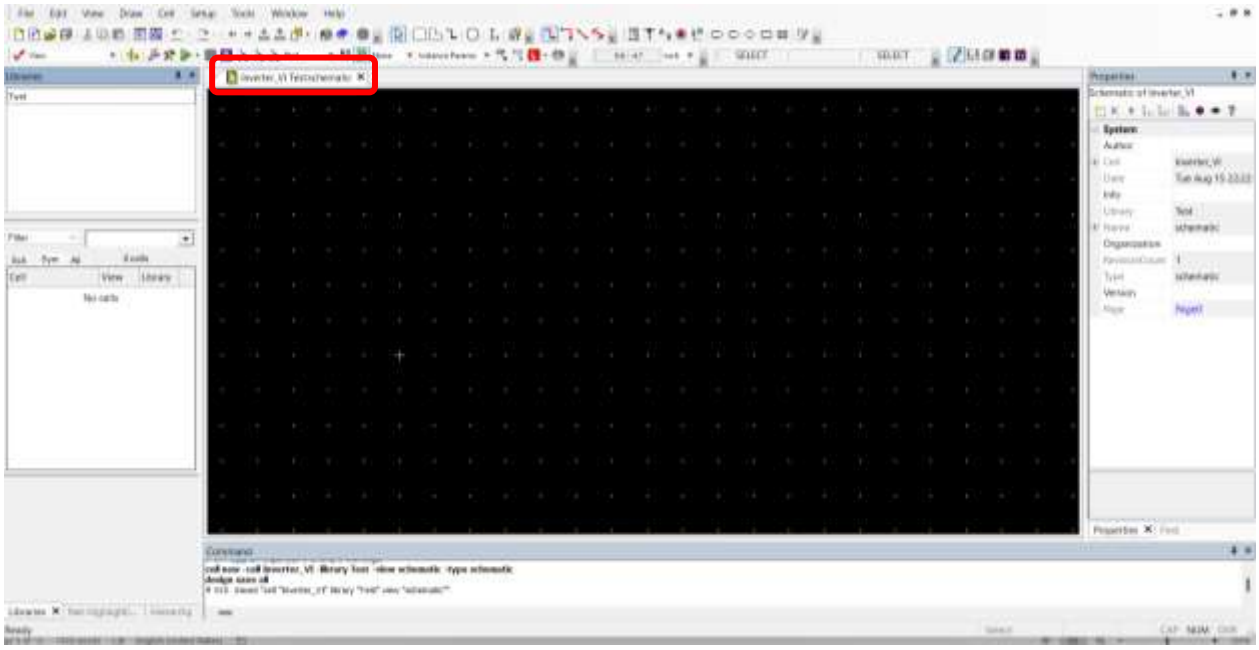
   A "cell" is a design element. A cell can contain multiple views such as schematics and 3 symbols. Cells can be instantiated in other cells. When performing a simulation, we will typically call the cell "Inverter_VI". When we are testing a circuit, for example an inverter, the inverter will have its own cell that contains a schematic of the devices and a symbol. The inverter cell is instantiated in the TOP cell that contains ideal elements such as voltage sources and probes that are only used for simulation. This allows us to separate the cells that are actually going to be implemented on the die versus cells that are only used for simulation. **Simply it is your breadboard.**

   Using the pull down menus, create a new cell view:

Cell >> New View:

Enter the cell name “Inverter_VI”. Ensure the library name is “your library name” and click OK. A blank schematic page will appear. **It is a good idea to save this right now.**

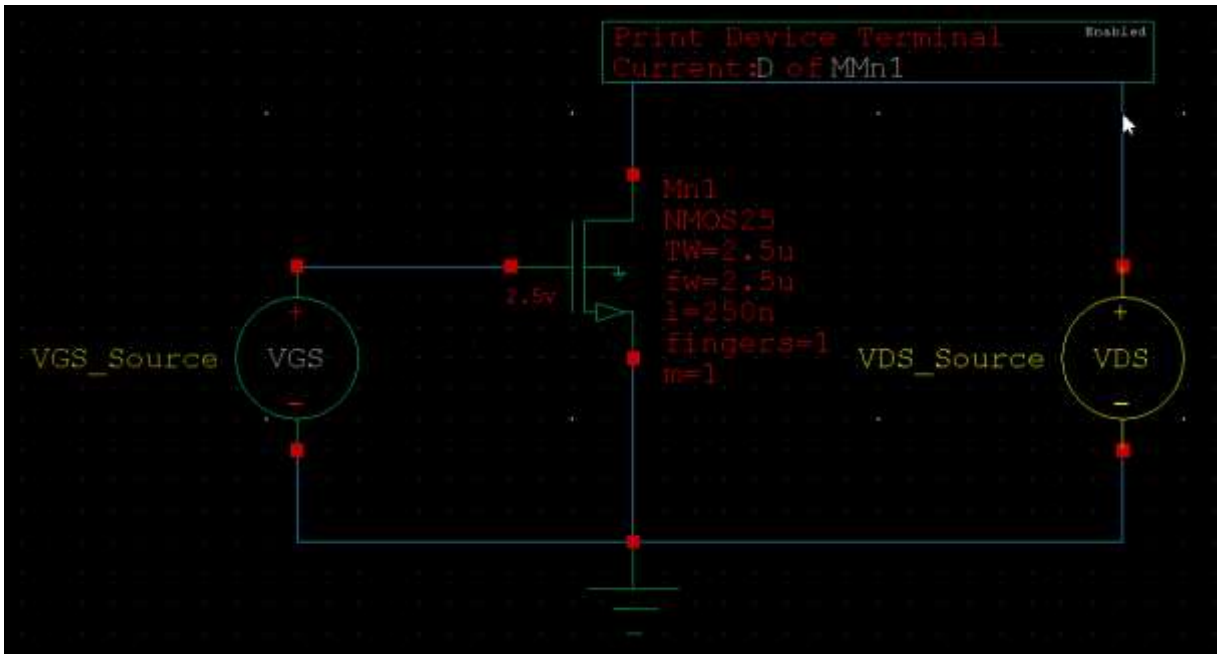




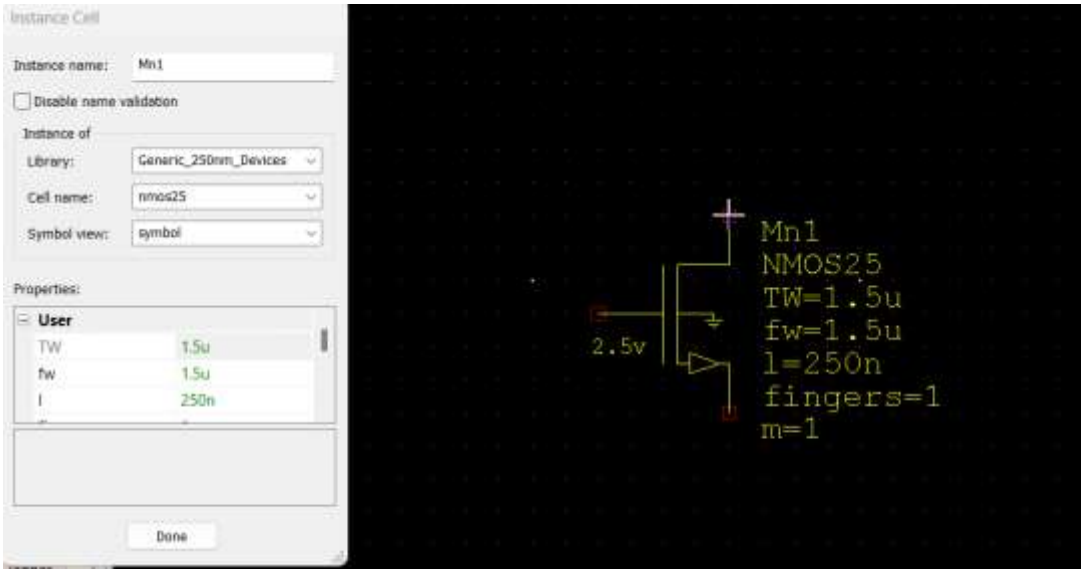
Note that edited files that isn’t saved will be followed by a * so don’t forget to save it

5. Enter the Schematic to simulate the IV behavior of an NMOS Transistor.

   We will be entering the following circuit:



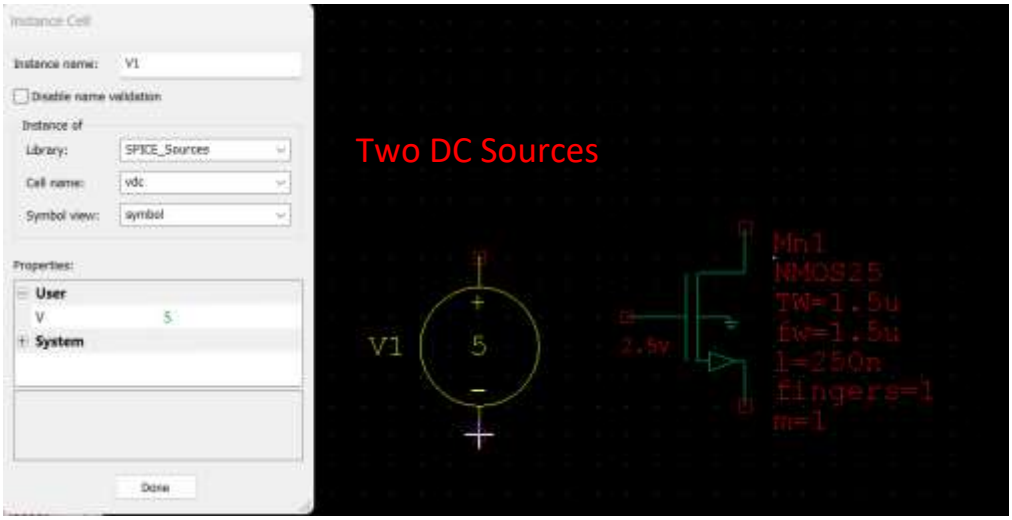
   a) Begin with adding the NMOS transistor. **To add any component you simply press 'I' on the keyboard to open the Instance Cell menu.** To add the NMOS transistor just select as following:



Then left click your mouse and then esc or right click to exit Instance Cell.

Remember to check your design by pressing ✓ on top left hand side.

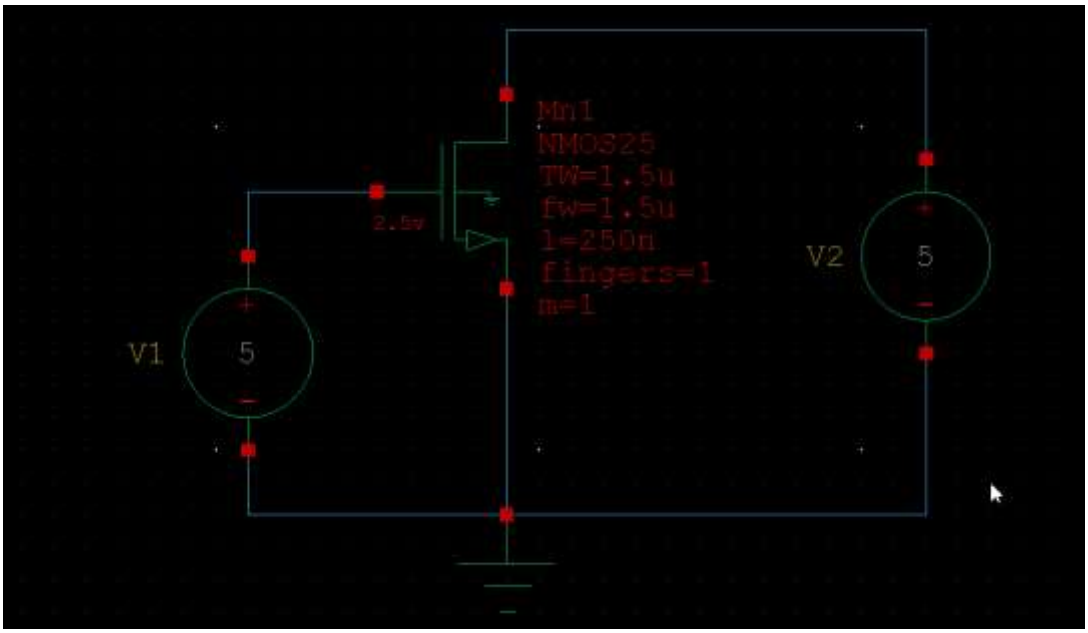
b) Just do the same with other components just as following:



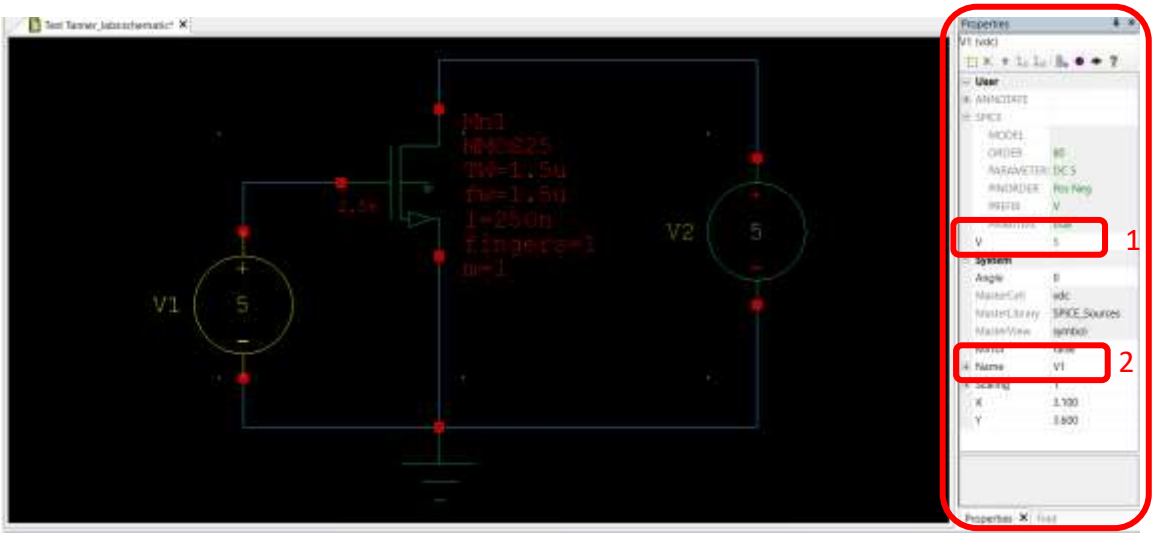
NOTES to help you with editing your Design:

- **To move any component just use this hotkey: Select >> keep pressing ALT and move it.**
- **To rotate any component just use this hotkey: Select >> press R.**
- **To move the page up and down press Ctrl and then scroll with mouse. Our by using keyboard arrows.**
- **To zoom in and out just scroll with mouse. You can also use "+, -" to respectively zoom in and out.**
- **To fit design in screen simply press the 'HOME' Button on the keyboard you might have to press the 'Fn' button with it.**

c) At this point, your schematic is almost complete. All the components have been placed. **To wire them together you need to press the wiring tool**  **from the bar below task bar and begin wiring. To exit Wiring mode simply press esc.**



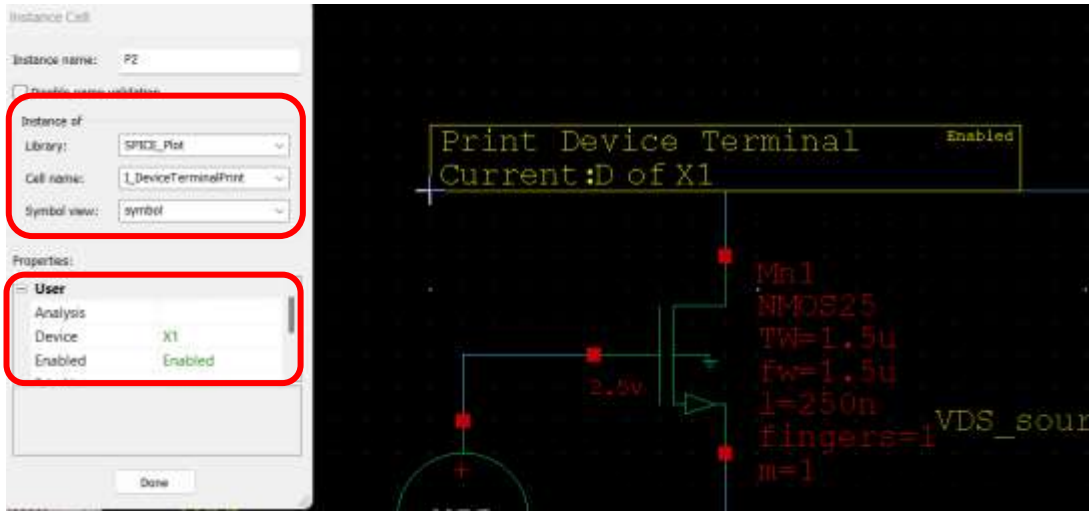
d) Now let us change the DC sources V1 and V2 names and values. To do that you firstly have to select the source you want to edit. A properties section on the right hand of the screen will be shown as following:



1. Change the Voltage source value V from **5 to VGS**.
2. Change the Name from **V1 to VGS_source.**

Remember to press SPACE to redraw window (refresh)

e) Lastly, you need to add the Print Current Spice command, which helps to plot the graph between IDS and VDS while changing the value of VGS as known for in the NMOS IV characteristics.



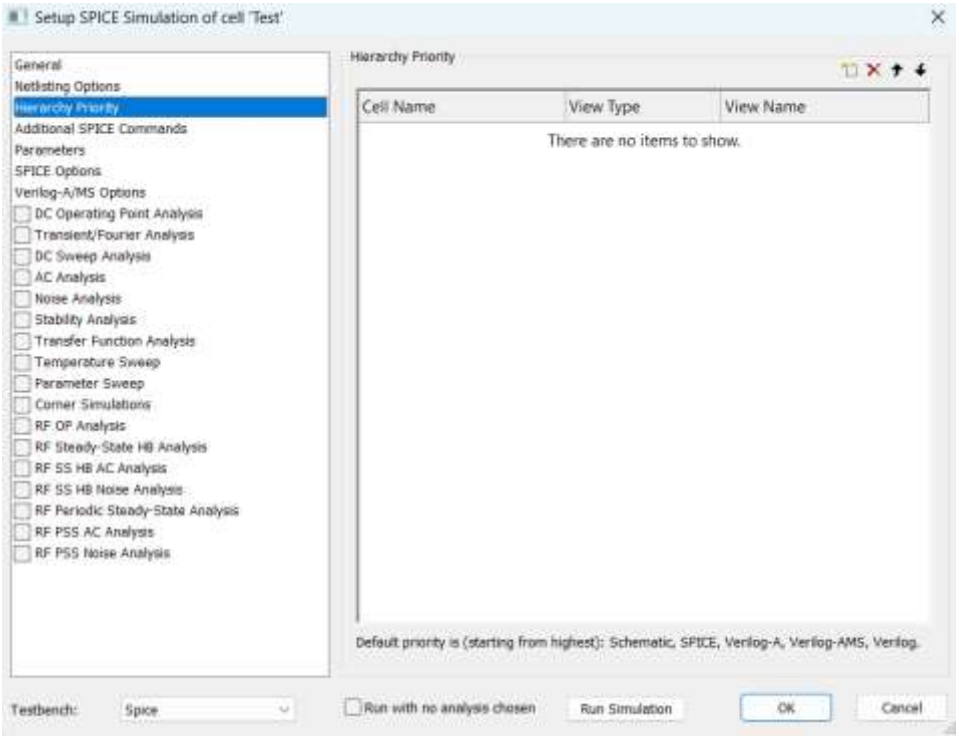
Now select it and change the term **Device** to the transistor name with respect to its prefix**. Also, the term Analysis to DC (VERY IMPORTANT)**

You can see the name and prefix from the properties section when selecting the NMOS transistor as following:

Add the prefix following the name in the Device section so it will go as MMn1.

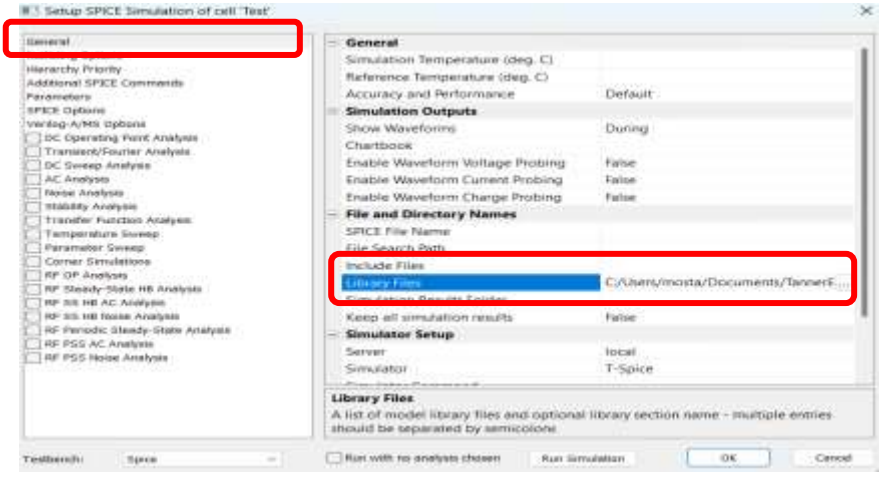
SIMULATION SETUP

1. To setup the simulation the first thing to do is pressing this icon from the toolbar the Setup Spice Simulation window will open.

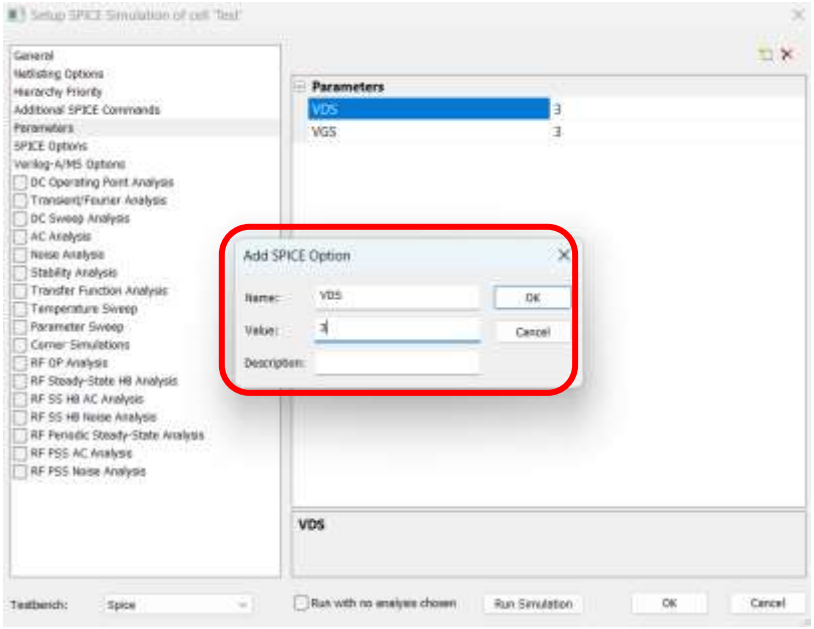


a) Begin with Highlighting "**General**" from the dialog on the left hand side. On the right, click in the "Library Files" field. This is where you will specify any SPICE models you will be using in your simulations. Browse & select: **"C:/Users/Documents/TannerEDA/TannerTools_v2019.2/Process/Generic_250nm/Models/Generic_250nm.lib TT"**

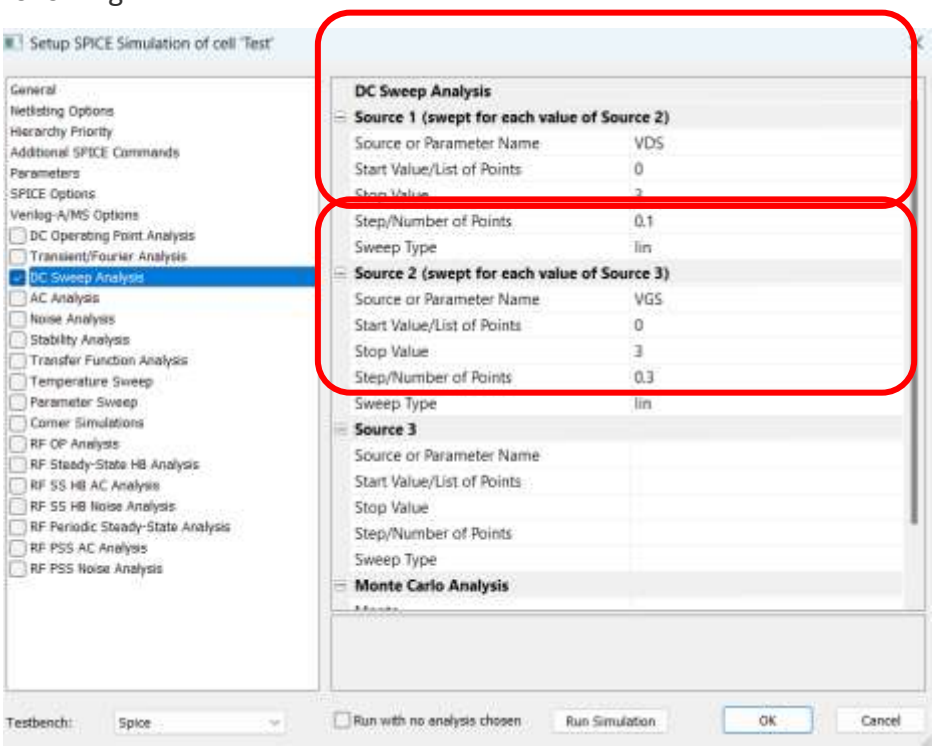
Remember to add 'TT' after the lib file manually



b) Now Highlight "**Parameter**" from the dialog on the left. On the right, click on this icon  on the top right to add a parameter. **Set the VGS parameter to 3V (Maximum possible value). Then set VDS parameter also to 3V.**

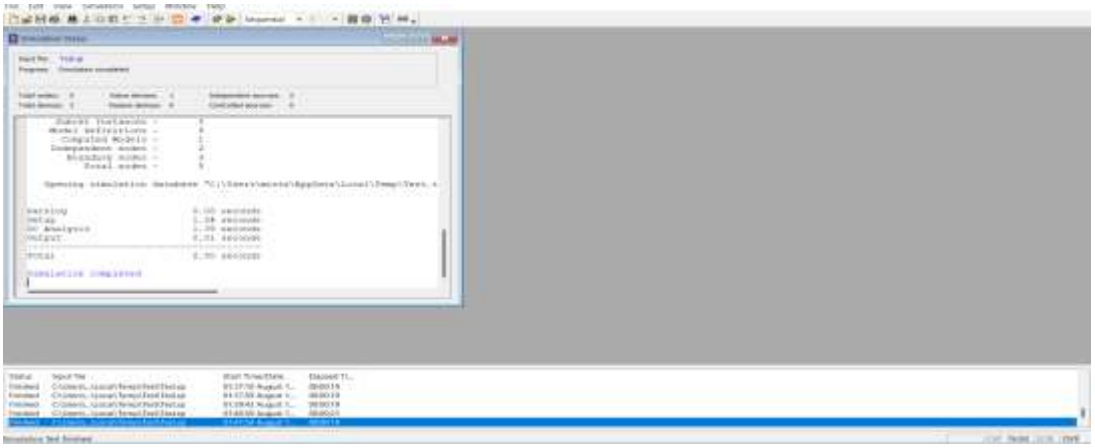


c) Before you can exit this window, you will need to select an analysis type. Just check the "DC Sweep Analysis". On the right begin to set the VDS and VGS as following:

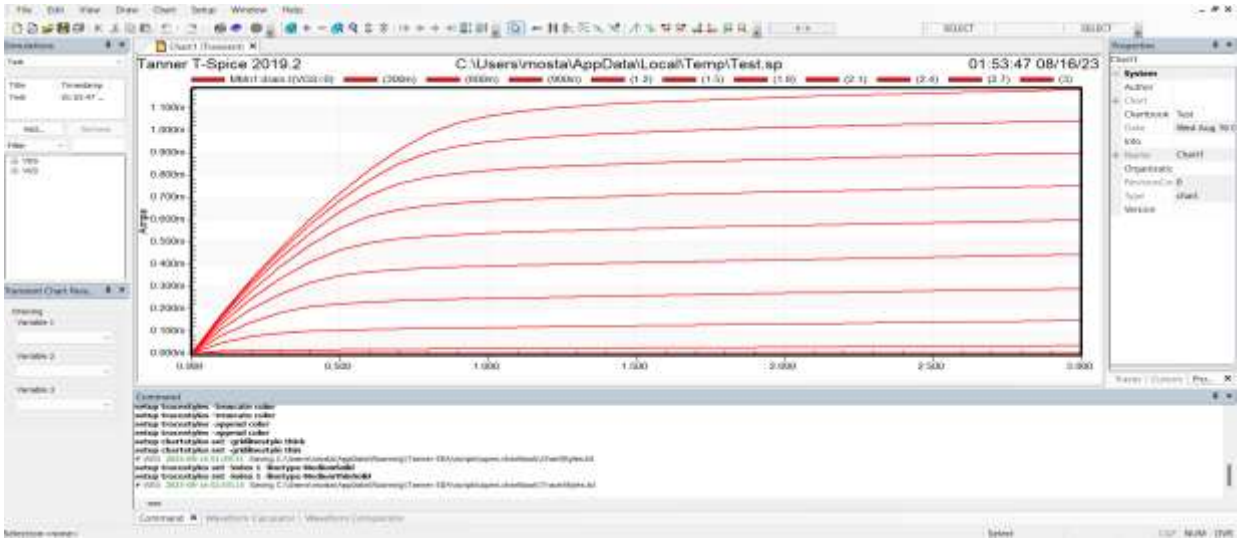


Concerning the ORDER of adding them to show VDS on the X-axis.

d) Now we **SAVE** and run Simulation by simply clicking  it should open another window holding the name "**T-Spice**" to run the spice file of the cell. It should give us Simulation completed.



e) At last, after Simulation completed another window will open holding the name "**Waveform Viewer**" it should show the IV Characteristics of the NMOS.



Assignment (1):

- Do the same as in this Lab, but for the PMOS transistor.
- **Bonus** – based on Generic 250nm Process using TannerEDA CAD tool do the following for NMOS transistor:
  - Analyze the effect of varying V_{BS} on V_{th}.
  - Analyze short and long channel effects and comment on the results.