Lab 6: Latch

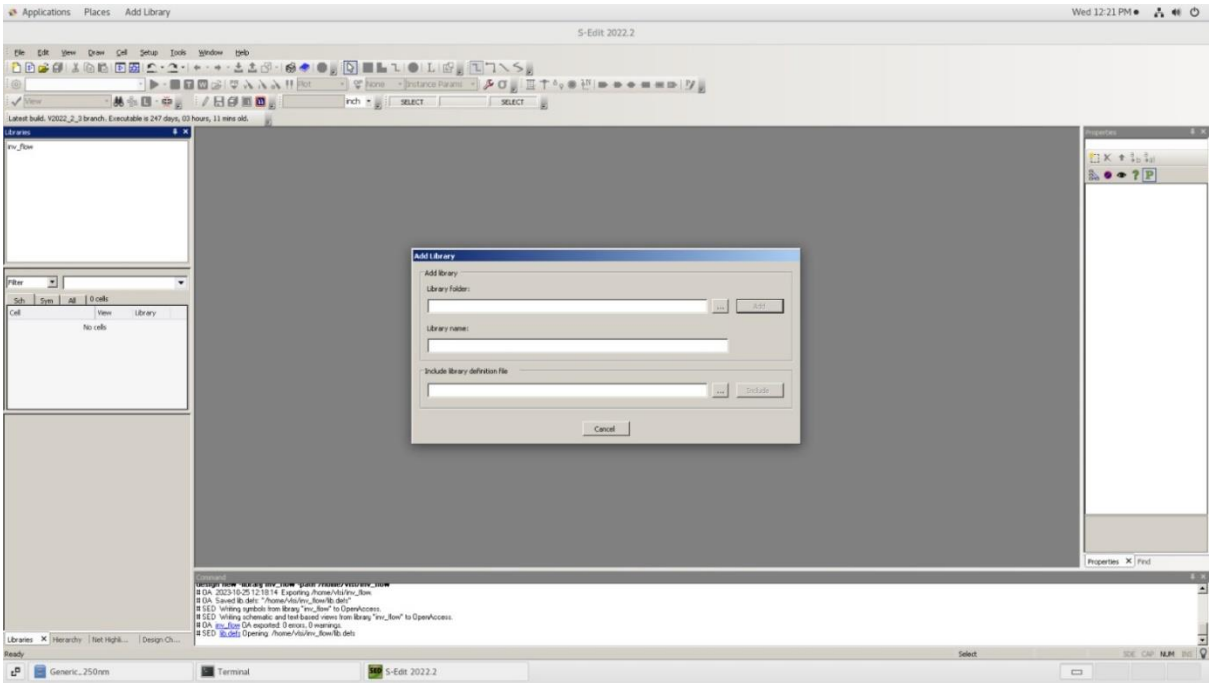
Objective

The objective of this lab is to go through the full design flow of positive latch, including frontend and backend flow (Design, Simulation, layout, DRC, LVS, Parasitic extraction and post layout simulation).

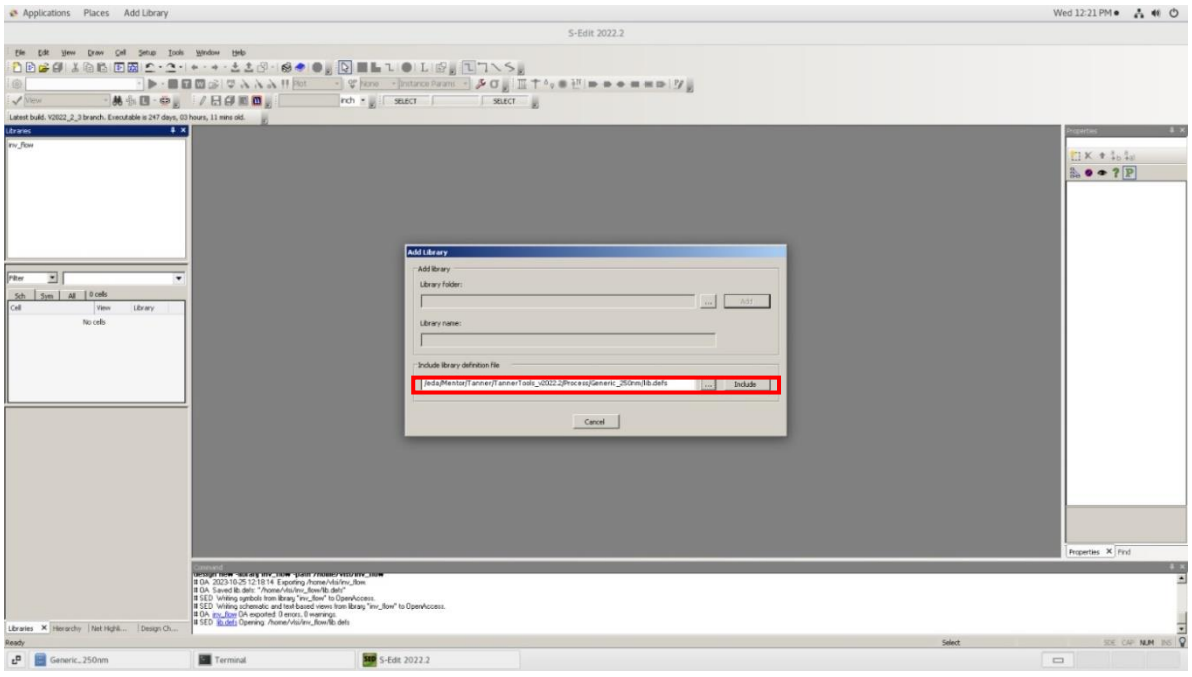
Frontend Flow

1. Include libraries

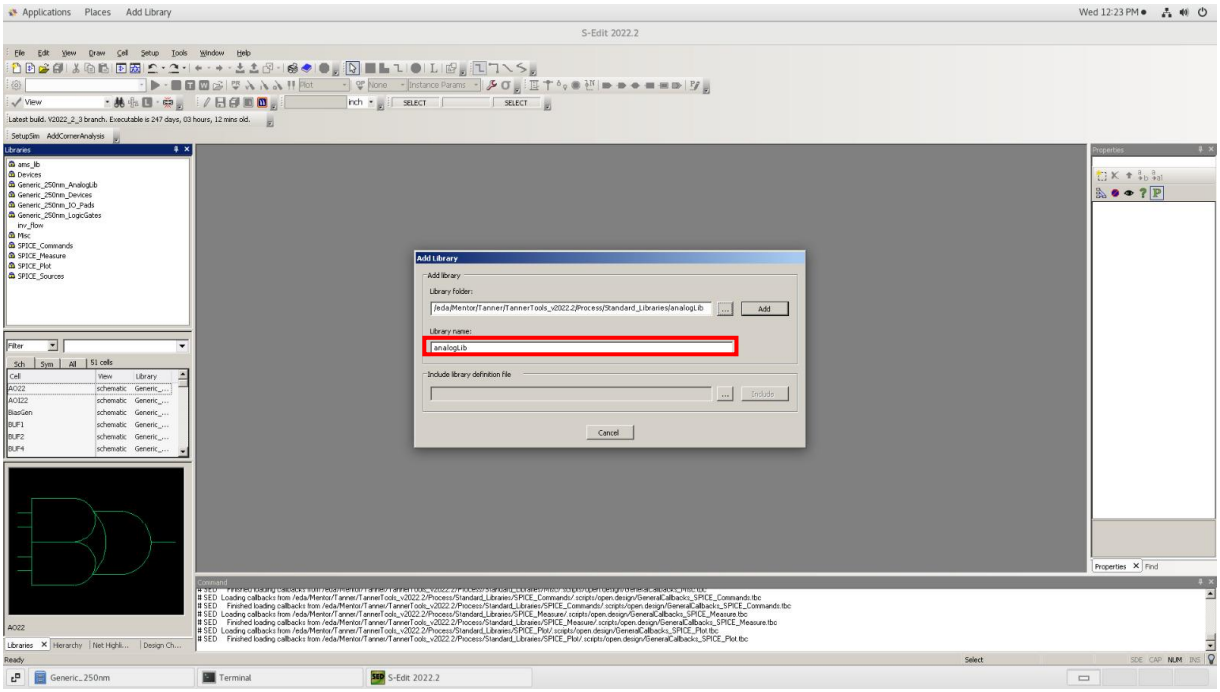
   Note: All Libraries used are from technology 2022.



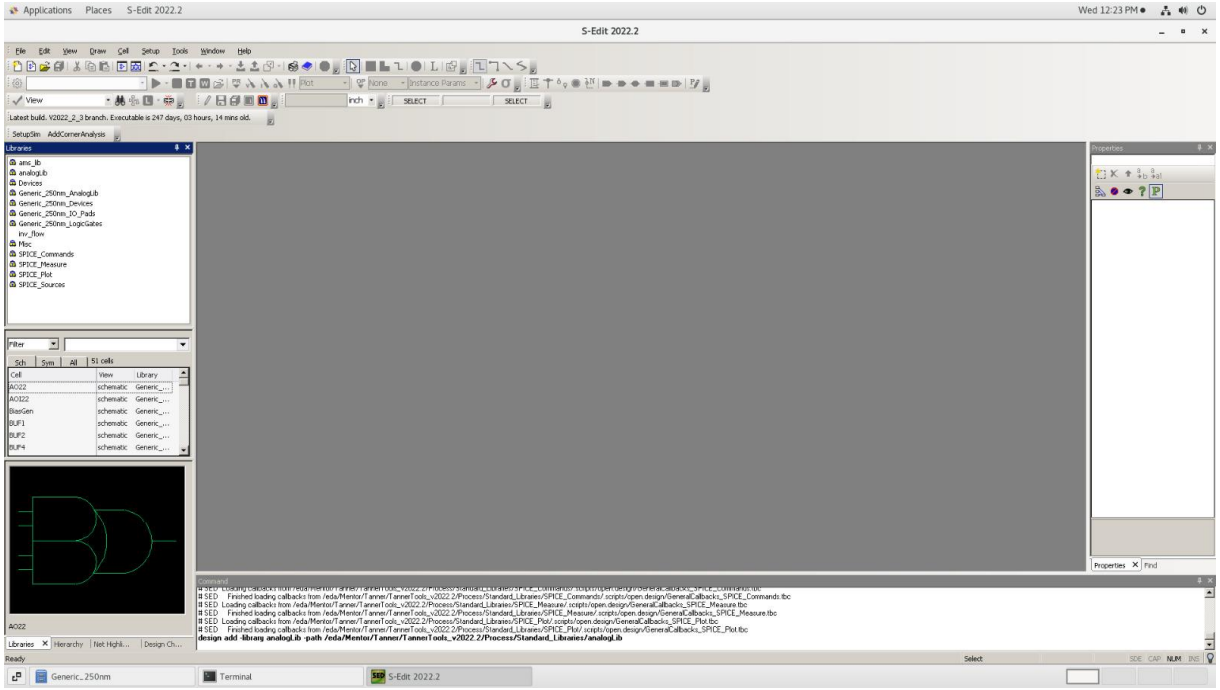
Include all libraries in one step ☺



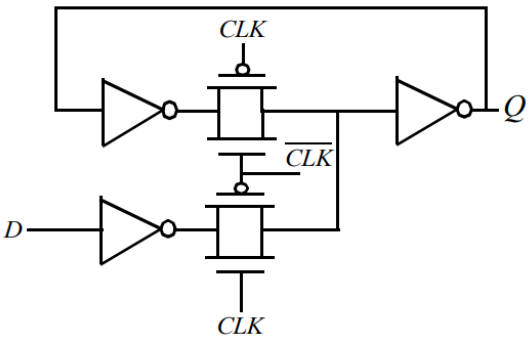
You also need to add **analog-lib** from standard libraries.



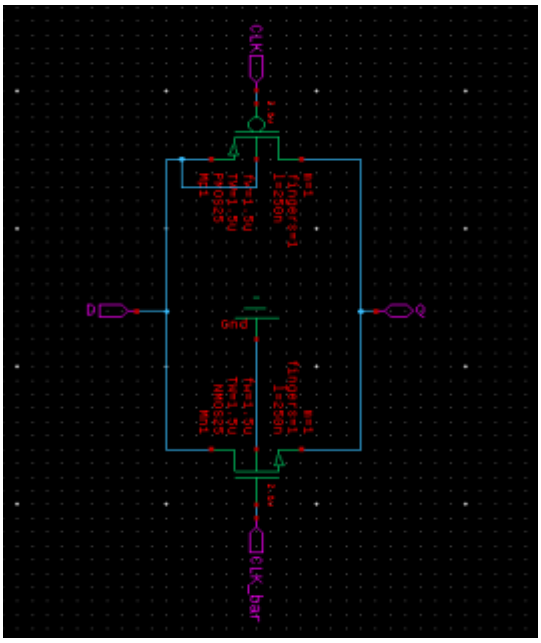
Now all done ☺



2. Design an Latch from scratch **(DON'T use generic gates)**

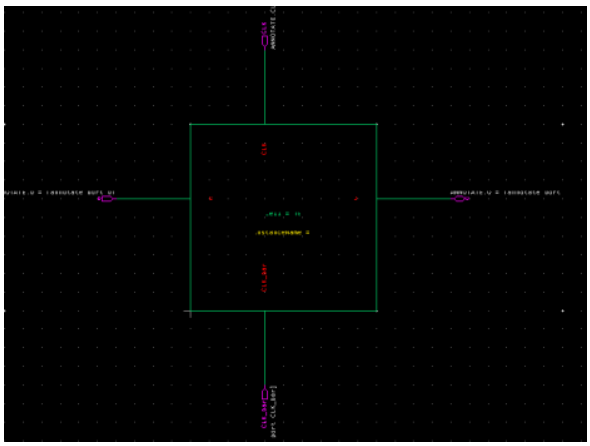


- **First**, you should design the transmission gate and create a symbol for it:

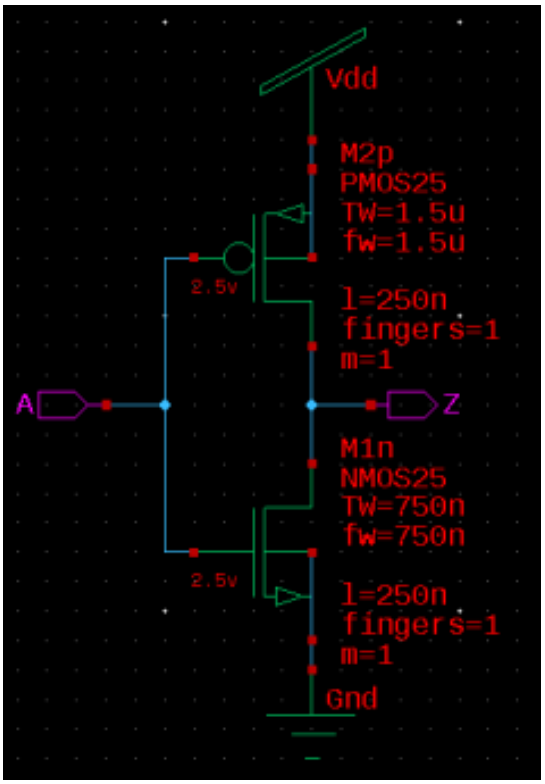


NOTE: Don't include global ports while generating symbol.

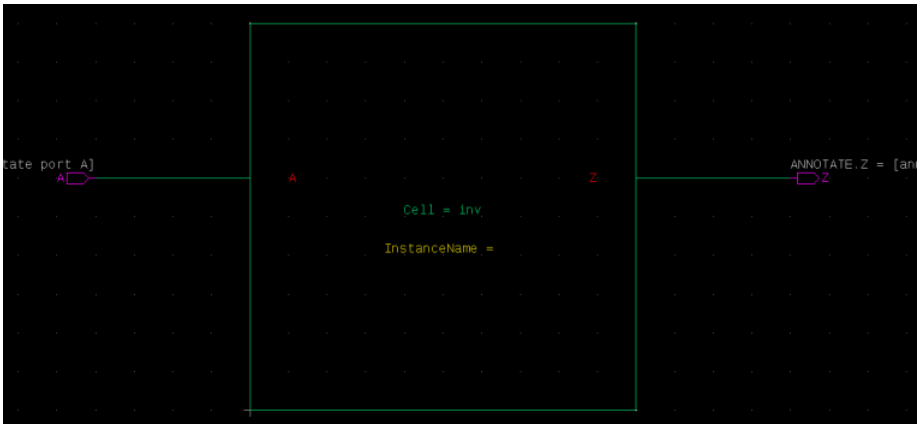
Hint: Use PMOS25x to connect bulk with source, on the other hand use NMOS25x but connect bulk to ground (to avoid errors in LVS because bulk pin by default connected to gnd in layout). **DON'T USE NMOS25 & PMOS25**.



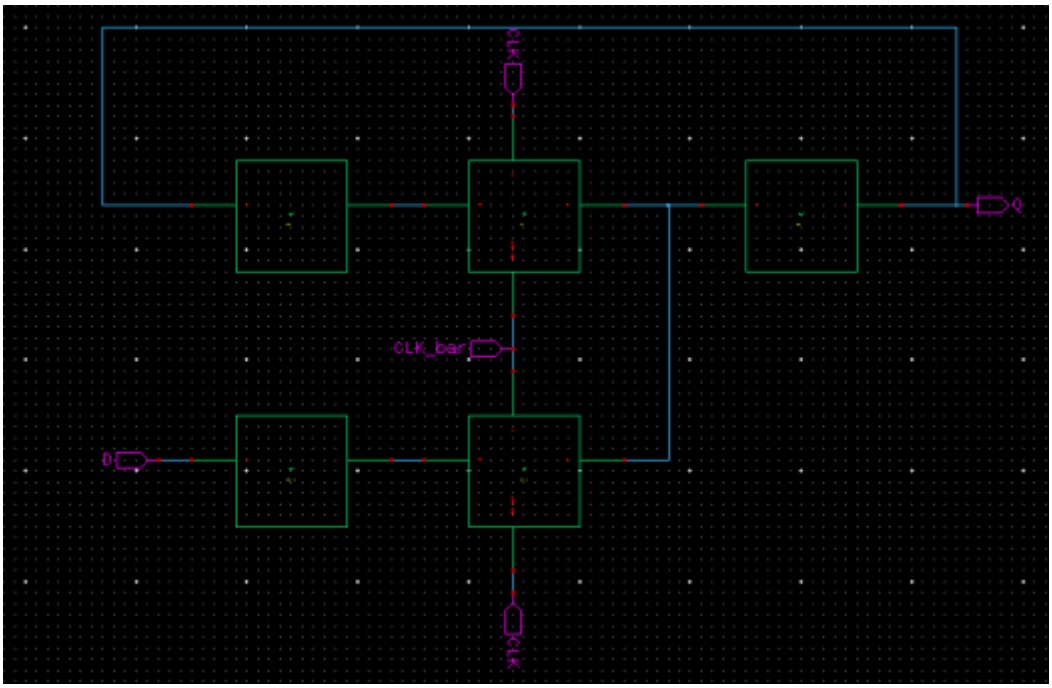
- **Second**, you should design the inverter from transistor level (or use the inverter from the previous lab) and create a symbol for it. (Avoid using generic gates)

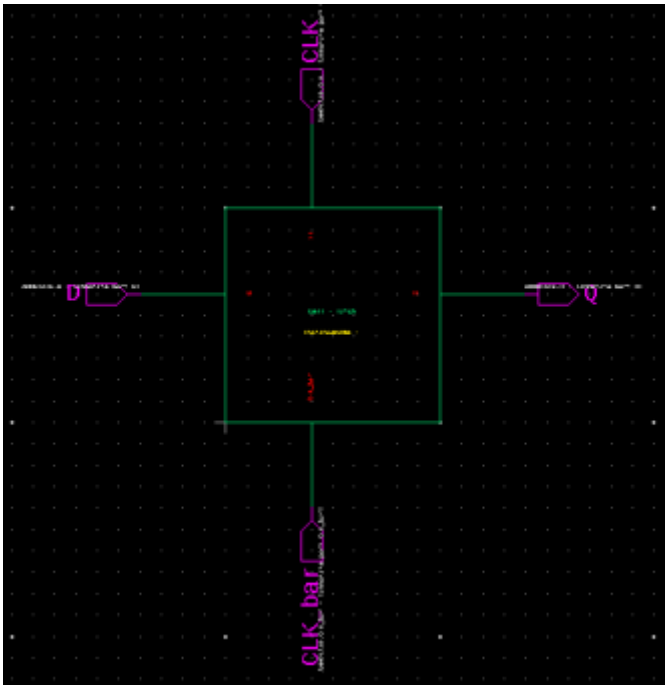


NOTE: Don’t include global ports while generating symbol.

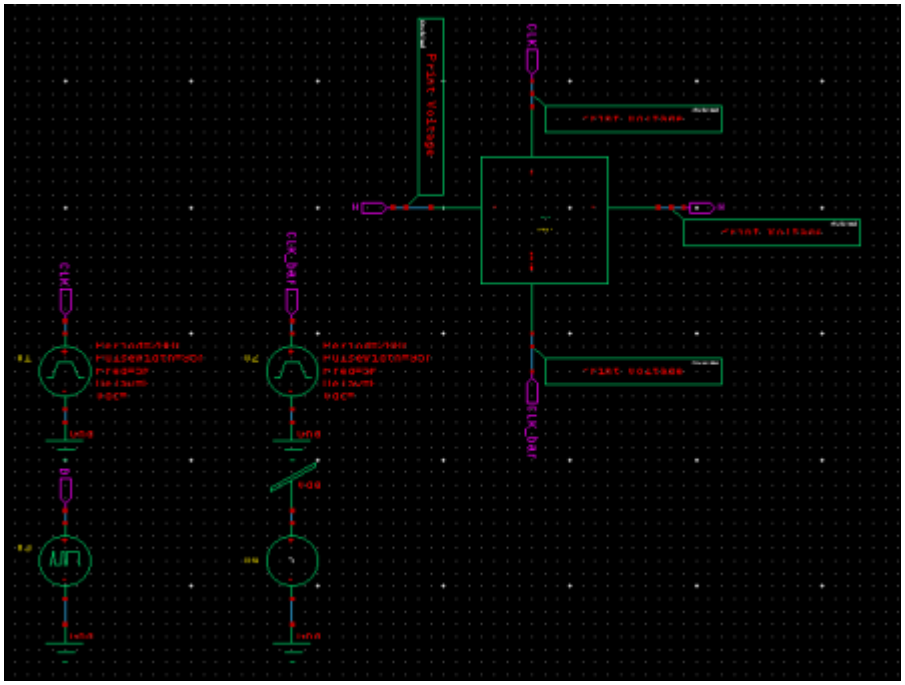


- **Finally**, use the TG and inverter symbol to build your latch and create a symbol for it:



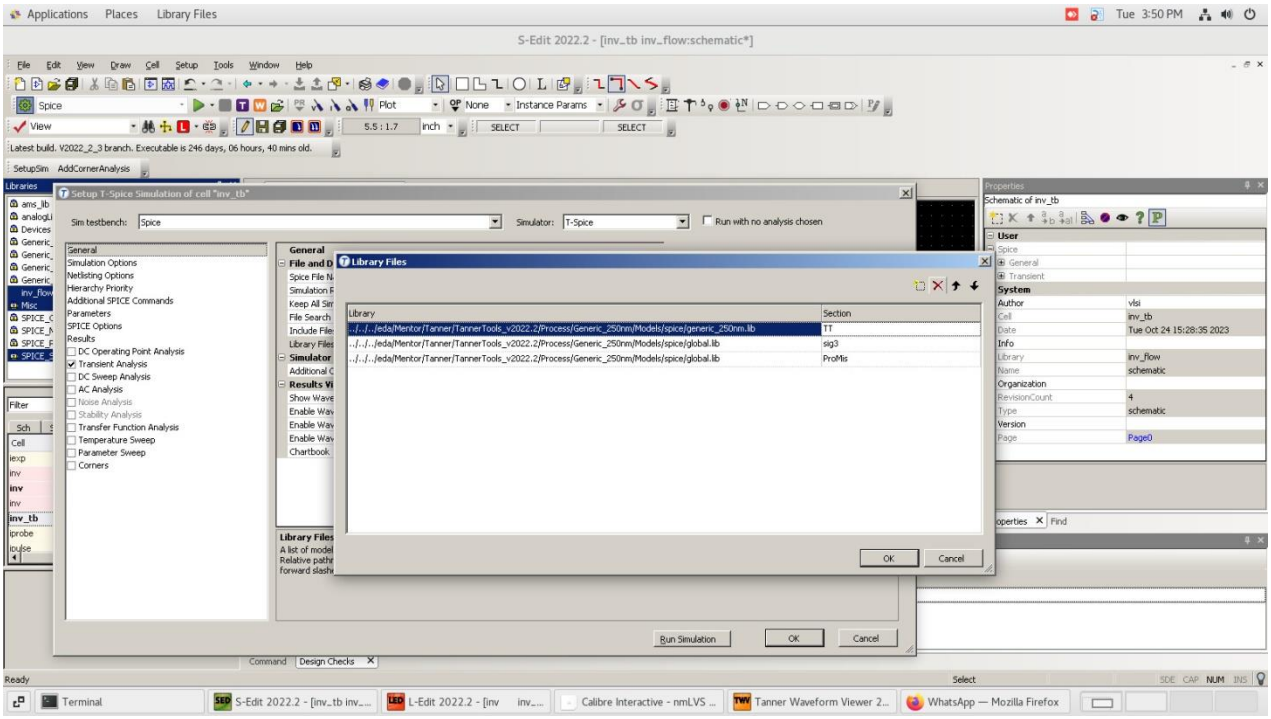


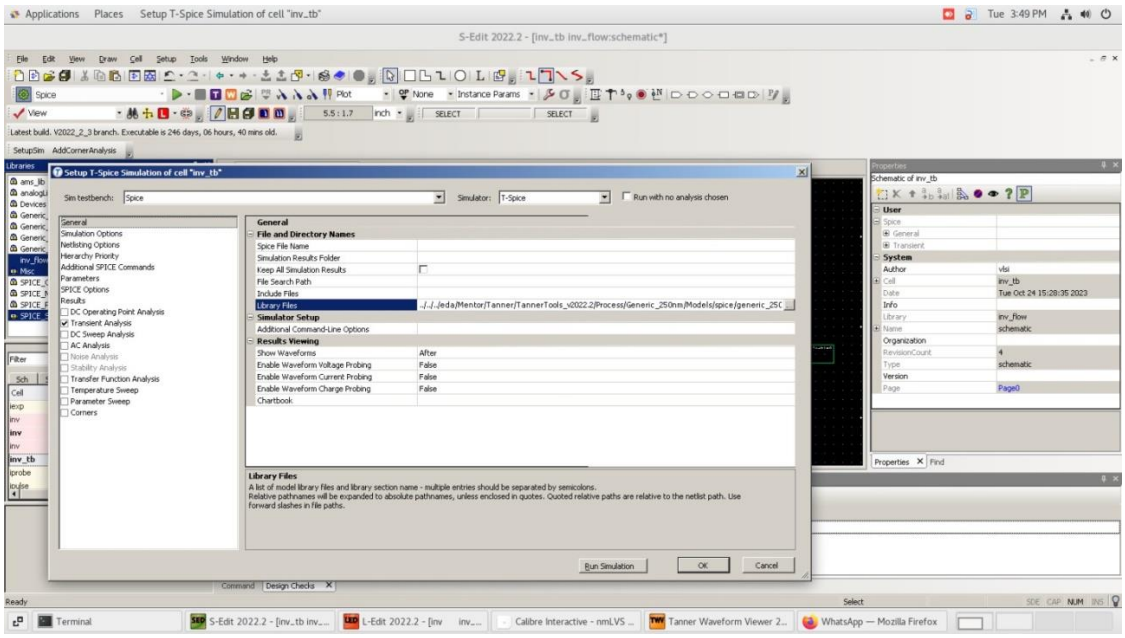
3. Test your design.

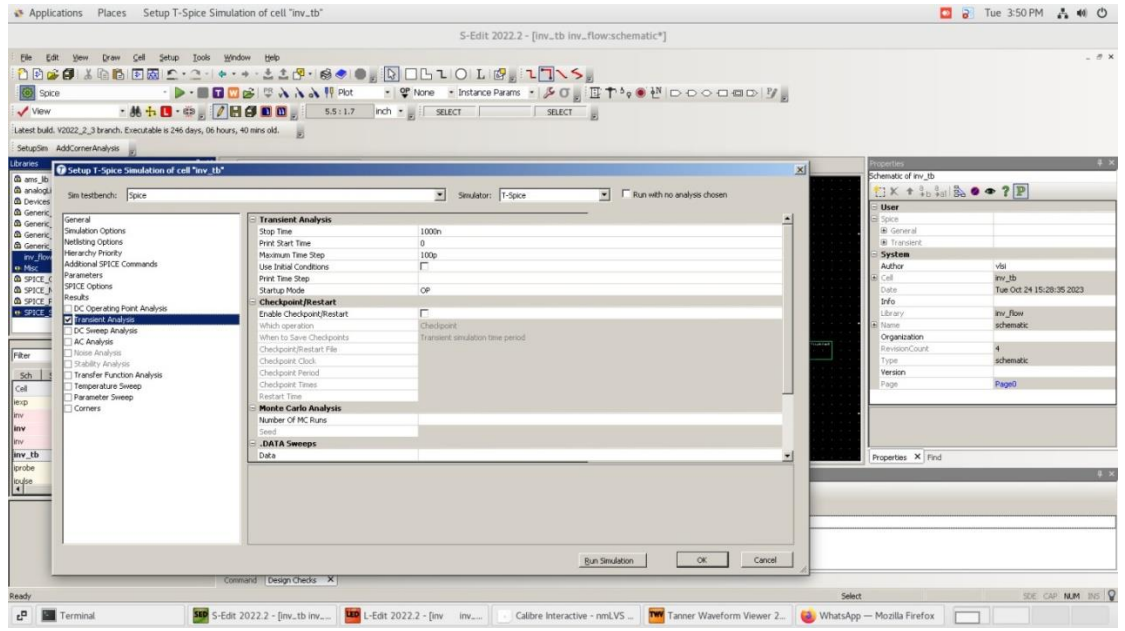


Hint: You can use Vpulse for CLK and CLK_bar, and Vbit for D. You can invert Vpulse polarity for for CLK & CLK_bar by **changing High and Low levels**.

4. Simulate




Applications Places Setup T-Spice Simulation of cell "inv_tb"
Tue 3:49 PM
S-Edit 2022.2 - [inv_tb inv_flow:schematic*]
Setup T-Spice Simulation of cell "inv_tb"
Sim testbench: Spice
Simulator: T-Spice
Run with no analysis chosen
General
Simulation Options
Netlisting Options
Hierarchy Priority
Additional SPICE Commands
Parameters
SPICE Options
Results
DC Operating Point Analysis
Transient Analysis
DC Sweep Analysis
AC Analysis
Noise Analysis
Stability Analysis
Transfer Function Analysis
Temperature Sweep
Parameter Sweep
Corners
File and Directory Names
Spice File Name
Simulation Results Folder
Keep All Simulation Results
File Search Path
Include Files
Library Files
Simulator Setup
Additional Command-Line Options
Results Viewing
Show Waveforms
Enable Waveform Voltage Probing
Enable Waveform Current Probing
Enable Waveform Charge Probing
Chartbook
Library Files
A list of model library files and library section name - multiple entries should be separated by semicolons.
Relative pathnames will be expanded to absolute pathnames, unless enclosed in quotes. Quoted relative paths are relative to the netlist path. Use forward slashes in file paths.
Run Simulation
OK
Cancel
Terminal
S-Edit 2022.2 - [inv_tb inv_...
L-Edit 2022.2 - [inv
Calibre Interactive - nmLVS ...
Tanner Waveform Viewer 2...
WhatsApp — Mozilla Firefox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Tue 3:50 PM
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Sim testbench: Spice
Simulator: T-Spice
Run with no analysis chosen
Transient Analysis
Stop Time
1000n
Print Start Time
0
Maximum Time Step
100p
Use Initial Conditions
Print Time Step
Startup Mode
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Checkpoint/Restart
Enable Checkpoint/Restart
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Number Of MC Runs
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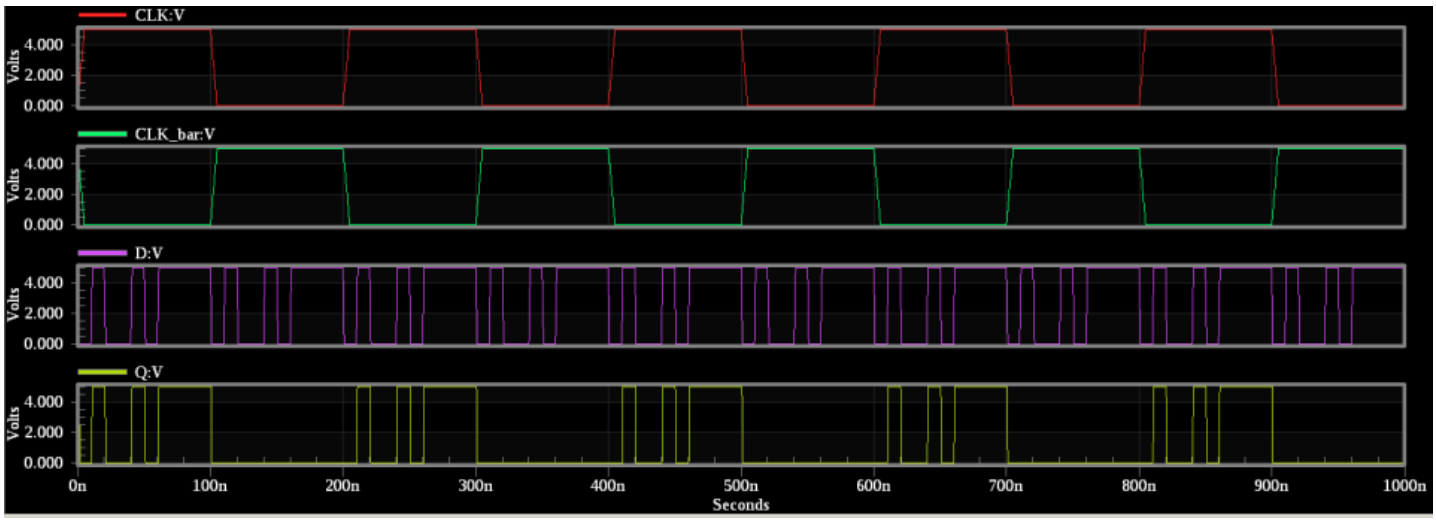
Data
Run Simulation
OK
Cancel
Terminal
S-Edit 2022.2 - [inv_tb inv_...
L-Edit 2022.2 - [inv
Calibre Interactive - nmLVS ...
Tanner Waveform Viewer 2...
WhatsApp — Mozilla Firefox

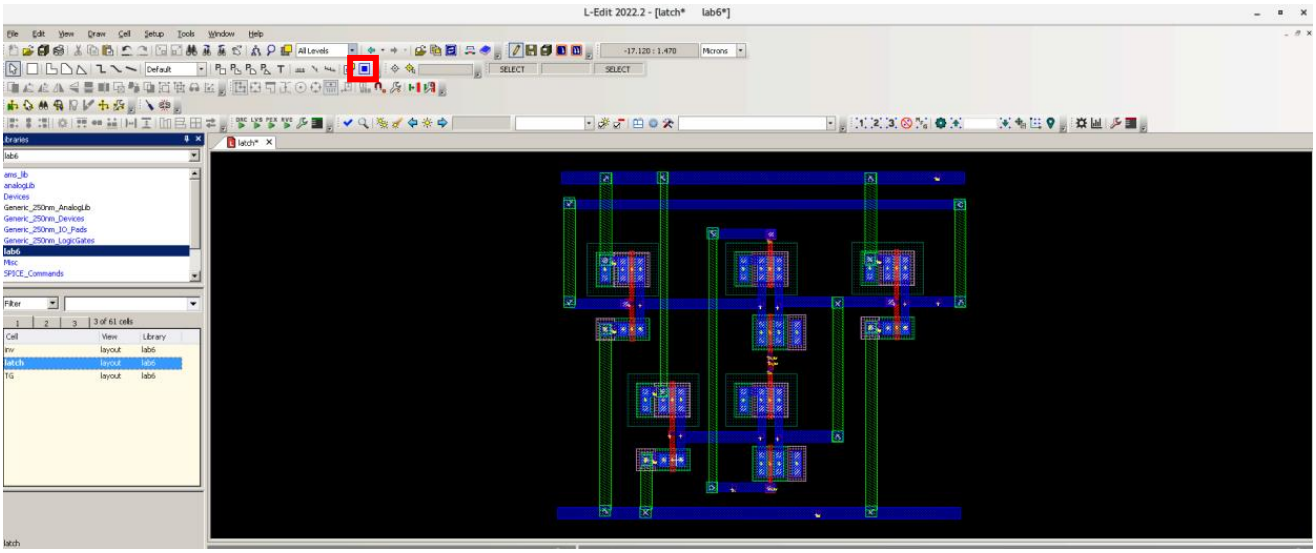

CLK:V
CLK_bar:V
D:V
Q:V
Volts
4.000
2.000
0.000
0n
100n
200n
300n
400n
500n
600n
700n
800n
900n
1000n
Seconds

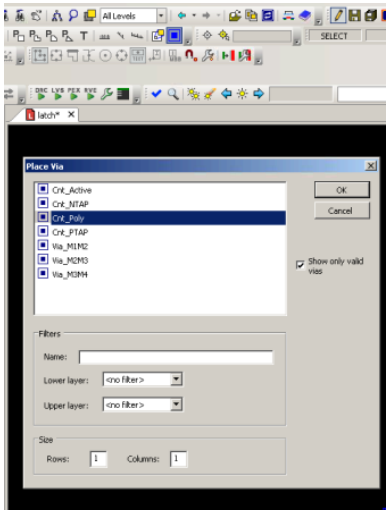
Backend Flow

After Finishing your Schematic, now it is time to setup your Layout. The next step is to publish to **SDL** (schematic driven layout).

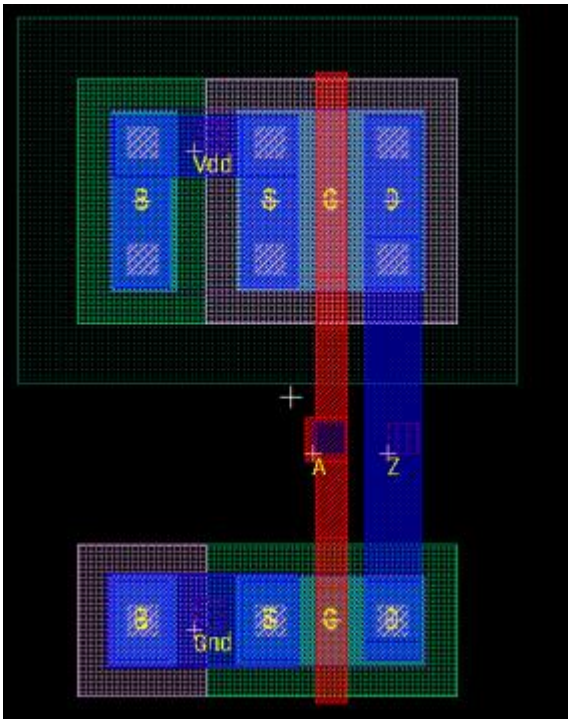
Important Note for Routing:

- Manhattan routing is a **routing strategy**. You use **one dedicated layer for horizontal tracks** and **another layer for vertical tracks**. No horizontal tracks are allowed on the vertical layer, and no vertical traces are used on the horizontal layer. **Here assume that all Horizontal connections are metal 1 and all Vertical connections are metal 2.**
- To connect metal 1 with metal 2 you will need via **Via_M1M2**.
- To connect poly with metal 1 you will need via **Cnt_poly.**
- To connect poly with metal 2 you will need two vias **Cnt_poly & Via_M1M2**.





1. Generate a layout for inverter and route it:

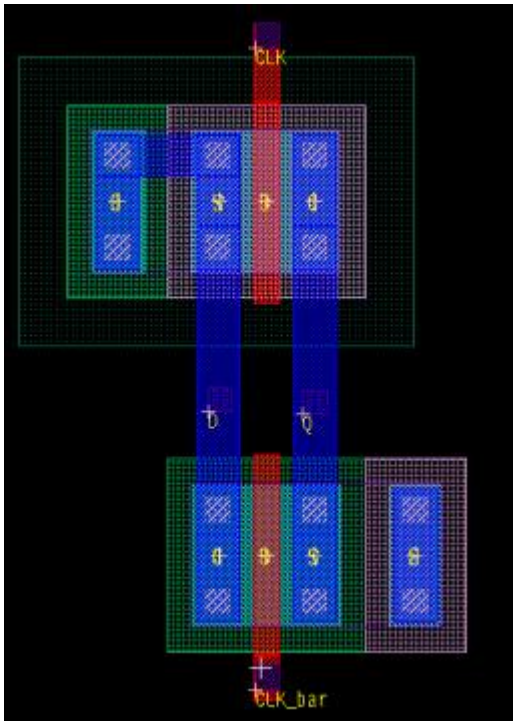


Routing Hints:

- Connect PMOS gate with NMOS gate using poly.
- Connect PMOS Drain with NMOS Drain using metal 1.
- Connect PMOS Source and Bulk with Vdd using metal 1.
- Connect NMOS Source and Bulk with Gnd using metal 1.
- Convert **Z, Vdd and Gnd** pins to **metal 1 pin** **(Ctrl + E)** and put them over metal 1.
- Convert **A** pin to **poly pin** **(Ctrl + E)** and put it over poly.

Don’t forget to run DRC & LVS to validate your inverter ☺

2. Generate a layout for Transmission gate and route it:

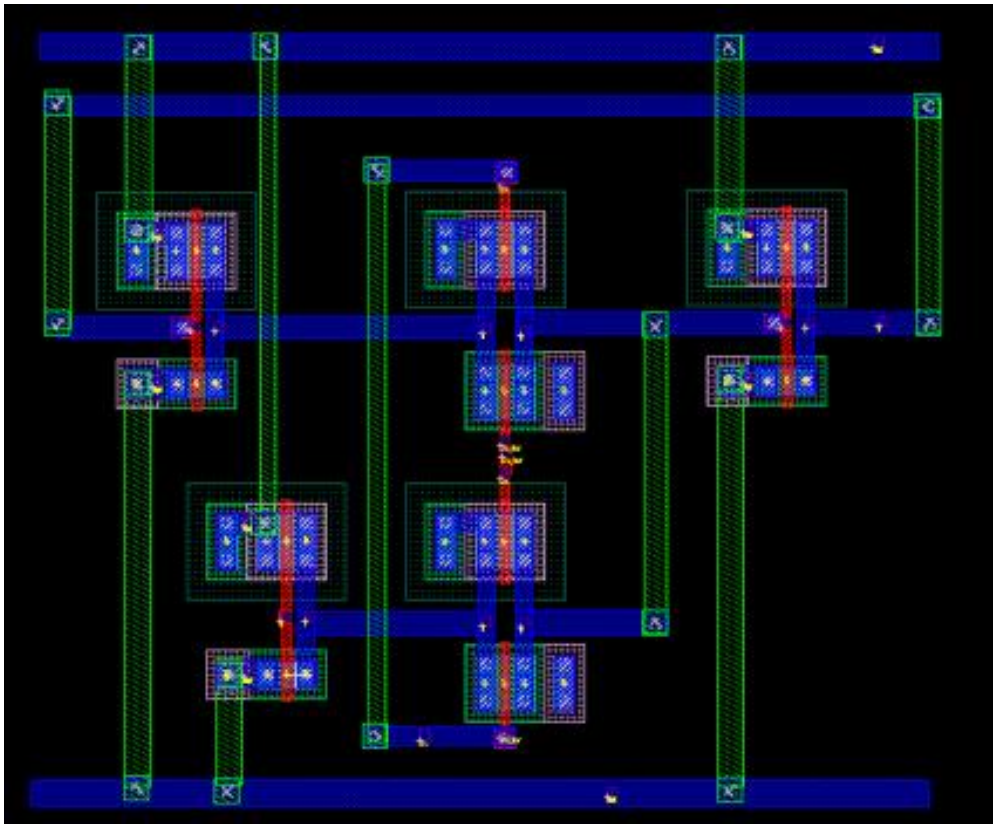


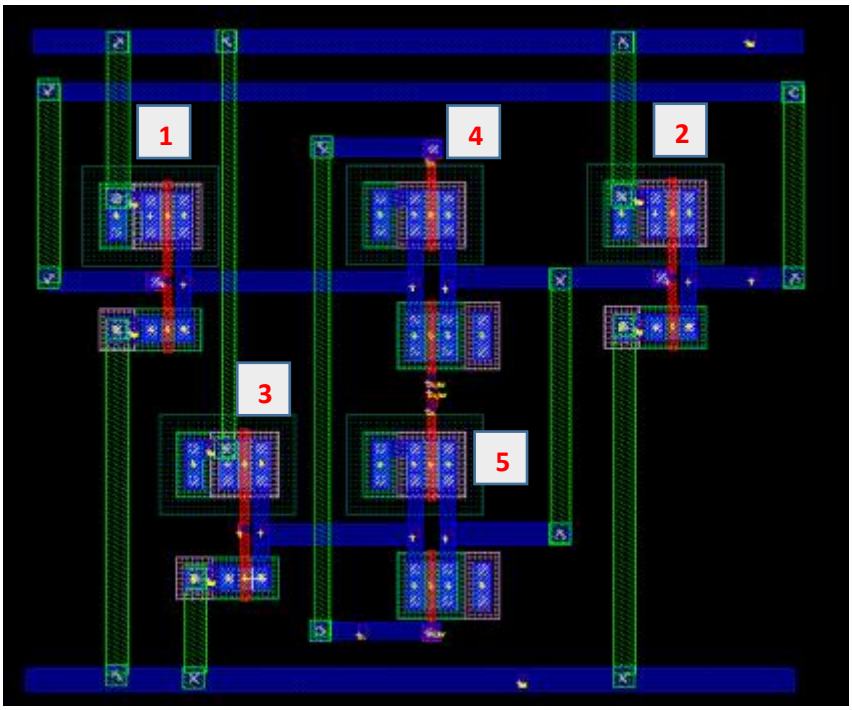
Routing Hints:

- Connect PMOS Source with NMOS Drain using metal 1.
- Connect PMOS Drain with NMOS Source using metal 1.
- Connect PMOS Source and Bulk using metal 1.
- Don't connect NMOS Source and Bulk with Gnd (fatal mistake because bulk grounded by default so it will ground source also).
- Convert **Q and D** pins to **metal 1 pin (Ctrl + E)** and put them over metal 1.
- Convert **Clk and Clk_bar** pin to **poly pin (Ctrl + E)** and extend some poly to put over it.

Don't forget to run DRC & LVS to validate your Transmission gate ☺

3. Generate a layout for all latch now and route it:



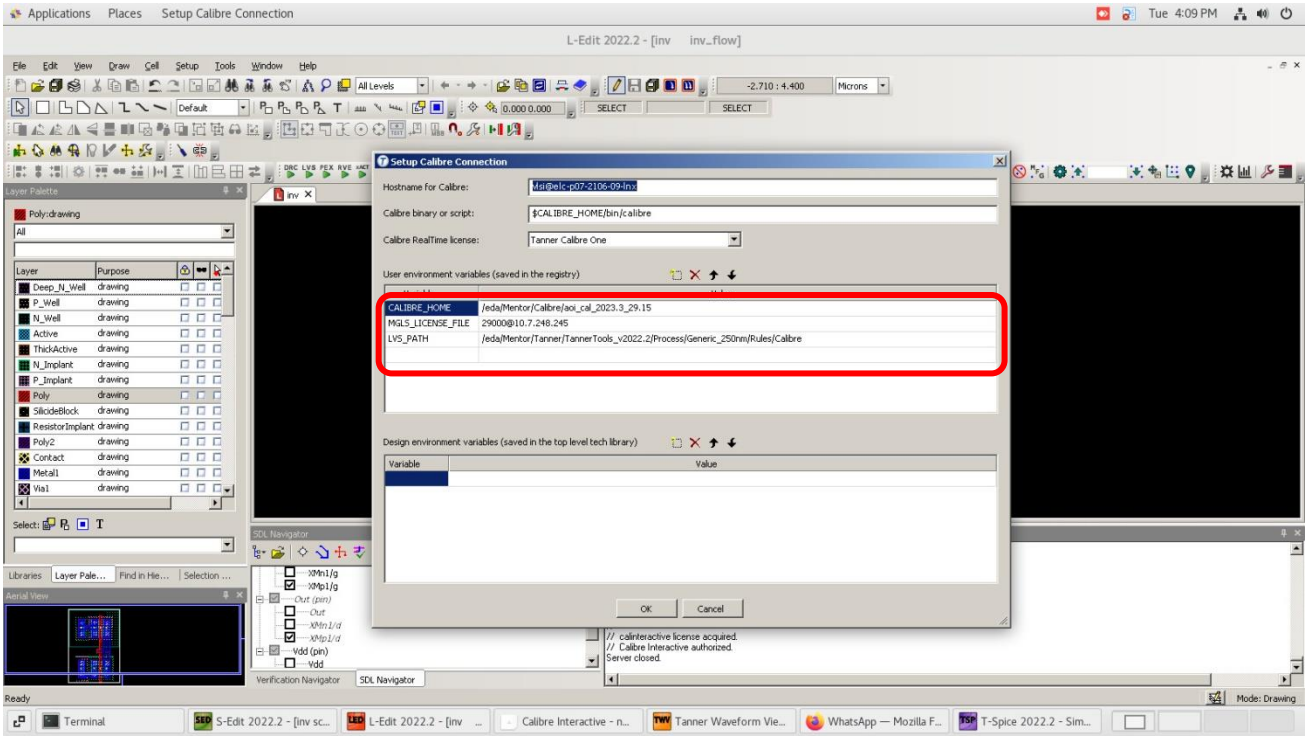


Routing Hints:

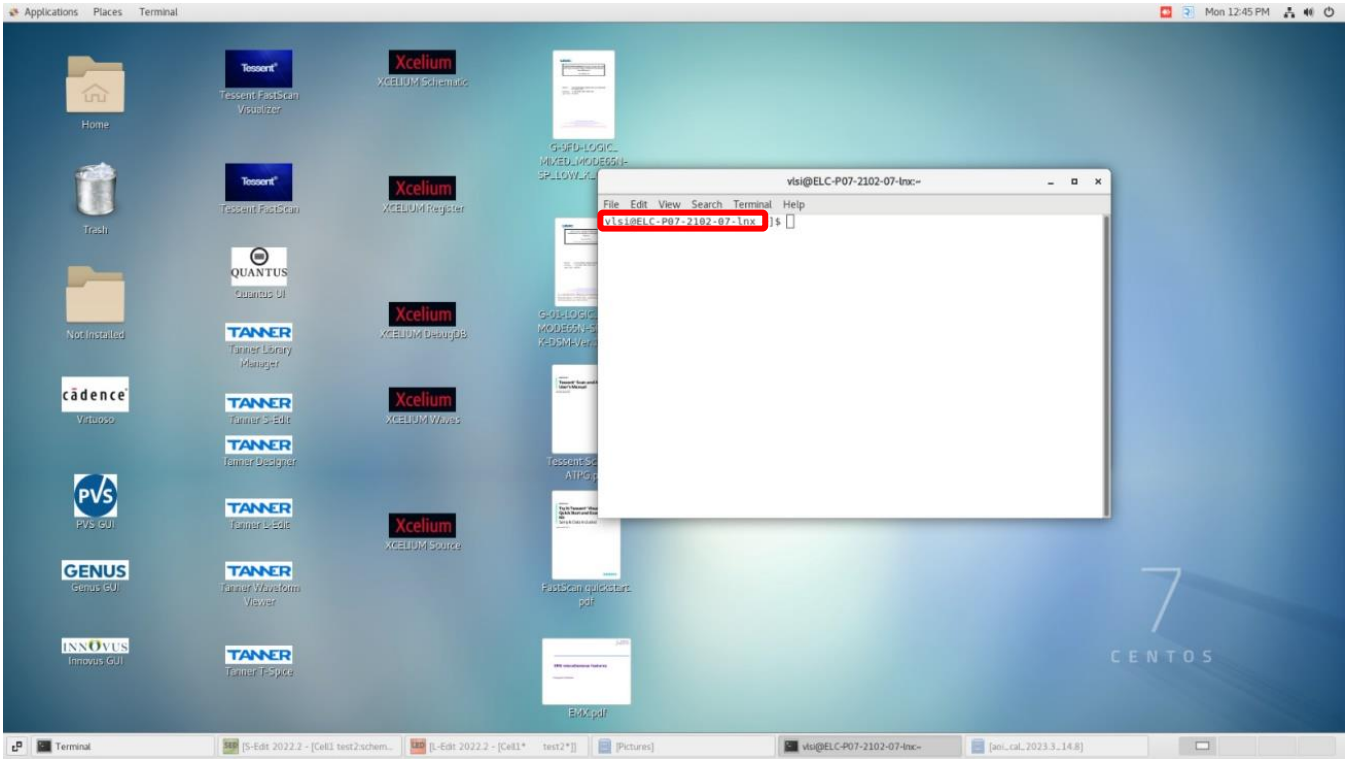
- Connect output of inverter 1 to input of Transmission gate 4.
- Connect output of Transmission gate 4 to input of inverter 2.
- Connect output of inverter 3 to input of Transmission gate 5.
- Connect output of Transmission gate 5 to output of Transmission gate 4.
- Connect Clk_bar pin of Transmission gate 4 to Clk pin of Transmission gate 5 (using poly) and connect both of them to latch Clk_bar pin after converting it to **poly pin (Ctrl + E).**
- Connect Clk pin of Transmission gate 4 to Clk_bar pin of Transmission gate 5 (using metal 1 & metal 2) and connect both of them to latch Clk_bar pin after converting it to **metal 1 pin (Ctrl + E).**
- Connect output of inverter 2 to input of inverter 1.
- Common Vdd for all inverters PMOS.
- Common Gnd for all inverters NMOS.

Calibre Setup

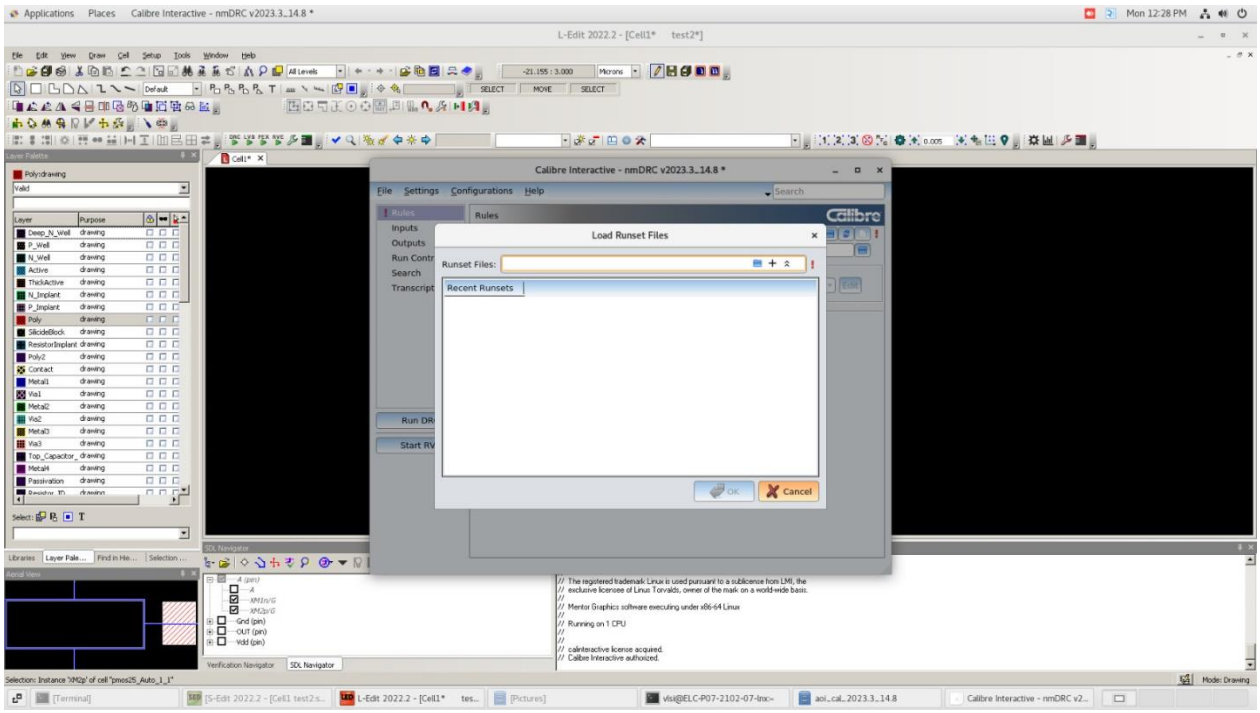
Setup Calibre connection **VERY IMPORTANT STEP**:



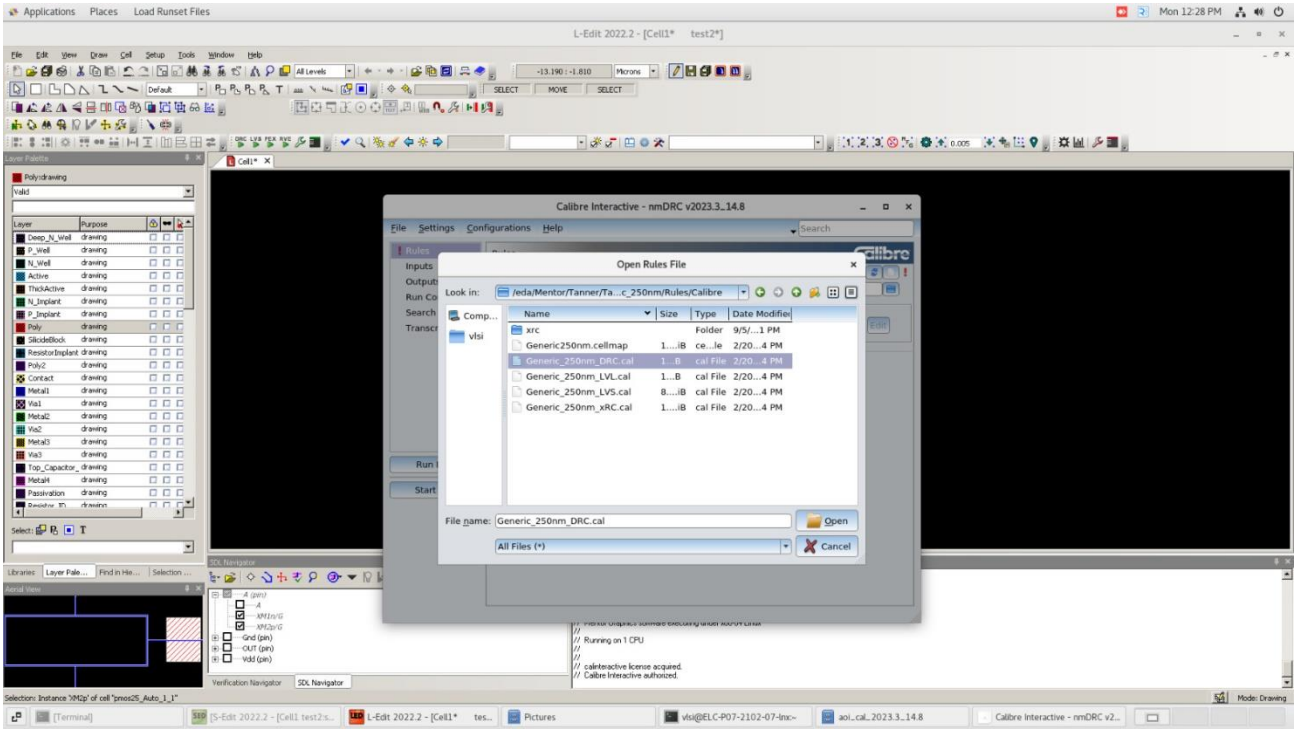
- Note: write **MGLS_LISENCE_FILE** instead of **MGLS_LICENSE_FILE.**
- Note: you can find Hostname for Calibre from your tanner location just open it in the terminal of the device.



DRC Setup

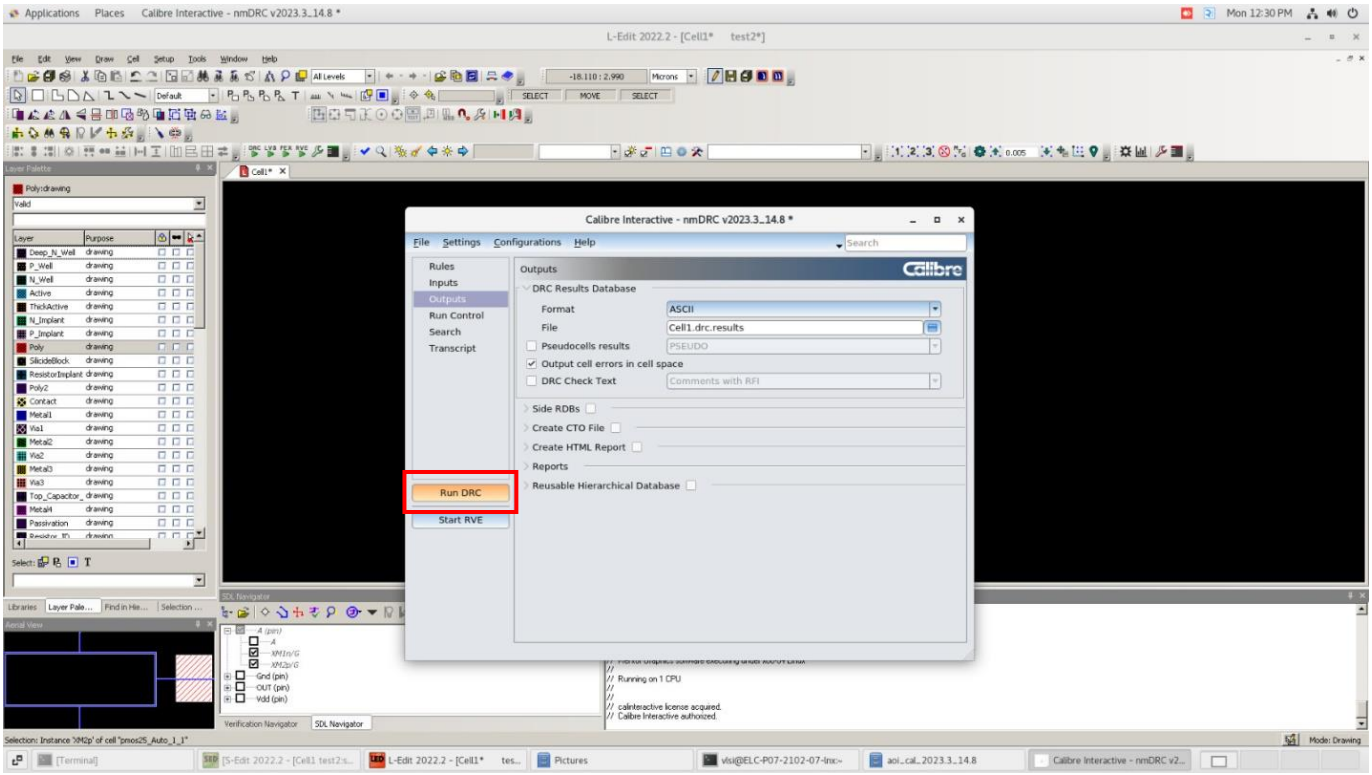


Cancel the first window appears.



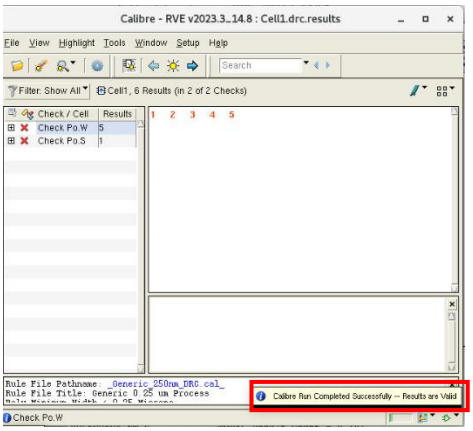
Add DRC library from Process file.
"/eda/Mentor/Tanner/TannerTools_v2022.2/Process/Generic_250nm/Rules/Calibre/Generic_250nm_DRC.cal"

Use default setting ……



Run DRC

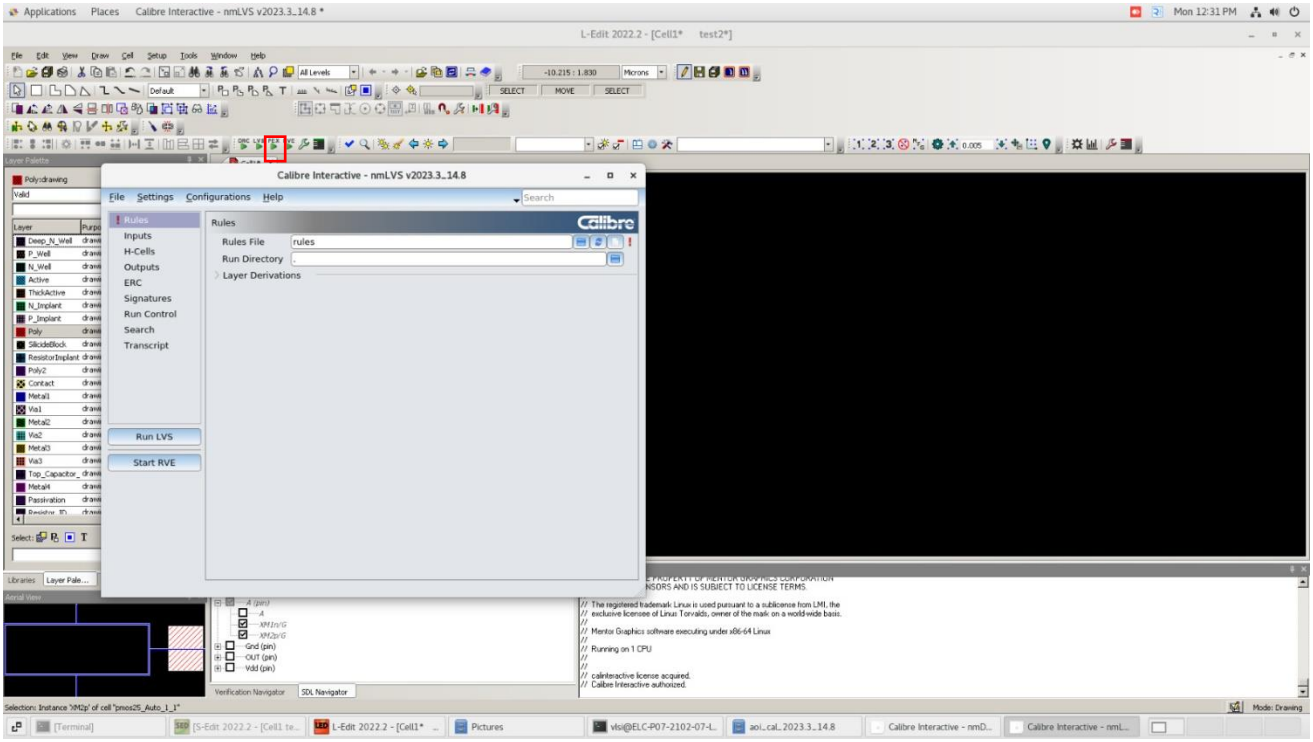
Result view (RVE) window will open



Fix all errors & **DRC** is Done Now ☺

LVS SETUP

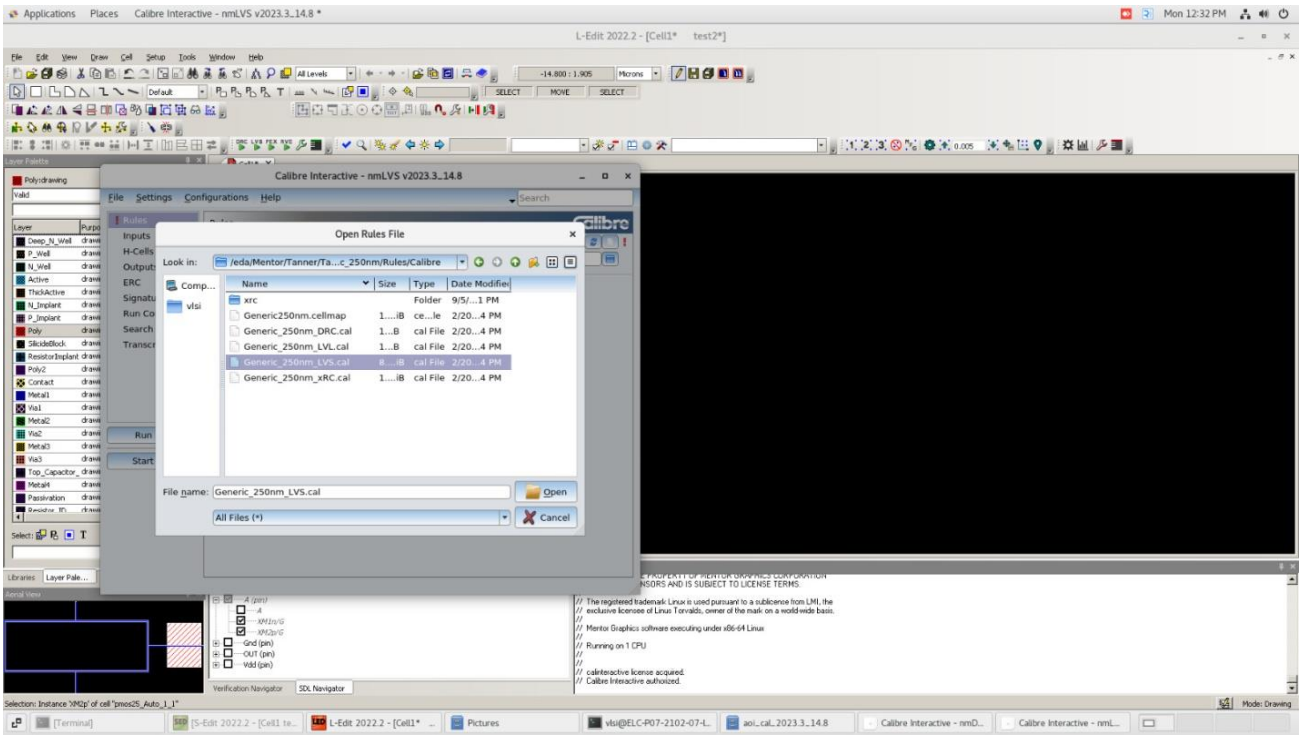
Run LVS

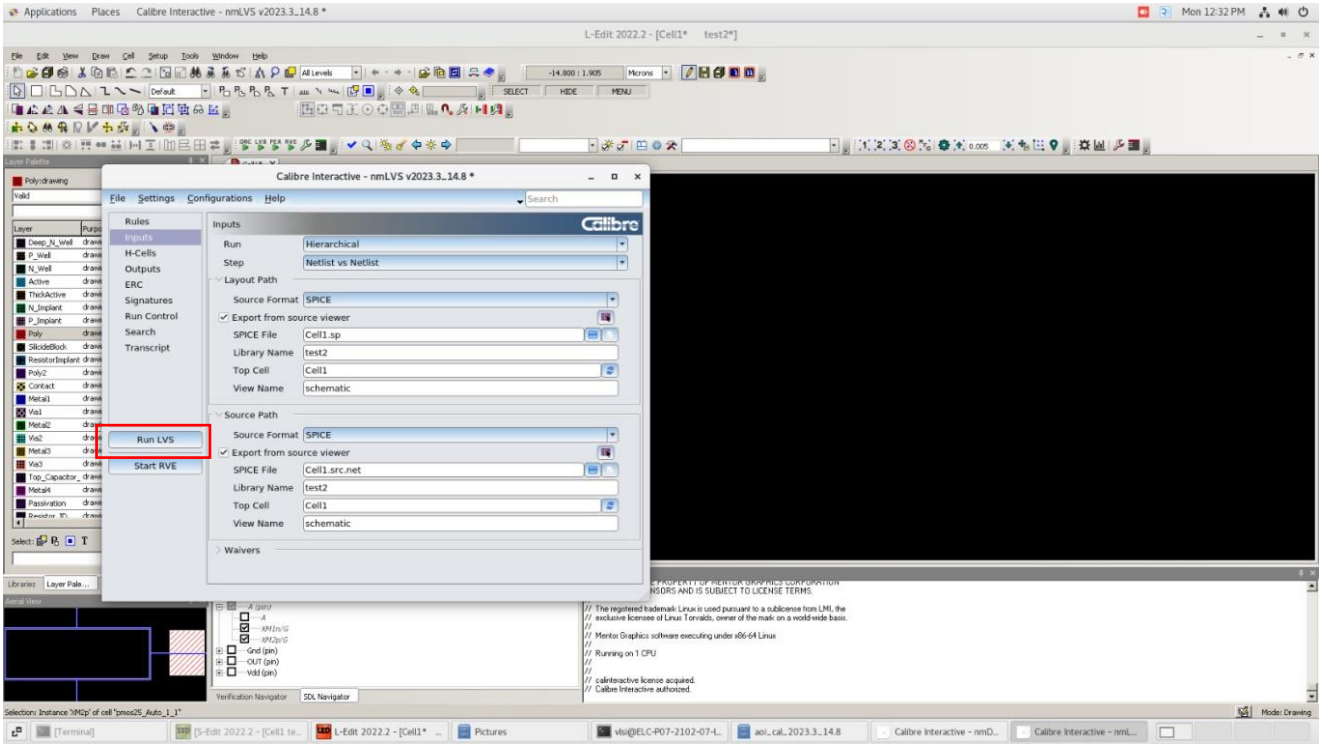


Cancel the first window appears.

Then add LVS library from Process file:

"/eda/Mentor/Tanner/TannerTools_v2022.2/Process/Generic_250nm/Rules/Calibre/Generic_250nm_LVS.cal"





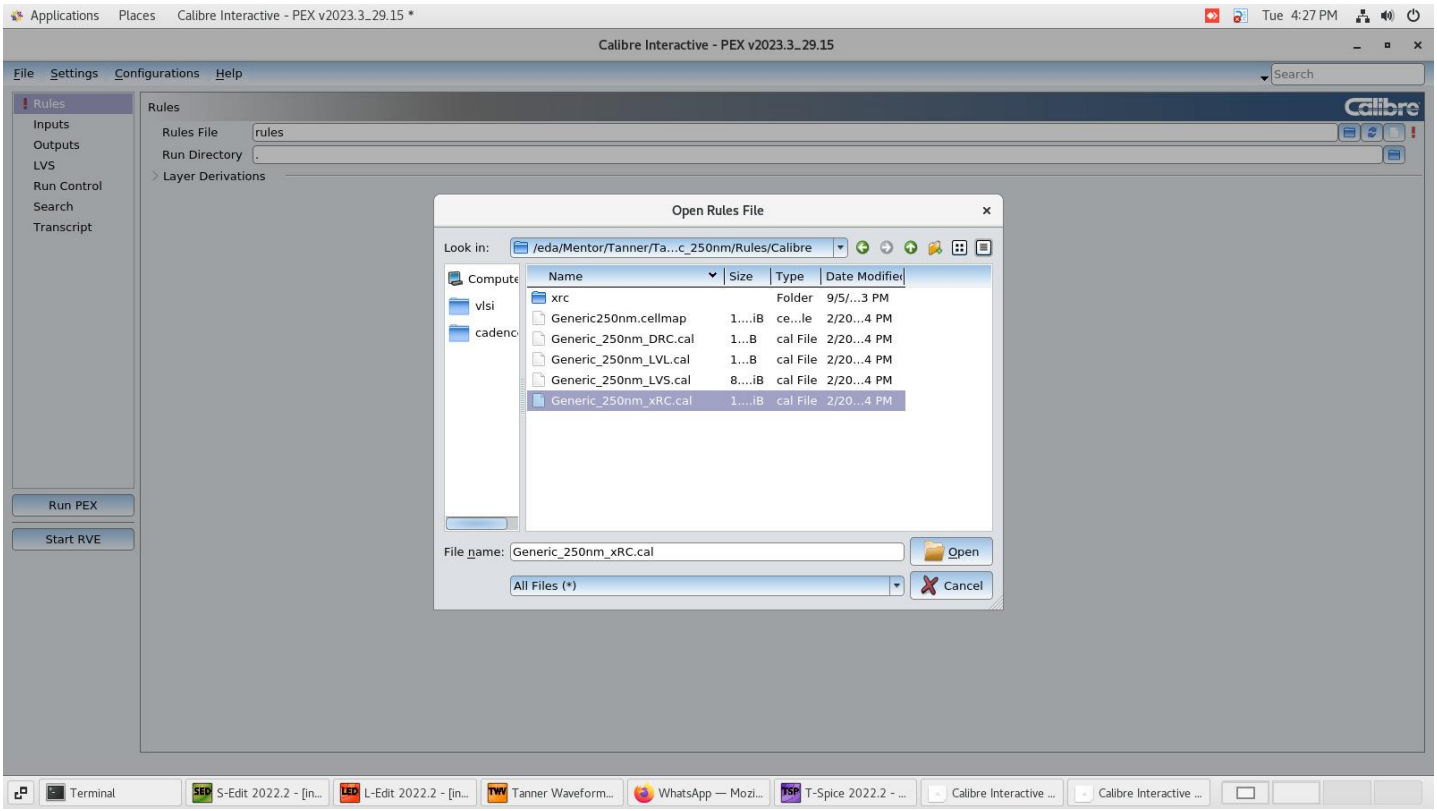
Run LVS

Fix all errors & LVS is Done Now ☺

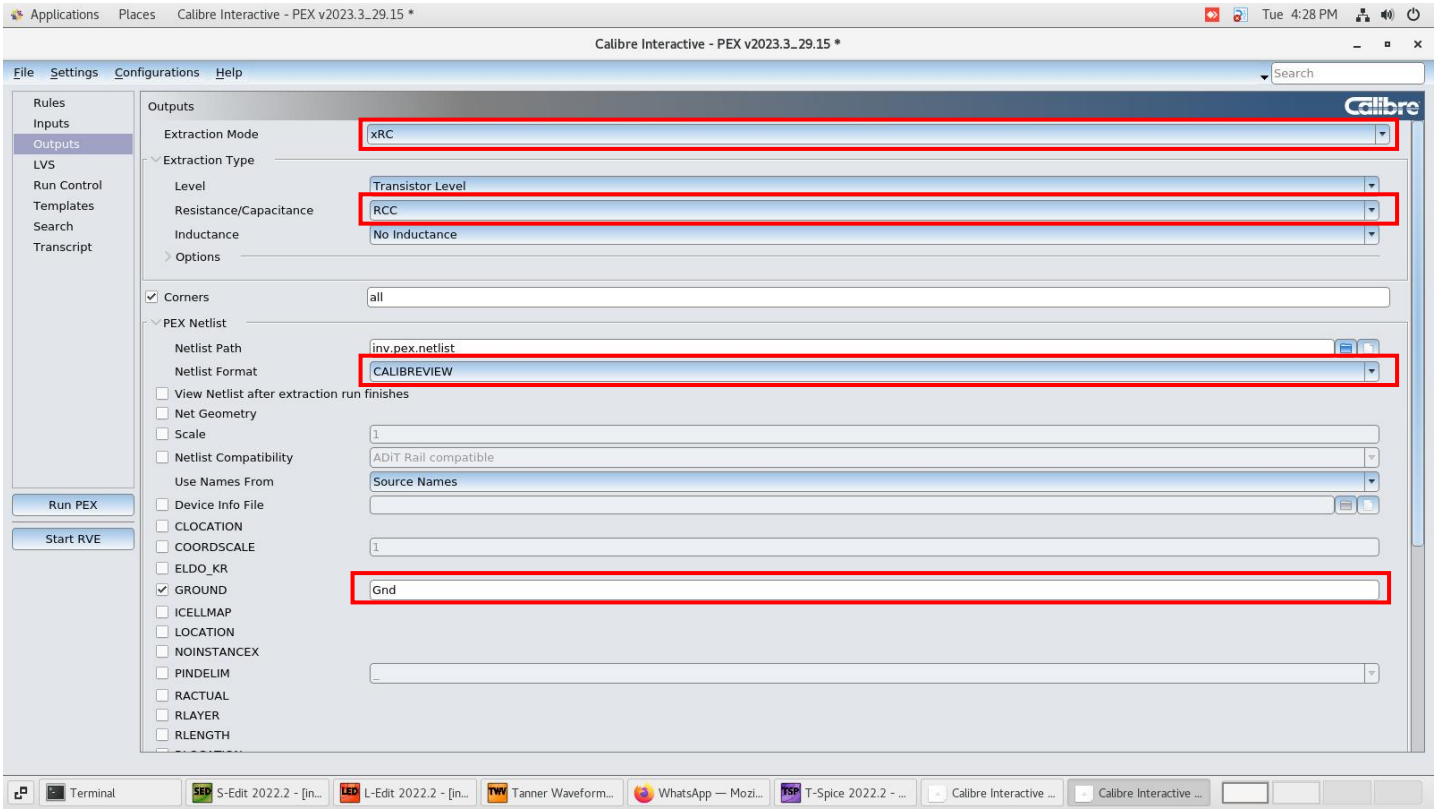
Extraction SETUP

Run **PEX**

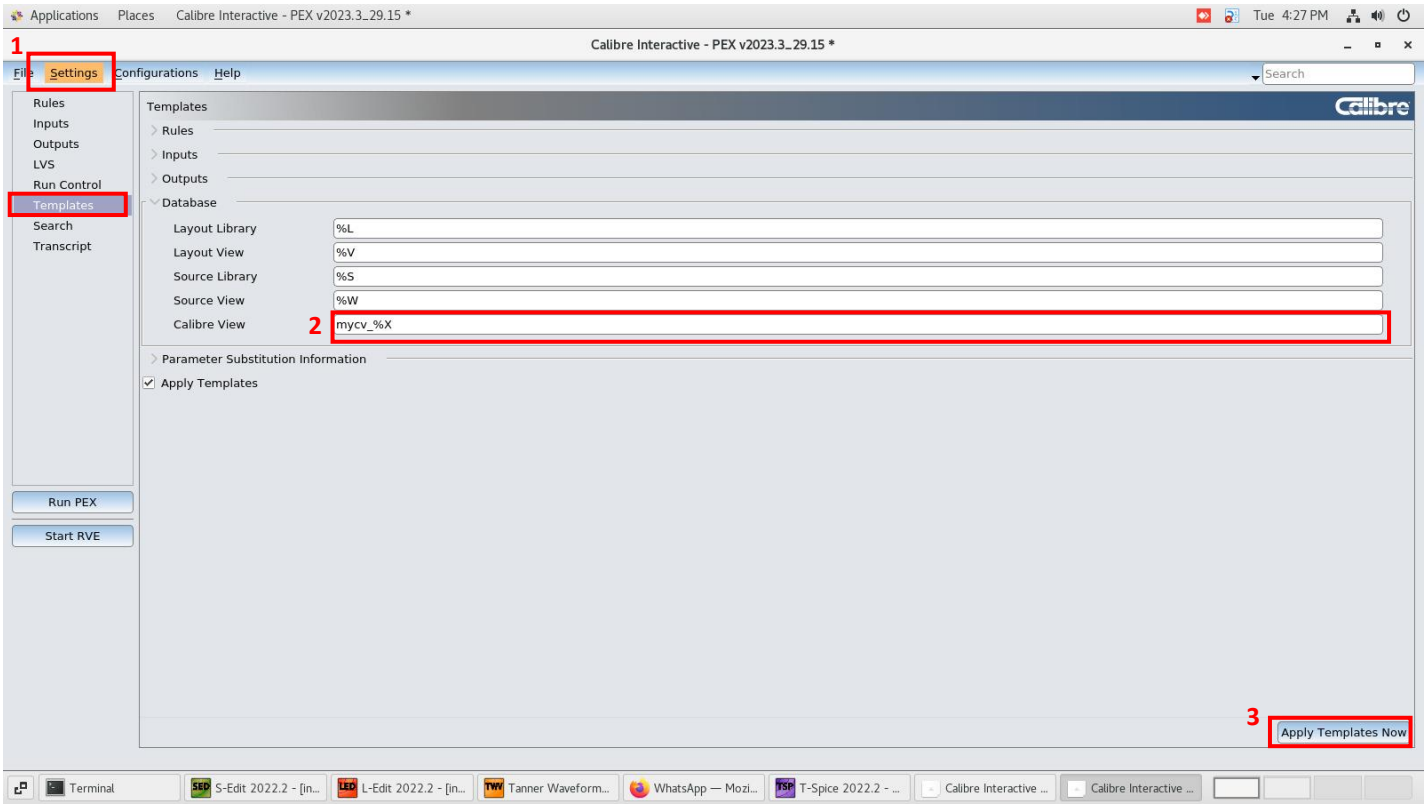
Cancel the first window appears.

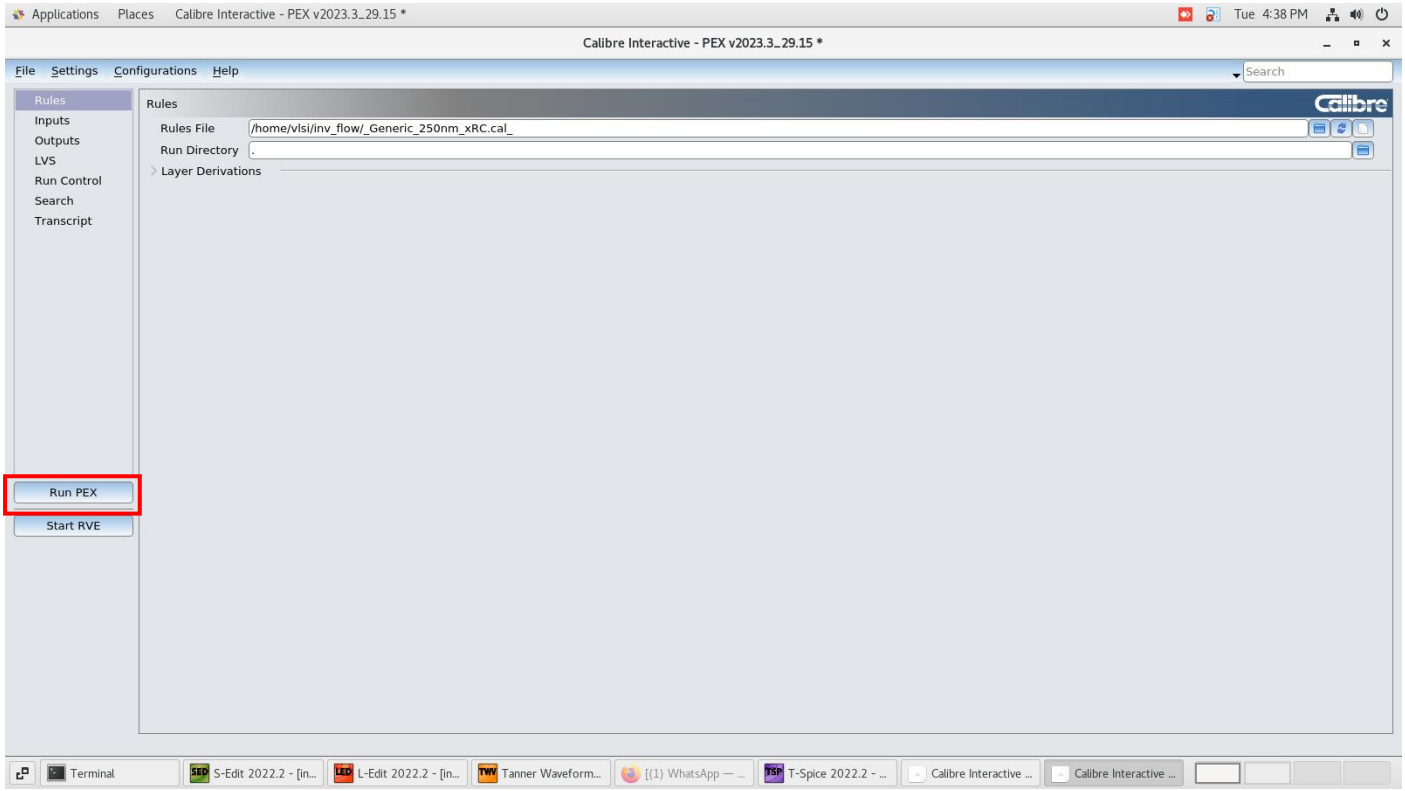


Then add PEX library from Process file.
"/eda/Mentor/Tanner/TannerTools_v2022.2/Process/Generic_250nm/Rules/Calibre/Generic_250nm_xRC.cal"



If Templates not appears show it from setting >> show pages

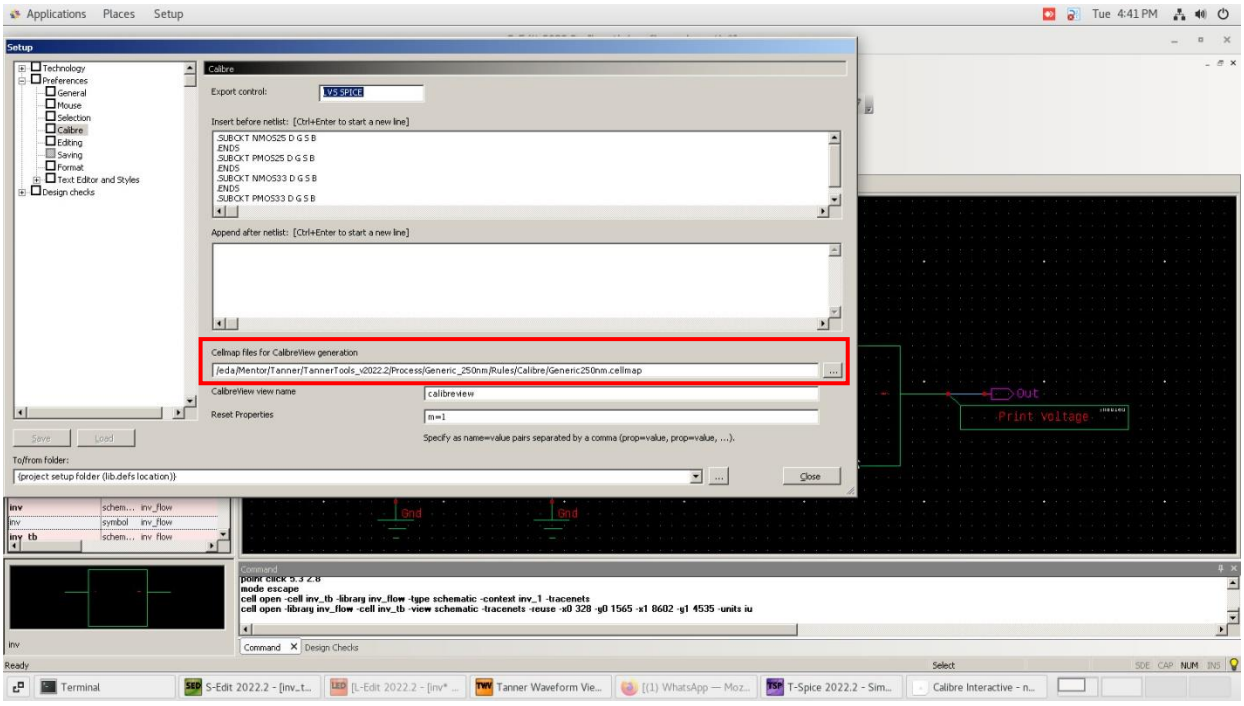



Applications
Places
Calibre Interactive - PEX v2023.3_29.15 *
Tue 4:38 PM
Calibre Interactive - PEX v2023.3_29.15 *
File
Settings
Configurations
Help
Search
Rules
Inputs
Outputs
LVS
Run Control
Search
Transcript
Rules
Calibre
Rules File
/home/vlsi/inv_flow/_Generic_250nm_xRC.cal_
Run Directory
.
Layer Derivations
Run PEX
Start RVE
Terminal
S-Edit 2022.2 - [in...
L-Edit 2022.2 - [in...
Tanner Waveform...
(1) WhatsApp — ...
T-Spice 2022.2 - ...
Calibre Interactive ...
Calibre Interactive ...

Post Layout Simulation

Open S-edit

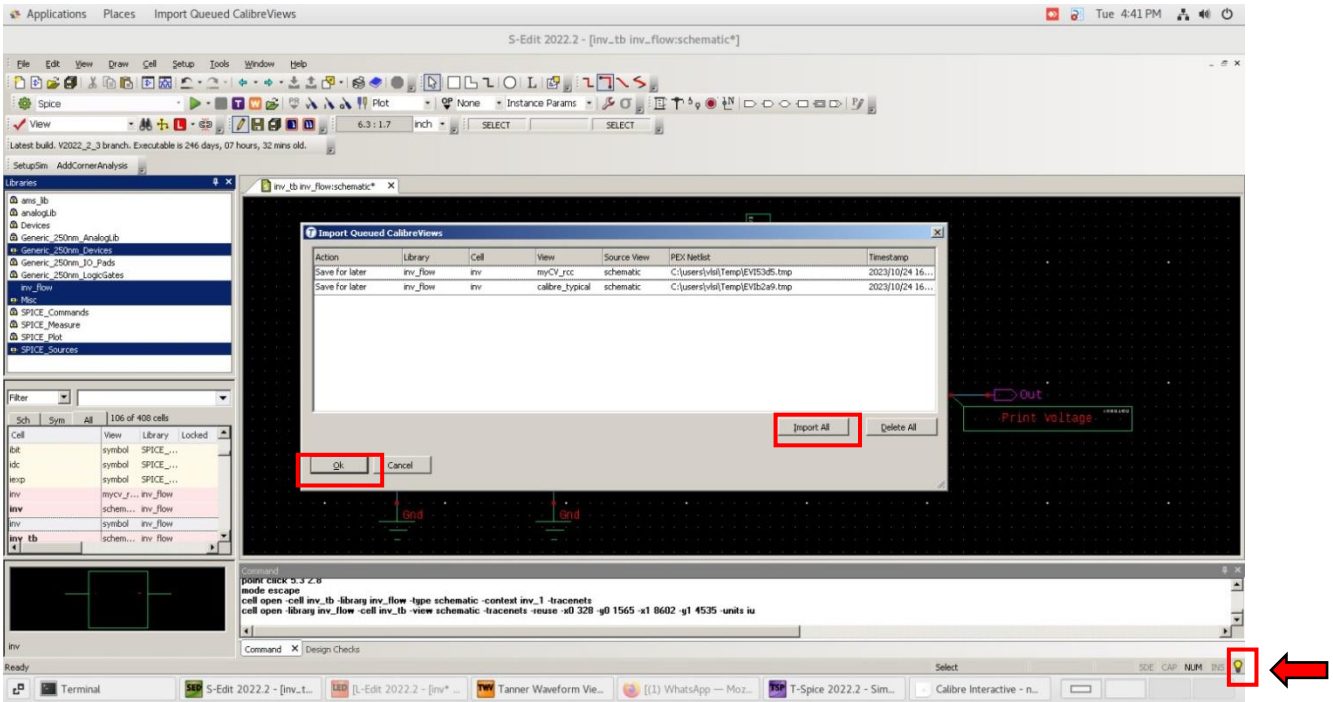
Setup >> Preferences >> General >> Calibre



Remove the old cellmap file and add the new path:

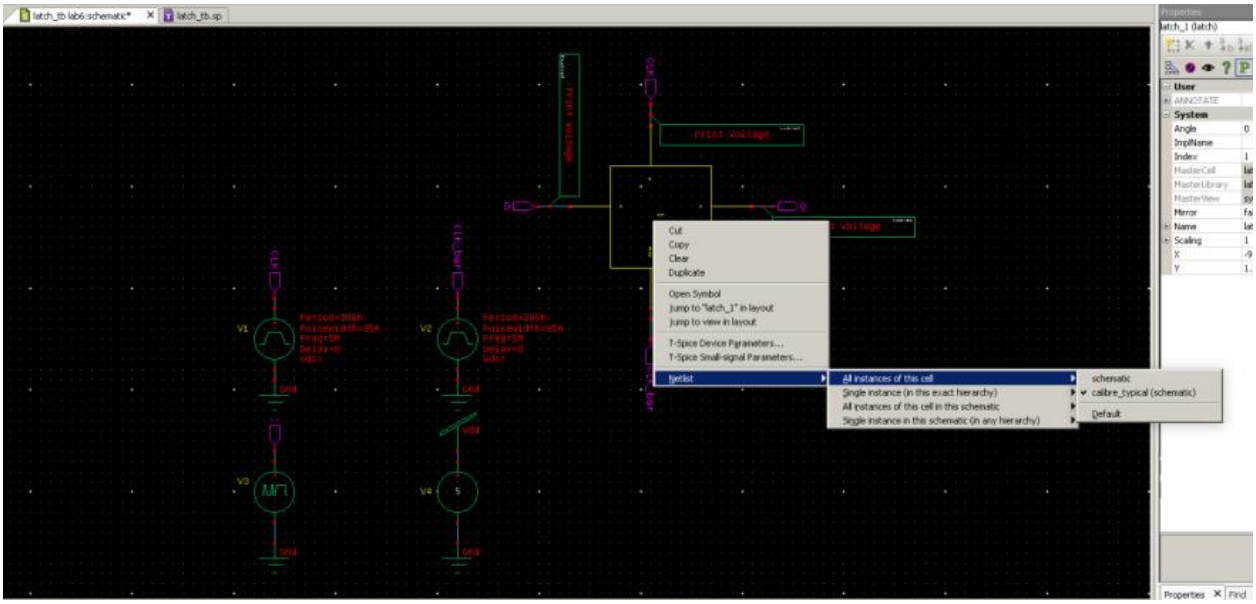
"/eda/Mentor/Tanner/TannerTools_v2022.2/Process/Generic_250nm/Rules/Calibre/Generic_250nm.cellmap"

Press the **lamp** in the **bottom right**, import calibre view and press ok



Now right click in your symbol (long click) and choose….

Netlist >> All instance of this cell >> Choose schematic or mycv_rcc.



Now open your extracted view contains all parasitics and add Vdd & Gnd symbol then save and r-simulate .