CENTER OF NANOELECTRONICS & DEVICES

CND 121: Introduction to Silicon Process & VLSI

Assignment #: 6

Section #: 16

Submitted by:

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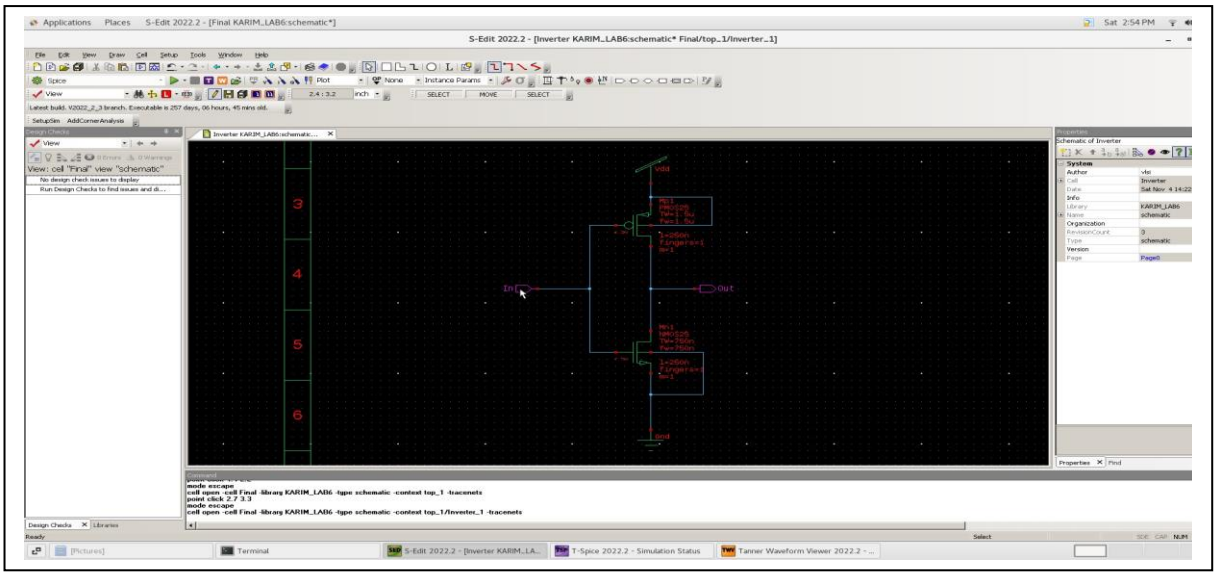
Submitted to TA: Mariam Taher

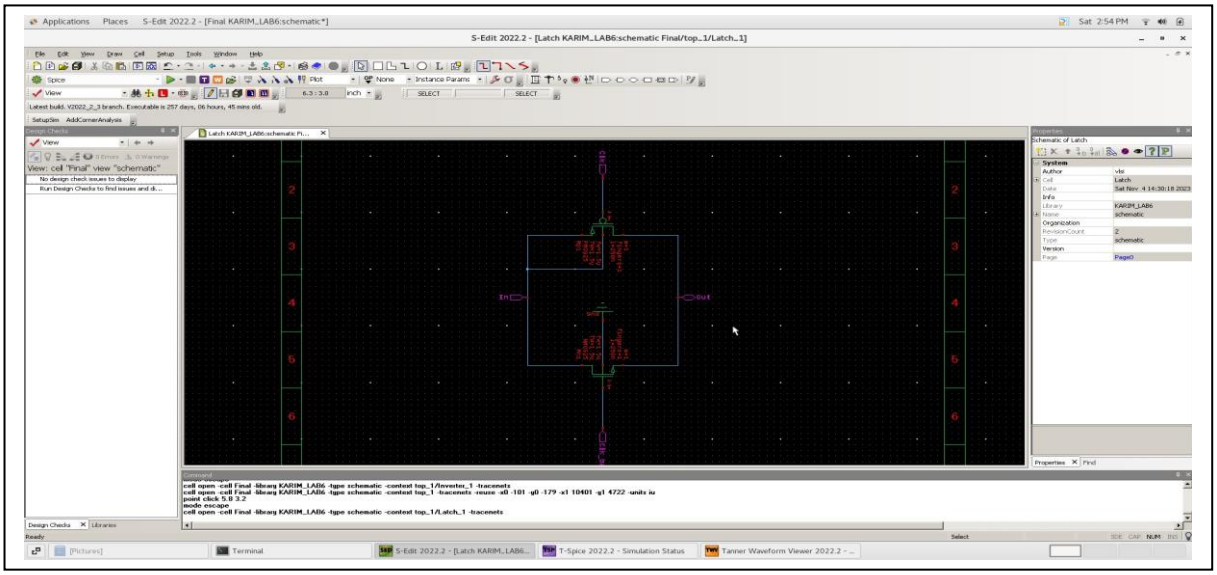
Date: 9/11/2023

1. Frontend flow

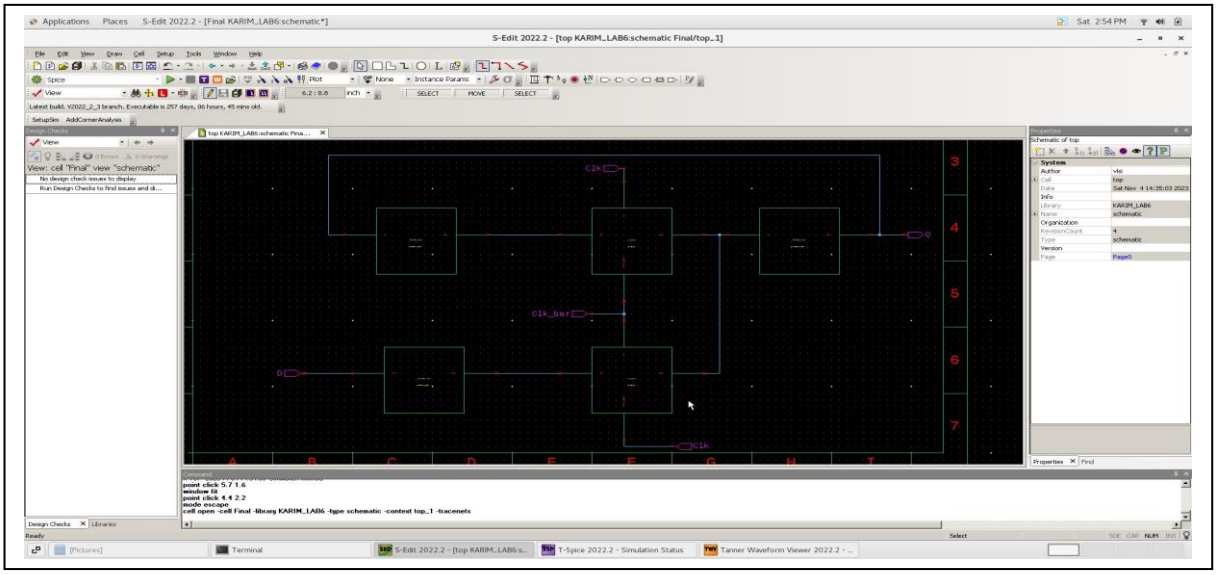
i. Add screenshot from your inverter **schematic:**



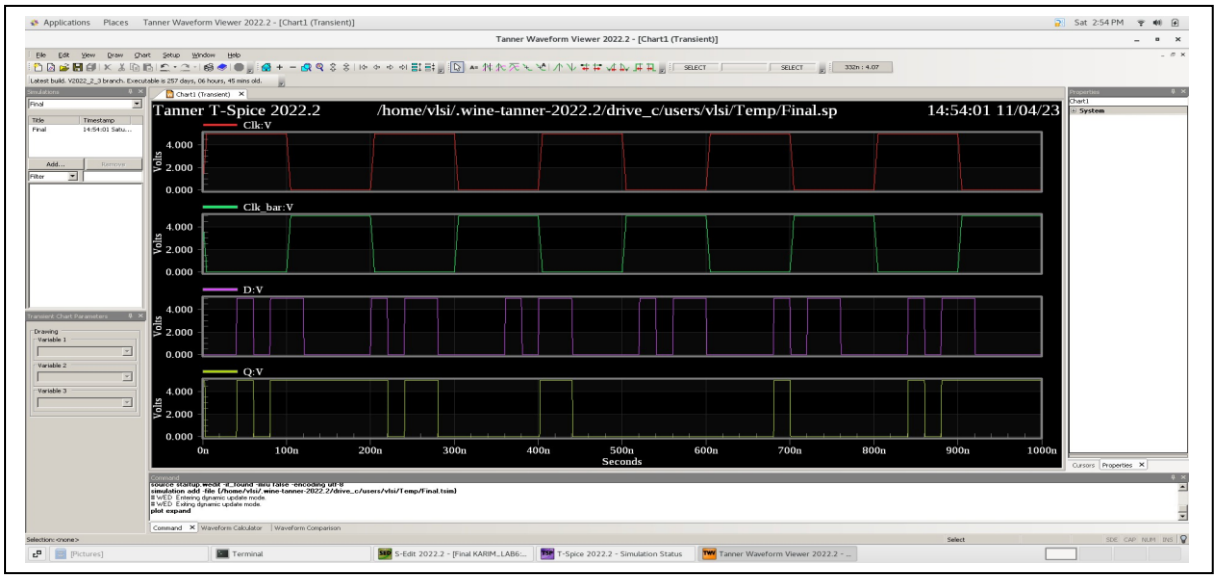
ii. Add screenshot from your Transmission gate **schematic:**



iii. Add screenshot from your latch **schematic:**



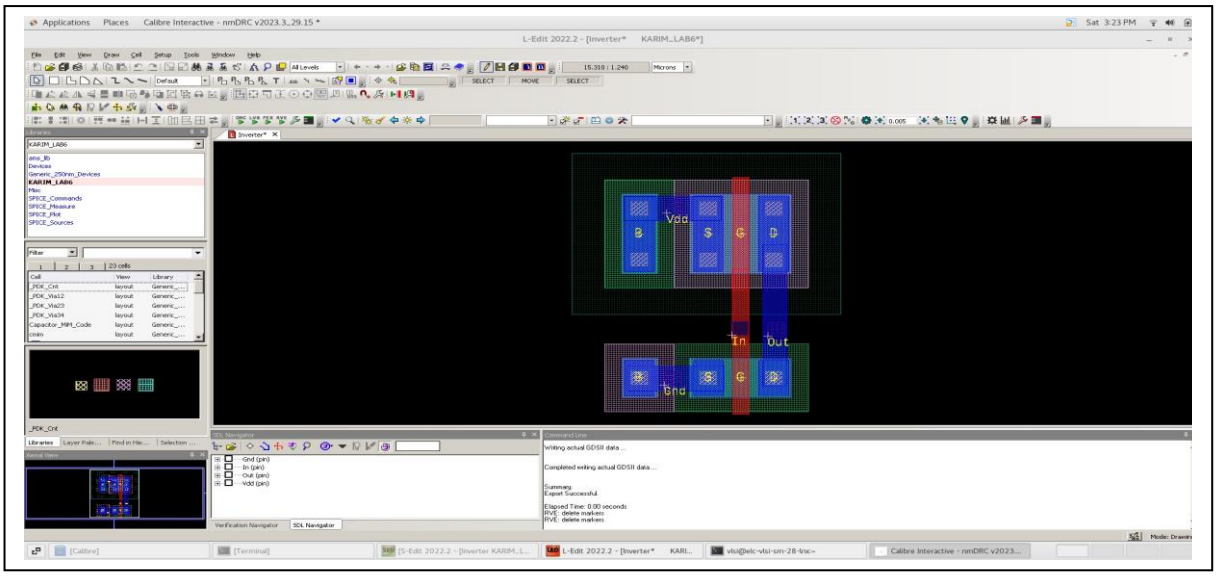
iv. Add screenshot from your **testbench:**



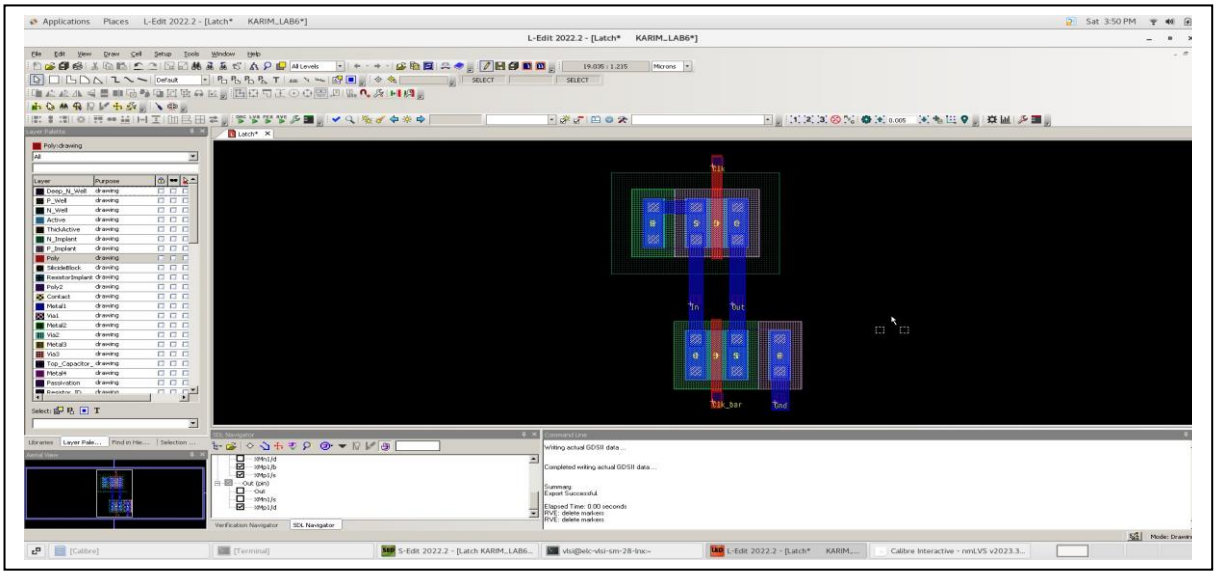
v. Propagation delay = **970.57psec**

2. Backend flow

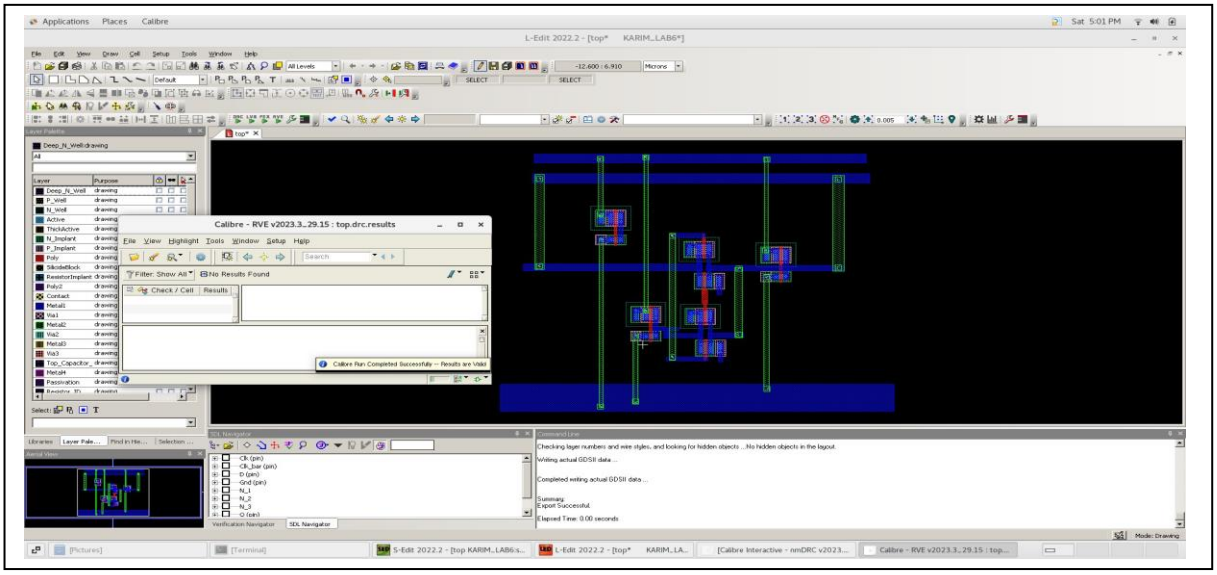
i. Add screenshot from your inverter **Layout:**



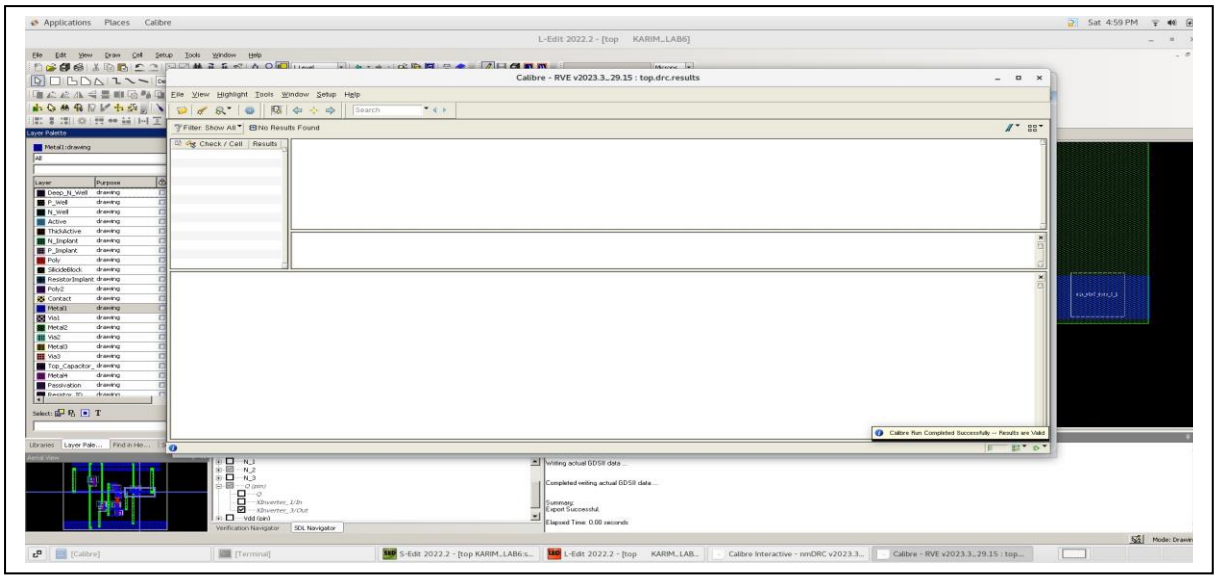
ii. Add screenshot from your Transmission gate **Layout:**



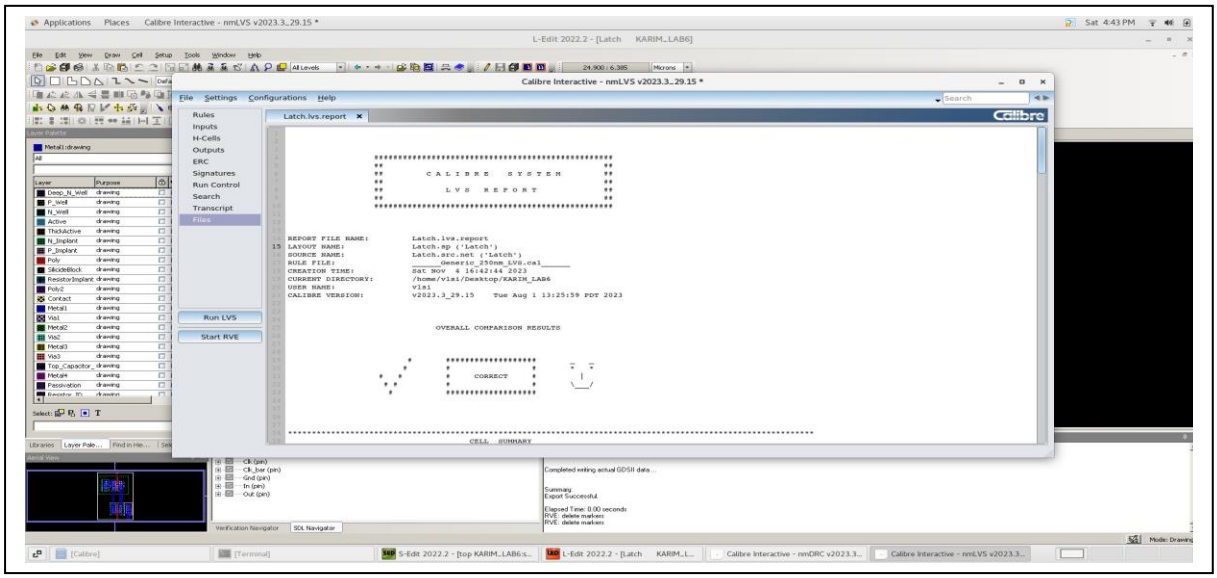
iii. Add screenshot from your latch **Layout**:



iv. Add screenshot after finishing **DRC** to grantee that no errors:



v. Add screenshot after finishing **LVS** to grantee that your design is matched:



vi. Propagation delay after post layout simulation = **975.1303psec**