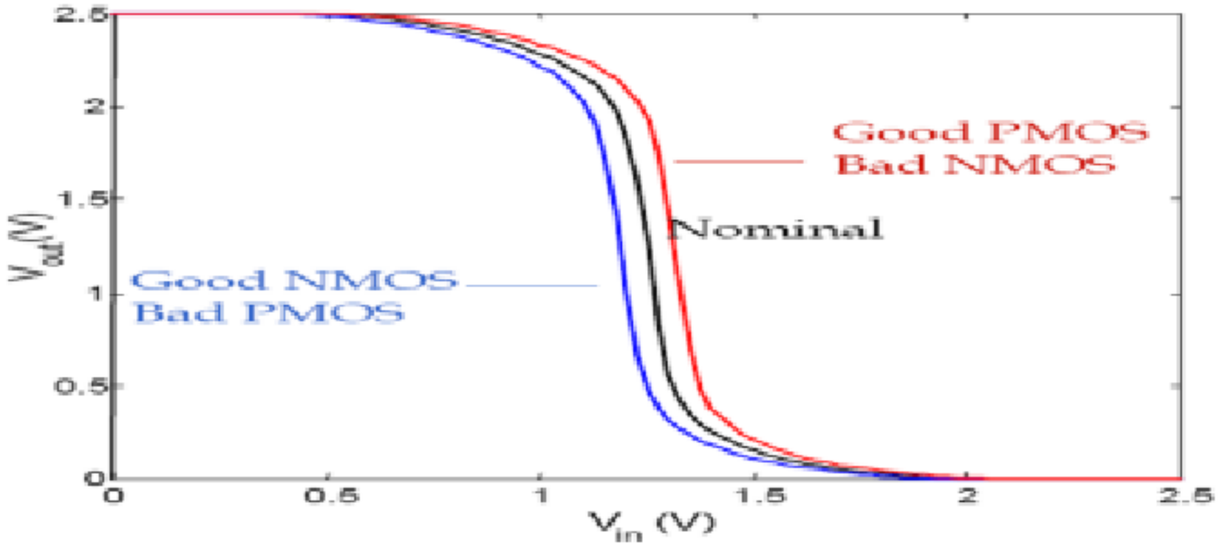
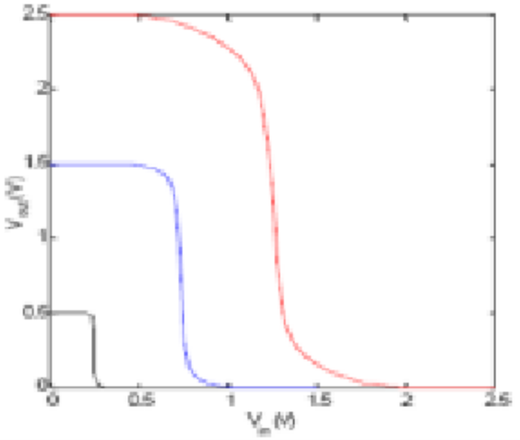
Impact of Process Variations

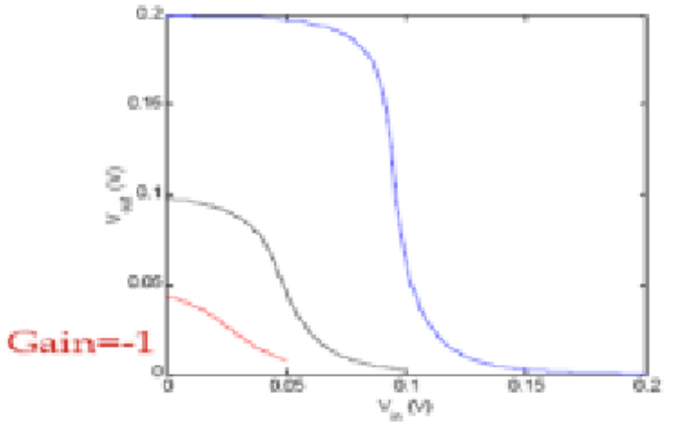
- *A CMOS inverter remains functional under a **wide range** of operating conditions.*
- We showed that variations in device sizes have minor impact on switching threshold.
- This robust behavior, which ensures functionality of the gate over a wide range of conditions, has contributed in a big way to **the popularity of the static CMOS gate.**



Gain as a function of VDD

- The gain of the inverter actually increases with a reduction of VDD .
- At a VDD =0.5V, which is just 100mV above VT of the transistors. **So why can't we operate all digital circuits at low VDD values?**
- **Yes, you get lower power consumption. But the delay of the gate drastically increases.**
- DC characteristics become very sensitive to variations in device parameters such at V_T once **V_{DD} and intrinsic voltages become comparable.**
- **The signal swing is reduced. Although this is good for internal noise (crosstalk), this is bad for external noise sources that do not scale.**

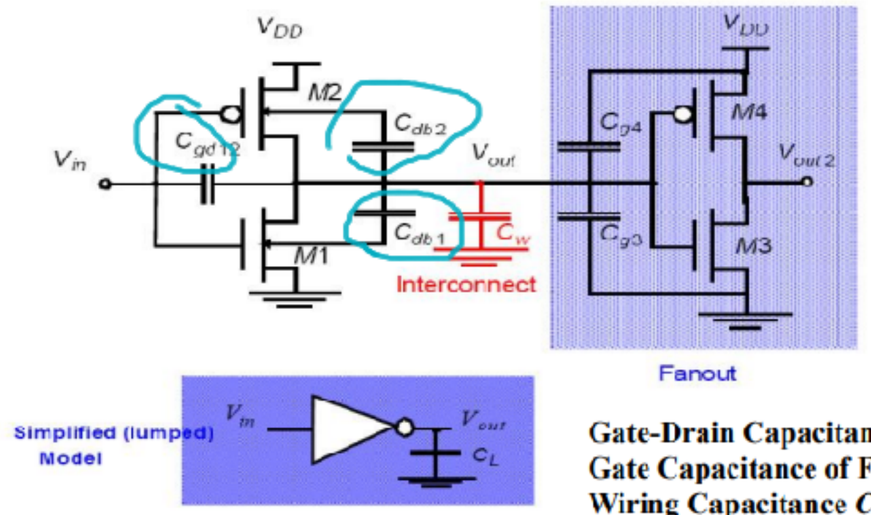




CMOS Inverter - DC Analysis

1. *High and low outputs = V_{DD} and Ground. Voltage swing= V_{DD}.* ***(High Noise Margins).***
2. *Logic Levels are independent of device sizes (**ratioless logic**)*
3. *In steady state, a path exists from O/P to V_{DD} or GND. Thus,* ***low output impedance. (Less sensitive to noise).***
4. *Input resistance is extremely high, since MOS gate draws no dc input current. Steady-state input current ~ zero. An inverter can theoretically drive infinite number of gates and be functionally operational.*

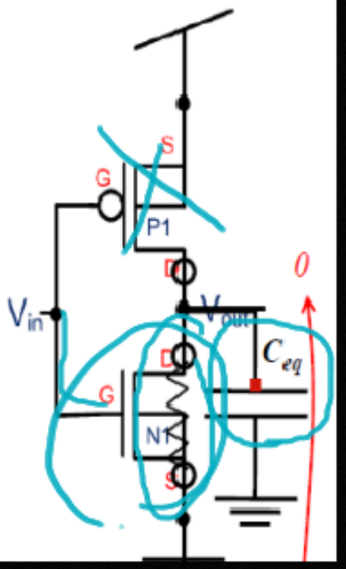
Computing the Capacitances

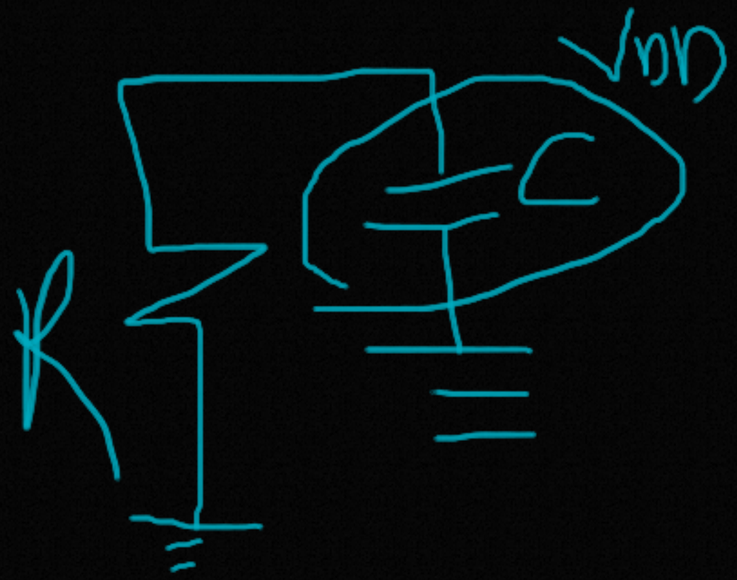


Gate-Drain Capacitance C_{gd12}
Gate Capacitance of Fanout C_{g3} and C_{g4}
Wiring Capacitance C_w
Diffusion Capacitances C_{db1} and C_{db2}

Parasitic Capacitances

- When the input is high, we essentially have closed the top switch and opened the bottom one.
- This creates a ***resistive path*** from the capacitor to ***GND***, and blocks the path from the supply to the output.
- Again we have an ***RC network***, though this time we are just ***discharging*** the capacitance to ***GND***.
- We end up with an output equal to ***GND***.



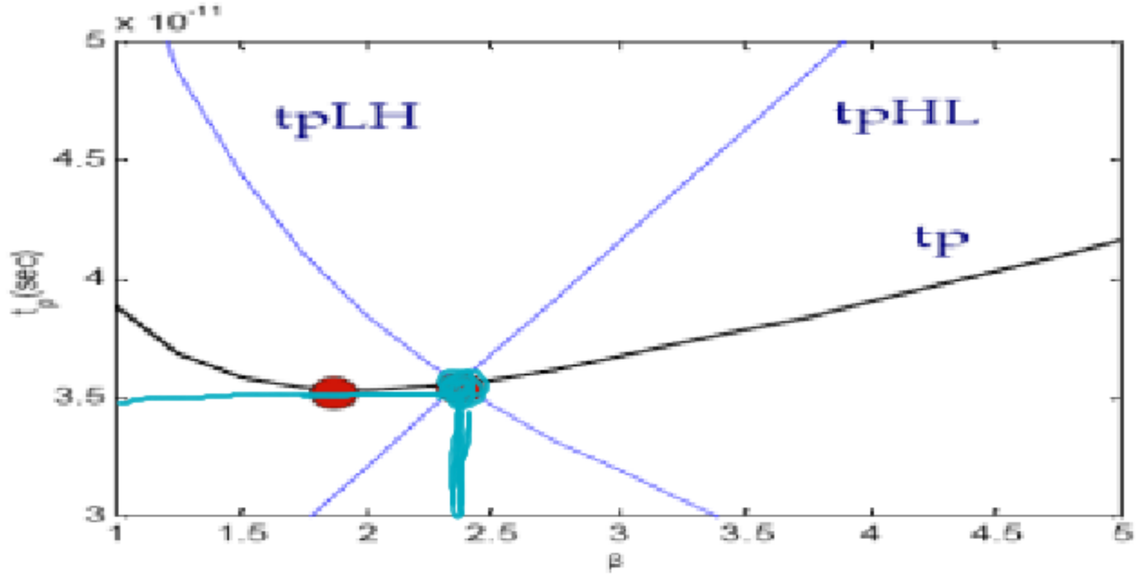


Parasitic Capacitances

- So we saw that, a switching CMOS inverter ***charges and discharges*** a parasitic output capacitance.
- During the switching process, we can create a model that will transform the circuit into **a *simple RC network*.**
- In this way, we can easily derive a first order analysis of the CMOS dynamic operation for ***propagation delay*** and ***power consumption*** calculation.

NMOS/PMOS ratio

Smaller devices yield faster designs at expense of symmetry and noise margin

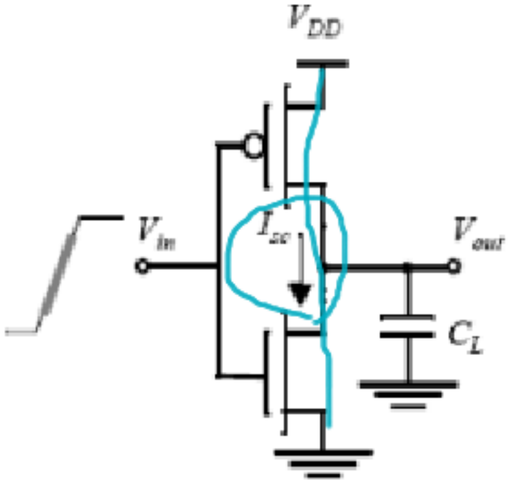


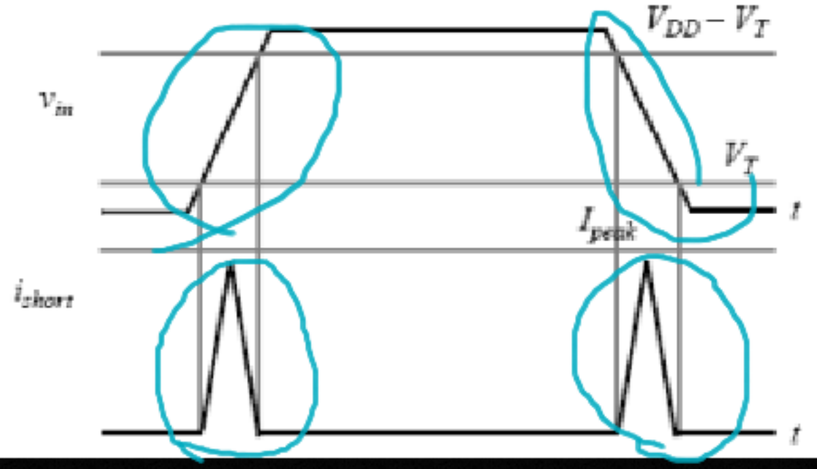
$$\beta = W_p / W_n$$

- **Increasing the transistor size also raises the diffusion capacitance and hence C_L.**
- *In fact, once the intrinsic capacitance (i.e. the diffusion capacitance)* starts to dominate the extrinsic load formed by wiring and fan-out, increasing the gate size does not longer help in reducing the delay, and only makes the gate larger in area. This effect is called "***self-loading***".
- *In addition, wide transistors have a larger gate* capacitance, which increases the fan-out factor of the driving gate and adversely affects its speed.

Dissipation Due to Direct-Path Currents

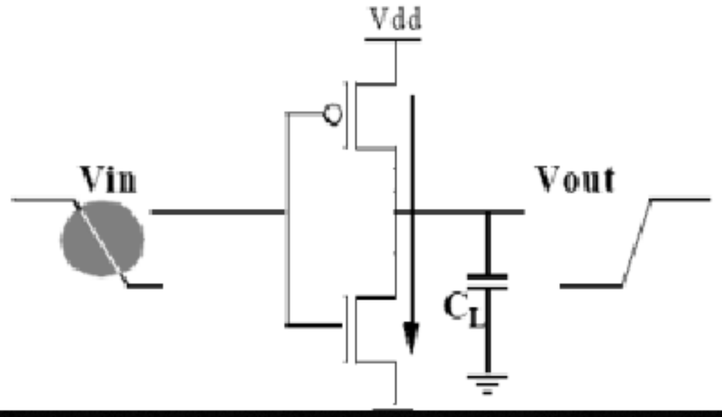
- In actual designs, the assumption of the zero rise and fall times of the input wave forms is not correct. The finite slope of the input signal causes a direct current path between *VDD* and *GND for a short period of time during switching, while the NMOS and the PMOS* transistors are conducting simultaneously.

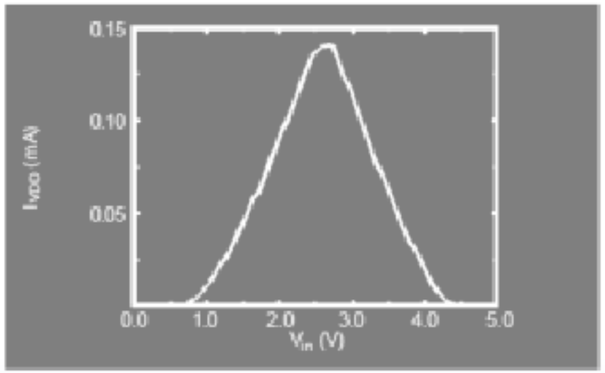




Short Circuit Currents

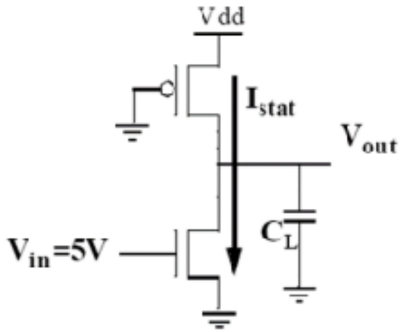
- The power dissipation due to short-circuit currents is minimized by matching the rise/fall times of the input and output signals. At the overall circuit level, this means that rise/fall times of all signals should be kept constant within a range.



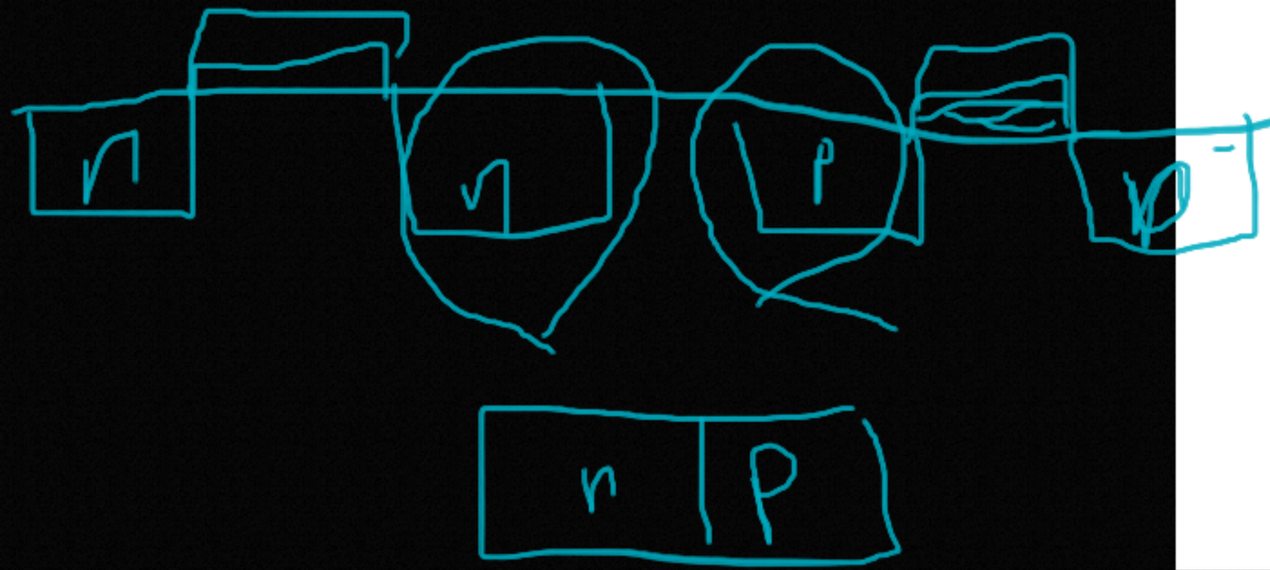


Static Power Consumption

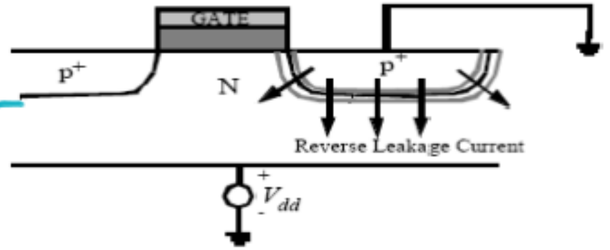
- Wasted energy …
- Should be avoided in almost all cases, but could help reducing energy in others (e.g. sense amps)



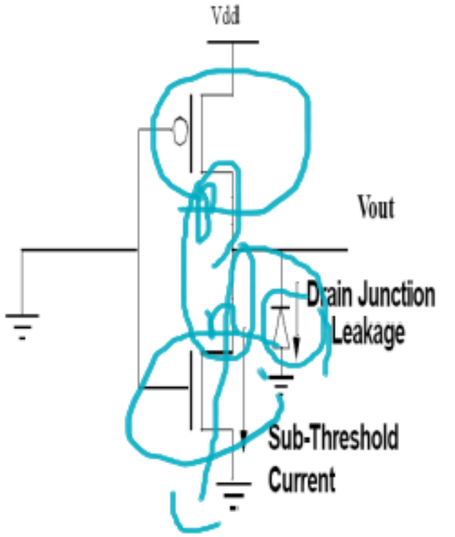
$$P_{stat} = P_{(In=1)} \cdot V_{dd} \cdot I_{stat}$$



Static Consumption - (Leakage)



$$P_{stat} = I_{stat} V_{DD}$$



Sub-threshold current one of most compelling issues in low-energy circuit design!

Putting It All Together

The total power consumption of the CMOS inverter is now expressed as the sum of its three components:

$$P_{tot} = P_{dyn} + P_{dp} + P_{stat} = (C_L V_{DD}^2 + V_{DD} I_{peak} t_s) f_{0 \to 1} + V_{DD} I_{leak}$$

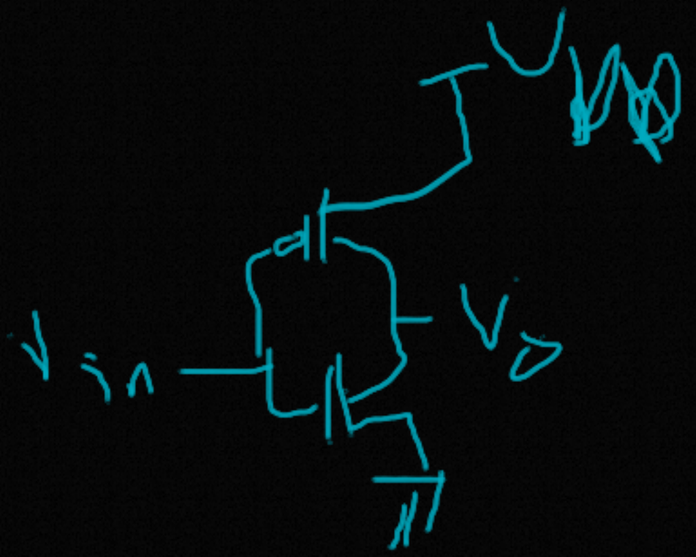
- The power dissipation is dominated by the dynamic power consumed in charging and discharging the load capacitor.
  It is given by $P_{0 \to 1} = C_L \ V_{DD}^{\ 2} \ f$.
- *The dissipation is* proportional to the activity in the network.
- *The dissipation due to the direct-path* currents occurring during switching can be limited by careful tailoring of the signal slopes.
- The static dissipation can usually be ignored but might become a major factor in the future as a result of subthreshold currents.

Performance vs. Power Trade-offs.

- Leakage currents cause a rise in static power.
- This is offset by dropping V_{DD}, which is enabled by reducing V_T at no cost in performance, and results in quadratic reduction in dynamic power.

Principles for Power Reduction

- Prime choice: Reduce voltage!
  - Recent years have seen an acceleration in supply voltage reduction
  - Design at very low voltages still open question (0.6 … 0.9V by 2010!)
- Reduce switching activity
- Reduce physical capacitance
  - Device Sizing



Impact of Technology Scaling

- ***Goals of Technology Scaling***
- Make things cheaper:
  - Want to sell more functions (transistors) per chip for the same money
  - Build same products cheaper, sell the same part for less money
  - Price of a transistor has to be reduced
- But also want to be faster, smaller, lower power.