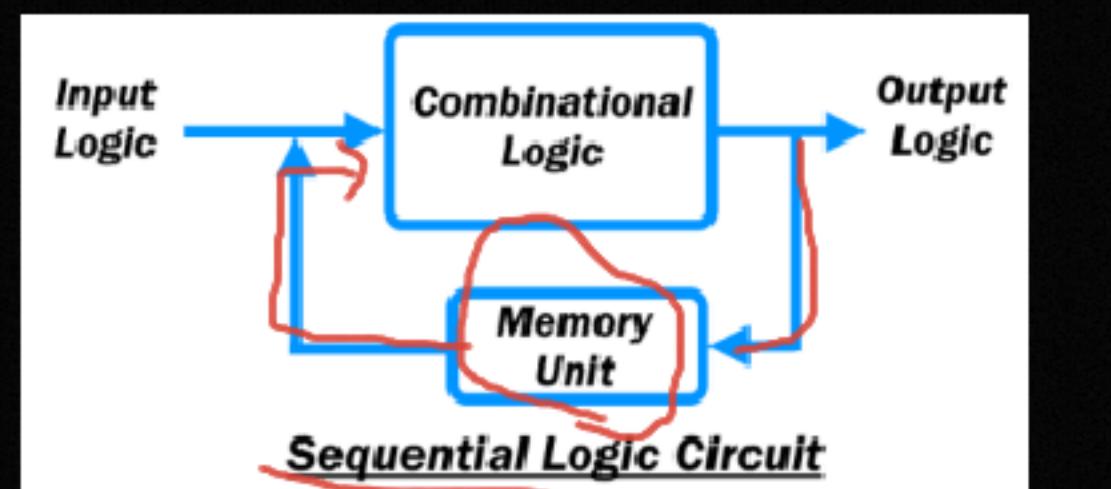
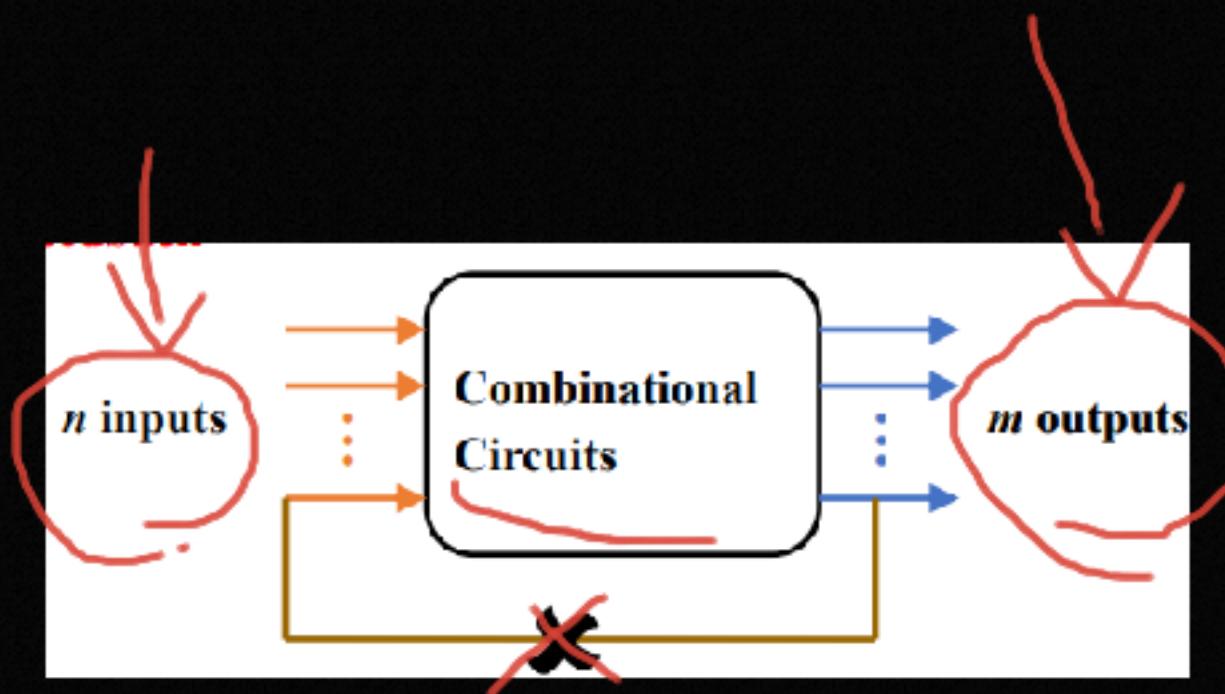
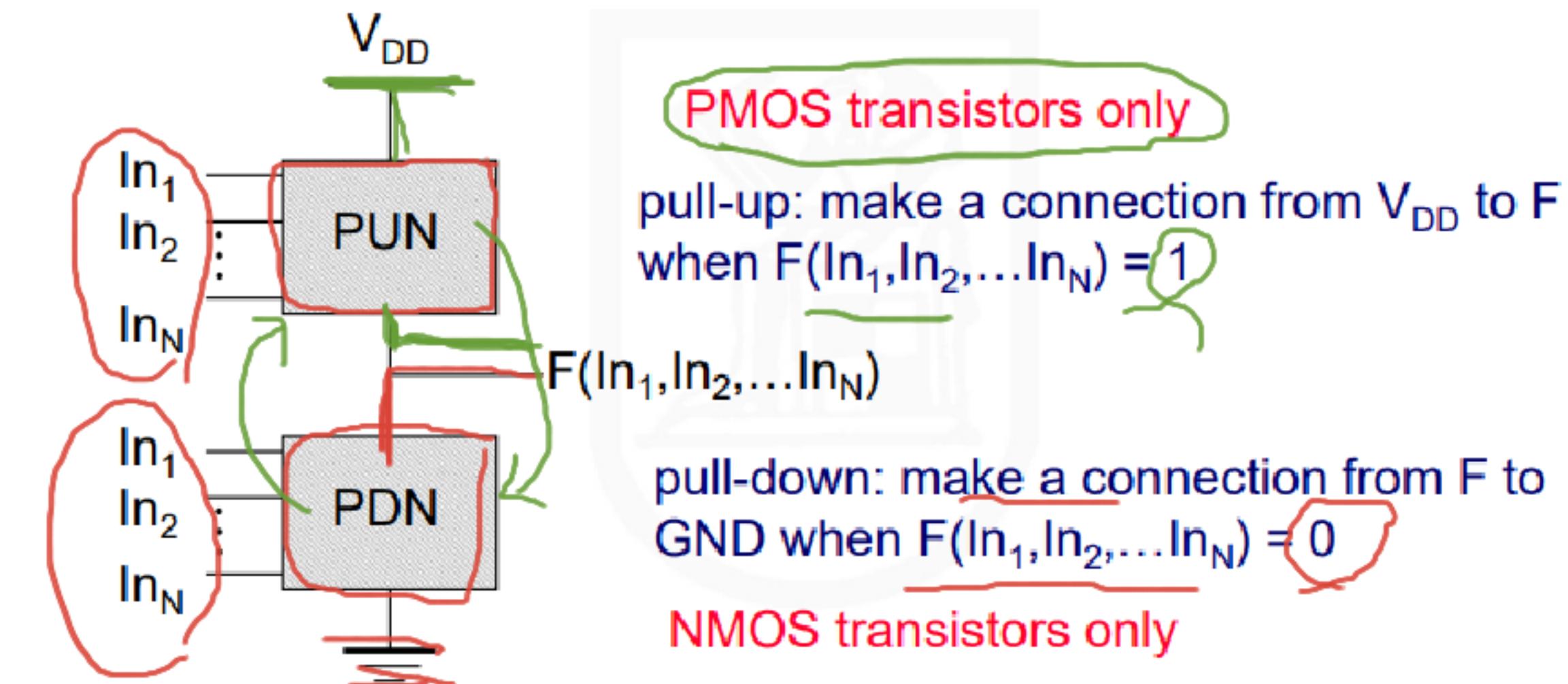


CMOS



Static Complementary CMOS: Complex Gates

- Pull-up network (PUN) and pull-down network (PDN)



PUN and PDN are dual logic networks

Now to understand NMOS pass strong 0 and weak 1, let's take one example. Suppose we have one NMOS. As shown in the following figure, let's take $V_{dd} = 1V$, $V_{gs} = 1V$, and Threshold voltage(V_t) = 0.2v. And Initially, Capacitor(V_{cc}) is 0v.

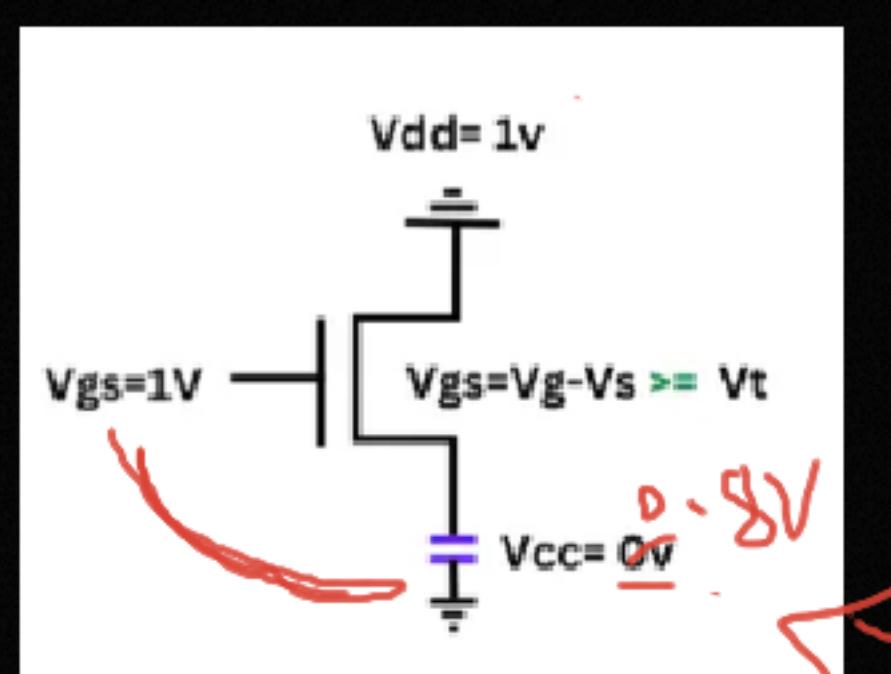
After Some time, lets assume that capacitor V_{cc} , Charged by 0.2v, so $V_{gs} = V_g - V_s = 1 - 0.2 = 0.8 > 0.2(v_t)$. So node V_{cc} charged by 0.2v and still V_{gs} is greater than V_t . So still current will flow from the drain to the source.

After Some time, that capacitor V_{cc} , charged by 0.8v, so $V_{gs} = V_g - V_s = 1 - 0.8 = 0.2 = 0.2(v_t)$. So node V_{cc} charged by 0.8v and still V_{gs} is equal to V_t . So still current will flow from the drain to the source.

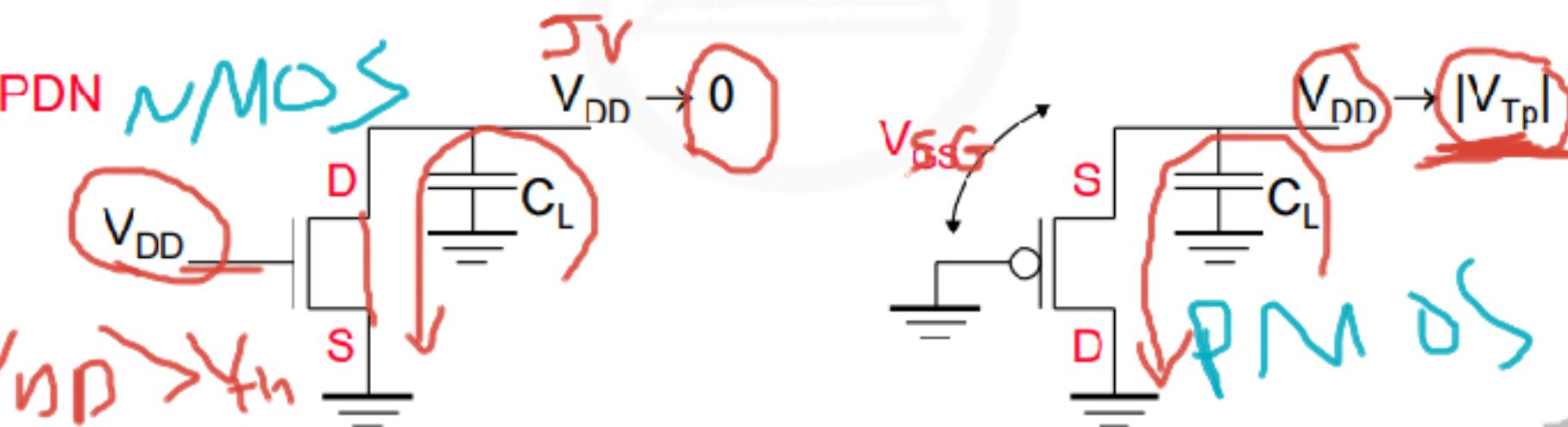
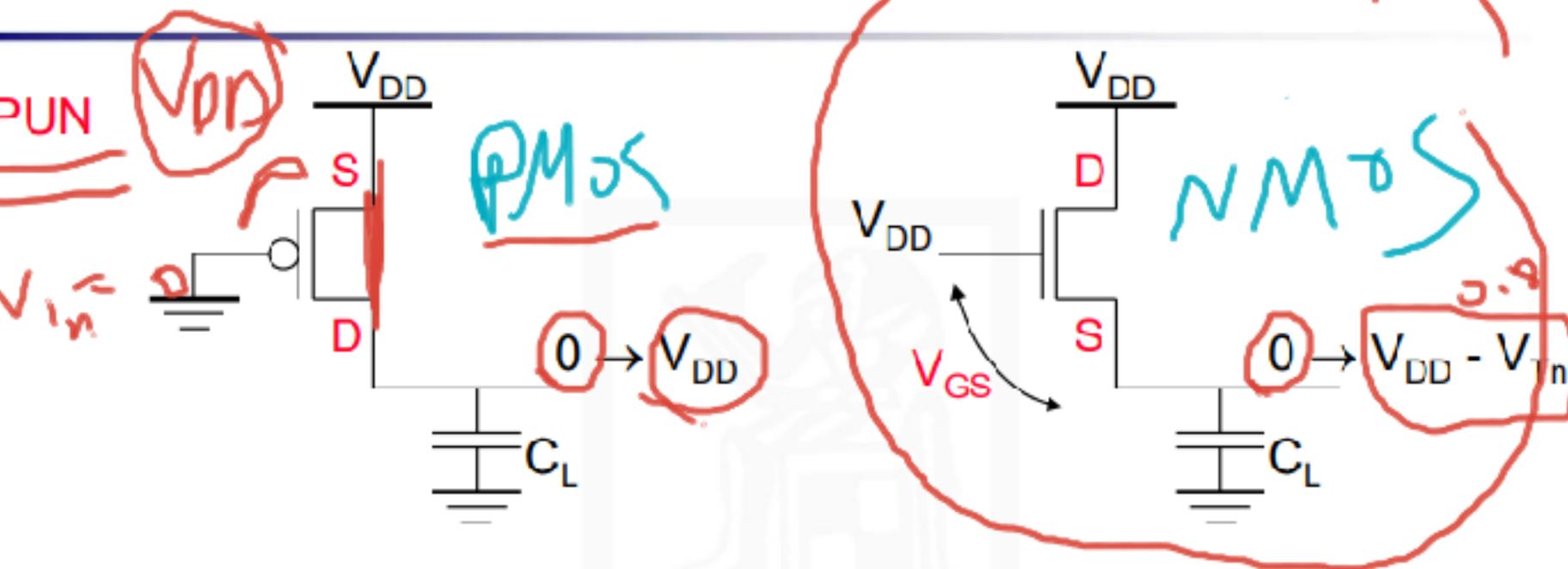
Now As soon As V_{cc} becomes 0.8v, after that, it will not charge further because $V_{gs} > V_t$, the condition is not satisfying, so at 0.8v only, NMOS will pass, and after that, it will stop charging that capacitor. Based on the above explanation, we can say that NMOS is Weak to pass 1, which means NMOS can not fully charge the capacitor. It will charge up to $V_{cc} = V_{dd} - V_t$.

$\text{PMOS} \xrightarrow{0 \rightarrow \text{weak}} \xrightarrow{1 \rightarrow \text{strong}}$

$\text{NMOS} \xrightarrow{\text{strong}} \xrightarrow{1 \rightarrow \text{weak}} \checkmark$
 $V_{gs} = V_{dd} > V_t$

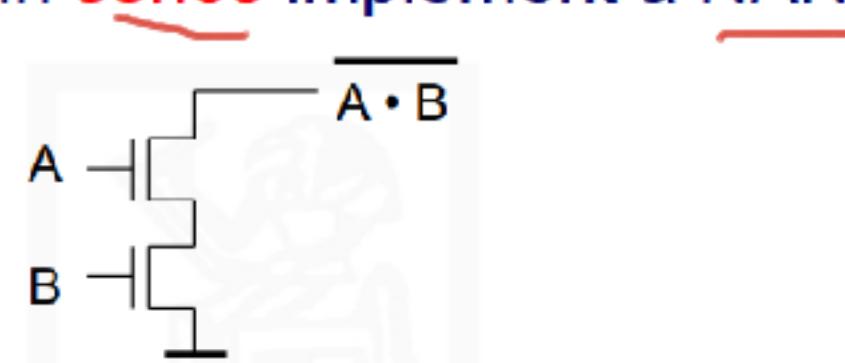


Threshold Drops

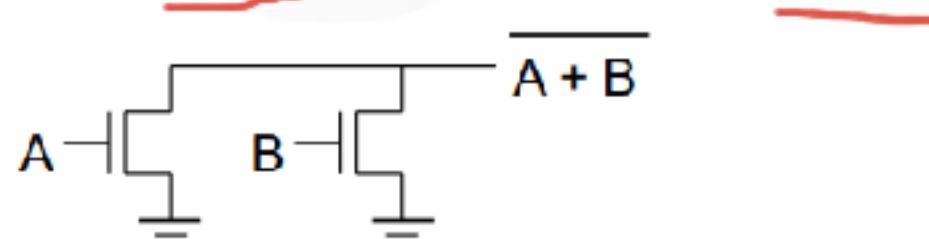


Construction of PDN

- NMOS devices in series implement a NAND function



- NMOS devices in parallel implement a NOR function



Dual PUN and PDN

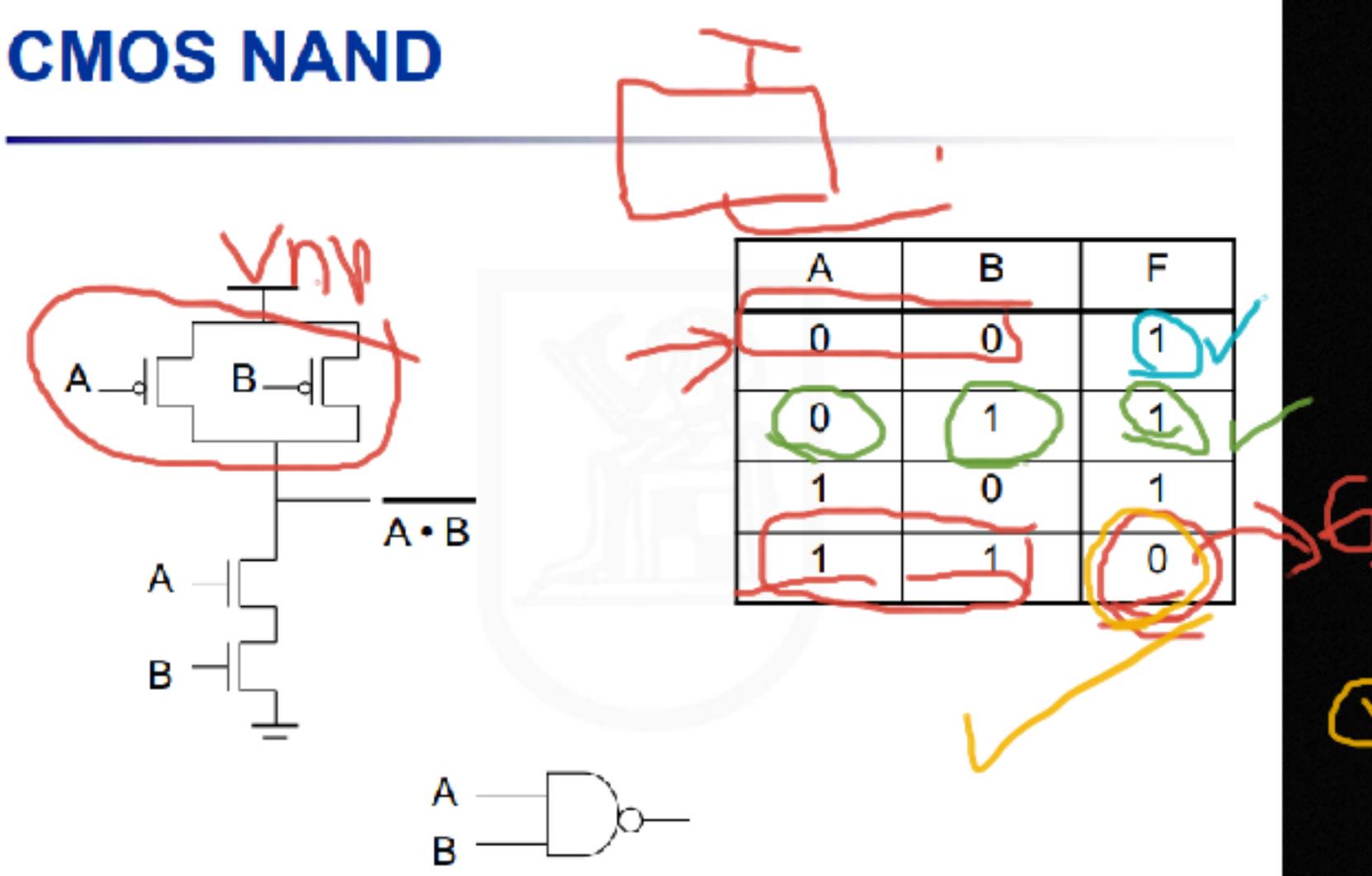
- PUN and PDN are dual networks
 - DeMorgan's theorems

$$\overline{A + B} = \overline{A} \cdot \overline{B} \quad [!(A + B) = !A \cdot !B \text{ or } !(A | B) = !A \& !B]$$

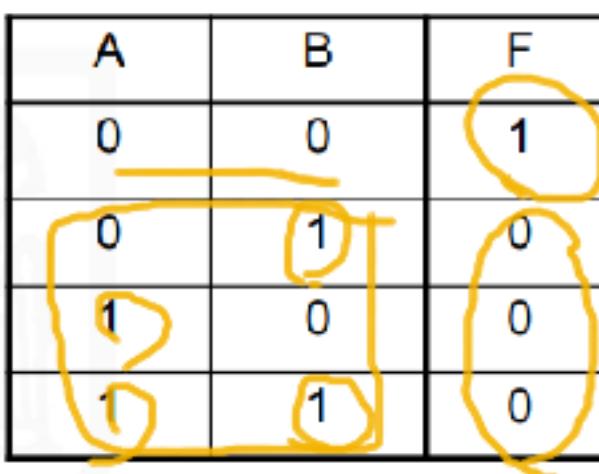
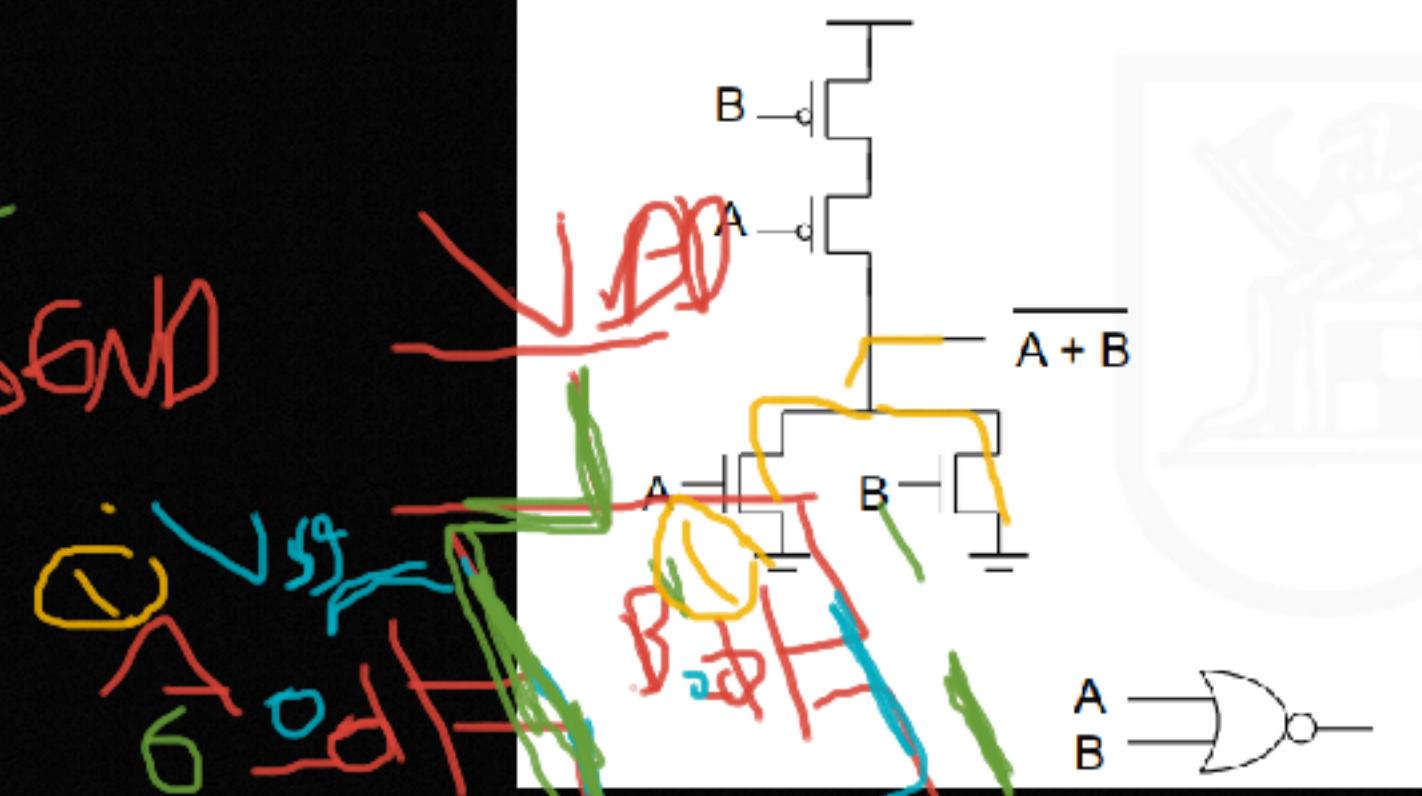
$$\overline{\overline{A \cdot B}} = A + B \quad [!(A \cdot B) = !A + !B \text{ or } !(A \& B) = !A | !B]$$

- a parallel connection of transistors in the PUN corresponds to a series connection of the PDN
- A “complementary gate” is naturally inverting (NAND, NOR, AOI, OAI)
- Number of transistors for an N-input logic gate is $2N$

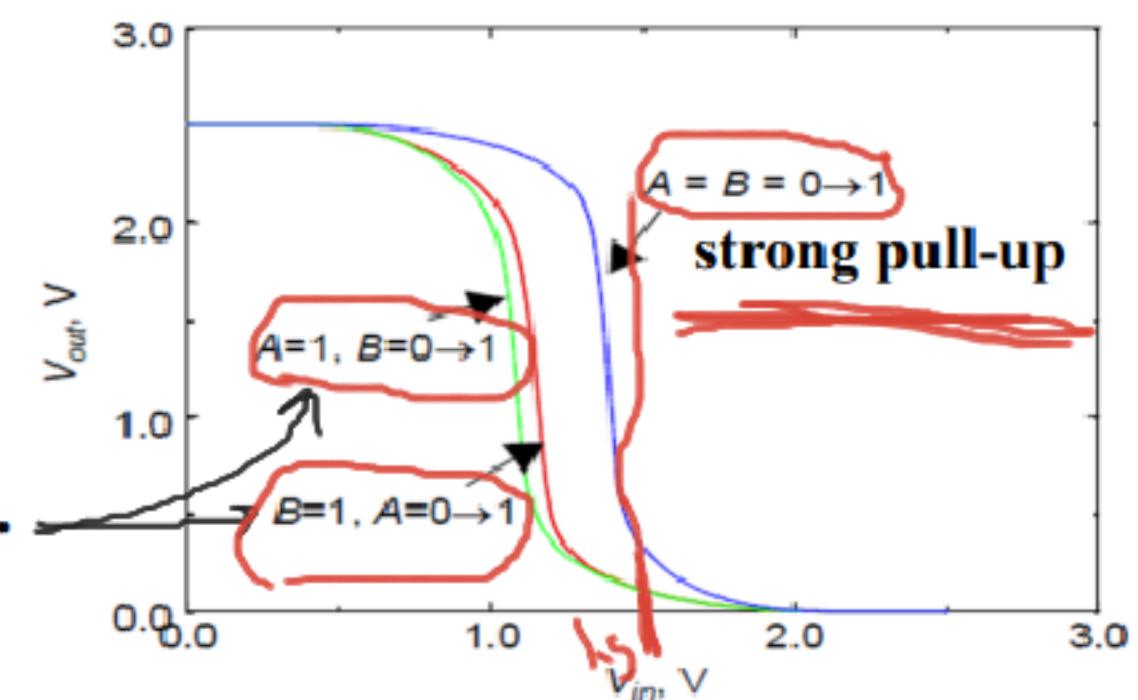
CMOS NAND



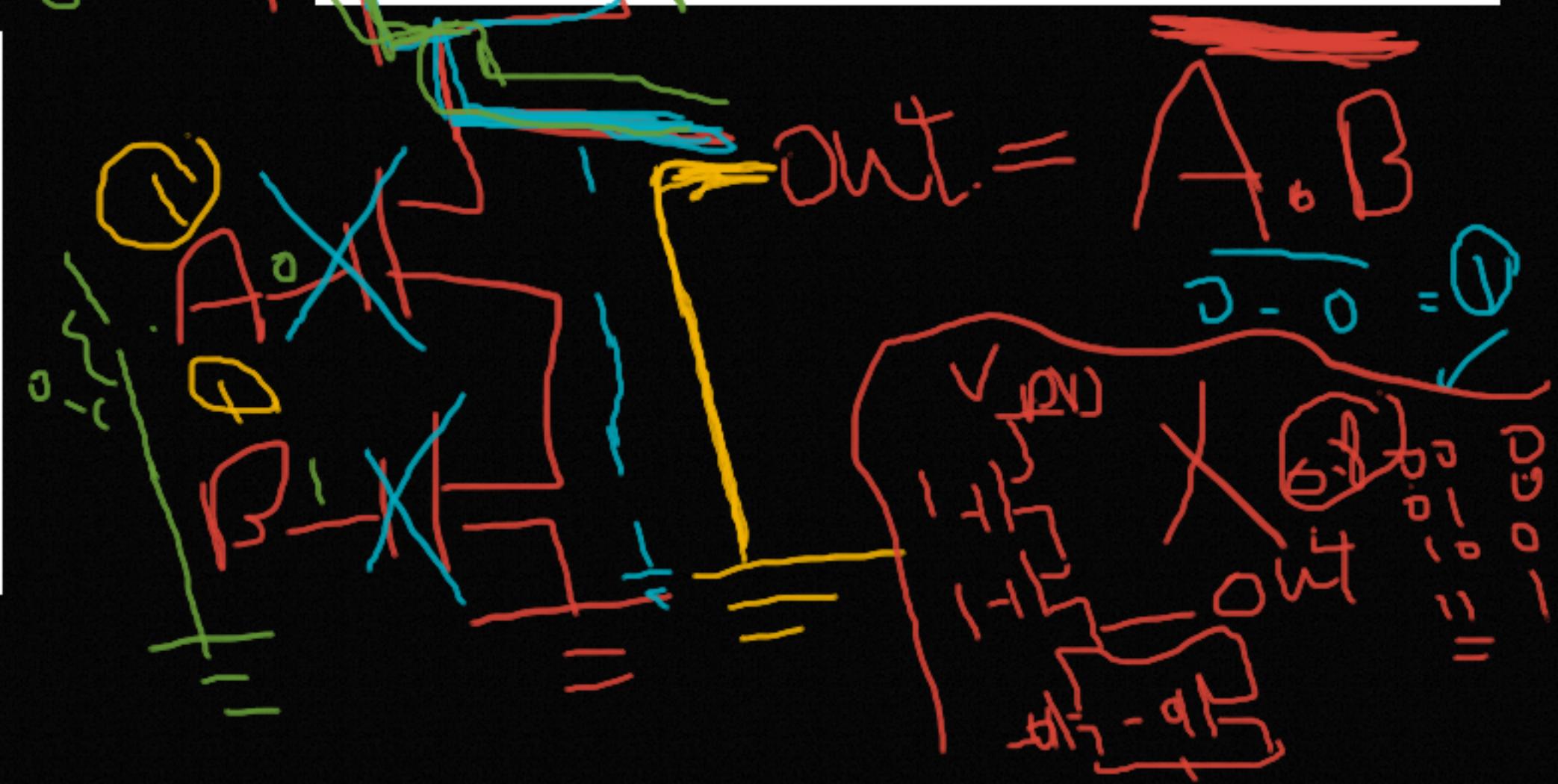
CMOS NOR



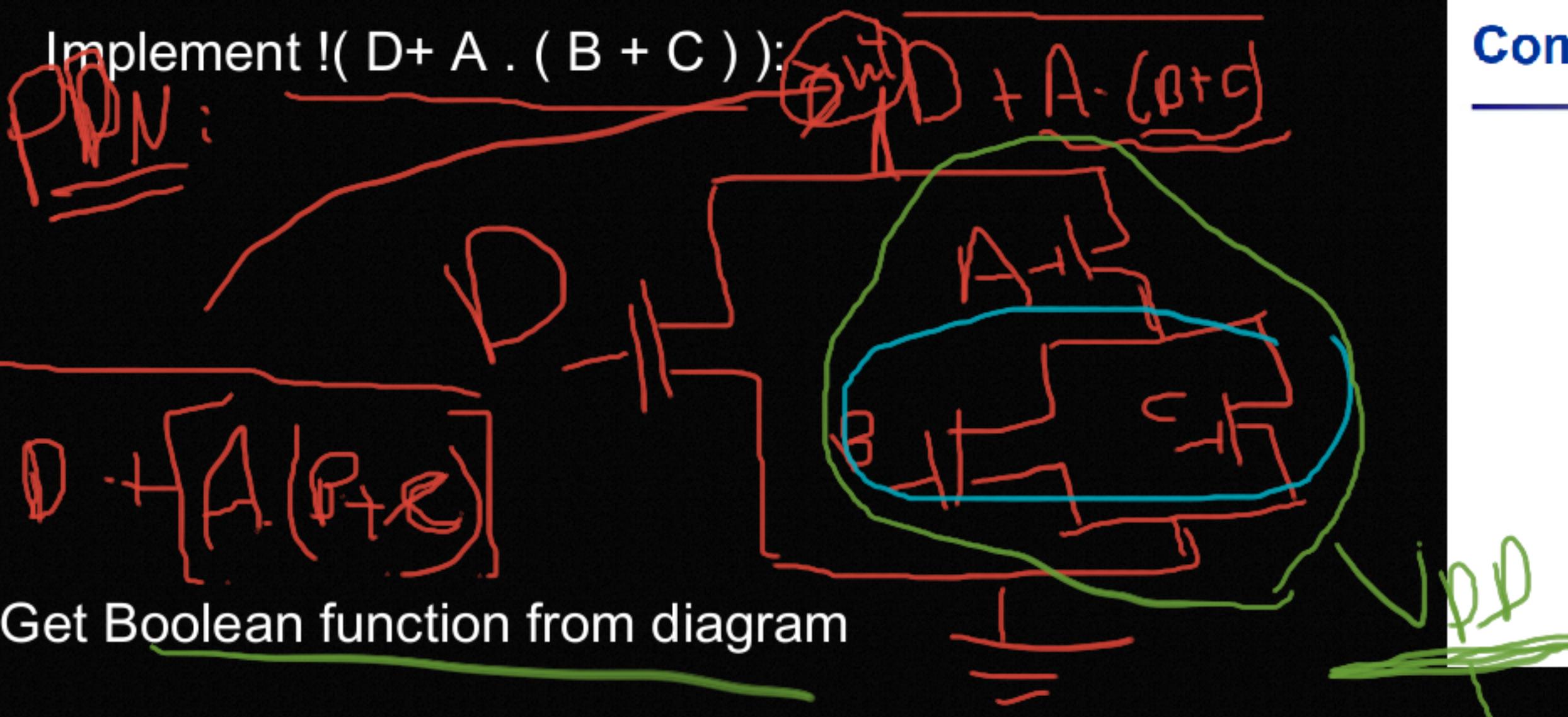
- a) $A = B = 0 \rightarrow 1$.
- b) $A = 1, B = 0 \rightarrow 1$.
- c) $B = 1, A = 0 \rightarrow 1$.



Why NO AND GATE??!

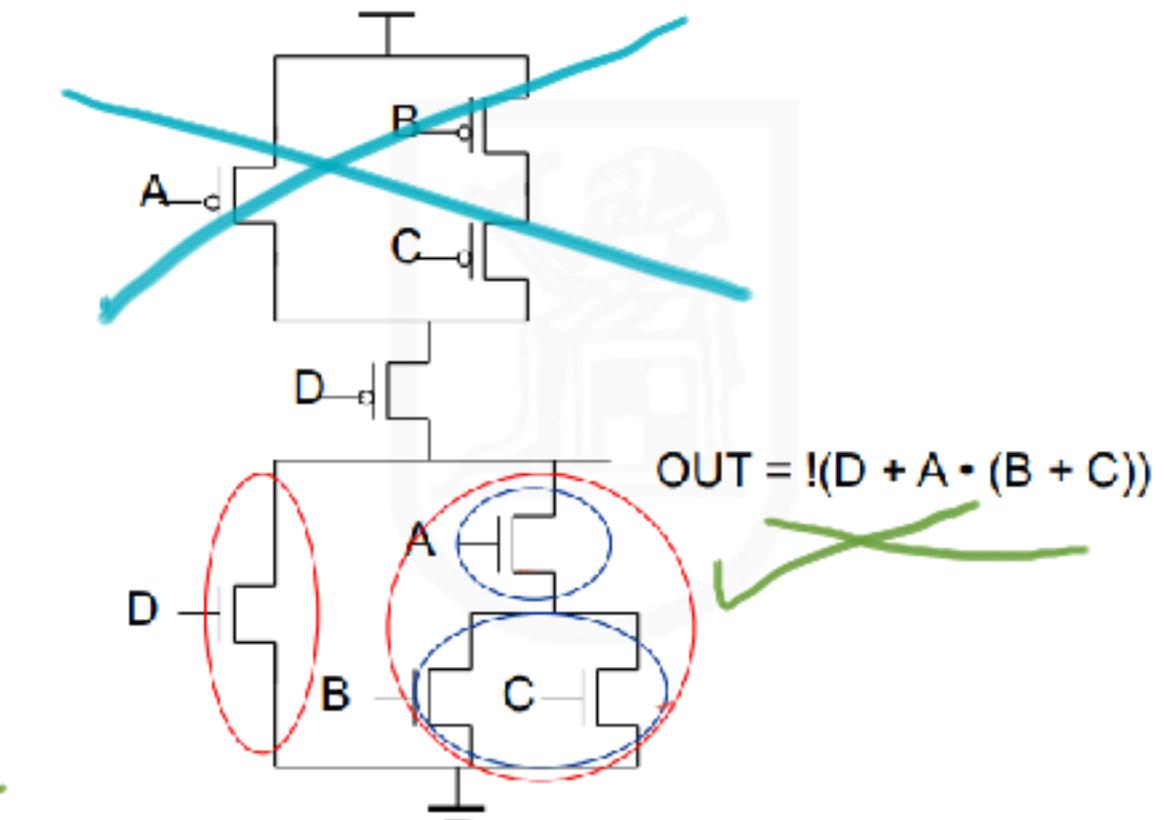


Implement $!(D + A \cdot (B + C))$:



Get Boolean function from diagram

Complex CMOS Gate

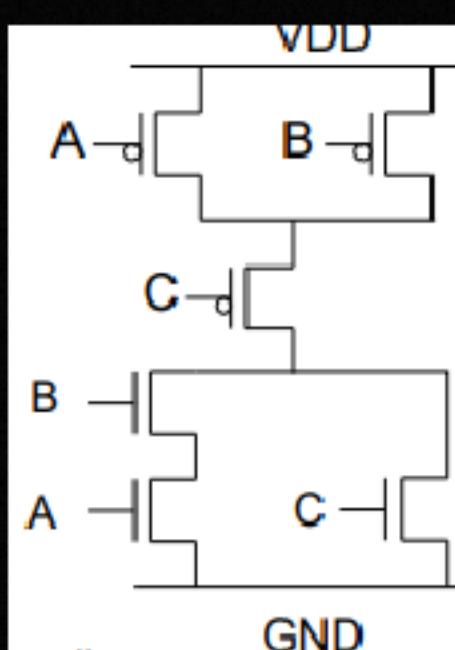


Fill Truth Table

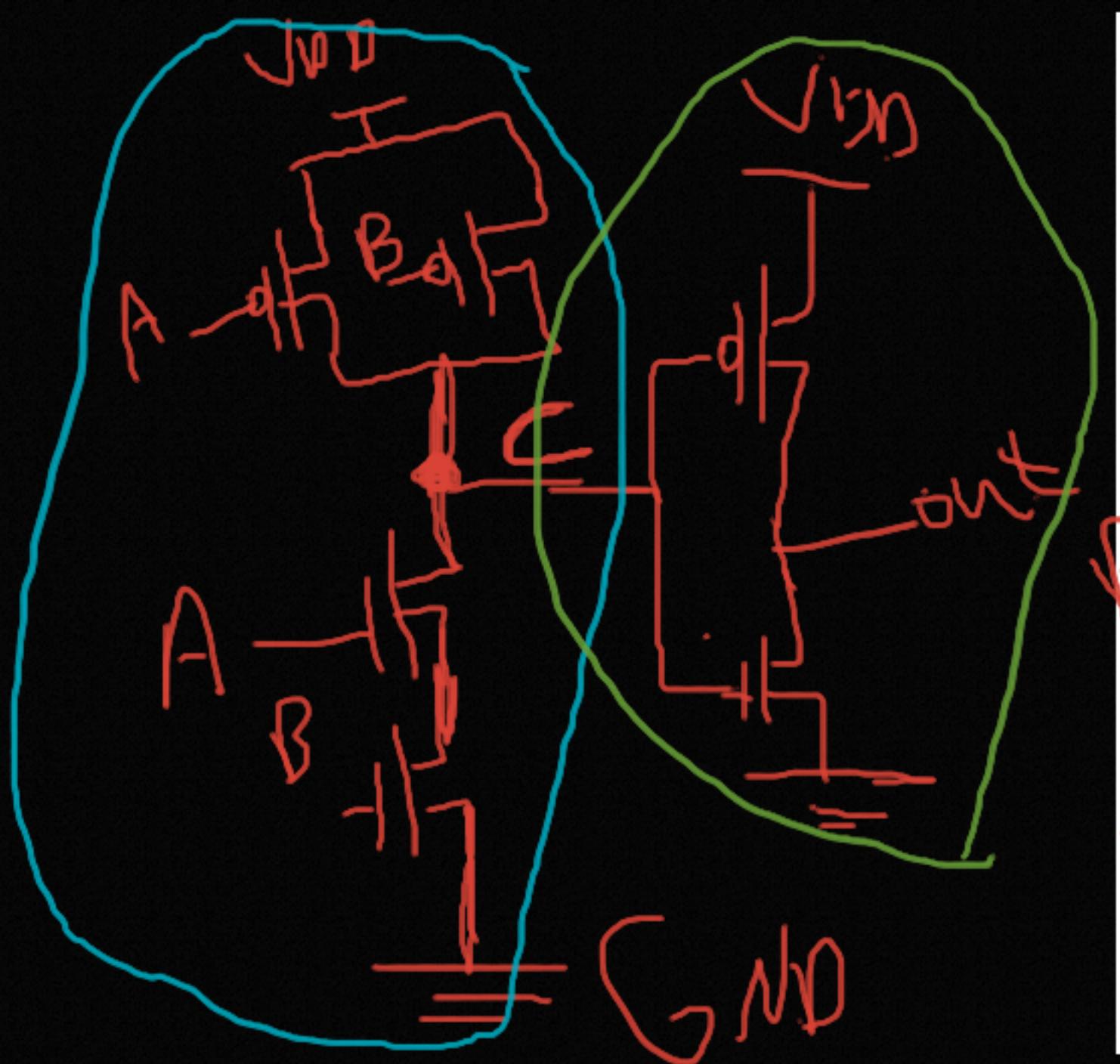
	VDD	A	B	C	D	Output
0	0	0	0	1		
0	0	0	1	0		
0	1	0	0	1		
0	1	1	1	0		
1	0	0	0	1		
1	0	0	1	0		
1	1	0	0	0		
1	1	1	1	0		
1	1	1	1	0		

Exercise

$$OUT = \overline{A \cdot B + C}$$

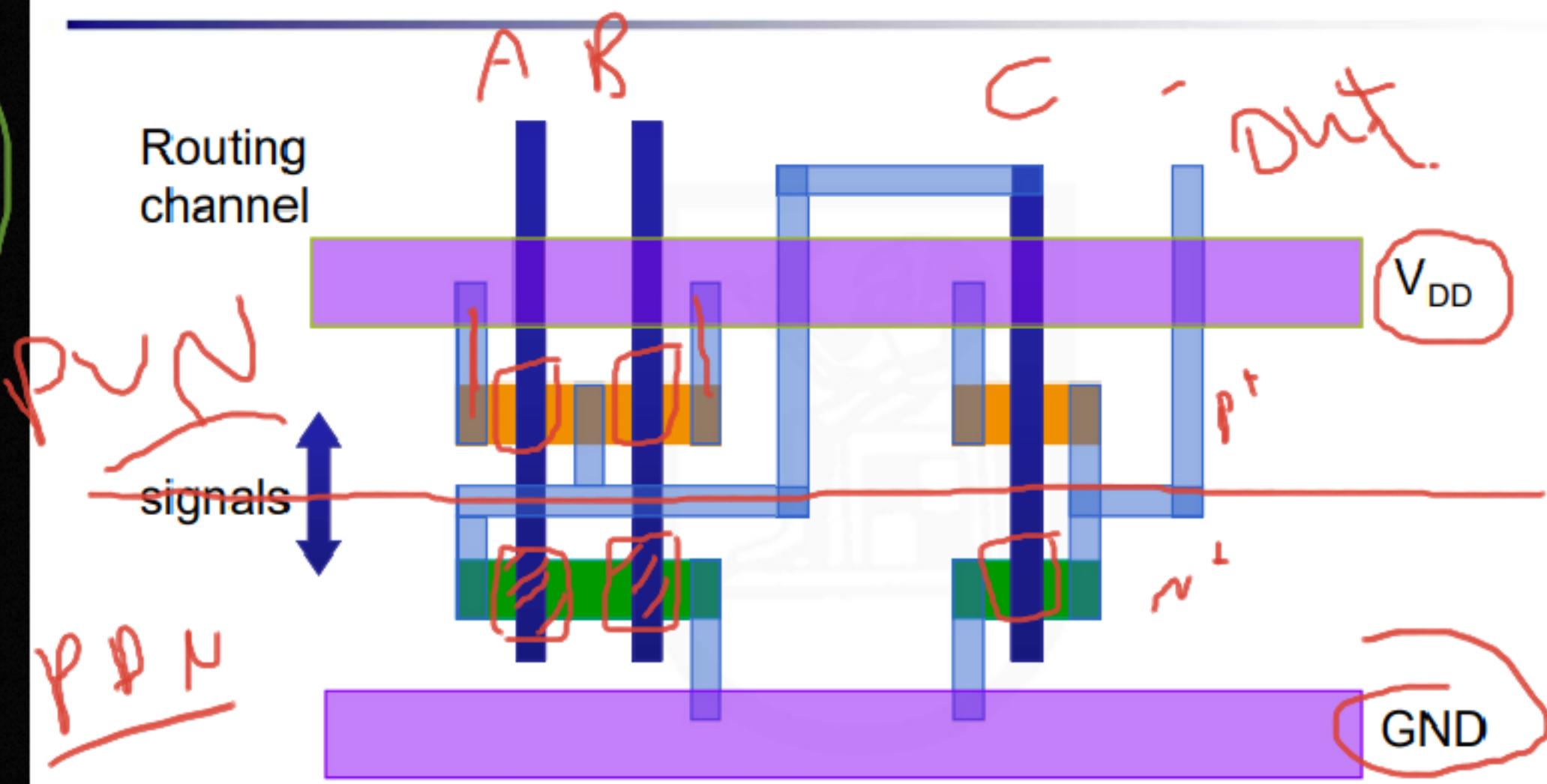


A	B	C	OUT
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



$$\overline{A \cdot B} = A \cdot \overline{B}$$

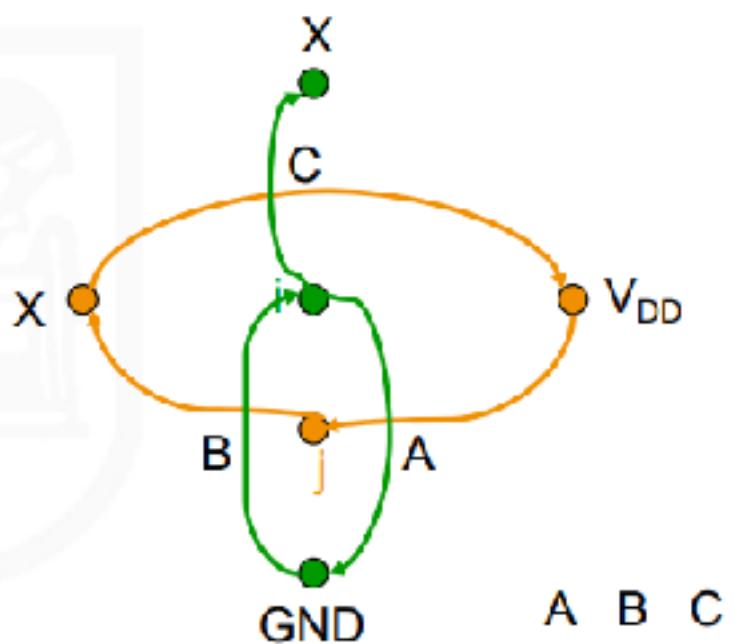
Standard Cell Layout Methodology



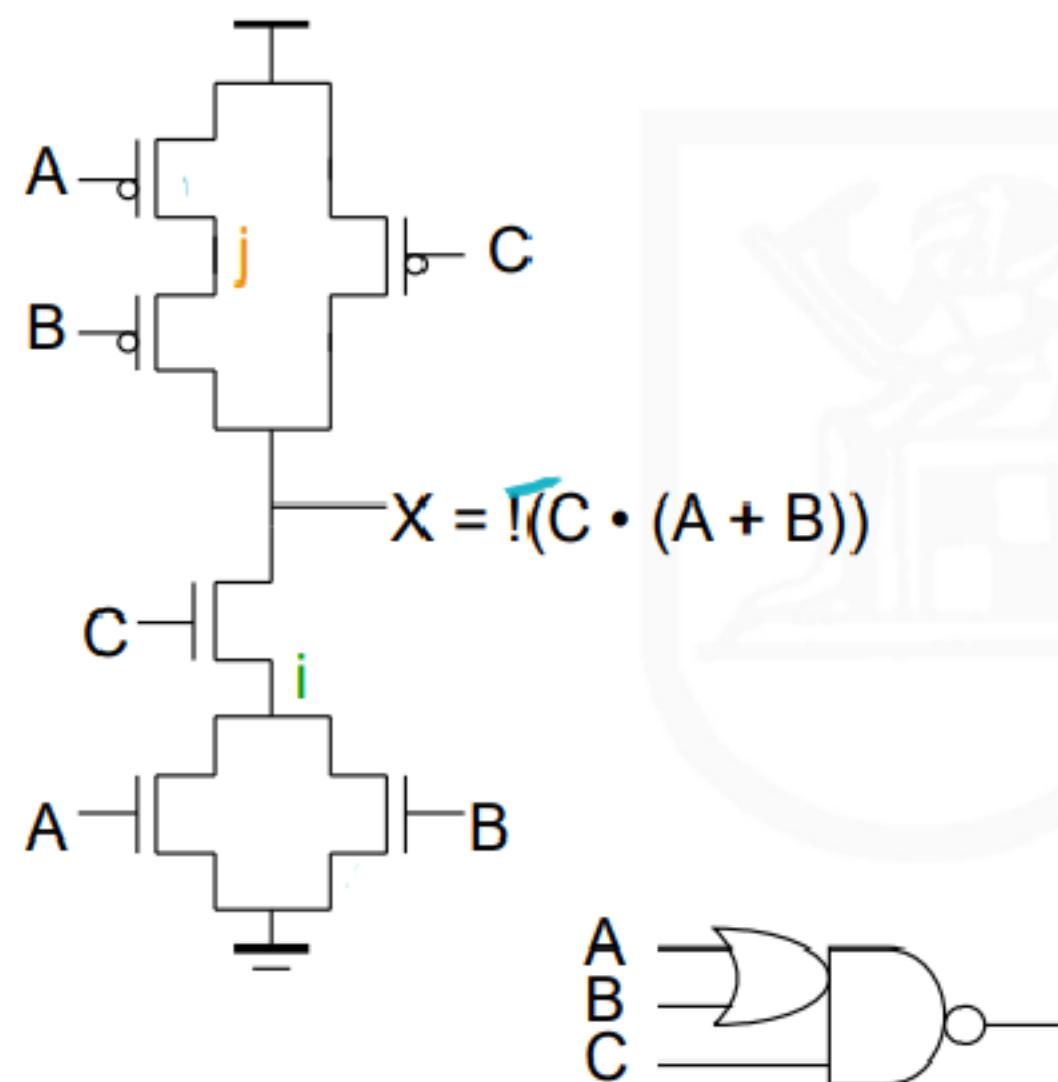
What logic function is this?

Consistent Euler Path

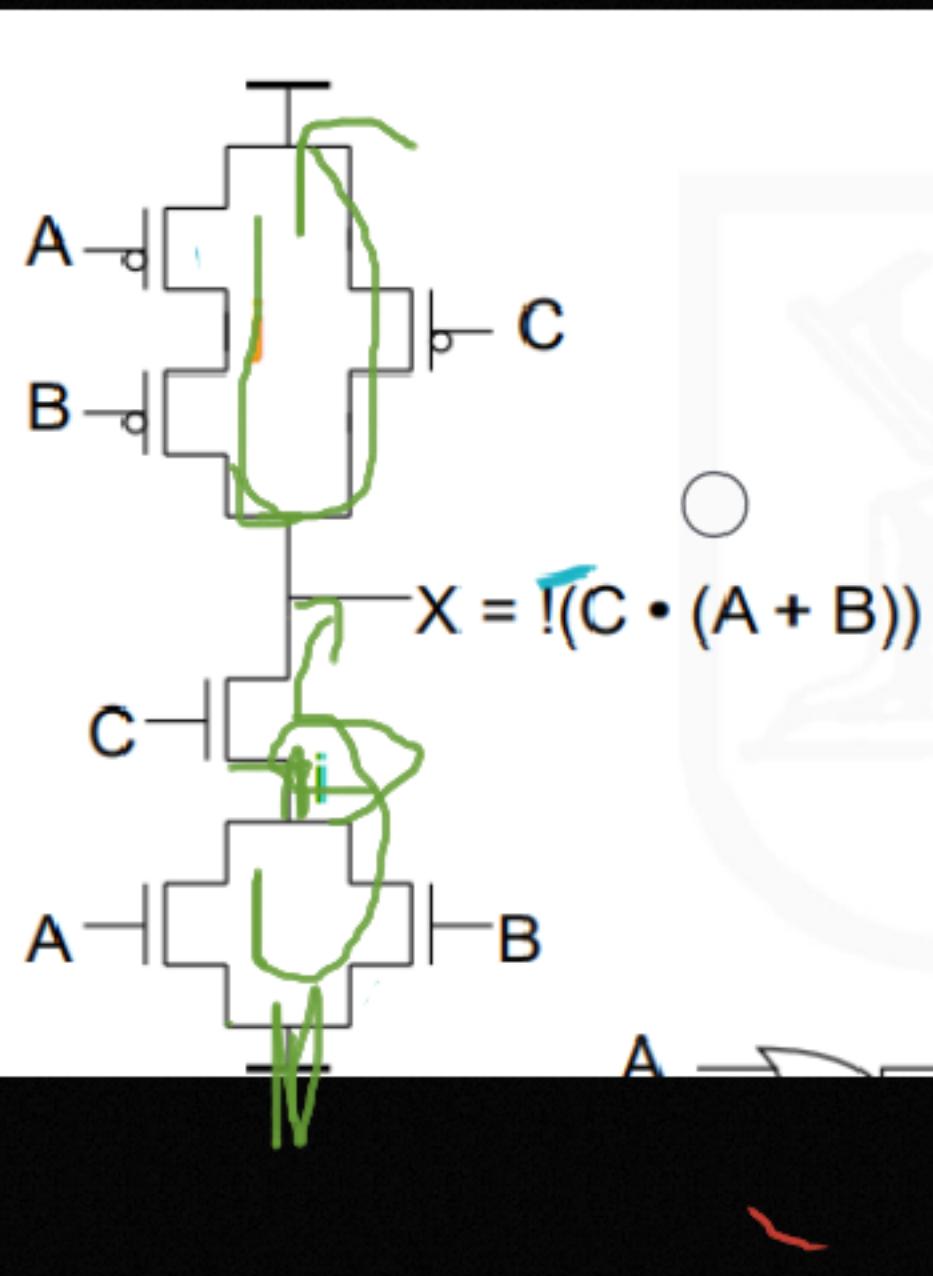
- An uninterrupted diffusion strip is possible only if there exists an Euler path in the logic graph
 - Euler path: a path through all nodes in the graph such that each edge is visited once and only once.
- For a single poly strip for every input signal, the Euler paths in the PUN and PDN must be **consistent** (the same)



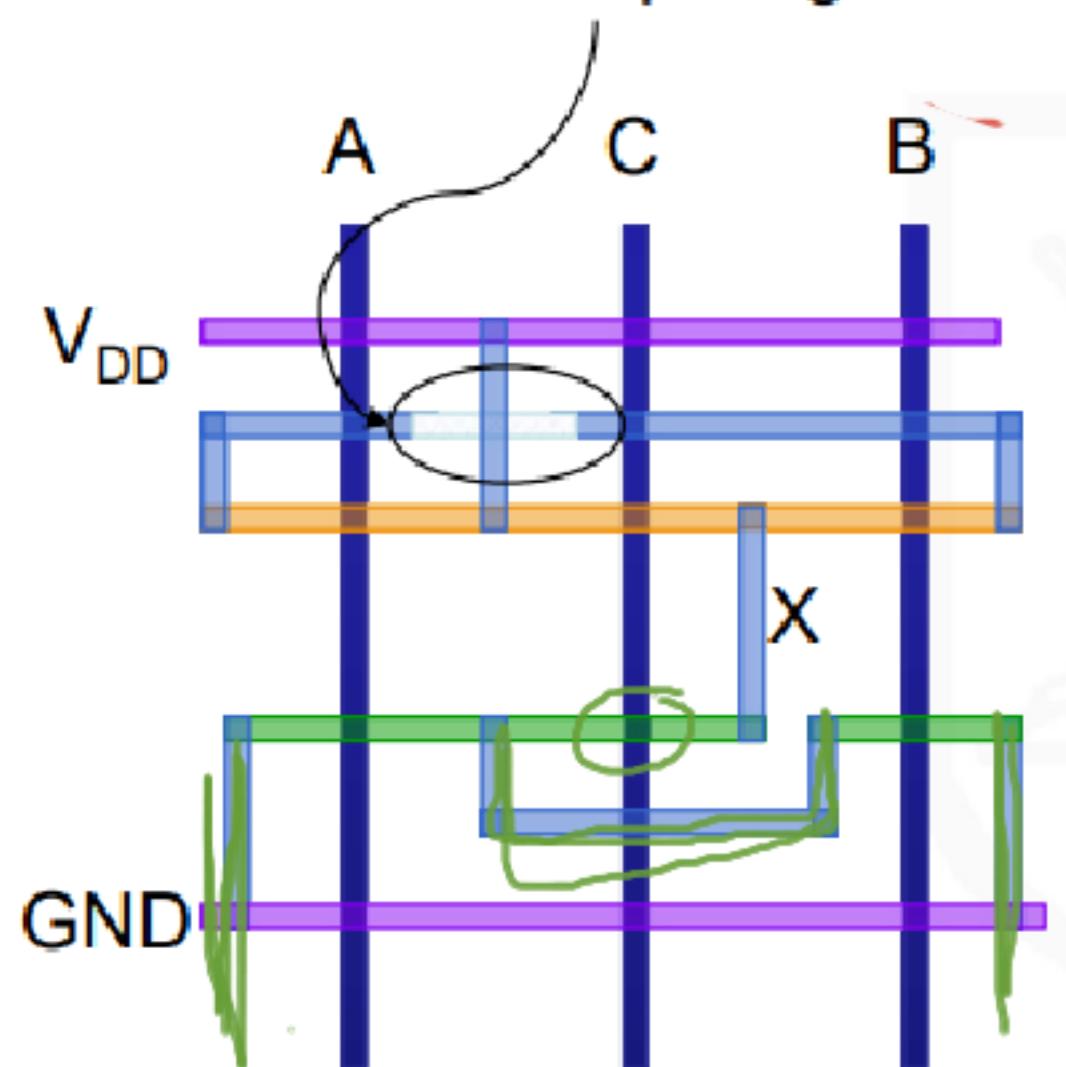
OAI21 Logic Graph



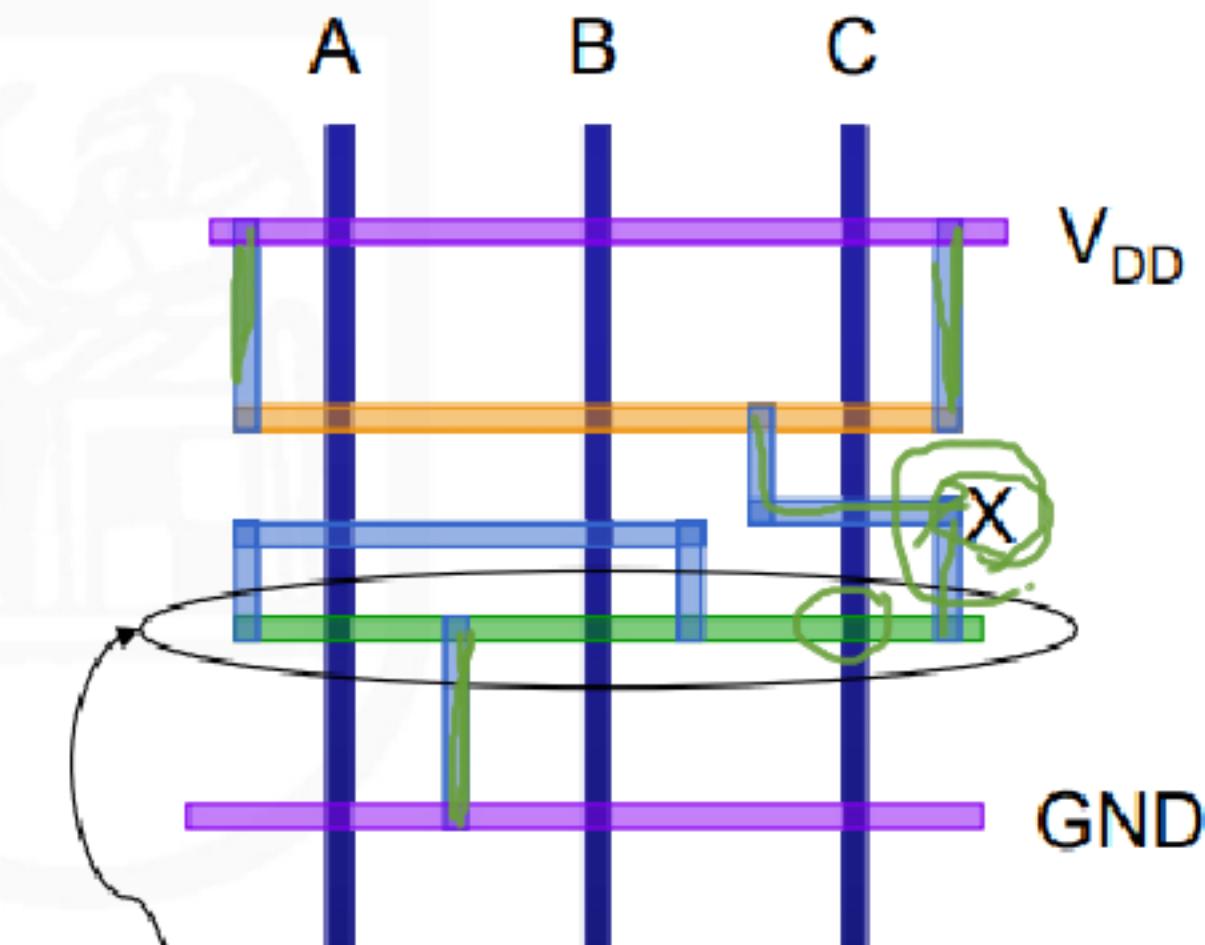
Two Stick Layouts of $!(C \cdot (A + B))$



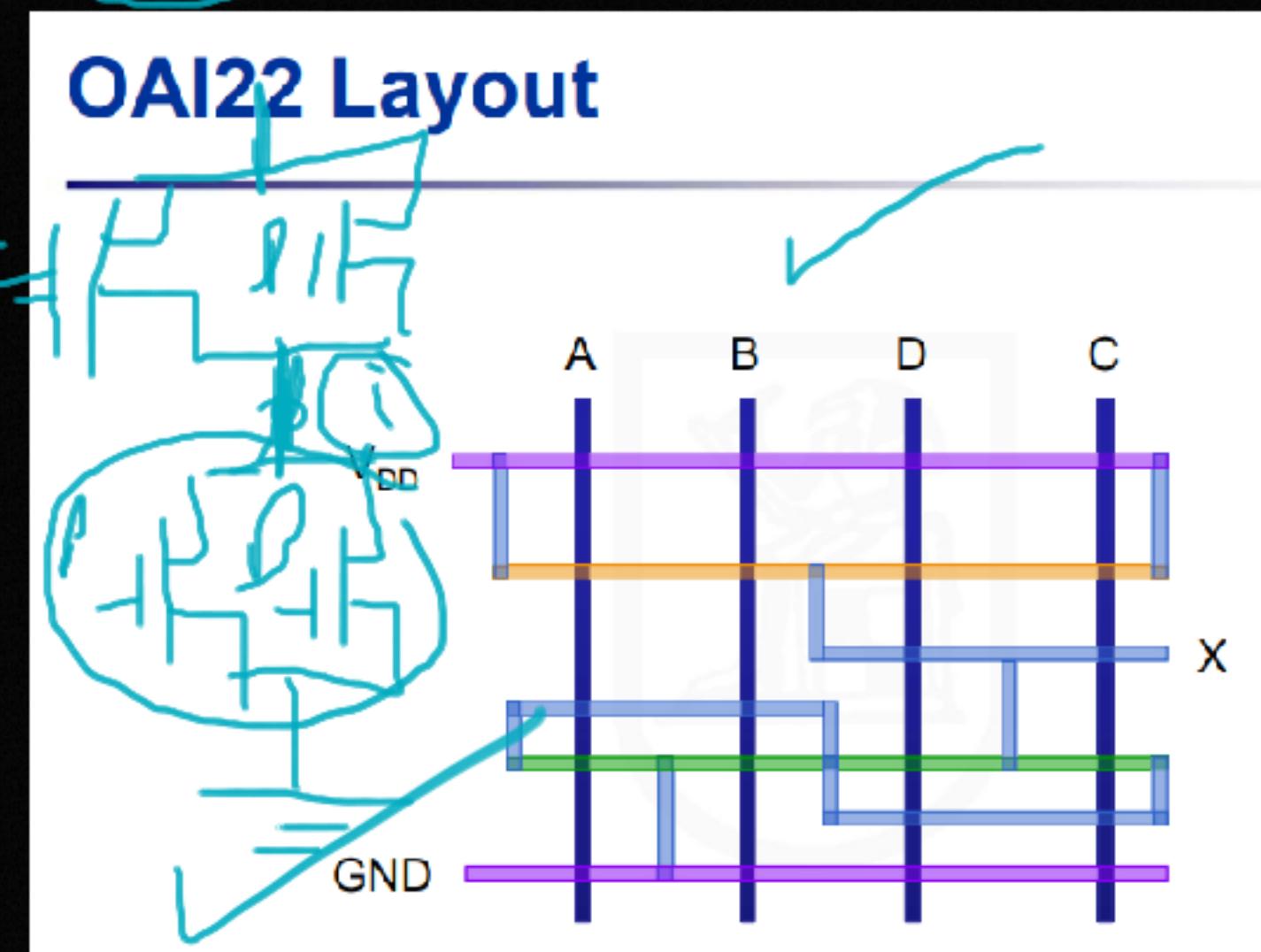
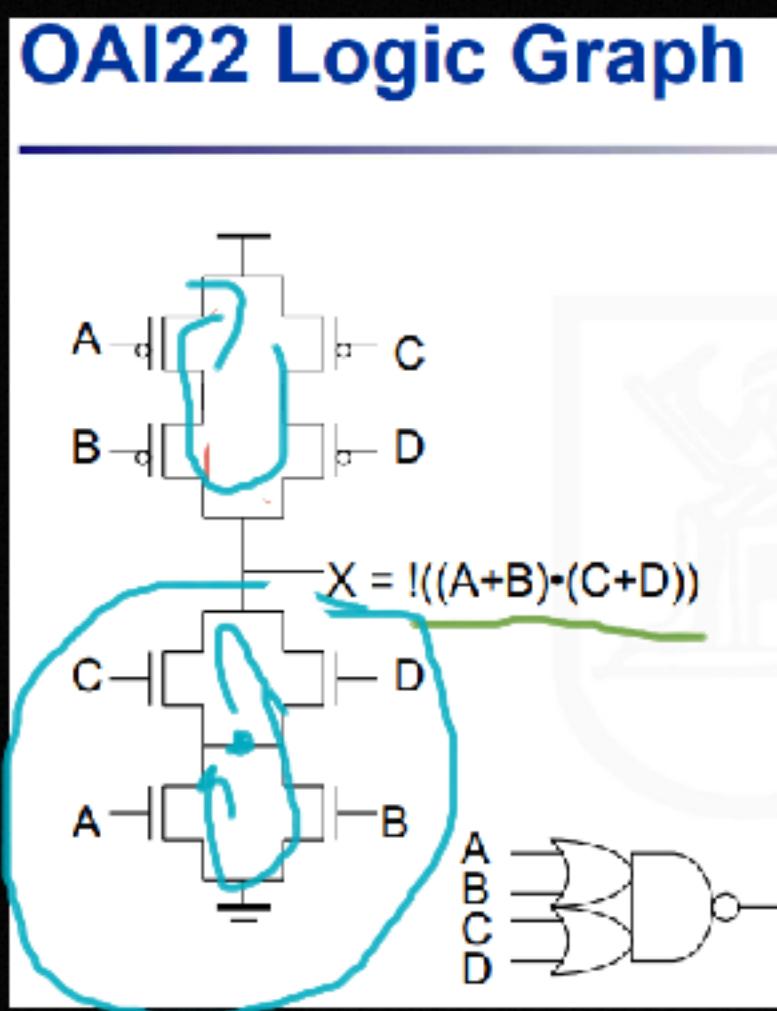
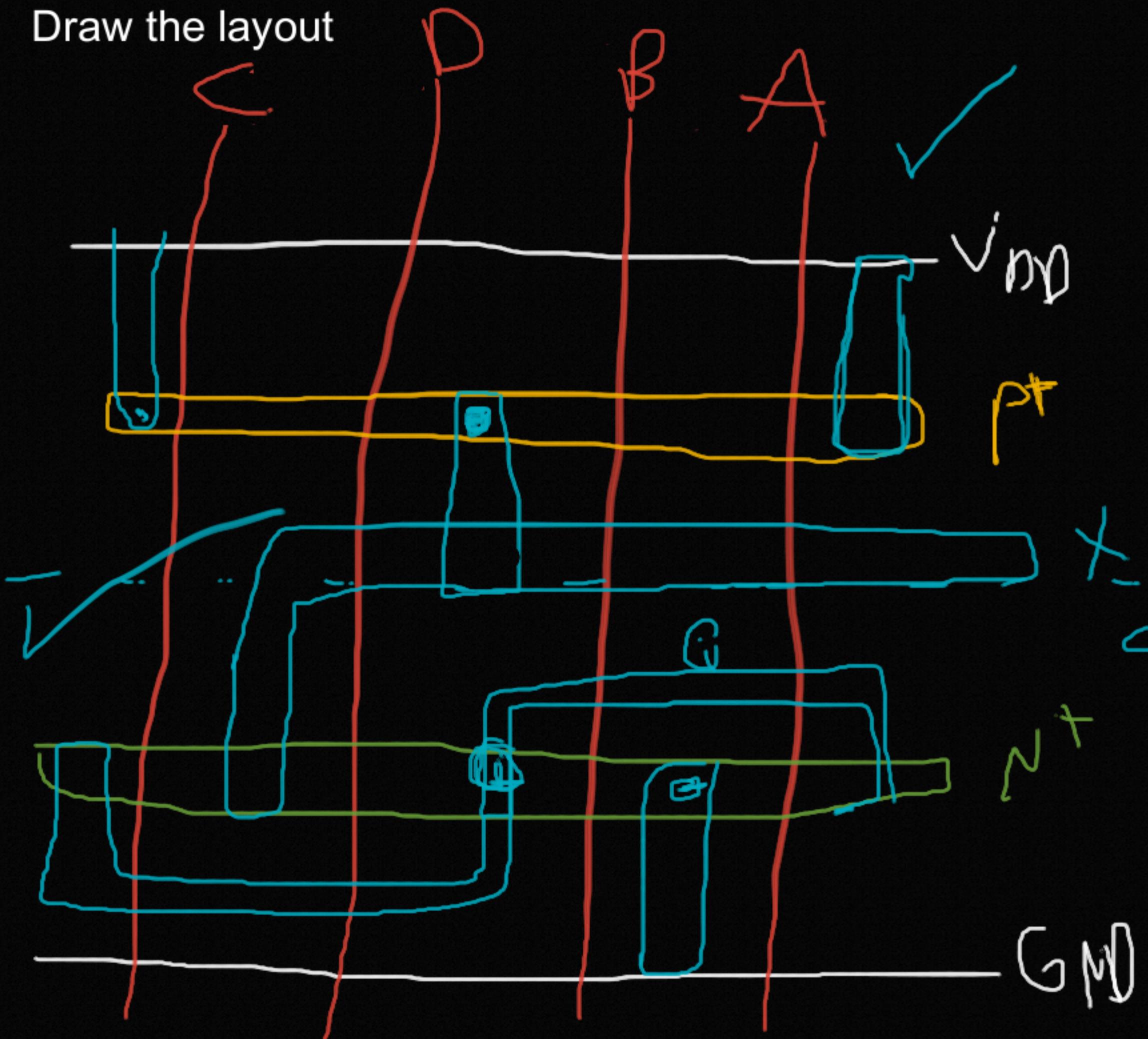
crossover requiring vias

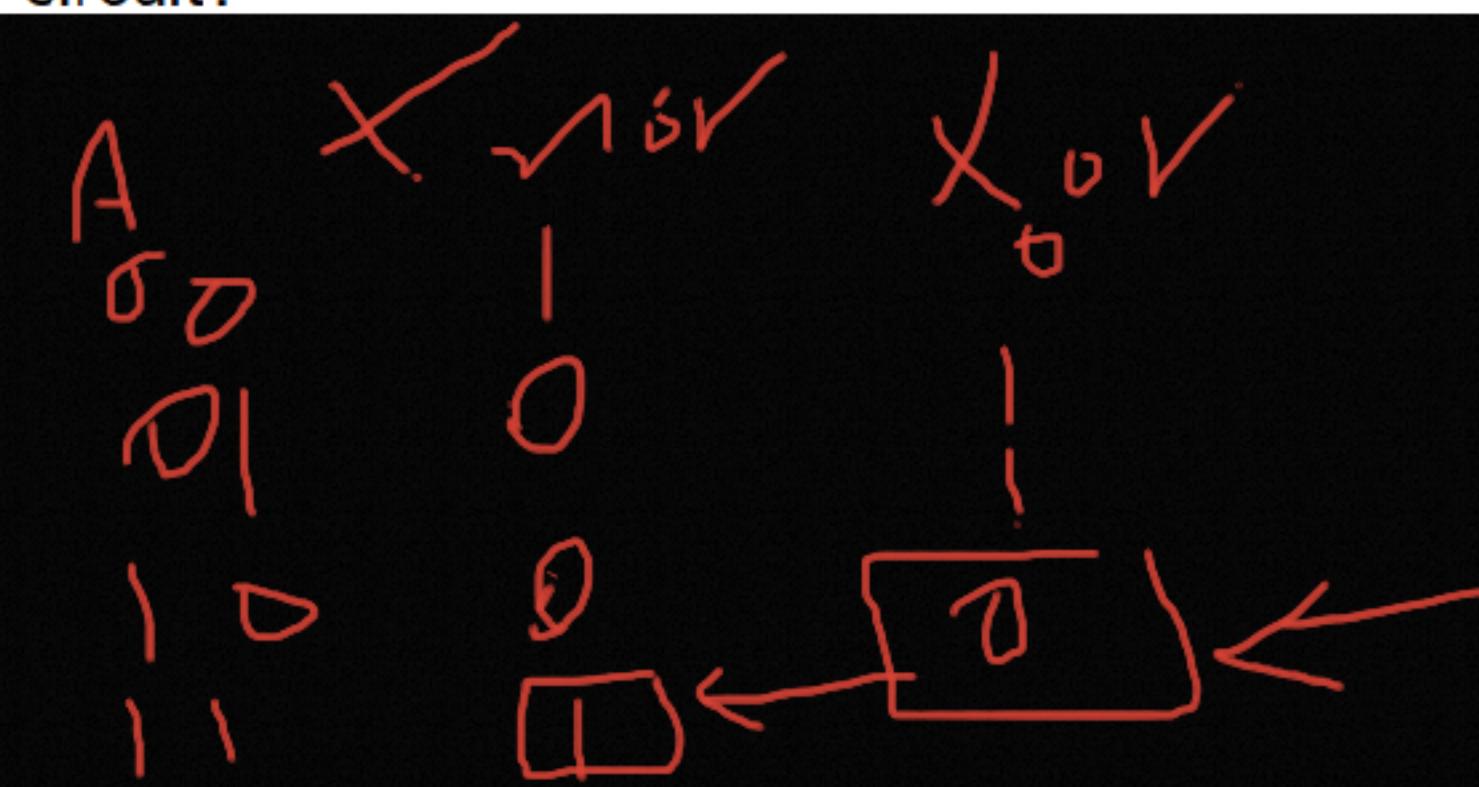
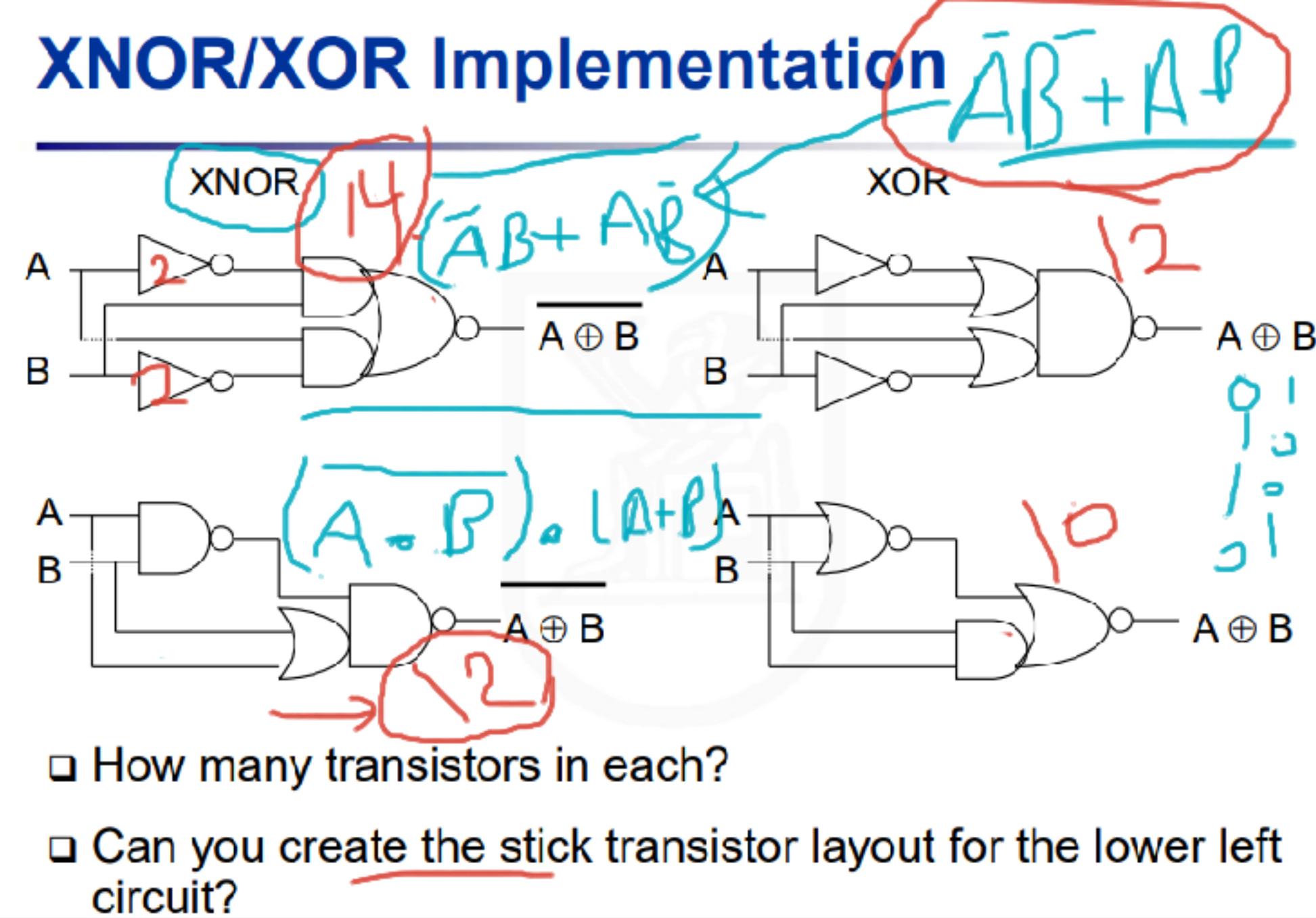
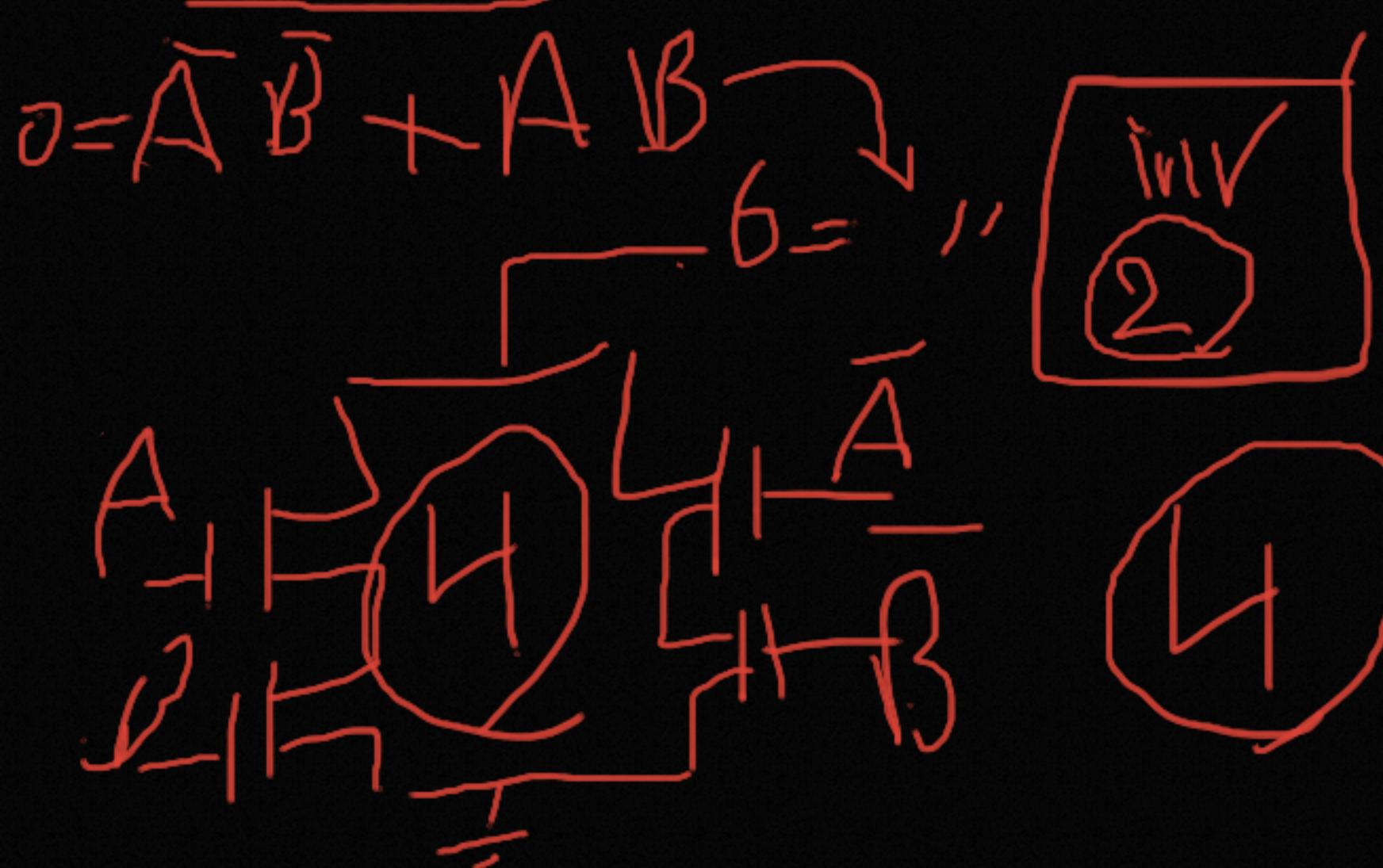


uninterrupted diffusion strip



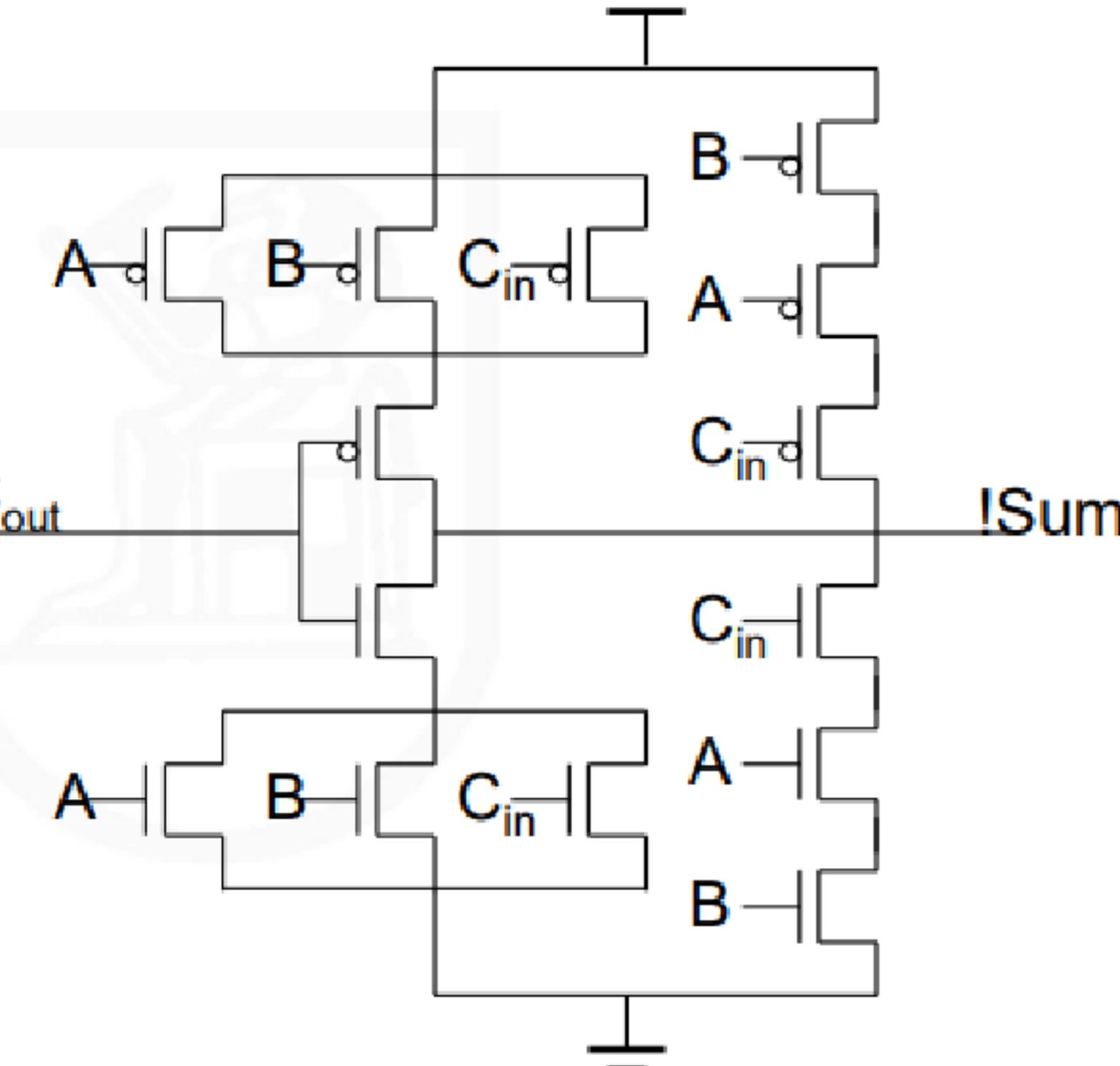
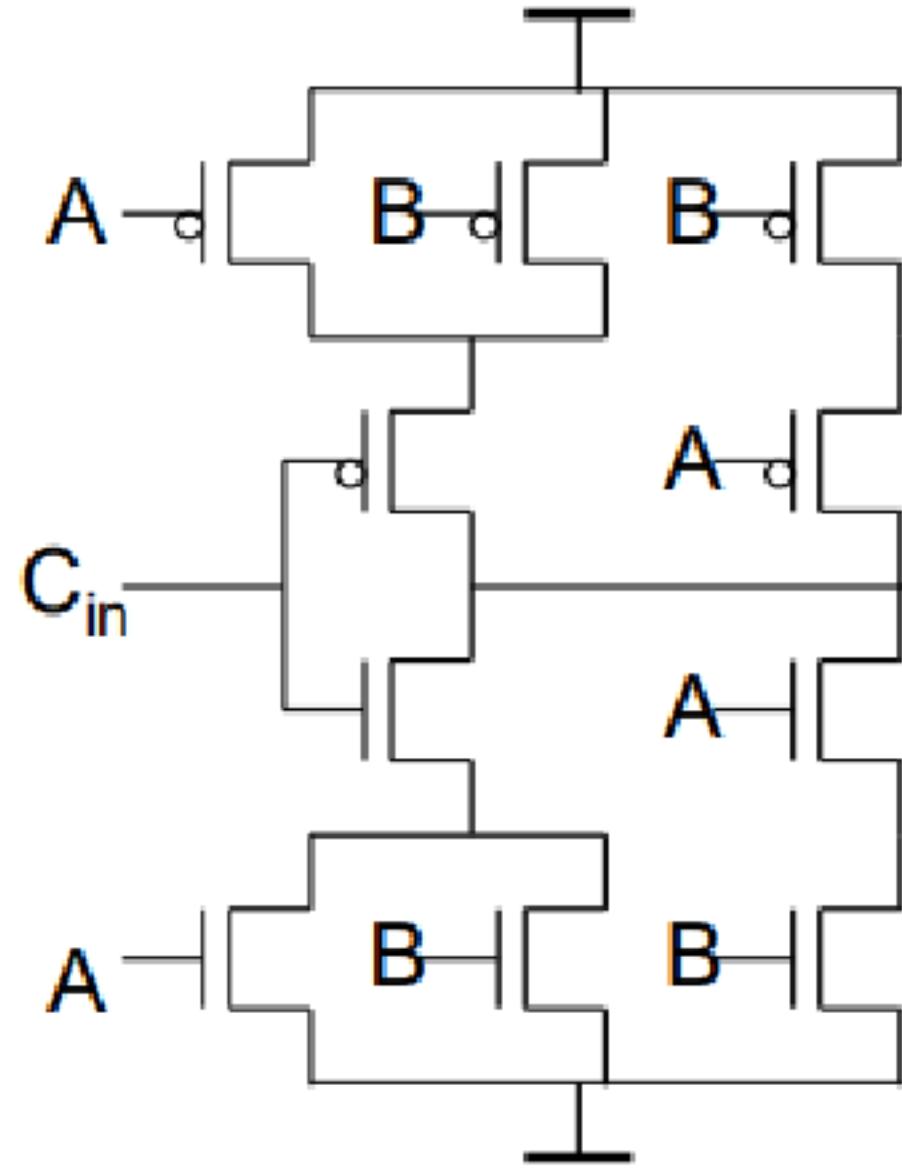
Draw the layout





Static CMOS Full Adder Circuit

$$\overline{C_{out}} = \overline{C_{in}} \& (\overline{A} \mid \overline{B}) \mid (\overline{A} \& \overline{B}) \quad \overline{Sum} = C_{out} \& (\overline{A} \mid \overline{B} \mid \overline{C_{in}}) \mid (\overline{A} \& \overline{B} \& \overline{C_{in}})$$

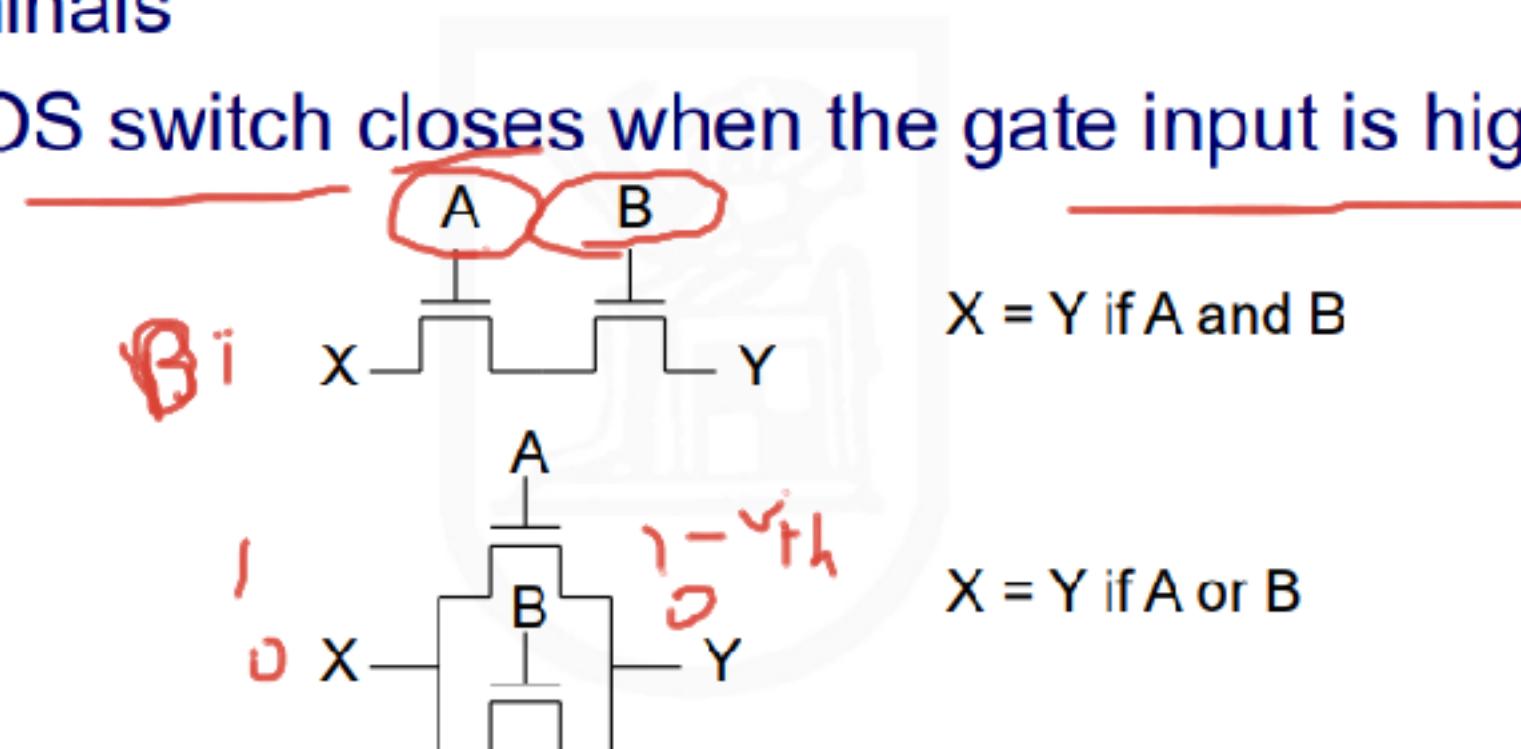


$$C_{out} = C_{in} \& (A \mid B) \mid (A \& B)$$

$$Sum = \overline{C_{out}} \& (A \mid B \mid C_{in}) \mid (A \& B \& C_{in})$$

NMOS Transistors in Series/Parallel

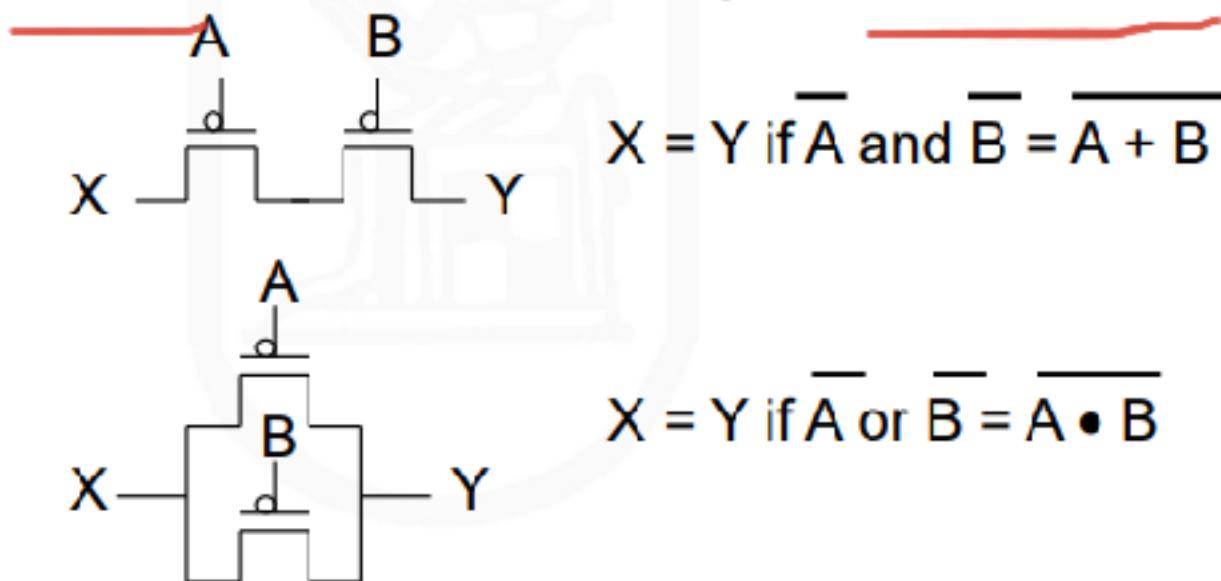
- Primary inputs drive both gate and source/drain terminals
- NMOS switch closes when the gate input is high



- Remember - NMOS transistors pass a strong 0 but a weak 1

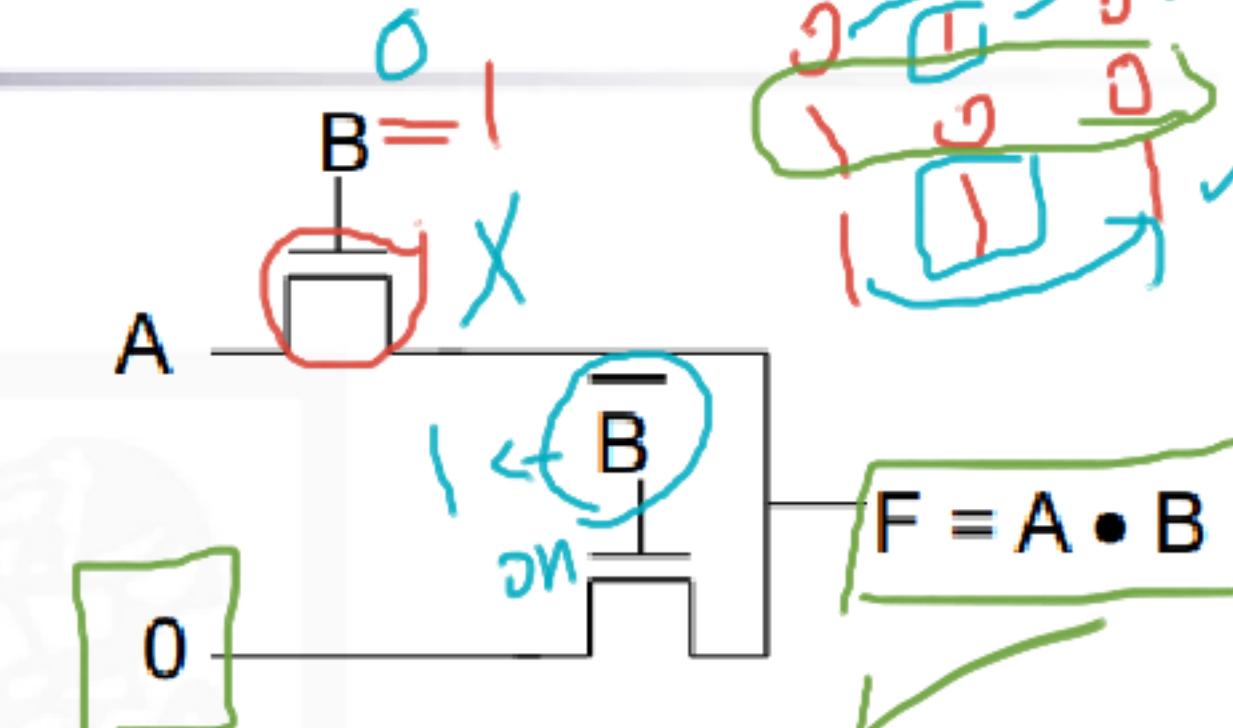
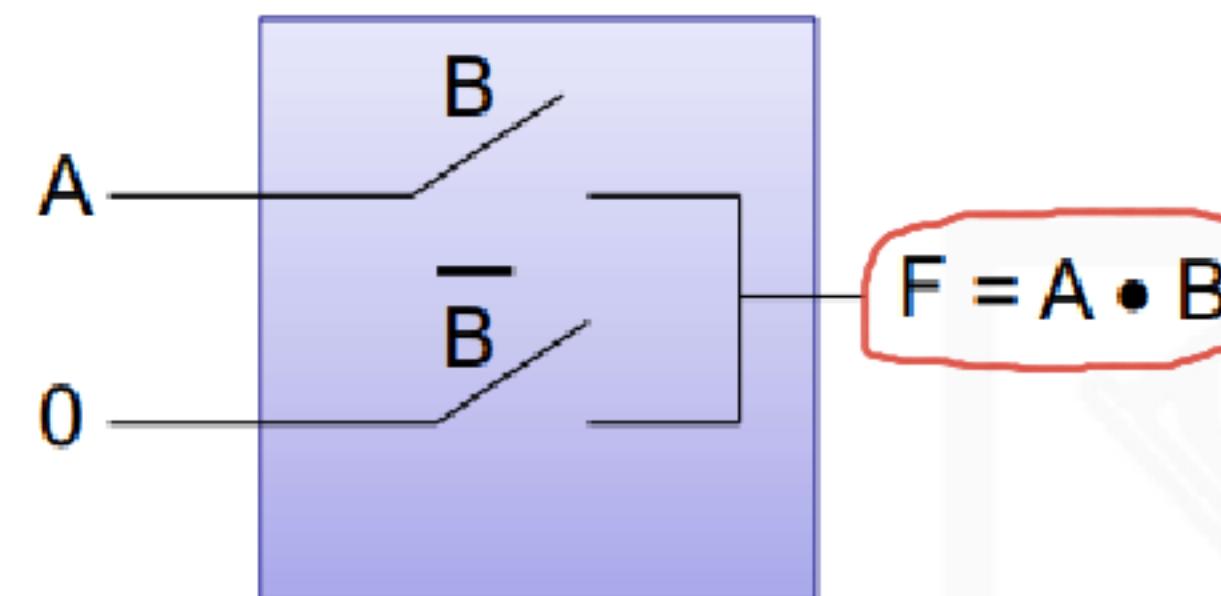
PMOS Transistors in Series/Parallel

- Primary inputs drive both gate and source/drain terminals
- PMOS switch closes when the gate input is low



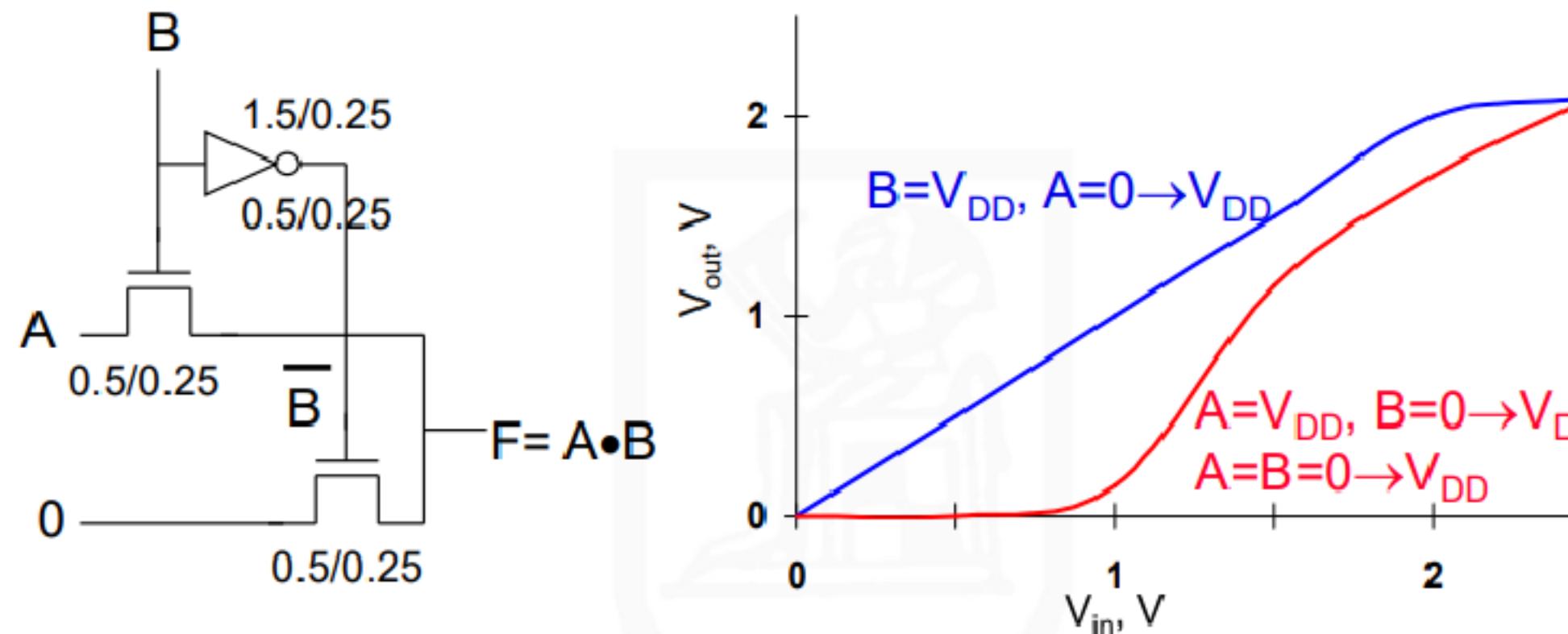
- Remember - PMOS transistors pass a strong 1 but a weak 0

Pass Transistor (PT) Logic



- Gate is static – a low-impedance path exists to both supply rails under all circumstances
 - N transistors instead of 2N
- No static power consumption
- Ratioless W/L
- Bidirectional (versus undirectional)

VTC of PT AND Gate



- Pure PT logic is not regenerative - the signal gradually degrades after passing through a number of PTs (can fix with static CMOS inverter insertion)



Remember

Voltage-Current Relation: Linear Mode

For long-channel devices ($L > 0.25$ micron)

- When $V_{DS} \leq V_{GS} - V_T$

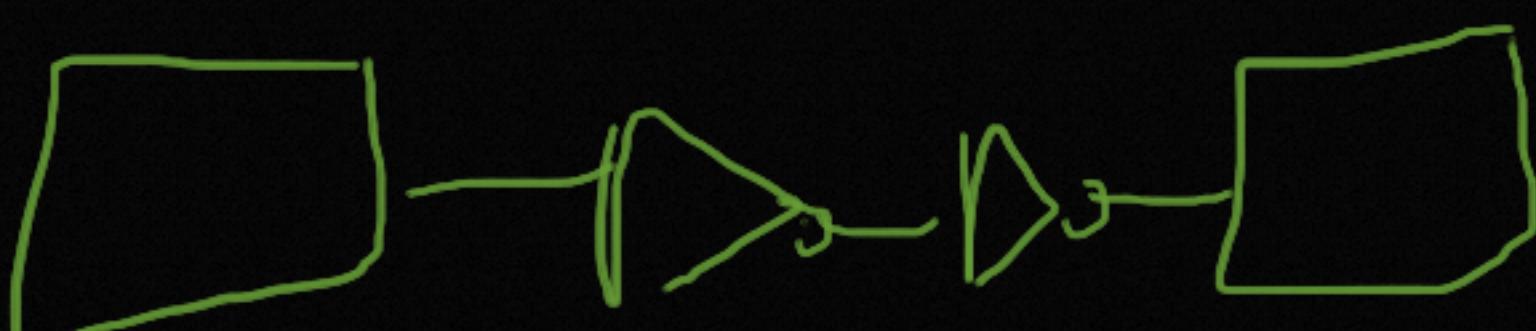
$$I_D = k'_n W/L [(V_{GS} - V_T)V_{DS} - V_{DS}^2/2]$$

where

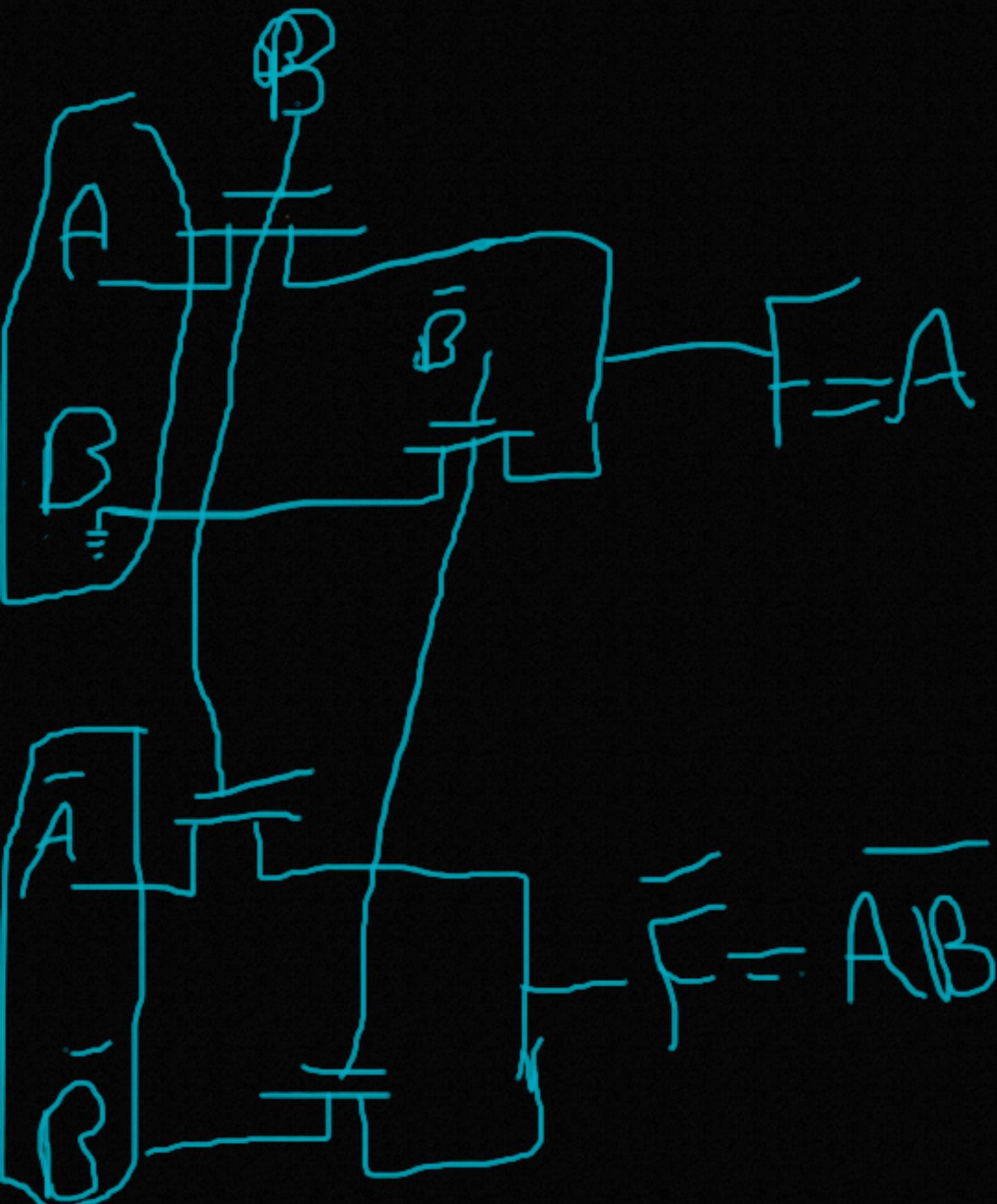
$k'_n = \mu_n C_{ox} = \mu_n \epsilon_{ox}/t_{ox}$ = is the process transconductance parameter (μ_n is the carrier mobility ($m^2/Vsec$))

$k_n = k'_n W/L$ is the gain factor of the device

For small V_{DS} , there is a linear dependence between V_{DS} and I_D , hence the name resistive or **linear** region

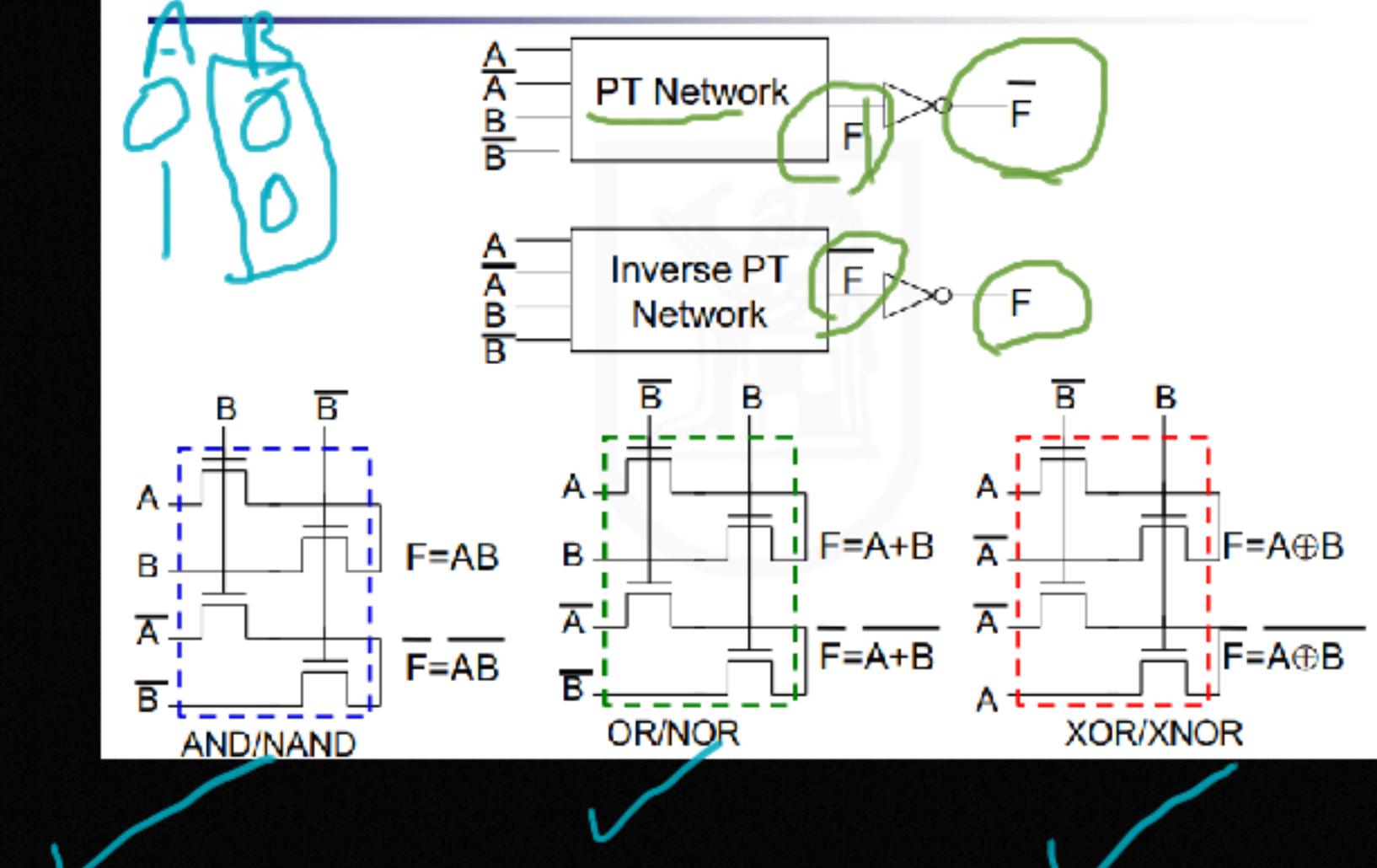


Implement AND/NAND Gates



A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

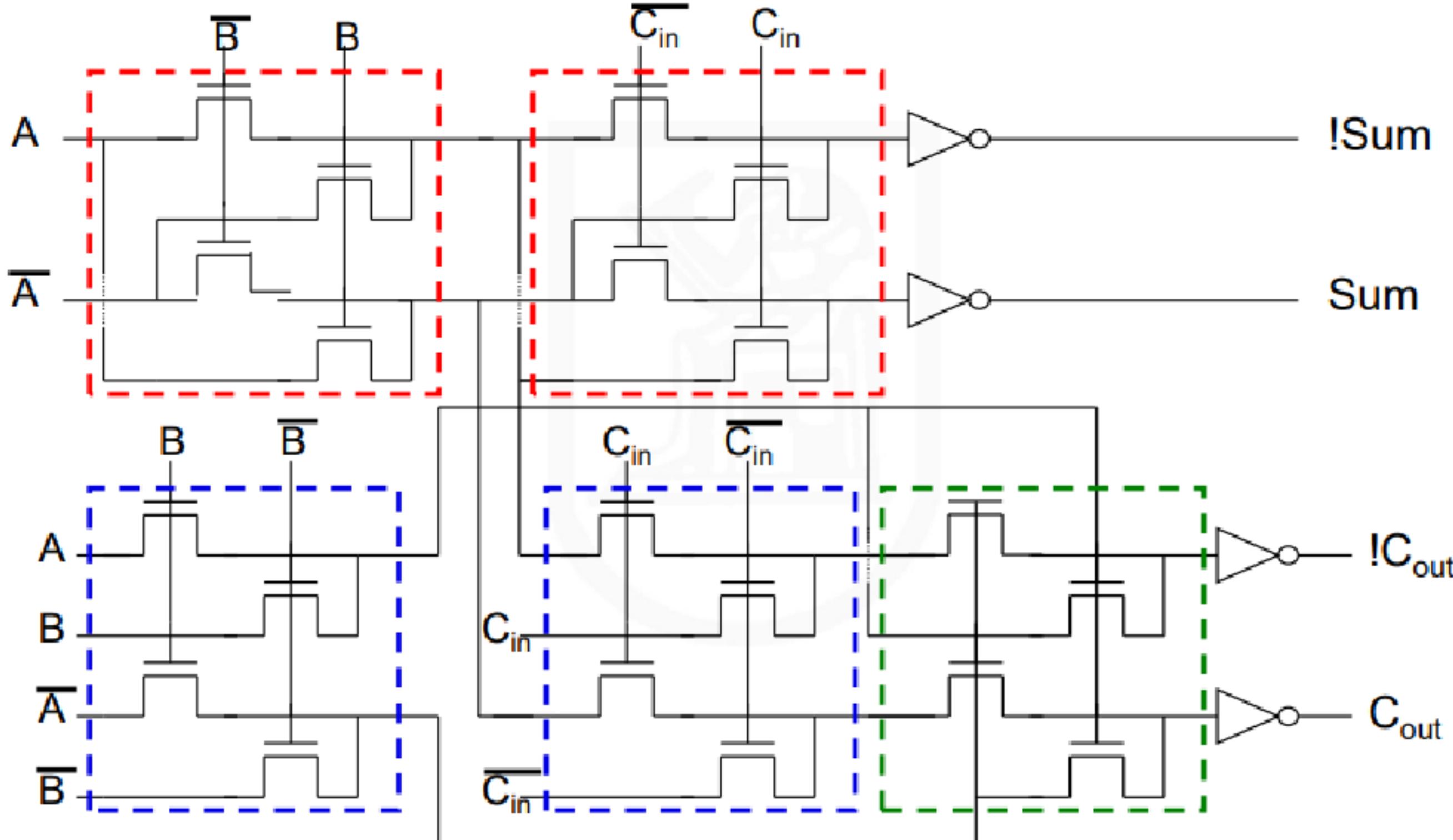
Differential PT Logic (CPL)



CPL Properties

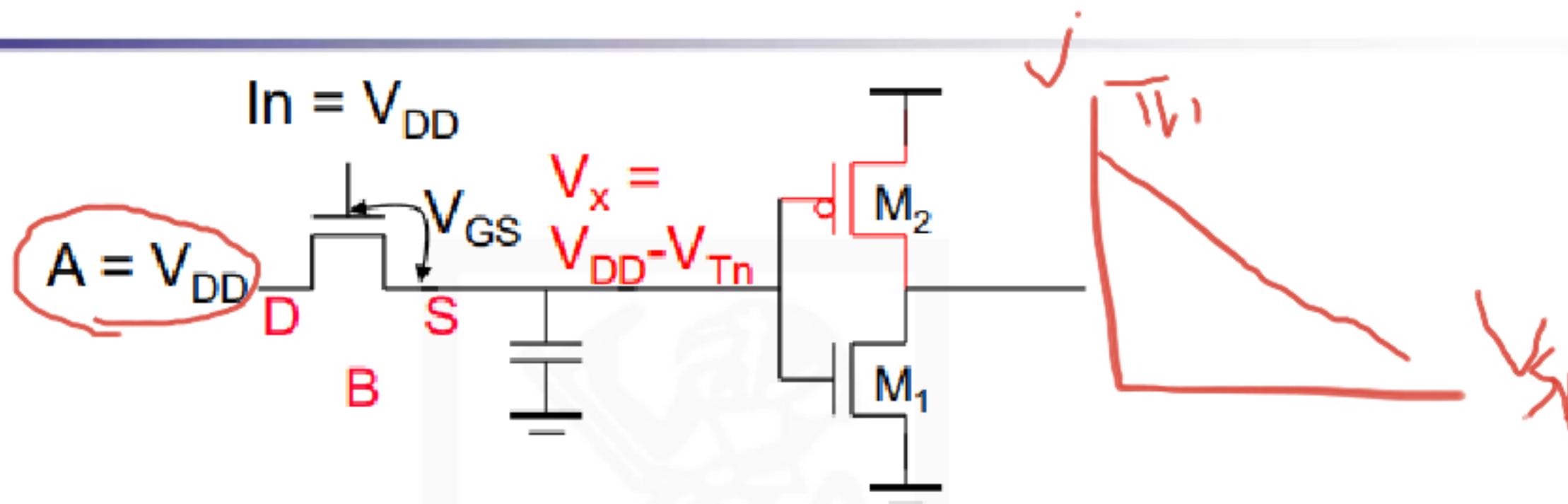
- Differential so complementary data inputs and outputs are always available (so don't need extra inverters)
- Still static, since the output defining nodes are always tied to V_{DD} or GND through a low resistance path
- Design is modular; all gates use the same topology, only the inputs are permuted.
- Simple XOR makes it attractive for structures like adders
- Fast (assuming number of transistors in series is small)
- Additional routing overhead for complementary signals
- Still have static power dissipation problems

CPL Full Adder



Compare between it and Full Adder Using CMOS (Pros and Cons)

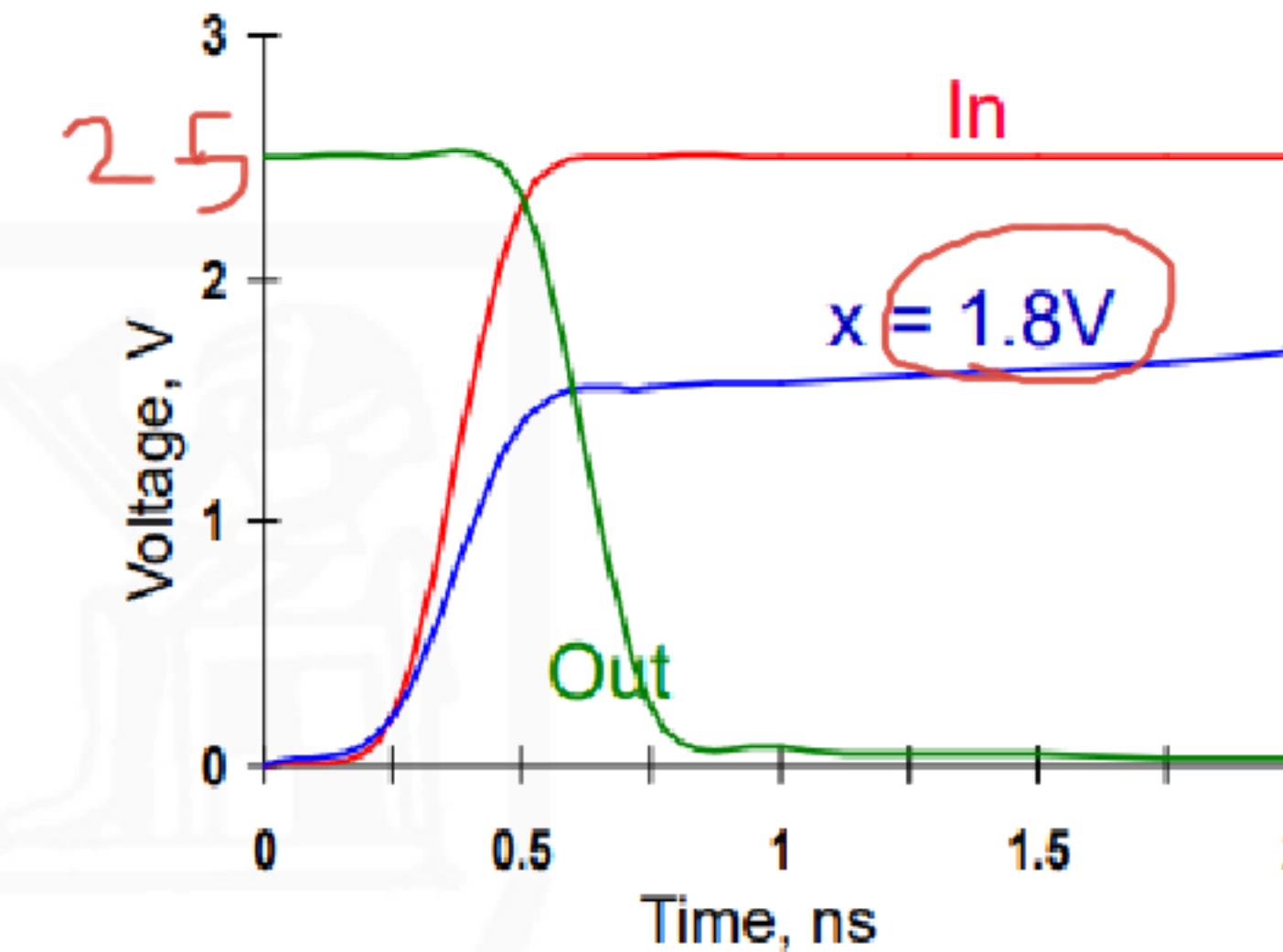
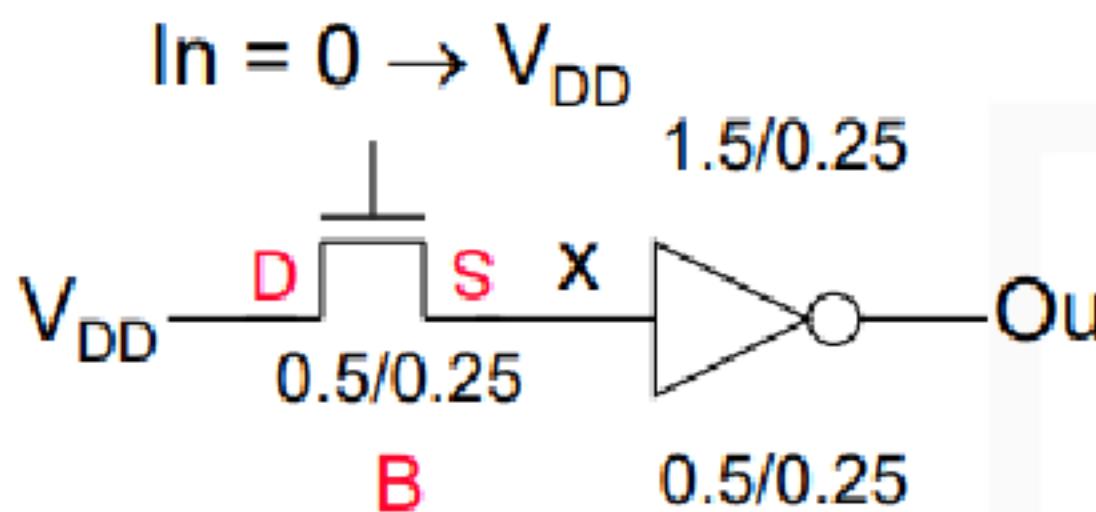
NMOS Only PT Driving an Inverter



- V_x does not pull up to V_{DD} , but $V_{DD} - V_{Tn}$
- Threshold voltage drop causes static power consumption (M_2 may be weakly conducting forming a path from V_{DD} to GND)
- Notice V_{Tn} increases for pass transistor due to body effect (V_{SB})

Voltage Swing of PT Driving an Inverter

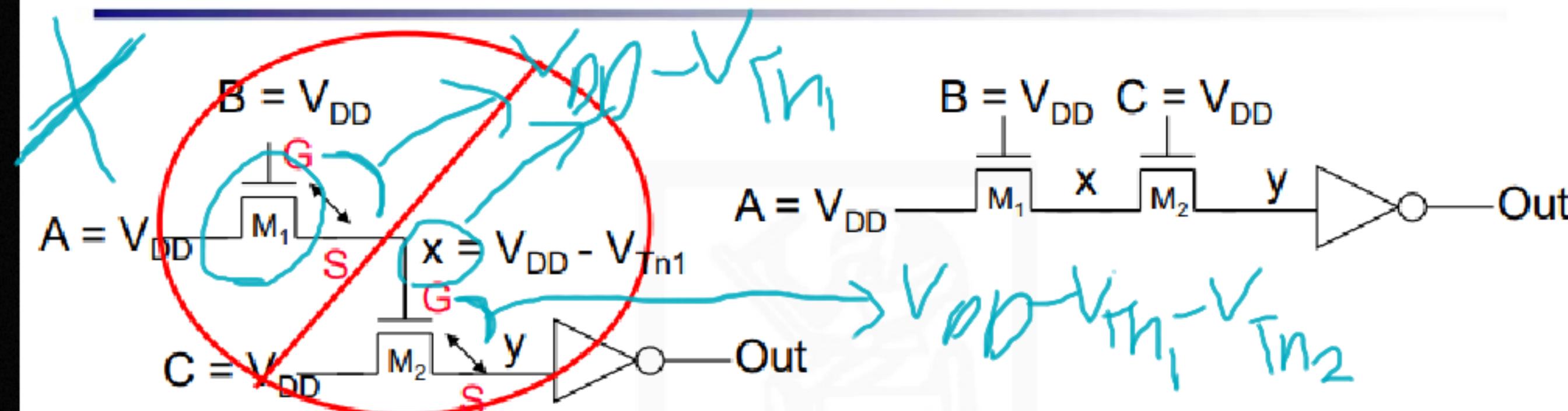
$$\sqrt{T_h} = 0.7V$$



- **Body effect** – large V_{SB} at x - when pulling high (B is tied to GND and S charged up close to V_{DD})
- So the voltage drop is even worse

$$V_x = V_{DD} - (V_{Tn0} + \gamma(\sqrt{|2\phi_f| + V_x}) - \sqrt{|2\phi_f|})$$

Cascaded NMOS Only PTs



Swing on $y = V_{DD} - V_{Th1} - V_{Th2}$

Swing on $y = V_{DD} - V_{Th1}$

- Pass transistor gates should never be cascaded as on the left
- Logic on the right suffers from static power dissipation and reduced noise margins