Exercise 5: State Machines

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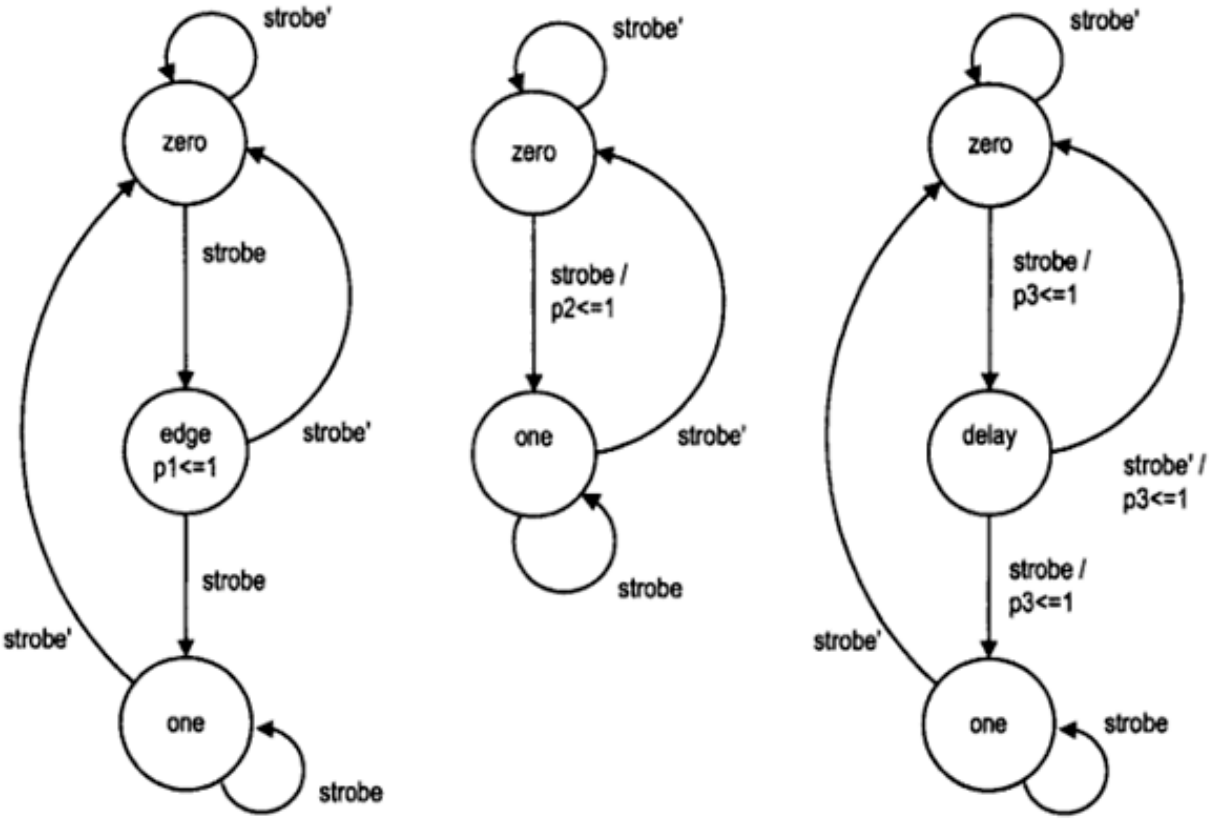
1 Edge detectors

Given the state diagrams depicted in the figure (and the entity in `edge_detector.vhd`):




```
entity edge_detector is
  port (
    rst    : in  std_logic;
    clk    : in  std_logic;
    strobe : in  std_logic;
    p1     : out std_logic;
    p2     : out std_logic;
    p3     : out std_logic);
end entity edge_detector;
```

- What is the task of every state machine?
- Which outputs are Mealy and which ones are Moore? Why?

- Describe the state machines in VHDL.
- Write a suitable testbench and simulate them.

2 Safe controller

You are hired to design a state machine for a safe. The owner of the safe wants the safe to be unlcoked only when the *right* sequence of bits is given. `psw` is the input and it is a one-bit signal synchronous with the clock. The output (`unlock`) is asserted for one clock cycle when the sequence 1,1,0,1,0 is encountered. The entity is in `unlocker.vhd`. If the design requirements are unclear, make reasonable assumptions!

```
entity unlocker is
  port (
    rst    : in  std_logic;
    clk    : in  std_logic;
    psw    : in  std_logic;
    unlock : out std_logic);
end entity unlocker;
```

- Draw the state diagram.
- Describe the machine in VHDL.
- Write a suitable testbench and simulate it.