VILNIAUS UNIVERSITETAS

MATEMATIKOS IR INFORMATIKOS FAKULTETAS

INFORMATIKOS STUDIJŲ PROGRAMA

Report

Comparison of two computer achitectures

Motorola 68HC11 vs. Intel i960

Karina Babenskaitė

ELEMENTARY BASE OF THE PROCESSOR

Intel i960
The Intel i960 is fabricated using CMOS technology and belongs to the Very Large Scale Integration (VLSI) category.

Motorola 68HC11
The Motorola 68HC11 is based on CMOS technology, which uses transistors fabricated as integrated circuits (ICs). It is categorized as a Large Scale Integration (LSI) device. The integration includes the CPU, RAM, ROM, EEPROM, and I/O peripherals on a single chip.

PHYSICAL CHARACTERISTICS

Intel i960
Typically available in advanced package types like HL-PBGA (High Lead Plastic Ball Grid Array), which are compact. For example, the encapsulant size is 22.38 mm x 22.38 mm, with a height of approximately 1.54 mm. It is designed to operate at 3.3V, with efficient power usage depending on workload. The processor includes features for power management.

Motorola 68HC11
Available in various package types such as PLCC (Plastic-Leaded Chip Carrier), DIP (Dual In-line Package), and QFP (Quad Flat Pack). These packages are small and light, typically weighing a few grams and measuring a few centimeters on each side. Operates on a 5V supply with low power consumption, typically drawing a few milliamps, depending on the operating mode.

ARCHITECTURE TYPE

Intel i960
The Intel i960 family is based on a RISC (Reduced Instruction Set Computer) architecture. This makes the i960 fundamentally a register-based architecture.

Motorola 68HC11
The Motorola 68HC11 microcontroller lineage is built upon the earlier 6800 architecture. This family is primarily accumulator-based.

ADDRESSING

Intel i960
Three-address machine, supporting instructions that specify two source operands and one destination operand explicitly, typical of RISC architectures.

Motorola 68HC11
One-address machine, with instructions typically involving one explicit operand and an implicit accumulator as the other operand and destination.

REGISTERS

Intel i960

Intel i960 includes a significant number of registers: general-purpose registers as well as specialized registers for certain functions.

Number of Registers:

- Global Registers: 16 registers
- Local Registers: 16 registers
- Control Registers: A set of specialized registers for system control, interrupt handling, and processor configuration.
- Total: 32 general-purpose registers plus several specialized control registers.

Register Widths:

All general-purpose registers are 32-bit wide. Specialized control registers vary in width but are typically 32-bit to match the processor's word size.

Motorola 68HC11

Motorola 68HC11 has registers as part of its Central Processor Unit (CPU). The architecture primarily features specialized registers, although a few have some general-purpose functionality depending on the context.

Number of Registers:

- Accumulators: A and B
- Index Registers: X and Y
- Stack Pointer (SP)
- Program Counter (PC)
- Condition Code Register (CCR), used for status flags.
- Total: 6 primary registers and one condition code register.

Register Widths:

- Accumulators: 8-bit
- Index Registers: 16-bit
- Stack Pointer: 16-bit
- Program Counter: 16-bit
- Condition Code Register: 8-bit

FLAGS

Intel i960

The Intel i960 uses memory-mapped control registers to check and manage status and conditions.

Flags:

- Fault Status Flags
- Debugging and Trace Flags
- Register State Flags

Motorola 68HC11

Motorola 68HC11 architecture includes a Condition Code Register (CCR), which contains several flags used for arithmetic, logical, and control operations**.**

Flags:

- C (Carry/Borrow): Indicates a carry out of the most significant bit in addition or a borrow in subtraction.
- V (Overflow): Indicates an arithmetic overflow.
- Z (Zero): Indicates if the result of an operation is zero.
- N (Negative): Indicates if the result of an operation is negative (most significant bit is 1).
- H (Half Carry): Used for BCD (Binary-Coded Decimal) arithmetic operations.
- I (Interrupt Mask): Masks interrupts when set.
- X (External Interrupt Mask): Masks non-maskable interrupts when set.
- S (Stop Disable): Used for controlling low-power modes.

DATA WIDTH

Intel i960
The machine word size for Intel i960 is 32 bits

Motorola 68HC11
The machine word size for Motorola 68HC11 is 8 bits, though it can handle 16-bit addresses and some 16-bit operations.

MEMORY LAYOUT

Intel i960
The i960 architecture features a 32-bit flat memory space. Address width is 32 bits. The total addressable memory is 4 GB.

Typical memory configuration:

- On-chip caches (4 KB instruction cache, 2 KB data cache).
- Integrated 1 KB data RAM.

Motorola 68HC11
Uses a flat, continuous address space of 64 KB. Address width is 16 bits. The total addressable memory is 64 KB.

Typical memory configuration:

- 768 bytes of RAM
- 12 KB of ROM/EPROM
- 512 bytes of EEPROM

VIRTUAL MEMORY

Intel i960
Intel i960 supports a memory model that can integrate with virtual memory systems. This capability is evident from its address translation units (ATUs), which allow mapping between local processor memory and external PCI address spaces.

The memory is segmented when addressing private processor memory, PCI addressable memory, or a combination of the two. The memory controller and ATUs manage these mappings, enabling flexibility in how memory is allocated and accessed.

Motorola 68HC11
Motorola 68HC11 did not support virtual memory. Its memory model is based on a simple flat, continuous address space of 64 KB, shared between on-chip resources (RAM, ROM/EPROM, EEPROM, I/O) and external memory if used in expanded mode.

The memory was not paged or segmented. However, some parts of the memory map could be relocated (e.g., RAM and register blocks could be positioned at different locations in the address space using configuration registers).

ISA TYPE

Intel i960
The Intel i960 is a RISC (Reduced Instruction Set Computer) architecture, emphasizing high-speed execution with fewer, simpler instructions.

Motorola 68HC11
The Motorola 68HC11 is based on a CISC (Complex Instruction Set Computer) architecture. It supports a rich set of instructions with multiple addressing modes.

NUMBER OF INSTRUCTIONS

Intel i960
The instruction set includes approximately 80 instructions, categorized into key operations like arithmetic, logical, data movement, and control.

Motorola 68HC11
The instruction set includes over 200 instructions, covering various operations like data movement, arithmetic, logic, branching, and control.

CLASSES OF INSTRUCTIONS

Intel i960

- Data Movement: Load, Store, Move.
- Arithmetic: Add, Subtract, Multiply, Divide.
- Logical: AND, OR, XOR, Shift.
- Control: Branch, Call, Return.
- System Control: Cache Control, Interrupt Management.

Motorola 68HC11

- Data Transfer: Load, Store, Transfer.
- Arithmetic: Add, Subtract, Multiply, Divide.
- Logic: AND, OR, NOT, XOR.
- Branching: Conditional and Unconditional Branch, Subroutine Call/Return.
- Control: Interrupt, Stop, Wait.

INSTRUCTION FORMATS

Intel i960

Most instructions are fixed-length (32 bits), with fields for opcode, registers, and immediate values. Supports register-to-register, immediate, and memory addressing modes.

Motorola 68HC11

Supports six addressing modes: immediate, direct, extended, indexed, inherent, relative. Instruction length varies between 1 to 5 bytes depending on the addressing mode and operands.

INSTRUCTION EXAMPLES

Intel i960

- ADD r1, r2, r3
- LOAD r1, [address]
- STORE r1, [address]
- JUMP [address]
- COMPARE r1, r2
- CALL [address]

Motorola 68HC11

- LDAA #value
- STAB $address
- ADDA $address
- JMP $address
- BNE $offset
- TSTA

Similar Instructions
Both architectures include basic instructions for data movement (LOAD/STAA), arithmetic (ADD, SUB), and control (JUMP/CALL).

Different Instructions
Motorola 68HC11 supports more diverse and complex addressing modes typical of CISC architectures.Intel i960 focuses on simpler instructions with fewer cycles, optimized for RISC performance. The i960's instruction set is smaller and highly optimized for compiler efficiency.

ADDRESSING MODES

Intel i960

- Immediate: The operand is directly in the instruction.
- Direct: The low byte of the address is specified, and the high byte is assumed to be $00.
- Extended: The full 16-bit address is specified in the instruction.
- Indexed: Adds an 8-bit offset to the value in the index registers (X or Y) to determine the effective address.
- Inherent: The instruction implicitly specifies the operand, using internal CPU resources like accumulators.
- Relative: Used for branching, where an offset is added to the program counter to calculate the target address.

Motorola 68HC11

- Absolute: The full address is specified in the instruction.
- Register Indirect: Operands are accessed through registers, with optional displacement.
- Index with Displacement: Combines a base register, index register, and displacement to calculate the address.
- IP with Displacement: Adds a displacement to the instruction pointer to determine the address

Similar Modes

- Immediate
- Indexed