VILNIUS UNIVERSITY

FACULTY OF MATHEMATICS AND INFORMATICS

INFORMATICS STUDY PROGRAMME

Report

Comparison of Two Computer Achitectures

Motorola 68HC11 vs. Intel i960

Karina Babenskaitė

Contents

ELEMENTARY BASE OF THE PROCESSOR

Intel i960

The Intel i960 is fabricated using CMOS technology and belongs to the Very Large Scale Integration (VLSI) category.

Motorola 68HC11

The Motorola 68HC11 is based on CMOS technology, which uses transistors fabricated as integrated circuits (ICs). It is categorized as a Large Scale Integration (LSI) device. The integration includes the CPU, RAM, ROM, EEPROM, and I/O peripherals on a single chip.

PHYSICAL CHARACTERISTICS

Intel i960

Typically available in advanced package types like HL-PBGA (High Lead Plastic Ball Grid Array), which are compact. For example, the encapsulant size is 22.38 mm x 22.38 mm, with a height of approximately 1.54 mm. It is designed to operate at 3.3V, with efficient power usage depending on workload. The processor includes features for power management.

Motorola 68HC11

Available in various package types such as PLCC (Plastic-Leaded Chip Carrier), DIP (Dual In-line Package), and QFP (Quad Flat Pack). These packages are small and light, typically weighing a few grams and measuring a few centimeters on each side. Operates on a 5V supply with low power consumption, typically drawing a few milliamps, depending on the operating mode.

ARCHITECTURE TYPE

Intel i960

The Intel i960 family is based on a RISC (Reduced Instruction Set Computer) architecture. This makes the i960 fundamentally a register-based architecture.

Motorola 68HC11

The Motorola 68HC11 microcontroller lineage is built upon the earlier 6800 architecture. This family is primarily accumulator-based.

ADDRESSING

Intel i960

Three-address machine, supporting instructions that specify two source operands and one destination operand explicitly, typical of RISC architectures.

Motorola 68HC11

One-address machine, with instructions typically involving one explicit operand and an implicit accumulator as the other operand and destination.

REGISTERS

Intel i960

Intel i960 includes a significant number of registers: general-purpose registers as well as specialized registers for certain functions.

Number of Registers

- Global Registers: 16 registers
- Local Registers: 16 registers
- Control Registers: A set of specialized registers for system control, interrupt handling, and processor configuration.
- Total: 32 general-purpose registers plus several specialized control registers.

Register Widths

All general-purpose registers are 32-bit wide. Specialized control registers vary in width but are typically 32-bit to match the processor's word size.

Motorola 68HC11

Motorola 68HC11 has registers as part of its Central Processor Unit (CPU). The architecture primarily features specialized registers, although a few have some general-purpose functionality depending on the context.

Number of Registers

- Accumulators: A and B
- Index Registers: X and Y
- Stack Pointer (SP)
- Program Counter (PC)
- Condition Code Register (CCR), used for status flags.
- Total: 6 primary registers and one condition code register.

Register Widths

- Accumulators: 8-bit
- Index Registers: 16-bit
- Stack Pointer: 16-bit
- Program Counter: 16-bit
- Condition Code Register: 8-bit

FLAGS

Intel i960

The Intel i960 uses memory-mapped control registers to check and manage status and conditions.

Flags

- Fault Status Flags
- Debugging and Trace Flags
- Register State Flags

Motorola 68HC11

Motorola 68HC11 architecture includes a Condition Code Register (CCR), which contains several flags used for arithmetic, logical, and control operations.

Flags

- C (Carry/Borrow): Indicates a carry out of the most significant bit in addition or a borrow in subtraction.
- V (Overflow): Indicates an arithmetic overflow.
- Z (Zero): Indicates if the result of an operation is zero.
- N (Negative): Indicates if the result of an operation is negative (most significant bit is 1).
- H (Half Carry): Used for BCD (Binary-Coded Decimal) arithmetic operations.
- I (Interrupt Mask): Masks interrupts when set.
- X (External Interrupt Mask): Masks non-maskable interrupts when set.
- S (Stop Disable): Used for controlling low-power modes.

DATA WIDTH

Intel i960

The machine word size for Intel i960 is 32 bits

Motorola 68HC11

The machine word size for Motorola 68HC11 is 8 bits, though it can handle 16-bit addresses and some 16-bit operations.

MEMORY LAYOUT

Intel i960

The i960 architecture features a 32-bit flat memory space. Address width is 32 bits. The total addressable memory is 4 GB.

Typical memory configuration

- On-chip caches (4 KB instruction cache, 2 KB data cache).
- Integrated 1 KB data RAM.

Motorola 68HC11

Uses a flat, continuous address space of 64 KB. Address width is 16 bits. The total addressable memory is 64 KB.

Typical memory configuration

- 768 bytes of RAM
- 12 KB of ROM/EPROM
- 512 bytes of EEPROM

VIRTUAL MEMORY

Intel i960

Intel i960 supports a memory model that can integrate with virtual memory systems. This capability is evident from its address translation units (ATUs), which allow mapping between local processor memory and external PCI address spaces.

The memory is segmented when addressing private processor memory, PCI addressable memory, or a combination of the two. The memory controller and ATUs manage these mappings, enabling flexibility in how memory is allocated and accessed.

Motorola 68HC11

Motorola 68HC11 did not support virtual memory. Its memory model is based on a simple flat, continuous address space of 64 KB, shared between on-chip resources (RAM, ROM/EPROM, EEPROM, I/O) and external memory if used in expanded mode.

The memory was not paged or segmented. However, some parts of the memory map could be relocated (e.g., RAM and register blocks could be positioned at different locations in the address space using configuration registers).

ISA TYPE

Intel i960

The Intel i960 is a RISC (Reduced Instruction Set Computer) architecture, emphasizing high-speed execution with fewer, simpler instructions.

Motorola 68HC11

The Motorola 68HC11 is based on a CISC (Complex Instruction Set Computer) architecture. It supports a rich set of instructions with multiple addressing modes.

NUMBER OF INSTRUCTIONS

Intel i960

The instruction set includes approximately 80 instructions, categorized into key operations like arithmetic, logical, data movement, and control.

Motorola 68HC11

The instruction set includes over 200 instructions, covering various operations like data movement, arithmetic, logic, branching, and control.

CLASSES OF INSTRUCTIONS

Intel i960

- Data Movement: Load, Store, Move.
- Arithmetic: Add, Subtract, Multiply, Divide.
- Logical: AND, OR, XOR, Shift.
- Control: Branch, Call, Return.
- System Control: Cache Control, Interrupt Management.

Motorola 68HC11

- Data Transfer: Load, Store, Transfer.
- Arithmetic: Add, Subtract, Multiply, Divide.
- Logic: AND, OR, NOT, XOR.
- Branching: Conditional and Unconditional Branch, Subroutine Call/Return.
- Control: Interrupt, Stop, Wait.

INSTRUCTION FORMATS

Intel i960

Most instructions are fixed-length (32 bits), with fields for opcode, registers, and immediate values. Supports register-to-register, immediate, and memory addressing modes.

Motorola 68HC11

Supports six addressing modes: immediate, direct, extended, indexed, inherent, relative. Instruction length varies between 1 to 5 bytes depending on the addressing mode and operands.

INSTRUCTION EXAMPLES

Intel i960

- ADD r1, r2, r3
- LOAD r1, [address]
- STORE r1, [address]
- JUMP [address]
- COMPARE r1, r2
- CALL [address]

Motorola 68HC11

- LDAA #value
- STAB $address
- ADDA $address
- JMP $address
- BNE $offset
- TSTA

Similar Instructions

Both architectures include basic instructions for data movement (LOAD/STAA), arithmetic (ADD, SUB), and control (JUMP/CALL).

Different Instructions

Motorola 68HC11 supports more diverse and complex addressing modes typical of CISC architectures.Intel i960 focuses on simpler instructions with fewer cycles, optimized for RISC performance. The i960's instruction set is smaller and highly optimized for compiler efficiency.

ADDRESSING MODES

Intel i960

- Immediate: The operand is directly in the instruction.
- Direct: The low byte of the address is specified, and the high byte is assumed to be $00.
- Extended: The full 16-bit address is specified in the instruction.
- Indexed: Adds an 8-bit offset to the value in the index registers (X or Y) to determine the effective address.
- Inherent: The instruction implicitly specifies the operand, using internal CPU resources like accumulators.
- Relative: Used for branching, where an offset is added to the program counter to calculate the target address.

Motorola 68HC11

- Absolute: The full address is specified in the instruction.
- Register Indirect: Operands are accessed through registers, with optional displacement.
- Index with Displacement: Combines a base register, index register, and displacement to calculate the address.
- IP with Displacement: Adds a displacement to the instruction pointer to determine the address.

Similar Modes
- Immediate
- Indexed

I/O CAPABILITIES

Intel i960

Intel i960 provides advanced I/O capabilities integrated with its RISC architecture:

- PCI-to-PCI Bridge Unit: Enables high-speed communication between two PCI buses.
- I²C Interface Unit: Supports serial communication for peripheral management.
- Memory-Mapped I/O: Internal control registers and devices can be addressed directly using memory-format instructions.
- Local Bus I/O: A 32-bit multiplexed burst bus simplifies connectivity with external peripherals and memory.

Special Features

- DMA Controller
- Interrupt Controller
- Messaging Unit

Motorola 68HC11

The Motorola 68HC11 has 5 I/O ports (Port A, B, C, D, and E) that provide up to 38 I/O lines depending on the operating mode.
Ports have specialized and general-purpose functions:

- Port A: Timer system support (input/output captures, pulse accumulator).
- Port B: High-order address lines or general-purpose outputs.
- Port C: Multiplexed address/data signals or general-purpose I/O.
- Port D: Serial communication (SCI and SPI).
- Port E: Analog-to-digital (A/D) converter inputs.

Special Features

- Serial Communication Interface (SCI).
- Serial Peripheral Interface (SPI).
- Handshake Protocols.

INTERRUPT SUPPORT

Intel i960

Incorporates a priority interrupt controller, designed to handle low-latency interrupts efficiently. Interrupts are managed using memory-mapped control registers that store interrupt vectors and status information. Interrupt handling includes stacking the state of registers and fetching the appropriate vector from the interrupt controller to execute the service routine.

Interrupt Types

- Maskable Interrupts: For general-purpose events, configurable by software.
- Non-Maskable Interrupts (NMI): Critical, high-priority events like system failures.
- Faults: Internal processor exceptions for errors like illegal opcodes and misalignments.
- PCI Interrupts: Support for message-based and hardware interrupts from the PCI bus.
- Software Interrupts: Software-generated interrupts for debugging or system control.

Special Features:

- Advanced Priority System: The priority interrupt controller ensures low latency, critical for real-time applications.
- Integration with PCI Bus: The i960 can generate and handle interrupt messages directly through the PCI interface, providing system-level communication and fault handling capabilities.
- Memory-Mapped Interrupt Vectors: Interrupt vectors are stored in a dedicated memory space, allowing fast resolution of interrupt requests.

Motorola 68HC11

The Motorola 68HC11 supports 18 interrupt vectors corresponding to 22 interrupt sources. These include both maskable and non-maskable interrupts.

Interrupt Types

- Maskable Interrupts: timer, serial communication, and pulse accumulator interrupts.
- Non-Maskable Interrupts (NMI): XIRQ pin, illegal opcode trap, and software interrupt (SWI).

Special Features:

- Priority System: A detailed priority resolution mechanism determines which interrupt is handled first when multiple are pending.
- Software Interrupt (SWI): A specific instruction initiates an interrupt and is not affected by global mask settings.

DATA TYPES

Intel i960

Supported Data Types:

- Bit Data: Single-bit values for control and logical operations.
- Bit Fields: Subsets of bits within a register or memory location
- 8-, 16-, 32-, 64-bit Integers: Both signed and unsigned (ordinal types).
- Triple Word (96-bit): For extended precision arithmetic.
- Quad Word (128-bit): Used in advanced data processing tasks.

Integer
The architecture supports two's complement for signed integers, as well as unsigned integer operations for ordinals.

Floating Point
Floating-point operations are supported in software and may also be assisted by external floating-point hardware, depending on the system configuration.

Exotic Data Types
Ata types such as bit fields, triple words, and quad words provide extended functionality for specialized applications.

Motorola 68HC11

Supported Data Types:

- Bit Data: Single-bit values, used for flags and control bits.
- 8-bit Integers: Signed and unsigned.
- 16-bit Integers: Signed and unsigned.
- 16-bit Unsigned Fractions: Used in arithmetic operations requiring fractional representation.
- 16-bit Addresses: For memory referencing.

Integer
The architecture uses two's complement for signed integers, ensuring compatibility with modern arithmetic operations.

Floating Point
Floating-point operations are not natively supported in hardware but can be

implemented in software through libraries or custom routines.

Exotic Data Types

Limited support for specialized data types like BCD (Binary-Coded Decimal) through specific arithmetic instructions (e.g., Decimal Adjust Accumulator).

SPEED AND PERFORMANCE

Intel i960

Clock Frequencies
The Intel i960 is available in variants that operate at 33 MHz and 66 MHz, depending on the model (e.g., i960RP and i960RD).

Clock Cycles per Instruction
The architecture achieves one instruction per clock cycle for most operations, thanks to its RISC design and instruction pipeline.

Instruction Rate
At 66 MHz, the processor can execute up to 66 million instructions per second (MIPS).

Performance
The Intel i960 is a high-performance processor designed for multitasking and high-throughput applications, with features like an efficient instruction pipeline, caching, and parallel execution capabilities.

Motorola 68HC11

Clock Frequencies
The Motorola 68HC11 operates at frequencies between 1 MHz and 2 MHz, depending on the specific configuration and application.

Clock Cycles per Instruction
Instructions require between **2 and 41 clock cycles**, depending on the complexity of the operation. For example: simple instructions like INCA (increment accumulator) take 2 cycles. More complex operations like FDIV (fractional divide) require 41 cycles.

Instruction Rate
At a clock frequency of 2 MHz, the processor can execute approximately 500,000 instructions per second for simple operations.

Performance
The Motorola 68HC11 is designed for embedded systems, focusing on cost-effectiveness and real-time control rather than raw speed.

Which System Was Faster?

The Intel i960 is significantly faster than the Motorola 68HC11 in terms of clock speed, instruction throughput, and overall performance.

CACHE MEMORY

Intel i960

Intel i960 includes on-chip cache memory as part of its architecture:

- Instruction Cache: 4 KB, two-way set-associative.
- Data Cache: 2 KB, direct-mapped.

Motorola 68HC11

Motorola 68HC11 does not include cache memory. It relies entirely on internal RAM, ROM/EPROM, and optional external memory for its data and program storage needs.

APPLICATION AREAS

Intel i960

The Intel i960 was used in networking equipment, industrial computing, aerospace, and gaming systems. The processor continues to be used for a few military applications.

Example Installation
The Intel i960 was the main CPU for Sega's Model 2 arcade boards. The i960 handled 3D graphics computations, game logic, and real-time interactions with peripherals like controllers and displays.

Motorola 68HC11

The Motorola 68HC11 was used in automotive systems, industrial control, consumer electronics, and robotics.

Example Installation
In the field of robotics, the 68HC11 has been utilized in educational and hobbyist projects. For example, it has served as the central processing unit in small robots designed for the MicroMouse competition, where autonomous robots navigate a maze to find the shortest path to the center.

SOFTWARE

Intel i960

Compilers and Programming Tools

- Archelon's i960 C Compiler.
- Intel's Software Development Tools (C/C++ compilers, assemblers, debuggers, and utilities designed for embedded application development).

Libraries

The i960 development environment included runtime libraries compatible with ANSI C standards, offering functions for mathematical computations, memory management, and input/output operations.

While the i960 has been discontinued, some software tools and documentation remain accessible through archives and specialized vendors.

Motorola 68HC11

Compilers and Programming Tools

- GNU Development Chain.
- COSMIC C Cross Compiler.
- MiniIDE.

Libraries

Floating-point arithmetic libraries, device drivers, and peripheral interface libraries.

A significant portion of this software is still accessible through repositories like GitHub.