ARM Assembly for Embedded Applications 5th edition DANIEL W LEWIS

ARM Instructions Worksheet #9

Floating-Point Compares

And their effect on the NZCV Flags in the CPSR register:

N Z C V Q ···

Prerequisite Reading: Chapter 9

Revised: April 21, 2020

Objectives: To use the web-based simulator ("CPULator") to better understand ..

- 1. The use of VCMP and VMRS to perform floating-point comparisons.
- 2. The use of VSUB and VMOV to simplify some floating-point comparisons.
- 3. The use of floating-point equality comparisons.

To do offline: Answer the questions that follow the listing below. (Numbers at far left are memory addresses.)

```
.syntax
                                         unified
                            .global
                                         _start
              // *** EXECUTION STARTS HERE ***
                                                              // N flag = 0
00000000
              start:
                           MOVS
                                         R0,0
00000004
                           VLDR
                                         S0,posPt4
                                                              // S0 = +0.4
                                                              // S1 = +0.5
0000008
                           VLDR
                                         S1,posPt5
000000C
                           VCMP.F32
                                         S0,S1
                                                              // 0.4 < 0.5 ?
00000010
                           VMRS
                                         APSR nzcv, FPSCR
00000014
                           LDR
                                         R0,=1
                                                              // Assume MI
00000018
                           BMI
                                         L1
                                                              // Wasn't MI
0000001C
                           LDR
                                         R0,=0
00000020
             L1:
                           VSUB.F32
                                         S2,S0,S1
                                                              // S2 = 0.4 - 0.5
00000024
                           VMOV
                                         R1,S2
00000028
                                         R1,R1,31
                                                              // Same as R0?
                           LSR
0000002C
                           VLDR
                                         S3, negPt1
                                                              // S3 = -0.1
00000030
                           VCMP.F32
                                         S2,S3
                                                              // S2 == S3 ?
                           VMRS
                                         APSR_nczv, FPSCR
00000034
00000038
                           LDR
                                         R2,=1
                                                              // Assume EQ
0000003C
                           BEQ
                                         done
00000040
                           LDR
                                         R2,=0
                                                              // Wasn't EQ
              done:
                                                              // Infinite loop
00000044
                           В
                                         done
00000048
              point5:
                            .float
                                         +0.5
             point4:
                            .float
0000004C
                                         +0.4
                            .float
                                          -0.1
00000050
             point1:
                            .end
```

What is in the N flag (CPSR bit 31) after executing the VCMP at address 0000000C₁₆?

What is in the N flag (CPSR bit 31) after executing the VMRS at address 00000010₁₆?

What is in register R0 *before* executing the VSUB instruction at address 00000020₁₆?

What is in register S2 after executing the VSUB instruction at address 00000020₁₆?

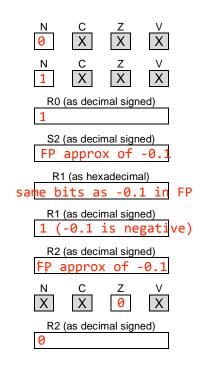
What is in register R1 after executing the VMOV instruction at address 00000024₁₆?

What is in register R1 after executing the LSR instruction at address 00000028₁₆?

What is in register S3 after executing the VLDR instruction at address 0000002C₁₆?

What is in the Z flag (CPSR bit 29) after executing the VMRS at address 00000034₁₆?

What is in register R2 *before* executing the B instruction at address 00000044₁₆?



Getting ready: Now use the simulator to collect the following information and compare to your earlier answers.

1. Click here to open a browser for the ARM instruction simulator with pre-loaded code.

Note: You can change the number format in the "Settings" window between hex, unsigned decimal and signed decimal as needed

Step 1: Press F2 once per ARM instruction as needed to see what the simulator says for the following:

What is in the N flag (CPSR bit 31) after executing the VCMP at address 0000000C₁₆?

What is in the N flag (CPSR bit 31) after executing the VMRS at address 00000010₁₆?

What is in register R0 *before* executing the VSUB instruction at address 00000020₁₆?

What is in register S2 after executing the VSUB instruction at address 00000020₁₆?

What is in register R1 after executing the VMOV instruction at address 00000024₁₆?

What is in register R1 after executing the LSR instruction at address 00000028₁₆?

What is in register S3 after executing the VLDR instruction at address 0000002C₁₆?

What is in the Z flag (CPSR bit 29) after executing the VMRS at address 00000034₁₆?

What is in register R2 *before* executing the B instruction at address 00000044₁₆?

