

## Chapter - 7

### Signal Conditioning and Processing:

#### \* Importance of Signal Conditioning:-

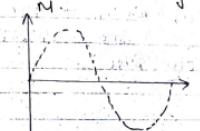
The physical quantity is converted into electrical form by using transducers. The output of the transducer may not be usable directly by the next stage. So it becomes necessary that the output of transducer has to be modified before it becomes usable and satisfactory to drive the next stage, so signal conditioner modify the transduced signal into a usable format for the next stage. The signal conditioning equipment may perform linear processes like amplification, attenuation, integration, differentiation, addition, subtraction, etc. They also perform non linear processes like modulation, demodulation, sampling, filtering, clipping and clamping, squaring, linearizing or multiplication etc.

#### \* Interference signals and their elimination:-

Interference is anything which modifies or disrupts a signal as it travels along a channel between a source and a receiver. The term typically refers to the addition of ~~useful~~ unwanted signals to a useful signal.

Int

Interference of signals can be reduced by using suitable filter circuit or by providing electromagnetic and electrostatic shielding etc.



Interference waveform

#### \* Importance of Signal Conversion:-

Since most sensors have analog output while much data processing is accomplished with digital computers, analog-to-digital and digital-to-analog conversion plays an important role. The process of changing an analog signal to an equivalent digital signal is accomplished with the help of an analog-to-digital converter (ADC). On the other hand, ADC is used to convert an analog signal from transducer into an equivalent digital signal. Digital-to-analog conversion involves digital signal. Digital-to-analog conversion involves translation of digital information into equivalent analog information and this is accomplished by the analog-to-digital converter (DAC). DAC's use of digital-to-analog converter (DAC) are used whenever the output of a digital circuit has to provide an analog voltage or current to drive an analog device.



### Digital to Analog Conversion:-

The process of taking a value represented in digital code and converting it into a voltage or current which is proportional to the digital value is known as digital to analog conversion.

- 1) Binary Weighted resistor DAC
- 2) R-2R ladder DAC

### Analog to Digital Conversion :-

The process of converting an analog input voltage into an equivalent digital signal is known as analog to digital conversion.

- 1) Counter type ADC / Ramp ADC
- 2) Successive approximation ADC
- 3) Flash type ADC

### Digital to analog Conversion :-

- 1) Binary weighted resistor DAC

Binary weighted resistor DAC uses an op-amp to sum 'n' binary weighted current derived from a reference voltage  $V_{ref}$ , via current scaling resistances  $2^0 R$ ,  $2^1 R$ ,  $2^2 R$  ---  $2^{n-1} R$  as shown in figure.

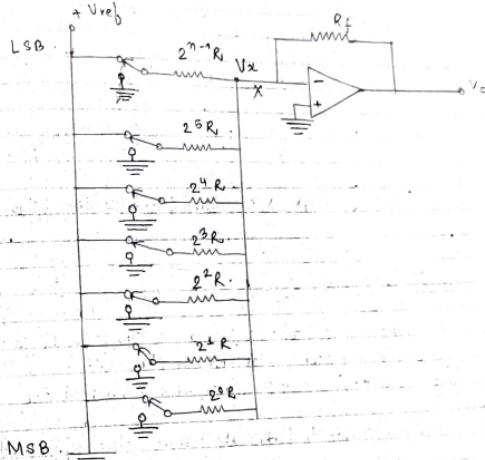


Fig: Binary Weighted resistor

Here, if the switch is connected to  $+V_{ref}$ , it is considered as logical '1' and if the switch is connected to the ground, it is considered as logical '0'.

Now, the output voltage  $V_o$  is determined applying KCL at node 'X'. We get:

$$V_x - V_{ref} + \frac{V_x - V_{ref}}{2^0 R} + \dots + \frac{V_x - V_{ref}}{2^{n-1} R} + \frac{V_x - V_o}{R_f} = 0$$

$$\text{Since, ideally } V_x = 0 \\ \frac{V_o}{V_{ref}} = - \left[ \frac{V_{ref}}{2^0 R} + \frac{V_{ref}}{2^1 R} + \frac{V_{ref}}{2^2 R} + \dots + \frac{V_{ref}}{2^{n-1} R} \right]$$

$$V_o = - \frac{V_{ref} \times R_f}{R} \left[ b_0 \times \frac{1}{2^0} + b_1 \times \frac{1}{2^1} + b_2 \times \frac{1}{2^2} + \dots + b_{n-1} \times \frac{1}{2^{n-1}} \right]$$

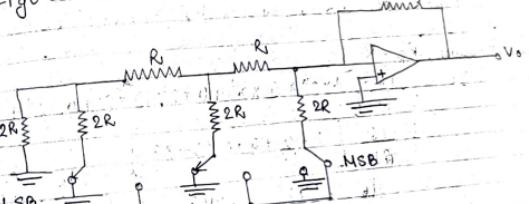
Here,  $b_0$  is the MSB and  $b_{n-1}$  is the LSB

### Drawbacks:

- 1) Wide range of resistance values are required. For an  $n$ -bit DAC the resistors required are  $2^0 R, 2^1 R, \dots, 2^{n-1} R$  i.e. the largest resistor is 128 times the smallest one.
- 2) It is impracticable to fabricate large value of resistor in ICs and the voltage drop across such a large resistor due to the bias current also affects the accuracy.
- 3) The finite resistance of the switches disturb the binary weighted relationship among the various currents particularly in the most significant bit position where the current setting resistances are smaller.

### R-2R ladder DAC:-

The drawbacks of binary weighted resistor DAC are removed or minimized in the R-2R ladder DAC where only two resistor values  $R$  and  $2R$  are used. Figure below shows the R-2R ladder DAC for a bit



V<sub>ref</sub>:

Here if the switch is connected to V<sub>ref</sub>, it is considered as logical '1' and if the switch is connected to the ground, it is considered as logical '0'.

In general, for 'n' bits, the analog output voltage is given by

$$V_o = - \frac{V_{ref}}{2^n} \left[ b_0 \times 2^0 + b_1 \times 2^1 + b_2 \times 2^2 + \dots + b_{n-1} \times 2^{n-1} \right] \times R_f / R$$

Where,  $b_0, b_1, b_2, \dots, b_{n-1}$  are binary digits with  $b_0$  as LSB and  $b_{n-1}$  as MSB and  $n$  as the numbers of bits of operation.

- \* Design a 6-bit R-2R ladder ADC digital input: 101011. If the input scales are 0 = 0V and 1 = +16V.

Here,  
 $V_o = -\frac{V_{ref}}{2^6} \cdot \frac{R_f}{R} [b_0 2^0 + b_1 2^1 + b_2 2^2 + b_3 2^3 + b_4 2^4 + b_5 2^5]$

Since, Here,  $b_0 = 1, b_1 = 1, b_2 = 0, b_3 = 1, b_4 = 0$  and  $b_5 = 1$ .

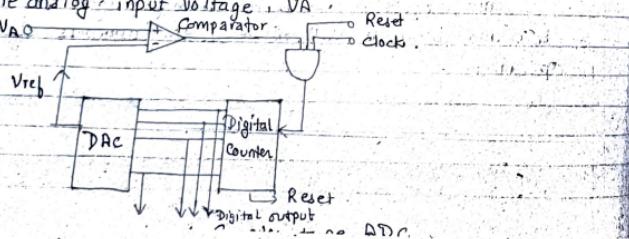
Assume,  $R_f = R$ :

$$\begin{aligned} V_o &= -\frac{16}{2^6} [1 \times 2^0 + 1 \times 2^1 + 0 \times 2^2 + 1 \times 2^3 + 0 \times 2^4 + 1 \times 2^5] \\ &= -\frac{16}{64} [1 + 2 + 0 + 8 + 0 + 32] \\ &= -\frac{16}{64} \times 43 = -\frac{43}{4} = -10.75V \text{ Also} \end{aligned}$$

### Analog-to-Digital Conversions

#### 1) Counter type ADC / Ramp ADC :-

A counter type ADC shown in figure consists of a digital counter, a DAC, an analog comparator, and a control AND gate. The digital counter advances from a zero count and increases by one step at a time until the reference ramp voltage,  $V_{ref}$  becomes equal to or exceeds the analog input voltage,  $V_A$ .



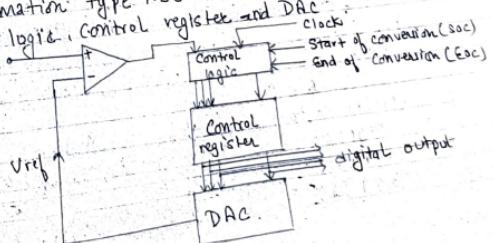
The output of comparator will high until  $V_A > V_{ref}$ . The high output of the Comparator enables the AND gate which allows the clock to reach to the counter and the counter counts up. The process continues until  $V_A$  equals  $V_{ref}$ . When  $V_A = V_{ref}$ ; the output of comparator again becomes high which enables the AND gate and one more clock pulse is counted by the counter.

The counter stops counting as soon as  $V_A < V_{ref}$ . At this stage, the comparator output drops which disables AND gate. Thus the clock pulses are stopped from reaching the counter.

This ADC circuit is counting one more count than the actual. So a slight modification in the circuit is necessary. This is main limitation of the counting type ADC.

#### 2) Successive approximation ADC :-

This type of ADC makes direct comparison between an unknown input signal and a reference signal. Figure below shows the basic block diagram of a successive approximation type ADC. It consists of a comparator, control logic, control register and DAC.



The control signal at the start of conversion (Csac) initiates an A/D conversion process and the end of the conversion signal (Eoc) is activated when the conversion is completed. The DAC provides a reference variable voltage in steps. The control logic modifies the contents of the register bit by bit until the register data are digital equivalent of the analog input  $V_A$ .

When the start of conversion is enabled, the control register sets the MSB high and others low. (For eg: for 4-bit ADC output will be 1000). Then DAC converts the digital word and the equivalent analog voltage ( $V_{ref}$ ) is compared to the comparator. If  $V_A > V_{ref}$ , then the successive or control register maintains MSB=1 and make second MSB=1 if  $V_A < V_{ref}$ , then it resets MSB=0 and second MSB=1.

The process is repeated for all bits until  $V_A = V_{ref}$ .

\* Convert an analog voltage ( $V_A$ ) = 19V into its equivalent digital form using 6-bit successive approximation ADC.

Here,

$$V_A = 19V$$

Digital output	$V_{ref}$	Remark
100000	32V	$V_{ref} > V_A$
010000	16V	$V_{ref} < V_A$
011000	24V	$V_{ref} > V_A$

010100	28V	$V_{ref} > V_A$
010010	18V	$V_{ref} > V_A$
010011	19V	$V_{ref} = V_A$

$$\therefore \text{digital output} = 010011_{\text{B}}$$

Hence, digital representation of  $V_A = 19V$  is 010011<sub>B</sub>.

\* Convert an analog voltage ( $V_A$ ) = 19V into its equivalent digital form using 6-bit successive approximation ADC.

### Flash or parallel ADC:

In this type of conversion, the input is simultaneously compared with the different reference voltages which are one LSB apart. The output of the comparators are then logically combined to provide the output digital code by the priority encoder that puts out the digital code for the highest-order input received by it.

One input of each comparator is connected to the input signal and the other input to the reference voltage level generated by the reference voltage divider.

The comparators gives an output '1' or '0' state depending on whether the input signal is above or below the reference level at that instant. The code resulting from the comparators is converted

to a binary code by the encoder

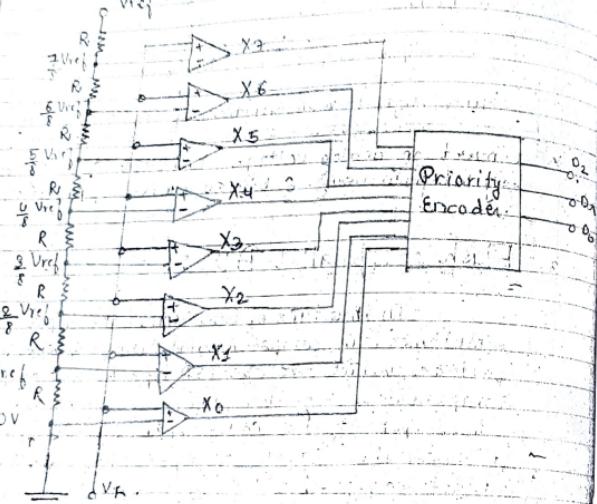


Fig: Flash or parallel ADC

The truth table for the flash ADC is shown below :-

VA	X7	X6	X5	X4	X3	X2	X1	X0	Vi
0 to $\frac{1}{8}V_{ref}$	0	0	0	0	0	0	1	0	0
$\frac{1}{8}V_{ref}$ to $\frac{2}{8}V_{ref}$	0	0	0	0	0	0	1	1	0
$\frac{2}{8}V_{ref}$ to $\frac{3}{8}V_{ref}$	0	0	0	0	0	1	1	1	0
$\frac{3}{8}V_{ref}$ to $\frac{4}{8}V_{ref}$	0	0	0	0	1	1	1	1	1
$\frac{4}{8}V_{ref}$ to $\frac{5}{8}V_{ref}$	0	0	0	1	1	1	1	1	0
$\frac{5}{8}V_{ref}$ to $\frac{6}{8}V_{ref}$	0	0	1	1	1	1	1	0	1
$\frac{6}{8}V_{ref}$ to $\frac{7}{8}V_{ref}$	0	1	1	1	1	1	1	1	0
$\frac{7}{8}V_{ref}$ to $V_{ref}$	1	1	1	1	1	1	1	1	1

THE END.

Ques:

2016 Fall

### 5a) Capacitive Transducer:-

Principle of change in separation distance 'd'

This principle is also used for measurement of displacement. It consists of two parallel plates, one fixed and another movable. The objective whose displacement is to be measured is attached with movable plate.

Construction:-



Fig :- 1 : Basic arrangement

The capacitance of the parallel plate is given by,

$$C = \frac{\epsilon A}{d} \quad (I)$$

So, the sensitivity is given by,

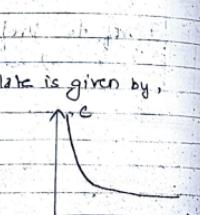
$S = \text{small change in O/P}$ .

small change in T/P.

Fig : 2

$$\text{Or, } S = \frac{dc}{dd} = \frac{d}{dd} \left[ \frac{\epsilon A}{d} \right]$$

$$\therefore S = -\frac{\epsilon A}{d^2} \Rightarrow S \propto \frac{1}{d^2}$$



Thus, Sensitivity varies inversely as the square of the separation distance as shown in fig. 2.

There exists a non-linear relation between capacitance and separation distance 'd'.

The above graph in fig 2 also shows a linear relation between C and d, the separation distance must be as much less as possible. But as separation distance decreases, the electrical stress on dielectric increases. So, separation distance can be made small to certain limit only which is determined by breakdown strength of the dielectric.

Another method to obtain linear relation is differential arrangement.

Differential Arrangement :

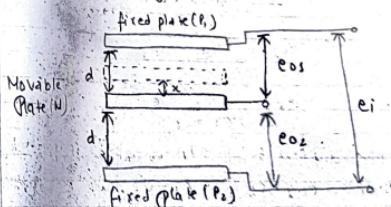


Fig :- Differential Arrangement

### Working Principle:-

When the plate M is at mid-point between P<sub>1</sub> and P<sub>2</sub> then,

$$C_1 = C_2 = \frac{\epsilon A}{d} \quad \text{--- (II)}$$

The voltage e<sub>o</sub> across C<sub>1</sub> and C<sub>2</sub> are respectively given by,

$$e_{o1} = \epsilon \frac{C_2}{C_1 + C_2} e_i = \frac{\epsilon i}{2}$$

$$e_{o2} = \frac{C_1}{C_1 + C_2} e_i = \frac{\epsilon i}{2}$$

Thus, differential o/p (e<sub>o</sub>) = e<sub>o1</sub> - e<sub>o2</sub> = 0

when the plate M moves upward by a distance 'x' as shown in figure, then

$$C_1 = \frac{\epsilon A}{d-x} \quad \text{and} \quad C_2 = \frac{\epsilon A}{d+x}$$

$$\therefore e_{o1} = \frac{C_2}{C_1 + C_2} e_i$$

$$e_{o2} = \frac{C_1}{C_1 + C_2} e_i$$

Thus, differential o/p voltage is given by,

$$\Delta e_o = e_{o2} - e_{o1} = \frac{C_1 - C_2}{C_1 + C_2} e_i \quad \text{--- (III)}$$

Now,

$$C_1 - C_2 = \epsilon A \left[ \frac{1}{d-x} - \frac{1}{d+x} \right]$$

$$\text{or, } C_1 - C_2 = \epsilon A \left[ \frac{2x}{d^2 - x^2} \right] \quad \text{--- (III)}$$

Similarly,

$$C_1 + C_2 = \epsilon A \left[ \frac{2d}{d^2 - x^2} \right] \quad \text{--- (IV)}$$

From eqns (II), (III) & (IV), we get;

$$\epsilon A \left[ \frac{2x}{d^2 - x^2} \right]$$

$$\Delta e_o = \epsilon A \left[ \frac{2d}{d^2 - x^2} \right] e_i$$

$$\therefore \Delta e_o = \frac{2}{d} e_i$$

$$\therefore \Delta e_o \propto x$$

Thus, the o/p varies linearly with the input.

Sensitivity of the device is given by.

$$S = \frac{\text{small change in o/p}}{\text{small change in i/p}}$$

$$= \frac{d(\Delta e_o)}{dx}$$

$$= \frac{d}{dx} \left[ \frac{x}{d} e_i \right]$$

$$\therefore S = \frac{e_i}{d} = \text{constant}$$

Thus the sensitivity of the device is constant.

