

① Address decoding circuit

Say Bank questions

(2¹²) 4 KB

Address decoding \Rightarrow Address को डिसेक्यूट करना।
Address ~~परिप्रे~~ परिप्रे लगाने।
(detect & generate)
peripheral device को address

↳ Detection of address of peripheral device is known to be address decoding. There are two types of address decoding:

① Full address decoding

② Partial address decoding

→ If all the address lines of the microprocessor system is used to address the memory or I/O devices, such type of decoding is known to be full address decoding. It is also known to be unique address decoding, or absolute address decoding.

→ But if only some of the address lines of the microprocessor system is used to address the memory or I/O devices, such kind of address decoding is known to be partial address decoding.

Hence the circuitry system that is used in address decoding & work, such type of circuit is known to be address decoding circuit. ③ Address decoding circuit which is often referred to as decoder, is an essential component in digital electronics and VLSI system whose primary function is to find the memory location of peripheral devices. It is the combination of decoder with peripheral devices of RAM, ROM, EPROM, etc.

Qn) Design an address decoding circuit to interface 2 kB RAM, 4 kB ROM and 8 kB RAM with 8085 up.

Soln) Here; no. of available address line of 8085 up = 16 line (A₀-A₁₅)

Also, no. of address line used to represent:

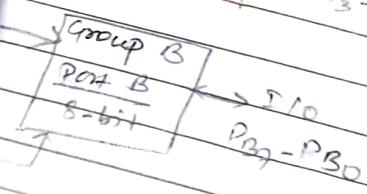
① 2 kB RAM is

$$= 2 \text{ kB} = 2^10 \text{ kB}$$

$$= 2^10 \times 2^{10}$$

$$= 2^{20} = 1024 \text{ Address lines per A}_0 - \text{A}_{10}$$

Fig.: Block diagram



$$\begin{aligned}
 \text{(ii) } & 4 \text{ KB Rom} \\
 & = 2^2 \text{ KB} \\
 & = 2^2 \times 1 \text{ KB} \\
 & = 2^2 \times 2^{10} \\
 & = 2^{12} \\
 & = 12 \text{ Address lines} \Rightarrow A_0 - A_{11}
 \end{aligned}$$

$$\begin{aligned}
 \text{(iii) } & 8 \text{ kB Ram} \\
 & = 2^3 \times 1 \text{ kB} \\
 & = 2^3 \times 2^{10} \\
 & = 2^{13} \\
 & = 13 \text{ Address lines are needed} \\
 & = A_0 - A_{12}
 \end{aligned}$$

② memory mapping

IC	Address	A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	
Ram ₁	Starting Address	X	X	V	V	V												
Ram ₁	0000H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Ram ₁	End Address	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
Rom	2000H	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Rom	2FFFH	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
Ram ₂	4000H	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Ram ₂	5FFFH	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

We know,

$$\begin{aligned}
 \text{End Address} &= \text{Starting address} + [2^{10} \times (83) - 1] \\
 \text{of Ram}_1 &= 0000 + [2^{10} \times 2 - 1] \quad \left\{ \begin{array}{l} \text{we have assumed the} \\ \text{S.A of Ram}_1 = 0000H \end{array} \right\} \\
 &= 0000 + [2^{11} - 1] \\
 &= 0000 + (2048)_{10} \\
 &= 0000 + 07FF \\
 &= 07FF
 \end{aligned}$$

$$\begin{aligned}
 \text{S.A of Rom} &= \text{E.A of Ram}_1 + 1 \\
 &= 07FF + 1 \\
 &= 0800 \text{ (not possible)}
 \end{aligned}$$

$$\begin{aligned}
 \text{Let S.A of Rom} &= 02000H \\
 \text{E.A of Rom} &= 0200 + (2^{10} \times 2^2 - 1) = 0200 + 0FFF \\
 &= 2FFFH
 \end{aligned}$$

Also, Last five S.A of Ram 2 = 4000H

$$\begin{aligned}\therefore E \cdot A &= 4000 + (2^{10} \times 2^3 - 1) \\ &= 4000 + 7FFF \\ &= 5FFFFH\end{aligned}$$

(3)

Also, A₁₅ goes to enable and A₁₃ and A₁₄ is the input for decoder.
So, the address decoding circuit is:

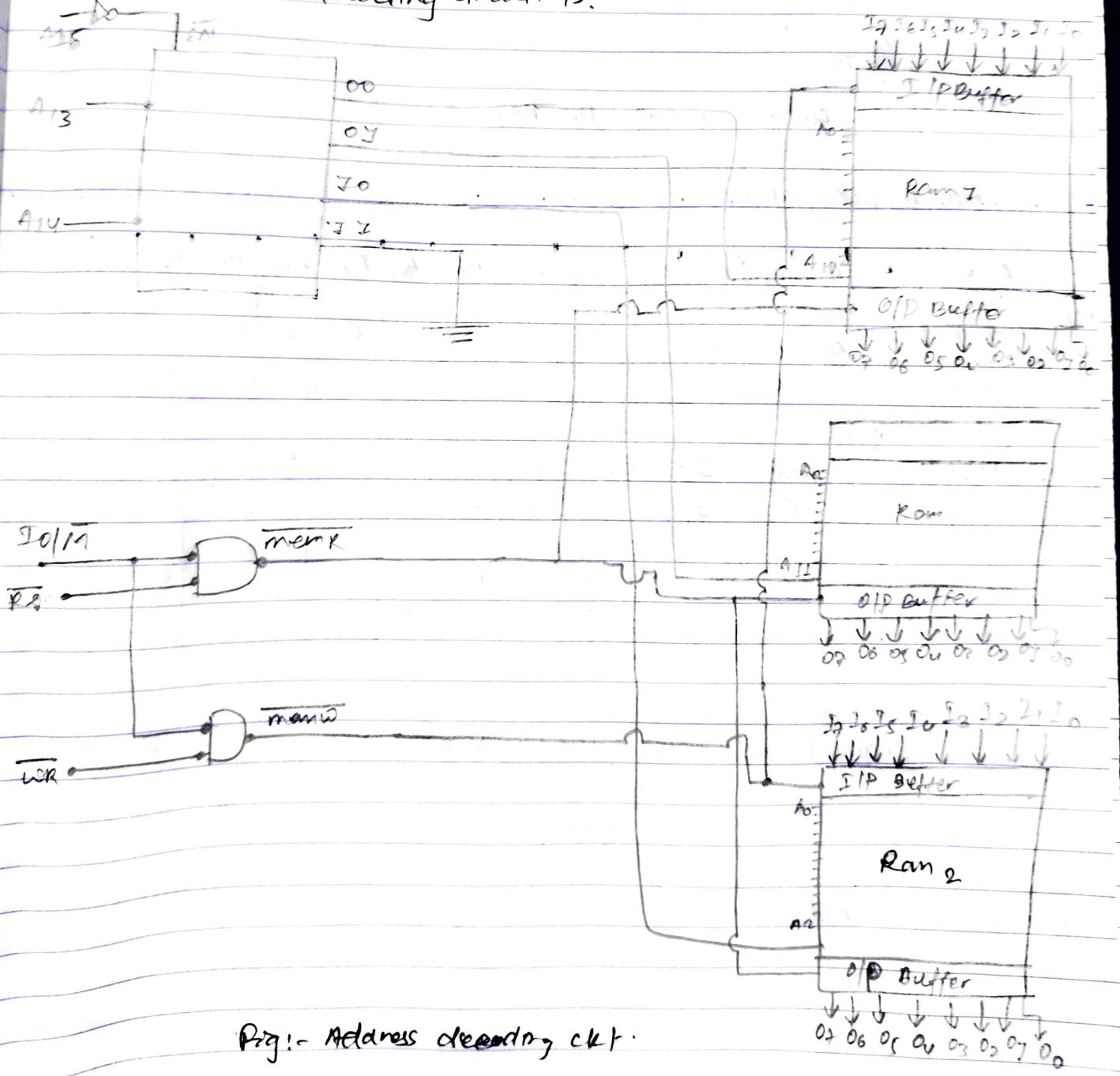


Fig:- Address decoding ckt.

Group A
Port (upper)
area

$\rightarrow I/O$
 $I/O - P_{11}$

Group B
Port (lower)
area

$\rightarrow I/O$
 $I/O - P_{10}$

Group C
 $\rightarrow I/O$

Q1 Design a 8 address decoding circuit to interface two RAM and a ROM each of 4 kB starting at address 21000H.

Ans Here we know the no. of available address lines in 8085 is
 $= 2^8 = A_0 - A_{15}$

Now, Address lines required for 4 kB Ram, ROM

$$\begin{aligned} &= 4 \text{ kB} \\ &= 2^2 \times 2^{10} \\ &= 2^{12} \end{aligned}$$

$= 12$ Address lines i.e. $A_0 - A_{11}$

S.A of

E.A

Here,
and

The memory mapping table is:

as 40P I.C.		Address	A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁
24 I/O Ram		Start address															
Port A		4000H	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Port B		4FFFFH	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
Ram		S.A	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0
		5000H	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1
		5FFFH	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1
Rom		S.A	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
		6000H	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1

Range 1: Starting Address = 4000H

$$\therefore \text{Ending Address} = 4000 + (2^{10} \times 2^2 - 1)$$

$$= 4000 + 0FFF$$

$$= 4FFFH$$

I/O M

RD

Range 2: Starting Address: E.A of Ram + 1

$$\begin{aligned} &= 4FFF + 1 \\ &= 5000 \end{aligned}$$

WR

$$\begin{aligned} E.A &= 5000 + 0FFF \\ &= 5FFFH \end{aligned}$$

$$\begin{aligned}
 S.A[6] \text{ of Rom} &= S.A[6] \text{ of Ram} + 7 \\
 &= 5FFF + 7 \\
 &= 6000H \\
 S.A[5] \text{ of Rom} &= 6FFFFH
 \end{aligned}$$

Here, A₁₅ and A₁₄ goes for Enable
and A₁₃ and A₁₂ for decoder input.

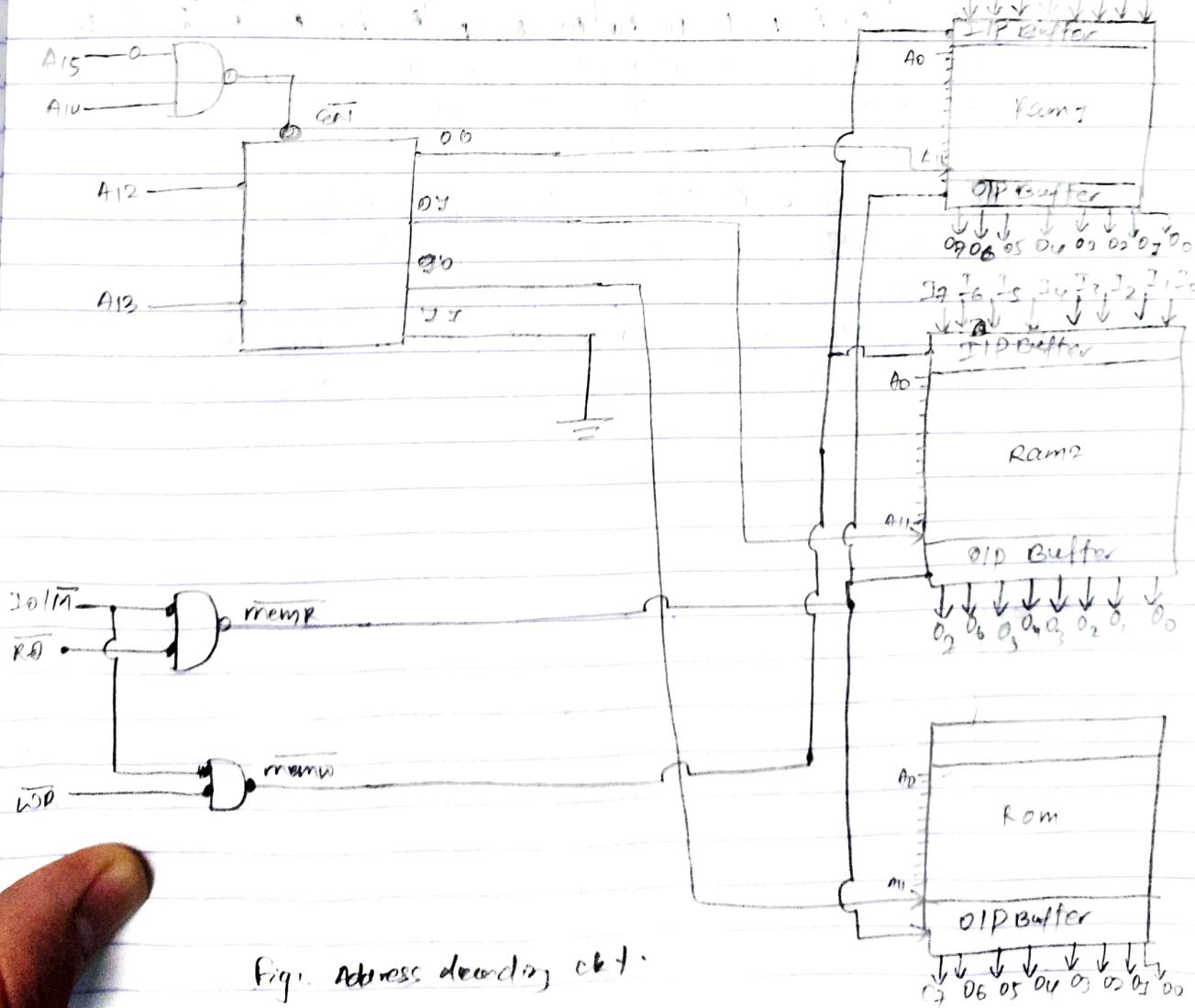
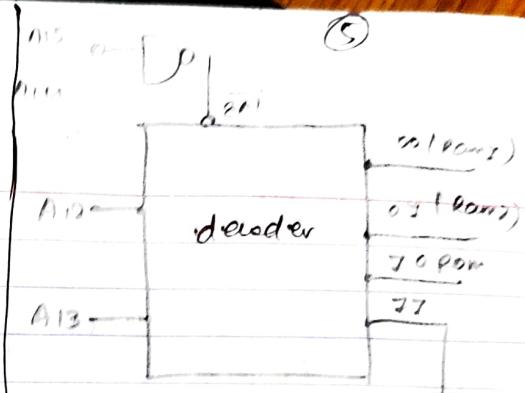
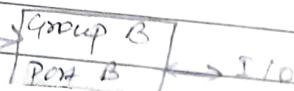
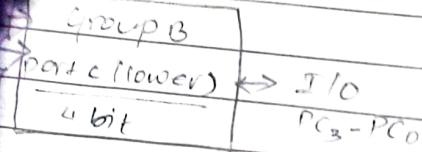


Fig: Address decoding circuit



Ques 3 Design an address decoding ckt interface like B
Rom, 16 kB Ram with S.A of 2000H

Blocks

Soln: Here the address line required for:

(a) 4 kB Rom

$$\hookrightarrow 2^2 \times 2^{10}$$

$$= 2^{12}$$

= 12 Address lines

$$= A_0 - A_{11}$$

(b) 16 kB Ram

$$= 2^4 \times 2^{10}$$

$$= 2^{14}$$

= 14 Address lines

$$= A_0 - A_{13}$$

I purpose
to perf.

inter. Now the memory mapping is:

as 40 IC		Address	A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	
24 I/O Rom		St. Address: 2000H	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Port 1		End Address: 2FFFH	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
Rom		St. Address: 0000H	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		End Address: 3FFFH	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Here the A₁₅ address line serves as enable and A₁₄ is the decoder input so 2x2 decoder is needed.

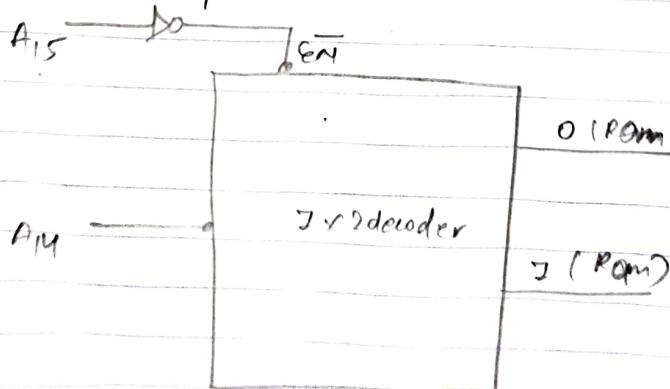
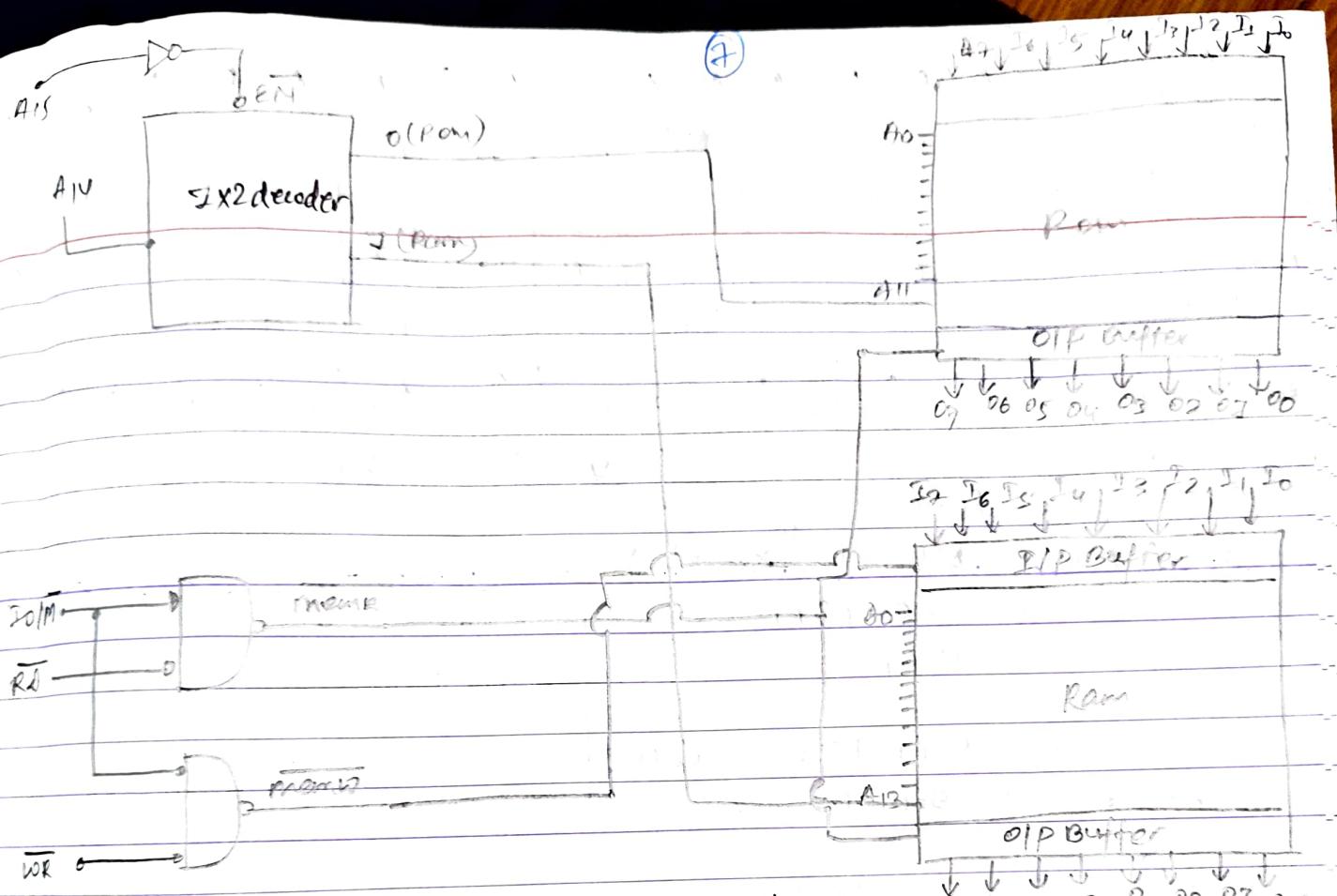


Fig:- decoder for Address decoding circuit.



Rig:- Address decoding circuit.

(Q) Address decoding ck to interface 2KB, 4KB Ram, 8KB Ram, with 8000H as starting address.

$$2KB = 2^3 \times 2^{10}$$

\Rightarrow 2 Address lines

$$= A_0 - A_{10}$$

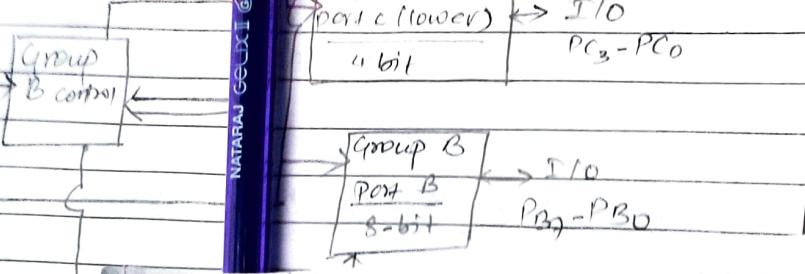
$$4KB = 2^4 \times 2^{10}$$

\Rightarrow 3 Address lines

$$= A_0 - A_{11}$$

$$8KB = 2^3 \times 2^{10} \\ = 2^{13}$$

$$= 13 (A_0 - A_{12})$$



B.g.:

$$\begin{aligned}
 S.A_{\text{of Ram}} &= 8000 \\
 S.A_{\text{of Ramd}} &= 8000 + (2^{10} \times 2 - 1) \\
 &= 8000 + 0.7 \text{PF} \\
 &= 87 \text{PF}
 \end{aligned}$$

$$S \cdot A_{of} \text{ Ram2} = 8FFF + I = 9000H$$

$$R \quad S \cdot A_{of} \text{ Ram2} = 9FFFH$$

02 fall 93 4 kb ROM, 4 kb Rom, 8 kB Ram with Z800H as S-A.

$$4k_B \Rightarrow 2^2 \times 2^{10} \Rightarrow 12 = A_0 - A_{11}$$

27 fall 4b

4 kB Ram, 8 kB Rom, 18 kB Ram with 8000H as SDA. (9)

$$\text{ROM } 4 \text{ KB} \Rightarrow 2^8 \times 2^{10} = 2^{12} = A_0 - A_{11}$$

$$g \text{ kB} = 2^3 \times 2^{10}$$

$$= 2^{13} = A_D - A_{12}$$

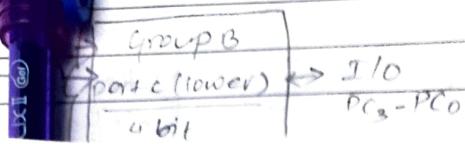
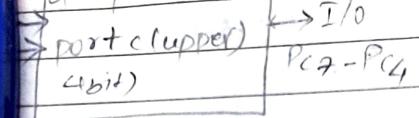
$$16 \text{ KB} \Rightarrow 2^4 \times 2^{10} = 2^{14} = A_0 - A_{13}$$

19 fall 4b

4K*8 EEPROM, 8K*8 RAM with \$000H ~ \$A

$$y_{4KB} = 2^2 \times 2^{10} \Rightarrow 12 \Rightarrow A_0 - A_{11}$$

$$8KB = 2^3 \times 2^{10} \Rightarrow 13 \Rightarrow B_0 = A_{12}$$



Group
B con

(2SPSB)

$$4k_B \Rightarrow 2^{X^2}^{10}$$

$$\Rightarrow 12$$

$$= A_{\text{left}} - A_{\text{right}}$$

$$SKB \Rightarrow 2^{\aleph_0} \times 2^{10} \\ \Rightarrow 13$$

$$\begin{aligned} & 16k^3 \\ \Rightarrow & e^{4x^2/10} \\ \Rightarrow & 14 \\ \Rightarrow & A_0 - A_{13} \end{aligned}$$

10

B.g.:

17 Fall 14b Draw an interfacing circuit for 24V Ram starting at \$300H and 12V Romat \$400H

$$\Rightarrow 2k_B \Rightarrow 2^{10} \times 2^1 = 2^{11} = A_0 \cap A_{10}$$