3 .5.	Microprocessor and Assembly Language Programming
	Microprocessor - CPU of a computer built into a single IC chip.
	* Microcomputer -> A computer having microprocessor as its CPU.
1	Microcontroller -> entire computer built into a single IC chip.
#	Generation of Computers
and the same of th	1st Generation -> Vacuum tubes
	2nd Generation > Transistors
	3rd (generation -> IC Chip/LSI (Integrated)
	4th Generation -> MP/VISI/ULSI
	5th Generation -> AI/ Bio-chips
#	I C Fabrication Technology
	557 → Small Scale Integration → Upto 10 gates/chi
	MSI - Medium Scale Integration > 10-100 gates/ch
	LSI → large Scale " → 1000 - 100 1000 "
	VISI -> Very Large Scale "-> 1000,000 "
	ULSI -> Ultra Large Scale ">> 100000 gates/chip
	History of Microprocessor INTEL Series
	1971 4004 → First microprocessor (4-bit)
	1972 8008 → 8- bit
11	1974 8080 → 8- bit
	1074
	1 ० सगम रटेसनरी सप्लायर्स एण्ड फोटोकपी सर्भिस
	8086 → 16 - bit बालखुमार्च, लिलार 오르×१५९९५९२ 8088 NCTT College
11	THE THE PARTY OF T

Inpu de A fob \Box_{Ω} Sin

Th

80:	Section of the sectio	slassmate One One
803	186	
	iom 1/11/111/1	
The second secon	The state of the s	
1/0 In	terfacing Devices	
The state of the s		or & microcomputer
A micros	Processor is a co	or a microcomputer
clock	niven register b	aud electronic device that
reads b	inary instructions	from a storage device
called m	emany, accepts	binary data as input
and pro	cesser data	according to those
instruction	& & provides H	according to those esult as output.
built int	T, CPV of a	digital computer
micropro	o a Single I	c chip is called
	203501	
		MPU
	Registerss	
	V	
	ALU	
	CU	
Other constraints or the contrast dates of t		
		MHz
1	1 5 116	ranges from MHC to

GHZ.

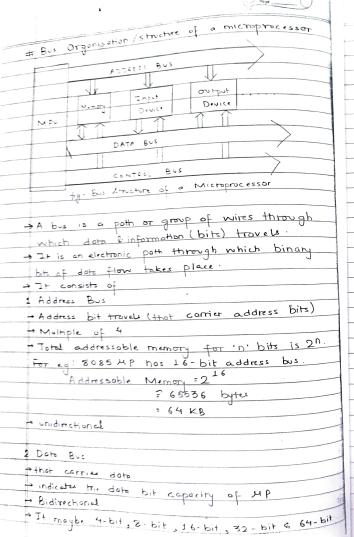
A microcomputer on the other hand is the digital computer having microprocessor as its cou MPU Registers ALU 20 ortput Input unit Primary storage Secondary storage tig: Microcomputer The advancement in the development of semiconductor devices (IC's) led to the invention of microcontroller A microcontroller is a semiconductor device which is fobricated to include mpu, memory, I/O and other (UB) penditive) within the same IC-package. In short, entire digital computer built into a single Ic-chip is known as microcontroller Microprocesso MPU Unit 1/0 Memory Peripheral Devices AID Converter Timer Serial I/O etc. fig: Microcontroller



	Date
	NAT
-	clock speed is in the range of MHZ. It is used for specific purpose.
#	Application of microprocessor Microprocessor can be found in variety of products Microprocessor can be classified primarily The applications can be classified primarily into two categories (1) Re-programable system (2) Embedded system
	Reprogrammable system is a microcomputer system that uses microprocessor as its computing unit.
	In embedded system, the MP is a part of final product and is not available for reprogramming to end-under user eg: Traffic light control system.
1	Summary of Applications Microcontroller Industrial Control
3 4.	Robotice Medical Equipment (CT Scanner etc) Washing Machine
6	Traffic light control etc
	3

#	Evolution	of mic	Toprocessor	(Summar)	Classoute Case Page Cable	
	Processor		Clock Speed	Databus	Address bus	T
I	4004	1971	108 KHz	4-bit	10-bit	t
2	8008	1972	200 KHz	8 - bit	14-bit	T
Т	8080	1974	2 MHz	8- P!+	16 - bit	T
E	8085	1976	5 MHz	8 - bit	16-bit	
L	8086	1978	5 MHz	. 16- bit	20-bit	
	8088	1979	5 MAZ	8 - P.H	20 - bi +	
5	80386	1985	16 MHz	32 - bit	32 - bit	
E	Pentium I	1993	60 MHz	32/64-bit	32 - bit	L
R	Penhum II	1997	233 MHz	64 bit	36- bit	
エ	:					L
E	Pentium IV	2 000	1.46Hz	64 bit	64-bit	L
S	Xenon	2001	1.79Hz			L
	Pentium M	2003	1.79HZ			-
	Dual Core	2005	2.8 GHZ	32611		1
	Core 2 Duo	2006	2.66 9 Hz	32-bit		-
	A tom	2008	1.86 9112			
	2nd gen core	2010	3.8 GHz			
	3rd gen core	2012	2.9 G Hz			_
	17	2008				
	Ιs	2009				
	T ₃	2010				_
	Ig					_
	2		•			_

- 5 -



	Control Bus That carries control signals The width of a bus depend upon the types of control signals used Control signals maybe memory read, memory write, I/O read, I/O write
-	Control signal maybe memory read, memory write,
#	Control signal maybe memory read, memory write,
#	1/0 reas , 1/0 v
#	
	Concept of Fetch, Decode & Execute:
_	It constitutes a basic instruction eyele of a
	microprocessor.
	(Fetch)
(5	Torage Decode - CU
	Executer
-	NEO .
#	Computer Architecture
	TOTAL CONTINUES
	Architecture Architecture
	No No man Architecture
7	33
	Nau Mann (Inden
	Program & CPU I/O Nomann Comp
	Program & CPU 170 by 1 Data Memory
	Data Memory
*	Data Memory A history Hardward Howard
*	Data Memory Hardvard Architecture Hardward Howard Hathaway Aiken
×	Program C PU Data Program C PU Data Memory Memory Memory
*	Hardvard Attentitecture Hardward Attentitecture Hathaway Aiken Program CPU Data
**	Von - Neumann Architecture John Von - Neumann Architecture

- 6 -

Billing - on the last in the first the form

Hardvard Architecture. Von-Nieumam Architecture - It is a theoretical design based. It is a modern computer anthitecture based on the Harvard on the stored-program computer Mark I relay-based comp model concept. + It uses separate memory - It uses some physical memory address for instructions and address for instructions and data. data + Processor needs two clock cycles + Processor needs one cycle to complete an instruction. to execute an instruction. Simpler control unit design and o control unit for two buses development of one is cheaper is more complicated which adds to the development and faster. cost. Data transfers and instruction. - Data transfers and instruction fetches cannot be performed fetches can be performed simultaneously at the same time Used in personal computers, + Used in micro controllers laptops and workstations and signal processing

CHAPTER 2: Introduction to 8085 Features: 1. Introduced in 1976 40-pin DIP (Dual Inline Package) 3. 8 - bit MP Data bus width = 8 - bit Address bus = 16 - bit Total Addressable memory . 2 16= 65536 bytes 4 It uses single +5V power supply 5 Operating frequency (max m) = 5 MHz Upward composible with 8080A 7 Supports large no of instructions. ×1 ×2 40 20 SID 28 High-Order Address Bus Ag SOD Tryph 6 8 - 19 AD2 ST 7. 5 Multiplexed T 5.5 Adress/Dota Lower- Order 5 12 A 30 EADY HOLD → 10/N ESET operation read strings in sand special on NTA 11 ME Milye & april por to 3- y califaction as LDA fig PIN Diagram of 8085 A CLE

on Explainter from a Clar