

## Chapter - 1

### how Frequency Transistor Amplifier Circuit

#### Multistage Amplifier :-

Amplifier that creates voltage, current and power gain through the use of two or more stage are gain called multistage amplifier.

In multi-stage amplifier, the output of the first stage becomes the input for the second stage, the output of the second stage becomes the input to the third stage and so on.

#### Need of cascading of amplifiers:

The output from a single stage amplifier is usually insufficient to drive the output device. In other words, the gain of a single amplifier is inadequate for practical purposes. So, additional amplification over two or three stages is necessary to achieve this output of each amplifier is coupled in some way to the input of the next stage. The resulting system is referred to as multistage amplifier.

In multistage amplifier, a number of single amplifiers are connected in cascade arrangement through a suitable coupling device and so on. The purpose of coupling device (capacitor, transformer etc) is:

- to transfer ac output of one stage to the input of the next stage.
- to isolate the dc conditions of one stage from the next stage.

### # Gain Calculation of n-cascaded amplifier :-

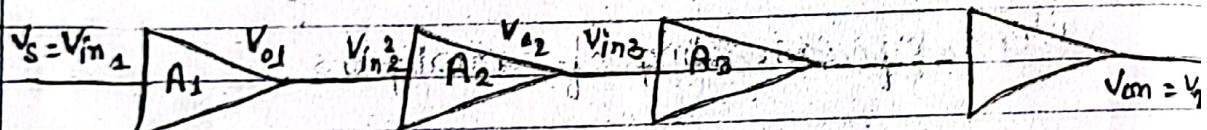


Fig: n-cascaded amplifier

Here input to the first stage is  $V_{in1} = V_s$  and the output of the last stage is  $V_{on} = V_L$ . Here,  $A_1, A_2, A_3 \dots A_n$  are the voltage gain of each stage.

Now,

$$A_1 = \frac{V_{o1}}{V_{in1}} \Rightarrow V_{o1} = A_1 \times V_{in1}$$

$$A_2 = \frac{V_{o2}}{V_{in2}} \Rightarrow V_{o2} = A_2 \times V_{in2}$$

Before:

Therefore,

$$V_{o2} = A_2 \times V_{o1} [\because V_{in,2} = V_{o1}]$$

$$\therefore V_{o2} = A_2 \times A_1 \times V_{in,1}$$

Similarly, for  $n$ -stage,

$$V_{on} = A_1 \times A_2 \times A_3 \times \dots \times A_{n-1} \times A_n \times V_s [\because V_{in,n} = V_s]$$

$$\text{or, } V_{on} = A_1 \times A_2 \times A_3 \times \dots \times A_{n-1} \times A_n \times V_s$$

$$\therefore V_L = A_1 \times A_2 \times A_3 \times \dots \times A_{n-1} \times A_n \times V_s$$

$$\therefore A_{\text{total}} = A_1 \times A_2 \times A_3 \times \dots \times A_{n-1} \times A_n \quad (I)$$

$$V_{os} = A_1 \times A_2 \times A_3 \times V_{in,1}$$

Thus, the overall voltage gain<sup>s</sup> of  $n$ -stage cascaded amplifier is equal to the product of the gain of individual stages.

Gain in dB :-

When the gains are expressed in dB, the overall gain of the multistage amplifier is equal to the sum of the individuals.

Gain expressed in dB:

Taking log on both sides of eq (I), we get

$$20 \log (A_{\text{total}}) = 20 \log (A_1 \times A_2 \times A_3 \times \dots \times A_{n-1} \times A_n)$$

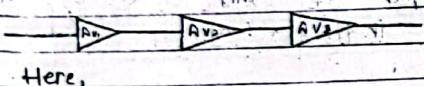
$$= 20 \log (A_1) + 20 \log (A_2) + 20 \log (A_3) + \dots + 20 \log (A_n)$$

$$\begin{aligned} 10 \log(P) &= 10 \log\left(\frac{V^2}{R}\right) = 10 \log(I^2 R) \\ &= 20 \log\left(\frac{V}{R}\right) = 20 \log(IR) \end{aligned}$$

In power  $\rightarrow 10 \log$   
In voltage + current  $\rightarrow 20 \log$

### Numerical

- \*1 A 3 stage amplifier has a voltage gain of 50, 100 & 200 for 1<sup>st</sup>, 2<sup>nd</sup> & 3<sup>rd</sup> stage. Find the overall voltage gain of the amplifier. Also express the gain of each stage and overall voltage gain in dB.



Here,

$$A_{v1} = 50, A_{v2} = 100, A_{v3} = 200$$

Now,

$$A_{\text{total}} = A_{v1} \times A_{v2} \times A_{v3} = 50 \times 100 \times 200 = 10,00,000$$

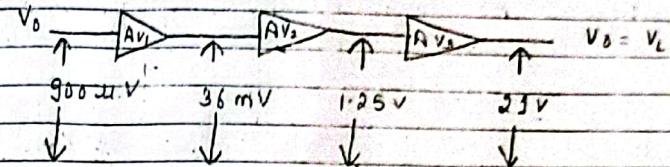
$$A_{v1} \text{ in dB} = 20 \log(50) = 20.98 \text{ dB}$$

$$A_{v2} \text{ in dB} = 20 \log(100) = 40 \text{ dB}$$

$$A_{v3} \text{ in dB} = 20 \log(200) = 46.02 \text{ dB}$$

$$(A_{\text{total}}) \text{ dB} = 20.98 + 40 + 46.02 = 120 \text{ dB}$$

The 3 stage amplifier is shown below:-



Find  $A_{v1}$ ,  $A_{v2}$ ,  $A_{v3}$  and  $V_L$  in dB.

Here,

$$A_{v1} = \frac{36 \times 10^{-3}}{900 \times 10^{-3}} = 40 \text{ V}$$

$$A_{v2} = \frac{1.25}{36 \times 10^{-3}} = 34.722 \text{ V}$$

$$A_{v3} = \frac{23}{1.25} = 16.8 \text{ V}$$

$$\frac{V_L}{V_s} = A_{v1} \times A_{v2} \times A_{v3} \quad \text{Also, } = 21$$

$$\frac{V_L}{V_s} = 23333.333 \quad 900 \times 10^{-6} = 23333.333$$

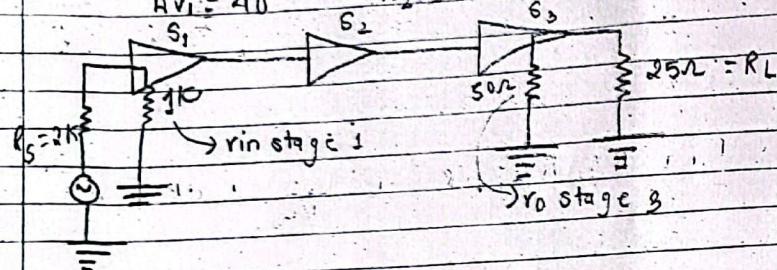
$$\left( \frac{V_L}{V_s} \right) \text{dB} = 86.93 \text{ dB}$$

Find  $V_L$  when the multistage amplifier is

driven by a single source having resistance of 2 k $\Omega$  and a load resistance of 250  $\Omega$ .

Stage-1 has the input resistance of  $1\text{ k}\Omega$  and  
stage-3 has output resistance of  $50\Omega$

$$AV_1 = 40 \quad AV_2 = 94.72 \quad AV_3 = 16.8$$



Solution.

$$\frac{V_L}{V_s} = \frac{AV_1 \times AV_2 \times AV_3 \times \text{rin stage } 1 \times R_L}{\text{rin stage } 1 + R_1 + \text{routage } 3}$$

$$= \frac{40 \times 94.72 \times 16.8 \times \frac{1k}{1k+2k} \times 25}{25+50}$$

The open circuit voltage gain of the stage in a multistage amplifier are

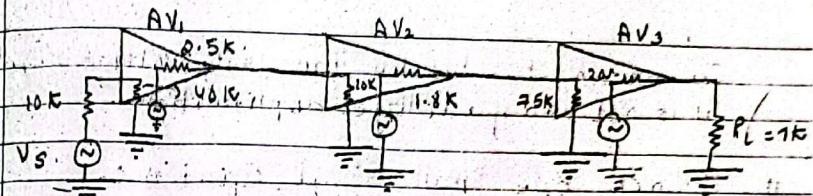
$$AV_1 = -40$$

$$AV_2 = -26$$

$$AV_3 = 1.8$$

Find the overall voltage gain  $\frac{V_L}{V_s}$

P.R.O



Here,

$$\begin{aligned} \frac{V_L}{V_s} &= \frac{AV_1 \times AV_2 \times AV_3 \times 40}{40+10} \times \frac{20}{20+2.5} \times \frac{75}{75+1.8+20} \\ &= \frac{1965.6 \times 4 \times 20}{5} \times \frac{45}{22.5} \times \frac{1000}{76.8} \times \frac{1020}{1020} \\ &= 1338.235 \end{aligned}$$

Choice of configuration in cascade :

→ In common base, common emitter and common collector configuration are compared in terms of their current gain, voltage gain, input impedance, output impedance.

→ The common emitter configuration has high current and voltage gain. It also has moderate input and output impedance. So, CE is preferred for amplification purpose.

→ The common base configuration also has high voltage gain but its input resistance is very low so, CB cannot be used in intermediate stage while calculating.

→ Common collector has less than unity voltage gain so it is not used for voltage amplification.

# Common Base Small Signal Equation :-

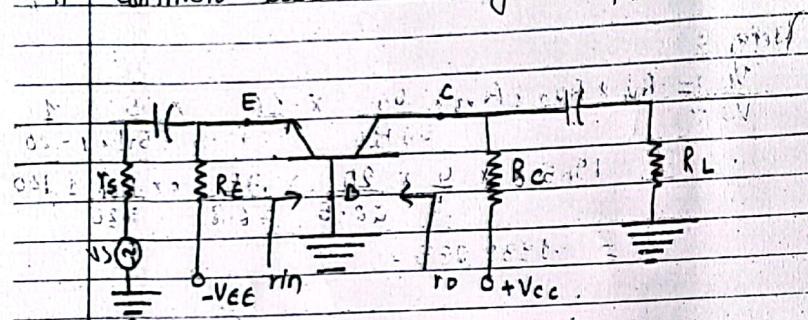


Fig : Common Base configuration

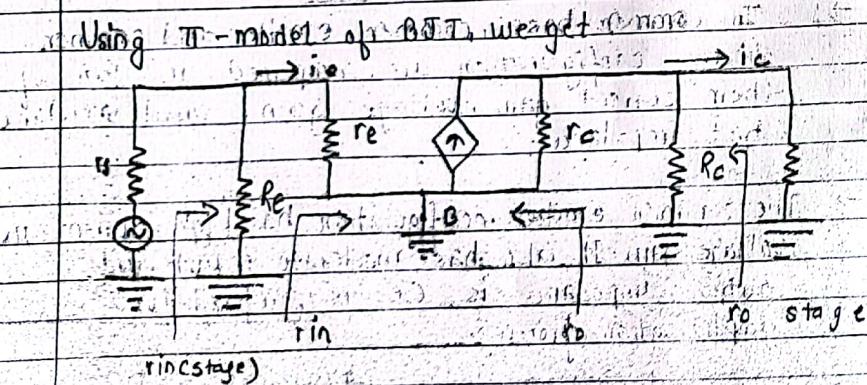


Fig : ac equivalent model of cb amplifier

Formula :-

$$r_e = \frac{26 \text{ mV}}{I_e} = 0.026$$

$$r_{in} = r_e$$

$$r_o = r_c$$

$$r_{in\ stage} = R_E // r_e \approx r_e$$

$$r_{o\ stage} = R_C // r_c \approx R_C$$

$$\text{Voltage gain (Av)} = \frac{\alpha R_C}{r_e}$$

$$= r_{o\ stage} = r_c // R_C \approx R_C$$

$$\text{Current gain (A_i)} = \frac{i_{output} - i_c}{i_{input} - i_e} = \frac{\alpha i_e - i_c}{i_e - i_e} = \alpha \approx 1$$

$$Av_s = \frac{V_L}{V_s} = \frac{Av}{(1 + r_{in\ stage}) (1 + \frac{R_L}{R_C + r_{o\ stage}})}$$

$$I_L = A_i s = \frac{V_L}{V_s} \left( \frac{r_s + r_{in\ stage}}{R_L} \right)$$

Common Emitter Bypassed :-

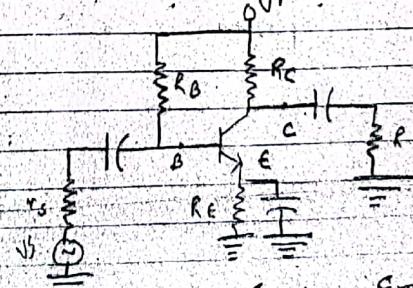
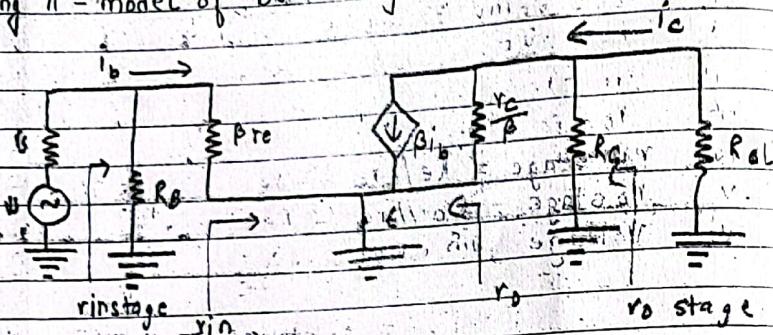


Fig :- Common Emitter Bypassed

Using  $\pi$ -model of BJT we get



Formula:-

$$i) r_e = 0.026 \text{ I}_E$$

$$vi) A_{vI} = \frac{R_C}{r_e}$$

$$ii) r_{in} = \beta_B r_{in}$$

$$iii) r_o = r_C / \beta_B$$

$$iv) r_{in stage} = R_B // r_{in}$$

$$v) r_{o stage} = R_C // r_C \approx R_C$$

$$\left( \frac{R_C}{R_L + r_{o stage}} \right)$$

$$ix) i_L = \frac{V_L}{V_S} \left( r_{in} + r_{in stage} \right)$$

Common emitter unbypassed :- Capacitor is absent  
 $r_{CE}$  is present.

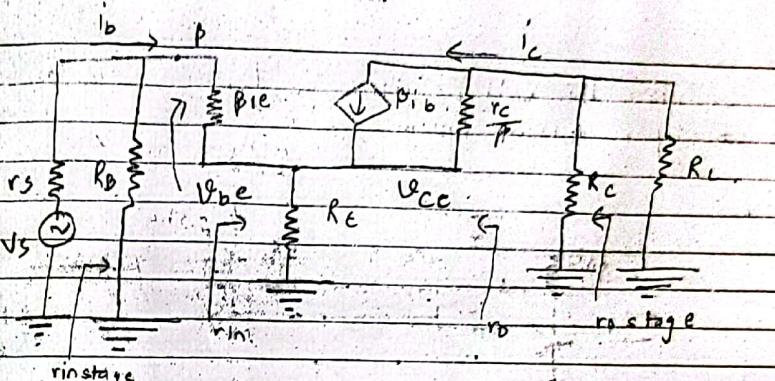
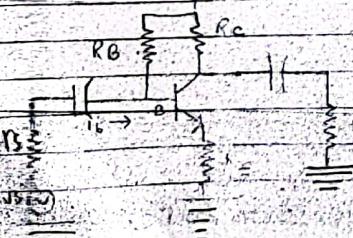


Fig: ac equivalent CE amp.

Formula:-

$$i) r_e = 0.026 \text{ I}_E$$

$$ii) r_{in} = \beta_B (r_{in} + r_C)$$

$$iii) r_{in stage} = R_B // r_{in}$$

$$iv) r_o = r_C / \beta_B$$

$$v) r_{o stage} = R_C // \frac{r_C}{\beta_B} \approx R_C$$

$$vi) A_{vI} = - \frac{R_C + R_L}{r_{in} + R_C}$$

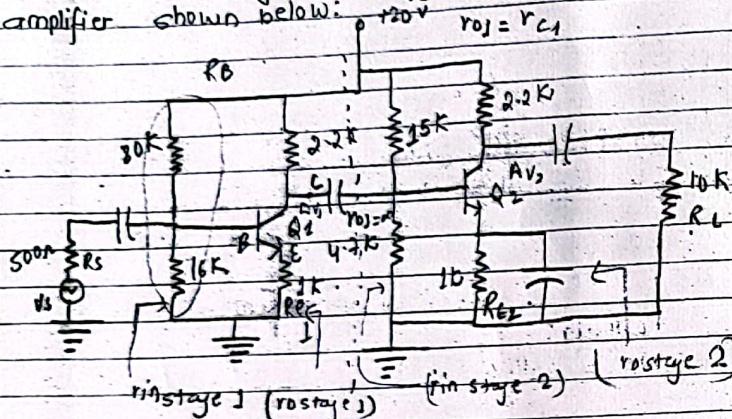
$$vii) \beta_A = \beta_B$$

$$viii) \frac{V_{Ls}}{V_S} = A_{vI} \left( \frac{r_{in} + r_{in stage}}{r_{in} + r_{in stage} + r_o} \right) \left( \frac{R_L}{R_L + r_{o stage}} \right)$$

$$ix) \frac{i_L}{i_s} = \frac{V_L}{V_S} \left( \frac{r_{in} + r_{in stage}}{R_L} \right)$$

Sire IMP. 8 mar<sup>2</sup>

Calculate the voltage gain  $V_L$  for the cascade BJT amplifier shown below:



$$\frac{V_L}{V_S} = A_{V_1} \times A_{V_2} \times \left( \frac{r_{in, stage 1}}{r_{in, stage 1} + R_S} \right) \times \left( \frac{r_{in, stage 2}}{r_{in, stage 2} + r_{out, stage 1}} \right) \times \left( \frac{R_L}{R_L + r_{out, stage 2}} \right) \quad (I)$$

Let us assume  $\beta_1 = \beta_2 = 100$  and  $r_{o1} = r_{o2} = 80\Omega$ ,  $r_{e1} = r_{e2} = 100\Omega$

For the first stage transistor, Q1,

$$r_{in, stage 1} = 80\Omega // 16k\Omega // \beta (r_{e1} + R_{E1})$$

$$= \frac{80 \times 16}{80 + 16} // \beta (r_{e1} + R_{E1})$$

$$= 10.33 // 100 \left( \frac{80 + 1}{1000} \right)$$

$$= \frac{10.33 \times 100}{100 + 10.33}$$

$$= 11.86 k\Omega$$

12.

$$r_{out, stage 1} = R_C // r_{o1} / \beta = R_C // \infty = R_C = 2.2k\Omega$$

$$A_{V1} = - \frac{R_C}{r_{e1} + R_E} = \frac{2.2k\Omega}{\frac{80 + 1}{1000}} = -2.037 k\Omega$$

For the second stage transistor, Q2,

$$r_{in, stage 2} = 15 // 4.7 // \beta r_{e2}$$

$$= \frac{15 \times 4.7}{15 + 4.7} // \frac{80 + 100}{1000}$$

$$= 2.44k\Omega$$

Now,

$$r_{out, stage 2} = R_C // r_{o2} / \beta$$

$$= R_C = 2.2k\Omega$$

$$A_{V2} = - \frac{R_C}{r_{e2}} = \frac{2.2k\Omega}{\frac{80}{1000}} = -27.5k\Omega$$

$$\frac{V_L}{V_S} = A_{V1} R_o A_{V2} \times \left( \frac{r_{in, stage 1}}{r_{in, stage 1} + R_S} \right) \times \left( \frac{r_{in, stage 2}}{r_{in, stage 2} + r_{out, stage 1}} \right) \times \left( \frac{R_L}{R_L + r_{out, stage 2}} \right)$$

$$= -2.037 \times -27.5$$

$$= -2.037 \times -27.5 \times \frac{11.86}{\frac{11.86 + 500}{1000}} \times \left( \frac{2.44}{2.44 + 2.2} \right) \times \left( \frac{10}{10 + 2.2} \right)$$

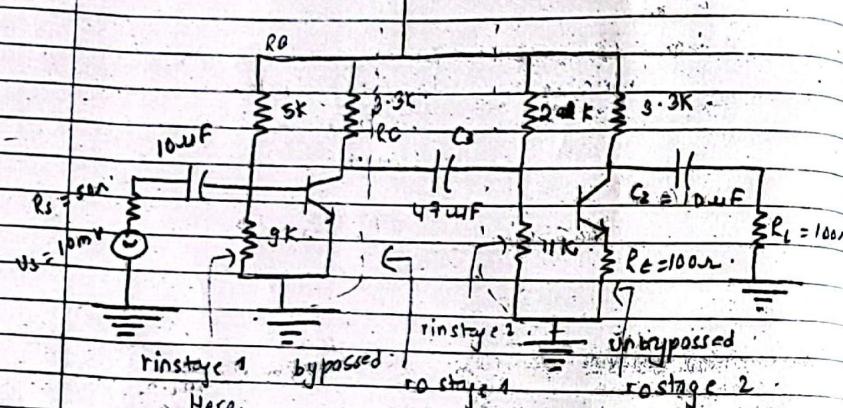
$$\therefore \frac{V_L}{V_S} = 28.2$$

13.

Surely

Calculate the voltage gain  $V_L$  for the cascade BJT amplifier shown below. Assume  $r_{e1} = r_{e2} > 20\text{ k}\Omega$ ,  $\beta_1 = \beta_2 = 100$ .

$$+V_{cc} = 10\text{V}$$



Now,

$$\frac{V_L}{V_S} = A_{v1} \times A_{v2} \times \left( \frac{r_{in, stage 1}}{r_{in, stage 1} + R_s} \right) \times \left( \frac{r_{in, stage 2}}{r_{in, stage 2} + r_{out, stage 1}} \right)$$

$\downarrow R_L$

$\downarrow R_L + r_{out, stage 2}$

$$\begin{aligned} r_{in, stage 1} &= R_B / r_{in} \\ &= 5k\Omega / 9k\Omega / \beta \cdot r_e \\ &= 5 \times 9 / \beta \cdot 5 \\ &= \frac{45}{14} \times 5 \beta \\ &= \frac{160.714}{14 + 5 \beta} \end{aligned}$$

14.

# Common Collector Small Signal Equation: (Emitter follower)  $+V_{cc}$

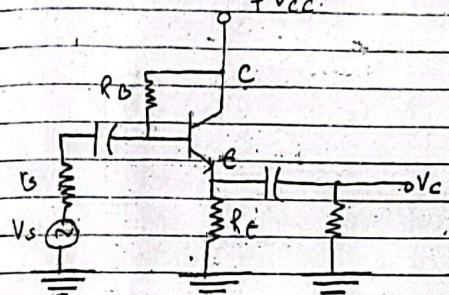


Fig: Common Collector.

Formula:

i)  $r_e = 0.026$   
 $I_E$

iv)  $r_{out, stage} = R_C / (\beta \cdot r_e)$

ii)  $r_{in} = \beta (r_e + r_{in})$   
where  $r_{in} = R_E / (R_E + r_L)$

v)  $A_v = r_L / (r_e + r_L)$

vi)  $A_i = \beta$

iii)  $r_{in, stage} = R_B / r_{in}$

vii)  $A_{vS} = \frac{V_L}{V_S} = A_v / (r_{in, stage} / (R_L + r_{in, stage}))$

viii)  $i_L = \frac{V_L}{R_L} \left( r_s + r_{in, stage} \right)$   
 $i_S = \frac{V_S}{R_L}$

15.

distortion can be divided into following types:-

Non-linear distortion

Linear distortion

Non-linear distortion :-

This type of distortion occurs when the transistor operates in non-linear region of its output characteristic.

In the time domain, this type of distortion is also called amplitude distortion, while in frequency, it is called harmonic distortion.

Linear distortion :-

This type of distortion occurs when the large signal is applied to the input of the device and the device operation are in the linear region of its characteristic.

Amplitude distortion :-

When the input signal is increased the operation in the amplifier becomes non-linear and the output current  $I_C$  no longer becomes the true sinusoidal sinusoidal so the upper part of the amplified waveform is more than the lower part such distortion is called amplitude distortion.

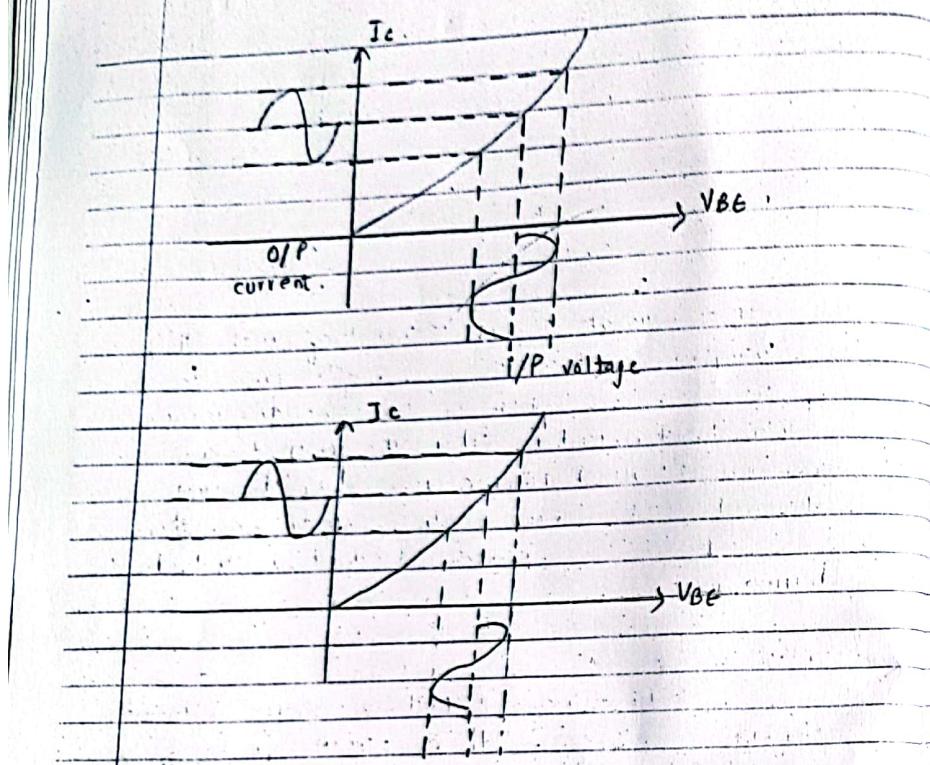
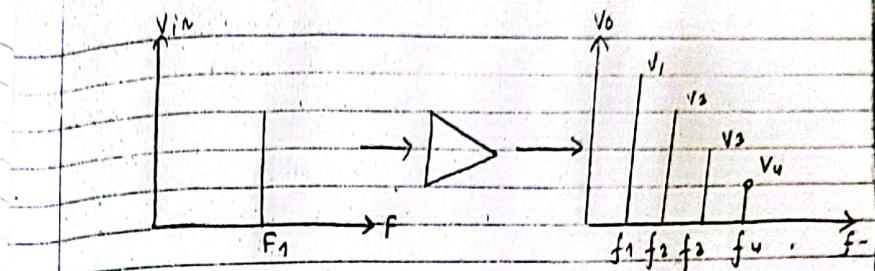


Fig : Amplified distortion .

#### \* Harmonic distortion :-

The frequency domain of non-linear distortion is shown below. Here, the input consists of single frequency but the output consists of dc components as well as different frequency components.



If the input signals consist of more than one frequency intermodulation distortion occurs. If the input signals contain two frequencies namely  $F_1$  and  $F_2$  then the output will contain their harmonic  $F_1, 2F_1, 3F_1$  and  $F_2, 2F_2, 3F_2$  etc. In addition, there would be the components  $(F_1+F_2)$  and  $(F_1-F_2)$  harmonics.

#### \* Frequency distortion :-

Frequency distortion occurs when the amplifier amplifies the different frequency components differently, i.e. the frequency components of the signals are not amplified equally.

#### \* Phase distortion :-

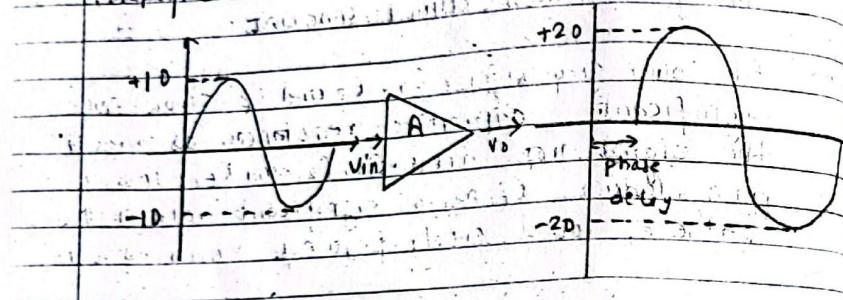
If the delay introduced by the amplifier is diff. different for various frequencies, a phase distortion occurs.

If this distortion is not important in

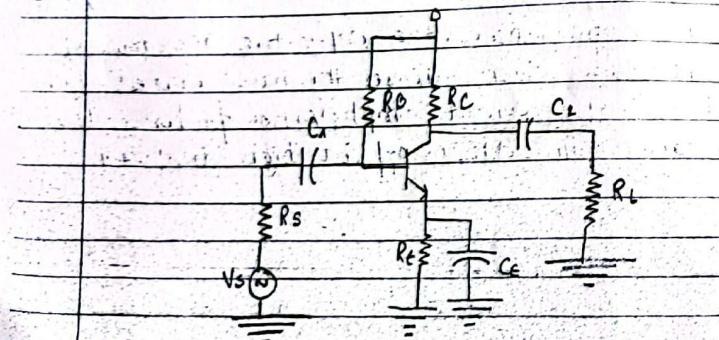
modulation is reflected in the output frequency to lower frequency

audio amplifiers as our ear are not capable of distinguishing the relative phase of different frequencies.

→ But this distortion is objectionable in video amplifiers used in television.



# Effect of bypass capacitor on frequency response:



A voltage divider or self-bias circuit is shown in the figure. Here,  $C_1$  and  $C_2$  are coupling

capacitor and  $C_c$  is the bypass capacitor.

→ At the medium frequencies,  $C_1$ ,  $C_2$  and  $C_c$  provides an effectively short circuit path for the signal, as a result there will be no signal drop across  $C_1$ ,  $C_2$  and  $R_e$ , thus the gain remain almost constant.

→ At lower frequencies,  $C_1$ ,  $C_2$  and  $C_c$  show some significant capacitive reactance, as a result the signal drop across  $C_1$ ,  $C_2$  and  $R_e$ , thus the gain reduces.  $C_c$  has a significant role on the value of lower cut-off frequency which equal to

$$f_l(C_c) = \frac{1}{2\pi R_e C_c}$$

$$\text{where, } R_{e'} = R_e // (r_{e'} + \frac{R_s // R_1 // R_2}{\beta})$$

→ At high frequencies, the capacitive reactance of  $C_c$  is low which increases the base current. This reduces the current amplification factor  $\beta$ . Thus, voltage gain drops off at high frequency.

## Frequency Response of BJT Amplifier

To voltage gain of the amplifier varies with the signal frequency due to the effect of variations in circuit capacitive reactance.

The graph plotted between the voltage gain and signal frequency of an amplifier is known as frequency response of an amplifier.

$F_1$  = lower cutoff frequency.

$F_2$  = higher cutoff frequency.

BW = Bandwidth.

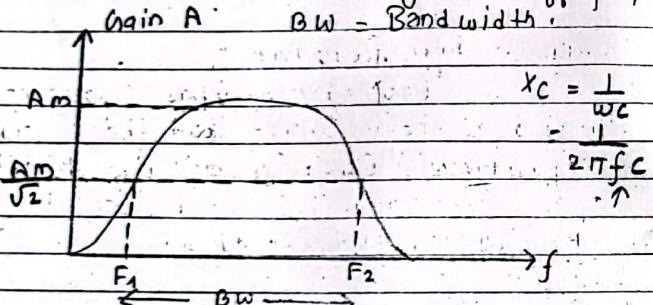


Fig : Frequency Response of an amplifier.

→ If the input voltage of the amplifier is kept constant and its frequency is varied, it is observed that the amplifier gain:

- remains constant over the mid-band gain frequency.
- falls off at low and high frequencies.

The low and high frequency at which the gain becomes  $1/\sqrt{2}$  times the mid-band gain are called lower and upper cut-off frequencies.

OR, low or high frequency at which the power become half of the mid-band power are called lower and upper cut-off frequency.

Gain at low frequencies :-

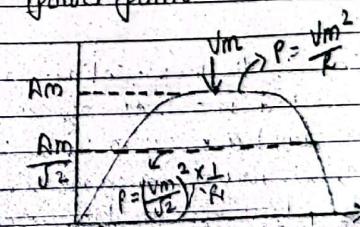
In low frequency, the gain is reduced as coupling and bypass capacitors are included in equivalent circuit.

Gain at high frequencies :-

Coupling and bypass capacitors are treated as short circuit but the internal capacitances  $C_{be}$ ,  $C_{ce}$  and  $C_{be}$  do not effectively open circuit and they provide shunt path. As a result, gain is reduced.

3dB frequencies or half-power point.

Let, the voltage at the mid-band range be  $V_m$ , then the power at the mid-band or cut-off frequencies are:



$$P_{\text{mid-band}} = \frac{V_m^2}{R}$$

$$\begin{aligned} P_{\text{cut-off}} &= \left(\frac{V_m}{\sqrt{2}}\right)^2 \times \frac{1}{R} = \frac{V_m^2}{2} \times \frac{1}{R} \\ &= \frac{1}{2} \times \frac{V_m^2}{R} \\ &= \frac{1}{2} \times P_{\text{mid-band}} \end{aligned}$$

The cut-off frequencies are also called half-power points.

Now in dB,

$$10 \log (P_{\text{cut-off}}) = 10 \log \left( \frac{P_{\text{mid-band}}}{2} \right)$$

$$\therefore 10 \log (P_{\text{cut-off}}) = 10 \log (P_{\text{mid-band}}) - 10 \log (2)$$

$$\therefore 10 \log (P_{\text{cut-off}}) = A_m (\text{dB}) - 3$$

$\therefore$  The difference between  $F_1$  and  $F_2$  is called bandwidth.

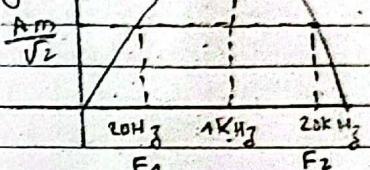
$$BW = F_2 - F_1$$

- # An audio-amplifier has a lower cutoff frequency of 20 Hz and upper cutoff frequency of 20 kHz. The amplifier delivers 20W to a 12Ω load at frequency 1 kHz
- What is the bandwidth of the amplifier.
  - What is rms load voltage at 20 kHz?
  - What is rms load voltage at 2 kHz?

Here,

$$\begin{aligned} BW &= F_2 - F_1 \\ &= 199.8 \text{ kHz} = 19.98 \text{ kHz} \end{aligned}$$

$$\frac{P_{\text{mid-band}}}{20W}$$



(ii) rms load voltage at 20 kHz

$$\begin{aligned} P_{\text{cut-off}} &= \frac{20}{2} = 10 \text{ W} \\ P &= \frac{V^2}{R} \end{aligned}$$

$$V^2 = P \times R$$

$$= 10 \times 12$$

$$V = \sqrt{120}$$

$$\therefore V = 10.95 \text{ V}$$

(iii) Similarly, rms load voltage at 1 kHz

$$P_{\text{cut-off}} = 20 \text{ W}$$

$$P = \frac{V_m^2}{R}$$

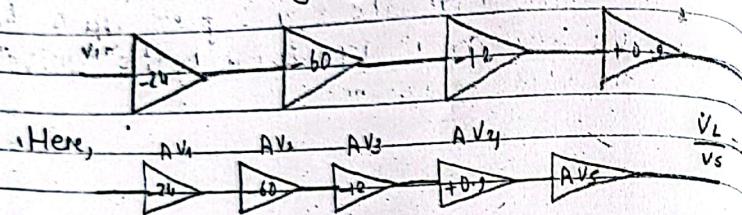
$$V^2 = 20 \times 12 = 240$$

$$V = 15.49 \text{ V}$$

TNP

The voltage gains of stages in a multistage amplifier are shown below.

- i) Find the voltage gain that would be necessary in the fifth stage which if added to the cascade could make the voltage gain  $10^6$ .



$$AV_5 = ?$$

In dB,

$$(AV_5)_{dB} = ?$$

$$\frac{V_L}{V_s} = AV_1 \times AV_2 \times AV_3 \times AV_4 \times AV_5$$

$$10^6 = -24 \times -60 \times -12 \times 0.9 \times AV_5$$

$$AV_5 = -64.3 \text{ dB} \quad (\text{round off by } \pm 0.1 \text{ due to negative sign})$$

Now,

In dB,

$$\begin{aligned} (AV_5)_{dB} &= 20 \log (-64.3) \\ &= -36.16 \text{ dB} \end{aligned}$$

Coupling capacitance and low frequency response:-

The lower cut-off frequency of an amplifier is affected by the coupling capacitance in series with the signal flow path. An amplifier can be represented by its equivalent circuit as shown below :-

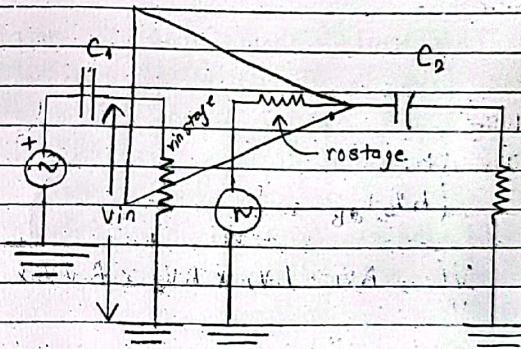


Fig :- Equivalent circuit

Now,

$$V_{in} = r_{instage} \times V_s$$
  
$$(r_{instage} = jX_{C1})$$

$$\text{where, } X_{C1} = \frac{1}{\omega C_1}$$

Taking absolute value,

$$|V_i| = \frac{r_{instage}}{\sqrt{(r_{instage})^2 + (X_{C1})^2}} \times |V_s|$$

$$|V_i| = \frac{r_{instage}}{\sqrt{(r_{instage})^2 + (\frac{1}{\omega C_1})^2}} \times |V_s|$$

$$= \frac{r_{instage} \cdot \omega C_1}{\sqrt{(\omega C_1 r_{instage})^2 + 1}} \times |V_s|$$

If  $\omega = 0$ , i.e. DC, then  $V_{in} = 0$

If  $\omega \rightarrow \infty$ ,  $r_{instage} = 1$ , then  $V_{in} = \frac{1}{\sqrt{2}} V_s$

This result shows that the amplifier input voltage falls to  $0.707$  ( $1/\sqrt{2}$ ) times the source voltage when the frequency is reduced to  $\frac{1}{2\pi C_1 r_{instage}}$ .

If the source resistance ( $R_s$ ) is also present, the lower cutoff frequency is given by:

$$F(C_1) = \frac{1}{2\pi(r_{instage} + R_s)C_1}$$

Similarly, due to  $C_2$ , the lower cut-off frequency is given by  $F(C_2)$ .

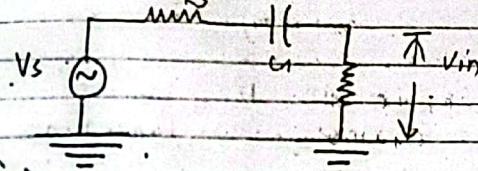
$$F(C_2) = \frac{1}{2\pi(r_{instage} + R_L)C_2}$$

If  $C_1$  and  $C_2$  are different, then overall cut-off frequency will be higher value choosing from  $F(C_1)$  and  $F(C_2)$ .

If  $F(C_1)$  and  $F(C_2)$  are same, then overall cut-off frequency will be

$$F_1 = 1.65 \times F(C_1) \quad \text{Or,}$$

$$F_1 = 1.65 \times F(C_2)$$



~~Derive the expression~~

# Shunt resist capacitance and high frequency response :-

Shunt capacitance affects the high frequency performance of an amplifier because at high frequency, the small capacitive reactance diverts the signal to the ground or to some other point besides the load.

The voltage divider or self-bias is shown below:-

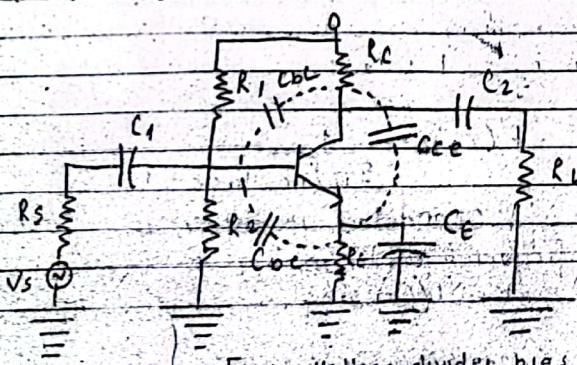


Fig: - Voltage divider bias circuit

Here,  $C_{bc}$ ,  $C_{be}$  and  $C_{ce}$  are inter-electrode capacitance. Their value are in the range of pico Farad (pF). At low and medium frequencies, their capacitive reactance is very high and they behave at an open circuit. At higher frequencies, the coupling capacitors ( $C_b$  and  $C_e$ ) and bypass capacitor ( $C_o$ ) effectively provide the short circuit path. The given voltage divider circuit can be replaced by its equivalent circuit as shown below:-

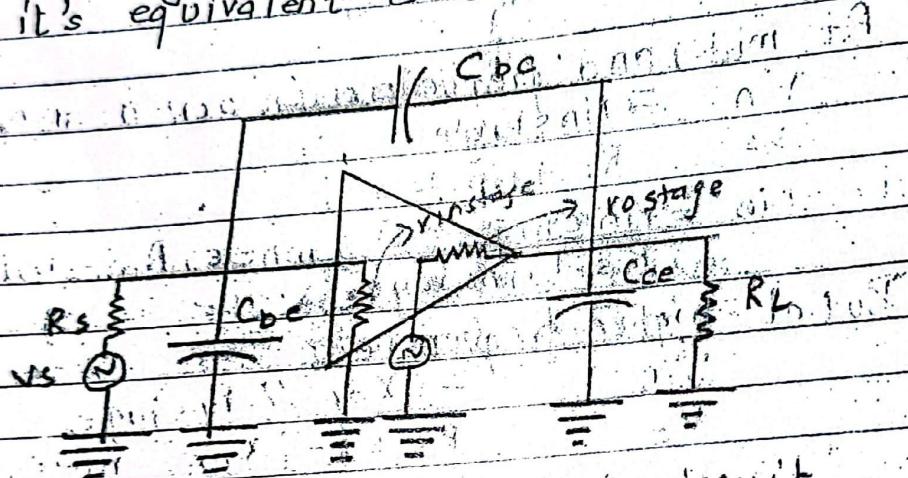


Fig :- Equivalent circuit

Here,  $C_{bc}$  is a capacitance between the input and the output terminals. Using Miller's theorem, this circuit is further simplified as shown below.

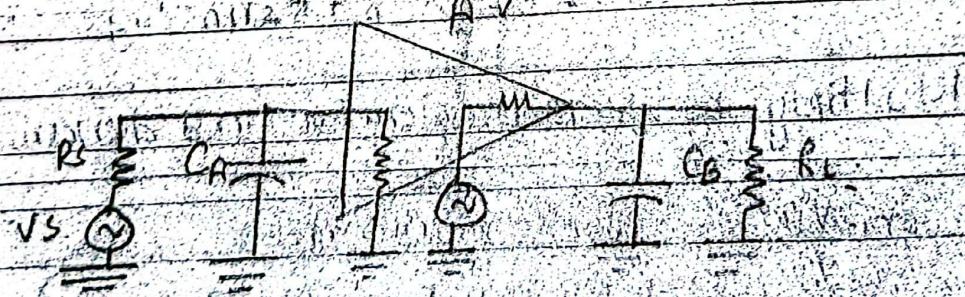


Fig : Simplified Equivalent Circuit

where,

$$C_A = C_{be} + (1 - A_v) C_{bc} + C_{w\text{input}}$$

and  $C_O = C_{ce} + \left(\frac{A_v - 1}{A_v}\right) C_{be} + C_{o\text{output}}$ ,

$$A_v = -R_C // R_L$$

$r_e$

where,  $A_v$  is the voltage gain,  $C_{w\text{input}}$  and  $C_{o\text{output}}$  are wire capacitance at the input and output side respectively.

At mid-band frequencies,  $C_A$  acts as an open circuit

$$\frac{V_{in}}{V_s} = \frac{r_{in\text{stage}}}{R_s + r_{in\text{stage}}}$$

$$\text{ie } A_m = \frac{r_{in\text{stage}}}{R_s + r_{in\text{stage}}} \quad \text{where, } A_m = \text{mid-band gain}$$

But at higher frequencies,

$$\frac{V_{in}}{V_s} = \frac{-jX_{CA} // r_{in\text{stage}}}{R_s + (-jX_{CA} // r_{in\text{stage}})}$$

$$\frac{V_{in}}{V_s} = \frac{-jX_{CA} \cdot r_{in\text{stage}}}{R_s + jX_{CA} \cdot r_{in\text{stage}}} = \frac{-jX_{CA} \cdot r_{in\text{stage}}}{-jX_{CA} + r_{in\text{stage}}}$$

$$\text{or, } \frac{V_{in}}{V_s} = \frac{-jX_{CA} \cdot r_{in\text{stage}}}{R_s jX_{CA} + R_s r_{in\text{stage}} - jX_{CA} r_{in\text{stage}}}$$

Multiply by  $j$  in numerator and denominator,

$$\text{or, } \frac{V_{in}}{V_s} = \frac{-j^2 X_{CA} \cdot r_{in\text{stage}}}{-j^2 R_s X_{CA} + j R_s r_{in\text{stage}} + j^2 X_{CA} r_{in\text{stage}}}$$

$$\text{ori } \frac{V_{in}}{V_s} = \frac{X_{CA} \cdot r_{instage}}{R_s X_{CA} + X_{CA} r_{instage} + j R_s r_{instage}}$$

$$\text{ori } \frac{V_{in}}{V_s} = \frac{\frac{1}{\omega_{CA}} \cdot r_{instage}}{\frac{1}{\omega_{CA}} (R_s + r_{instage}) + j R_s r_{instage}}$$

$$\text{ori } \frac{V_{in}}{V_s} = \frac{r_{instage}}{(R_s + r_{instage}) + j \omega_{CA} R_s r_{instage}}$$

$$\text{ori } \frac{V_{in}}{V_s} = \frac{r_{instage}}{(R_s + r_{instage})} \times \frac{1}{1 + j \omega_{CA} R_s / r_{instage}}$$

$$\text{ori } \frac{V_{in}}{V_s} = \frac{r_{instage}}{(R_s + r_{instage})} \times \frac{1}{\sqrt{1 + (\omega_{CA} R_s / r_{instage})^2}}$$

If  $\omega_{CA} R_s / r_{instage} = 1$ , then

$$\frac{V_{in}}{V_s} = \frac{A_m}{\sqrt{2}}$$

i.e gain is  $\frac{1}{\sqrt{2}}$  times mid-band gain when  $2\pi f_C$

$\parallel r_{instage} = 1$ . Thus value of upper cut-off frequency is given by

$$f_2(C_{CA}) = \frac{1}{2\pi (R_s / r_{instage}) C_A}$$

Similarly, due to  $C_B$ , the upper cut-off frequency is

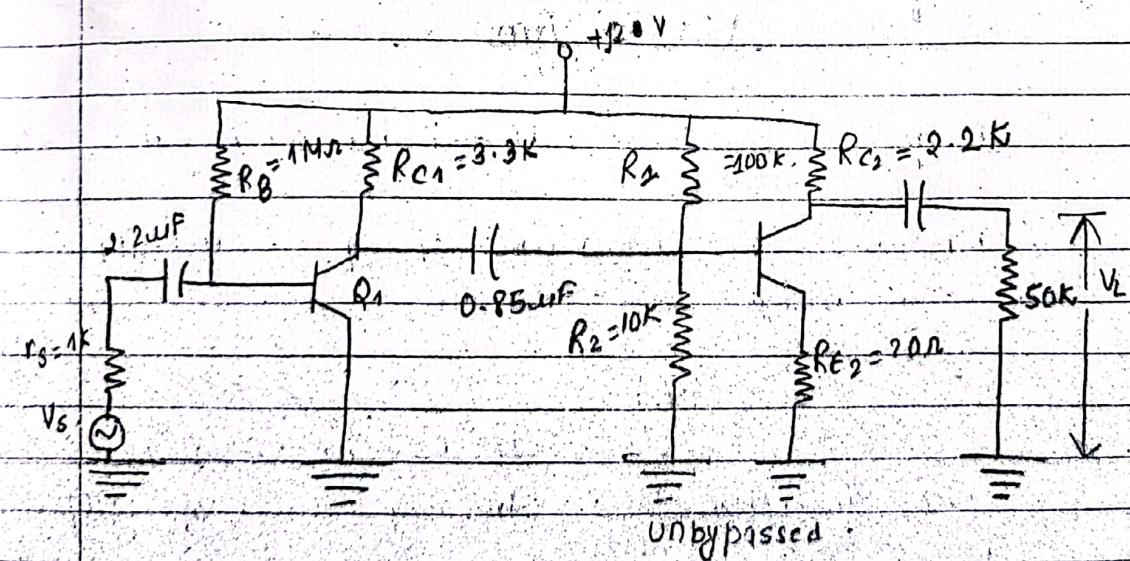
$$f_2(C_B) = \frac{1}{2\pi (r_{instage} / R_c) C_B}$$

The lower value between  $f_2(C_A)$  and  $f_2(C_B)$  will be the value of upper cut-off frequency.

- + The two capacitor coupled common emitter amplifier stages is shown in below. Notice that the ac signal develop at the output of the first stage is coupled ruled  $0.85\ \mu F$  to the input of second stage. Assuming that the transistor are identical and have  $\beta = 100$ ,  $r_c = 1\ m\Omega$  and  $r_e = 15\ \Omega$ . Find the small signal mid-band.

i) Voltage gain ( $\frac{V_L}{V_S}$ )

ii) Current gain ( $\frac{I_L}{I_S}$ )



$$r_{o\ 1} = R_{C1} // r_e$$

Here,

Input resistance of first stage is  
 $r_{in\text{stage } 1} = R_B1 // r_{re}$   
 $= 25\text{ k}\Omega$

Output resistance of stage 1 is

$$r_o \text{ stage 1} = R_E1 // r_{re} = 3.3\text{ k}\Omega // 1\text{ M}\Omega // 100$$
$$= 2.48\text{ k}\Omega$$

The voltage gain of stage 1 is;

$$A_{V1} = \frac{r_o \text{ stage 1}}{r_{re}}$$

$$= -2.48\text{ k}\Omega / 1.25\text{ k}\Omega = -99.2$$

$$r_{in\text{stage } 2} = R_B2 // r_{re} // (r_{o\text{stage 1}} + R_E2)$$
$$= 6.63\text{ k}\Omega$$

Input resistance to second stage is;

$$r_{o\text{stage 1}} = R_E1 // r_{re} = 2.2\text{ k}\Omega // 1\text{ M}\Omega // 100$$
$$= 1.8\text{ k}\Omega$$

Voltage gain of stage 2 is;

$$A_{V2} = \frac{-r_{o\text{stage 2}}}{R_E2 + r_{re}}$$
$$= -1.8\text{ k}\Omega / 2.2\text{ k}\Omega + 2.5\text{ k}\Omega = -7.35$$

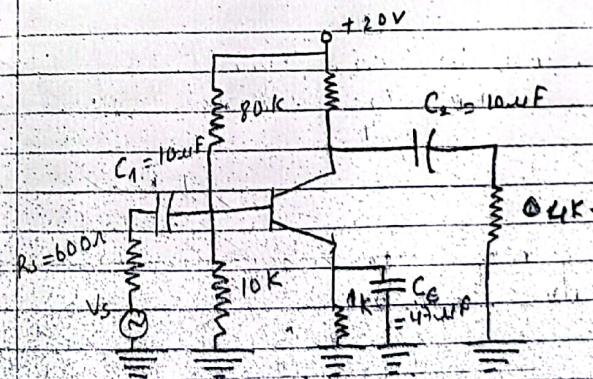
Now,

$$\frac{V_L}{V_S} = A_{V1} + A_{V2} \times \frac{r_{in\text{stage 1}} \times r_{in\text{stage 2}}}{r_o \text{ stage 1} \times r_{in\text{stage 1}} \times r_{in\text{stage 2}} + r_o \text{ stage 1}}$$
$$\times \frac{r_o \text{ stage 2}}{r_L + r_o \text{ stage 2}}$$

$$= 365.95$$

b)  $i_L = \frac{A_{V2}}{r_o \text{ stage 2} + R_L} \times \frac{A_{V1}}{r_o \text{ stage 1} + r_{in\text{stage 2}}} \times r_{in\text{stage 2}}$

For the further given voltage divider circuit determine the low value of lower cutoff frequency.  
Assume  $r_{re} = 2\text{ k}\Omega$ ,  $r_o = 20\text{ k}\Omega$ ,  $\beta = 100$ ,



Hint: Find  $r_{instage}$ ,  $r_{outstage}$  then find  $F(C_1)$ ,  $F(C_2)$  and  $F(C_C)$

$$F_1(C_1) = \frac{1}{2\pi(r_{instage})C_1}$$

$$F_2(C_2) = \frac{1}{2\pi(r_{outstage} + R_2)C_2}$$

$$F_C(C_C) = \frac{1}{2\pi r_E C_C}$$

where,

$$r_E = R_E / [1 + (\beta \times R_E)]$$

$\Rightarrow$  choose highest value among three as lower cutoff frequency.

$$r_{instage} = 80K // 1.6K // \frac{100}{1000} = 10.34K$$

$$r_{outstage} = R_E // r_C // \beta \approx R_E = 3K$$

$$F_1(C_1) = \frac{1}{2\pi \left( \frac{600}{1000} + 1.6K \right) \times 10^{-6}} = 6.58 \text{ Hz}$$

$$F_2(C_2) = \frac{1}{2\pi (3K // 10) \times 10^{-6}} = 20 \text{ Hz}$$

$$F_C(C_C) = \frac{1}{2\pi (3 \times 10^3 + 4 \times 10^3) \times 10^{-6}} = 12.2 \text{ Hz}$$

$$R_E = L_E // \left( \frac{20}{1000} + \frac{600 // 80K // 1.6K}{1000} \right)$$

$$= 20 \Omega$$

$$F_C(C_C) = \frac{1}{2\pi R_E C_C} = \frac{1}{2\pi \times 20 \times 10^{-6}} = 169.4 \text{ Hz}$$

$\therefore$  lower cut off frequency is  $169.4 \text{ Hz}$

Advantages and disadvantages of RC coupled Transistor Amplifier

# Advantages :-

- 1) It has excellent frequency response
- 2) It has lower cost since it employs resistor and capacitor which are cheap.
- 3) The circuit is very compact as the modern resistors and capacitors are small and extremely light.

# Disadvantages :-

- 1) It has low voltage gain and power gain.
- 2) It has the tendency to become noisy with

21<sup>st</sup>  
21<sup>st</sup>

start

age, particularly in old age.

- b) Impedance matching is poor

max KJ

N1