

Rig:- Timing diagram of MVI B, 32H

Q3

MVI M, 64H ($M \Rightarrow H$) [co | so] L COSDHT 64H 3T~~4T~~ (2T~~4T~~)

so | so

Here, Let the memory address for the given instruction set be,

COSDH: MVI M (4T)

COSLH: 64H (3T)

COS2H: write to memory location referred by M :- 3T

\therefore Total we need 70 T states

so, the timing diagram is:



Fig:- Timing diagram of `MVI M, 64H`

(Q1) timing diagram of LDA 8055H
 Let's consider the memory location for the given instruction be:
 DATE _____

(12)

Timing diagram

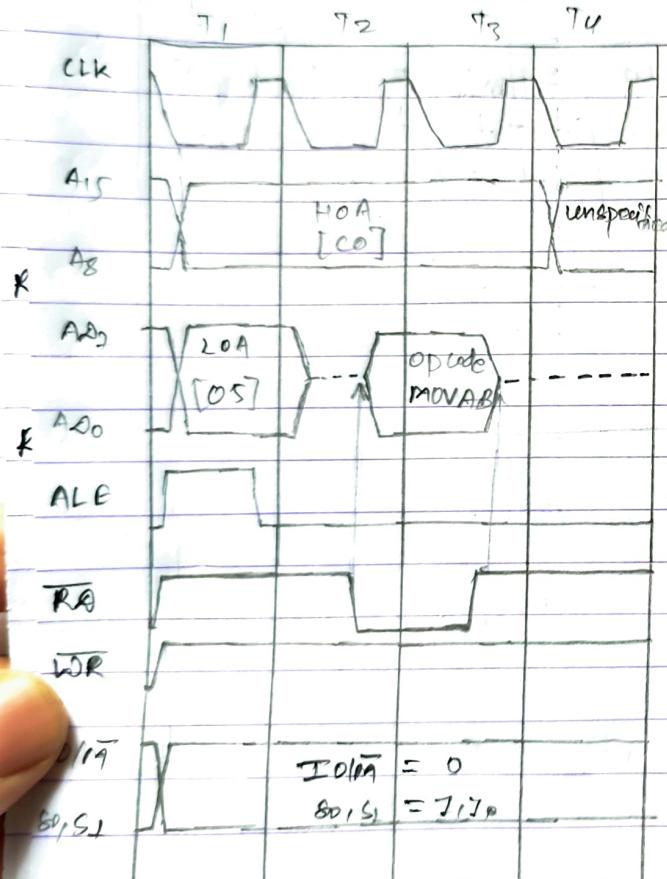
MOV A, B

Given

Let assume the memory location for the instruction. MOV A, B is:

0005H: MOV A/B

Here since being only opcode fetch, 4T state is needed.



	S ₀	S ₁	I/O M
mem	0	1	0
memw	1	0	0
Do read	0	1	1
Do write	1	0	1
opcode	1	1	0

	op	S ₀	S ₁	I/O M
MR	0	1	0	0
WD	1	0	0	0
IMR	0	1	1	1
DOW	1	0	1	1

Status Signals

Machine cycle	S ₀	S ₁	I/O M
opcode fetch	1	1	0
mem	0	1	0
memw	1	0	0
Do Read	0	1	1
I/O Write	1	0	1

Fig:- Timing diagram of MOV A, B

(Q2) MVI B, B2H

Given Let the memory location for the given instruction be

0004H: MVI B

0005H: B2H

∴ 4T state for opcode fetch and 8BT for B2H (memread)
 ∴ 7T state is needed.

(Q3)
 Soln

Q5SH

Draw timing diagram for the given instruction.

(Q3)

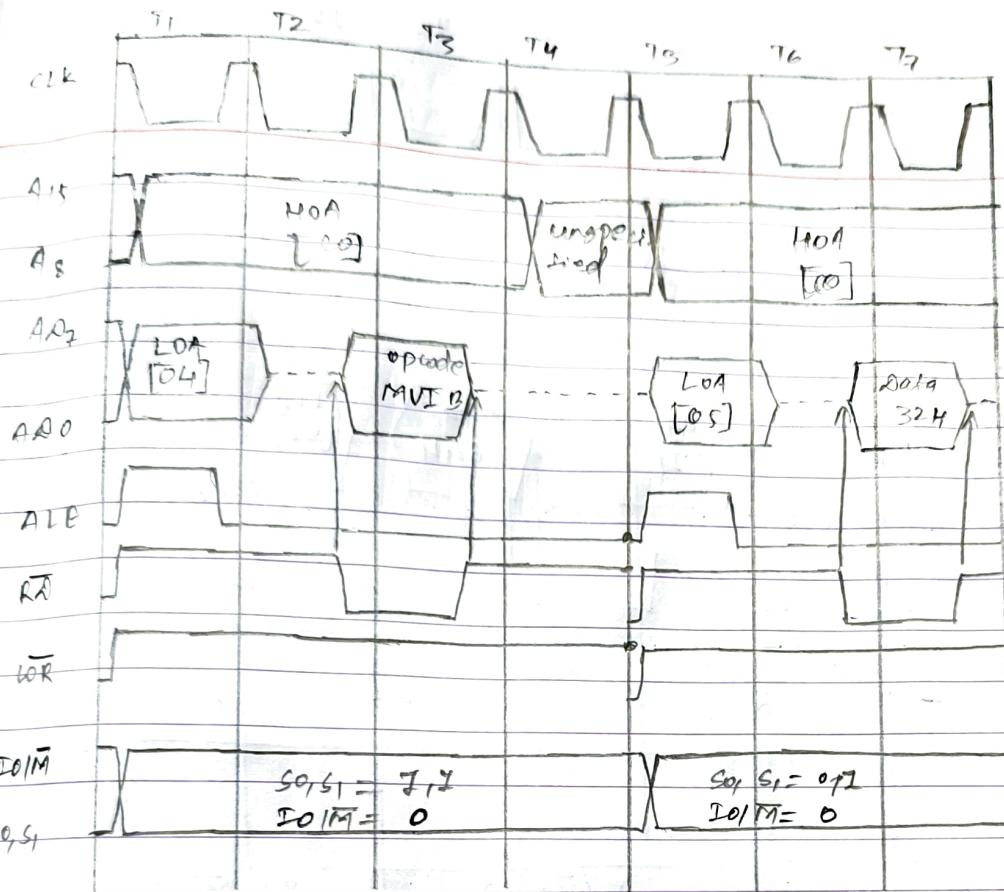


Fig:- Timing diagram of MVI B, 32H

(Q3) MVI M, 64 H ($M \Rightarrow H$ [co 180] L C050 JFT 64 H ~~3T~~ ~~2T~~)

Here, Let the memory address for the given instruction set be.

C050H: MVI M (4T)

C051H: 64H (3T)

C052H: write to memory location referred by M :- 3T

\therefore Total we need 10 T states

So, the timing diagram is:

(8n) Timing diagram of LDA 8085H
 Let's consider the memory location DA

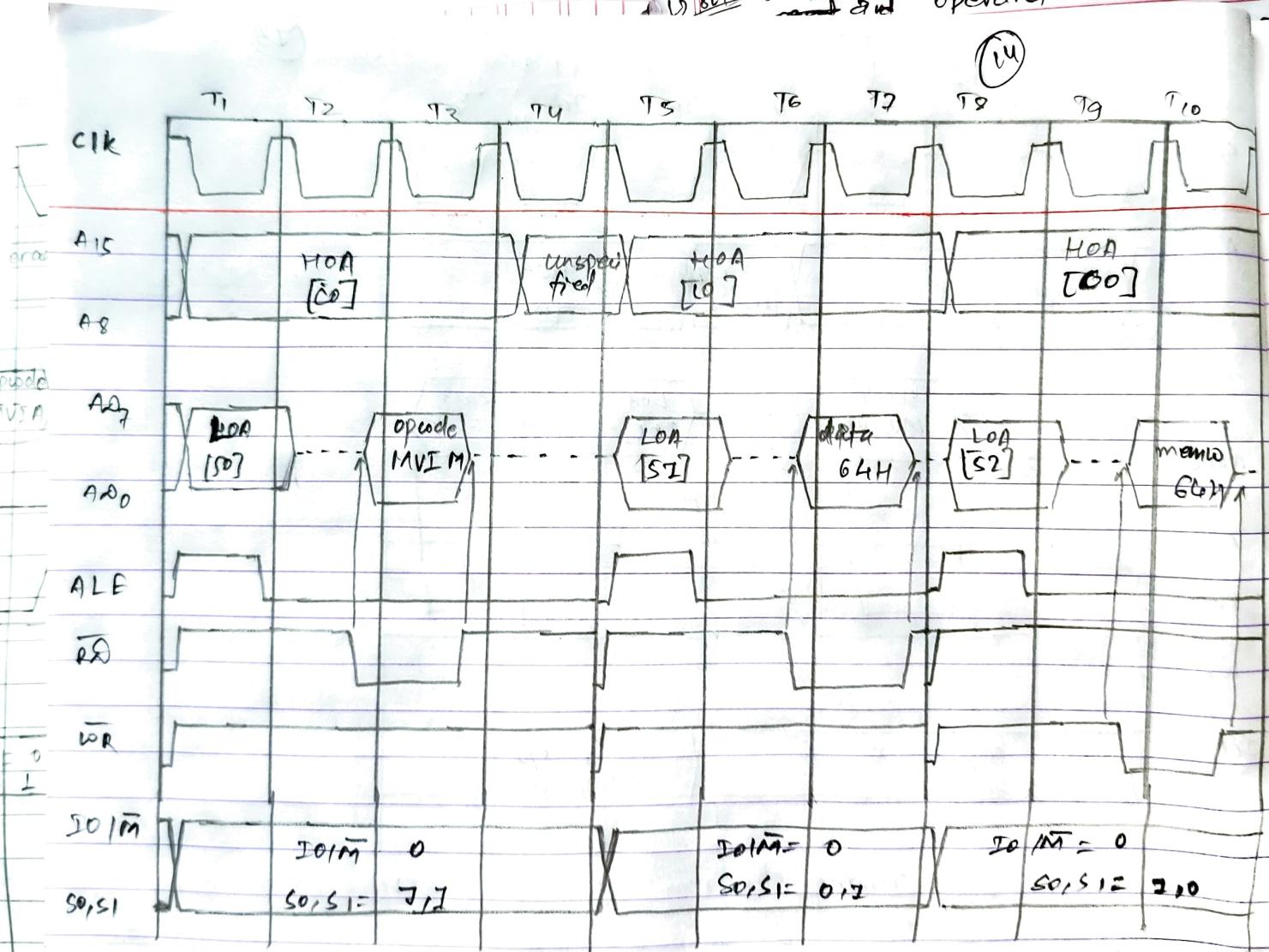


Fig.: Timing diagram of MVI M, 84H

program
order
and i

8085H
00061

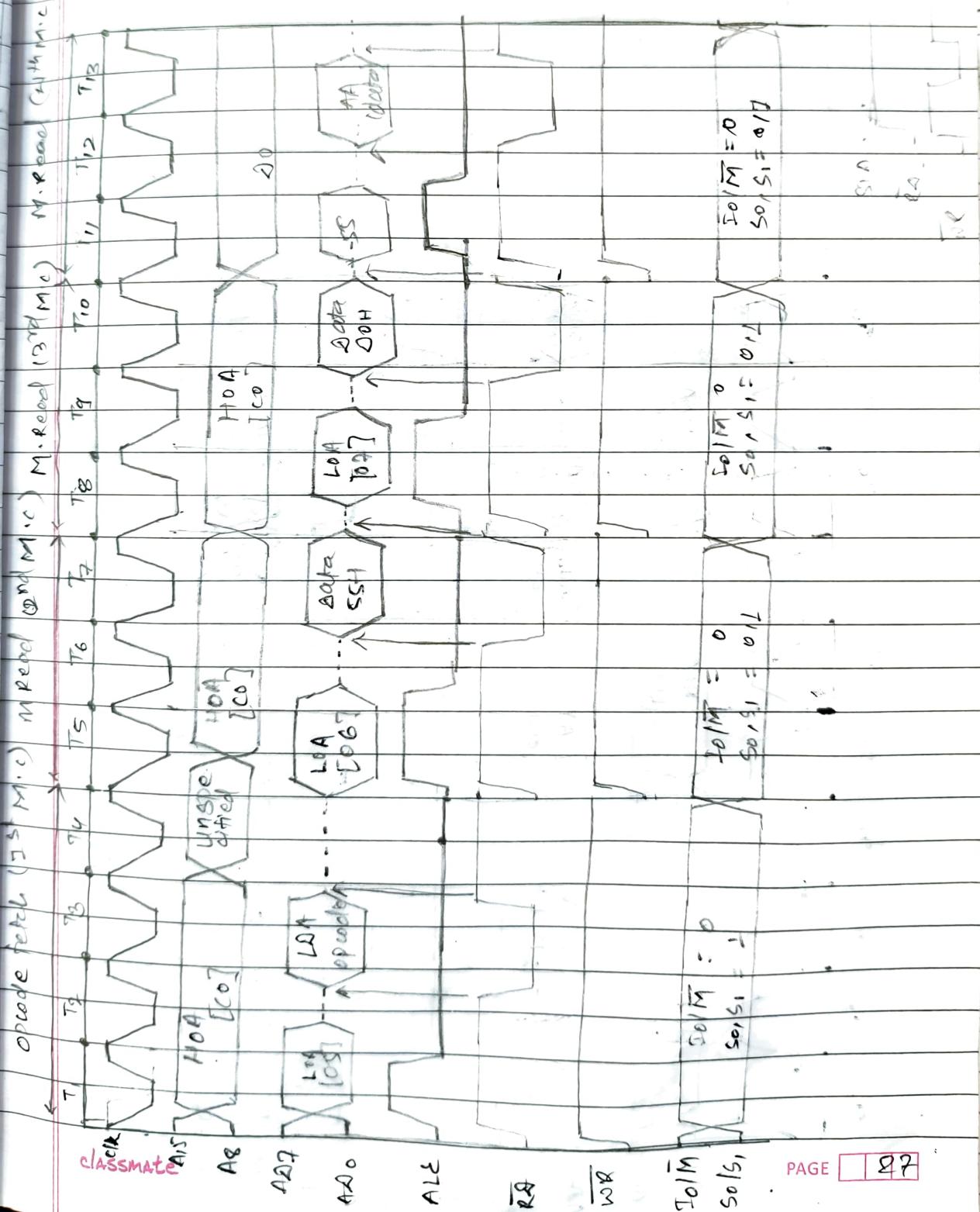
Timing diagram of LDA 8051H
Instructions

(8n) Let's consider the memory location for the given
operator and operand be! DATE

co05h. LDA (4T) opcode fetch

coo6H: ~~██████~~ | 85H (3T) (mem ~~write~~)

~~COOPH: 20H (BT) / 10T mem write~~



ISDP

IN B4H

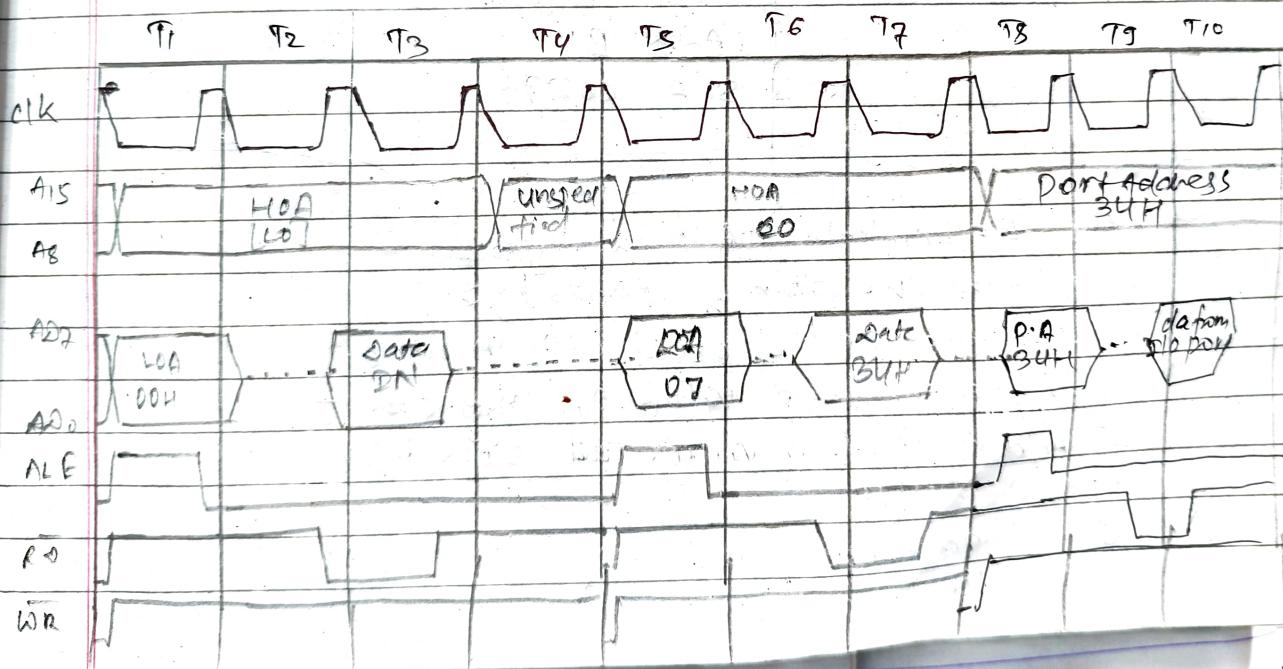
→ Let the memory address be 0000H for opcode
and 0001H for operand

0000H: IN (4T)

0001H: 34H (3T) (Reading port address)

7T + 3T (I/O device → microprocessor) data
receive }

= 20T



- Draw the timing diagram of LXI B, CO5H
 • Let's consider the memory location for given ~~DATE~~ opcode
 and operand is:

CO05 : LXI B [opcode fetch] $\frac{3T}{4T}$

CO06 : 50H [mem read] $\frac{3T}{4T}$

CO07 : COH [mem read] $\frac{3T}{10T}$



S0, S1

I01M = 0

S0, S1 = 1, 1

I01M = 0

S0, S1 = 0, 1

I01M = 0

S0, S1 = 1, 0

Fig.: Timing diagram of 8085, 84 H

13SP29

STA 203H

S01H Here, The memory address for the instruction is 20.

C0S0H: STA (BT)

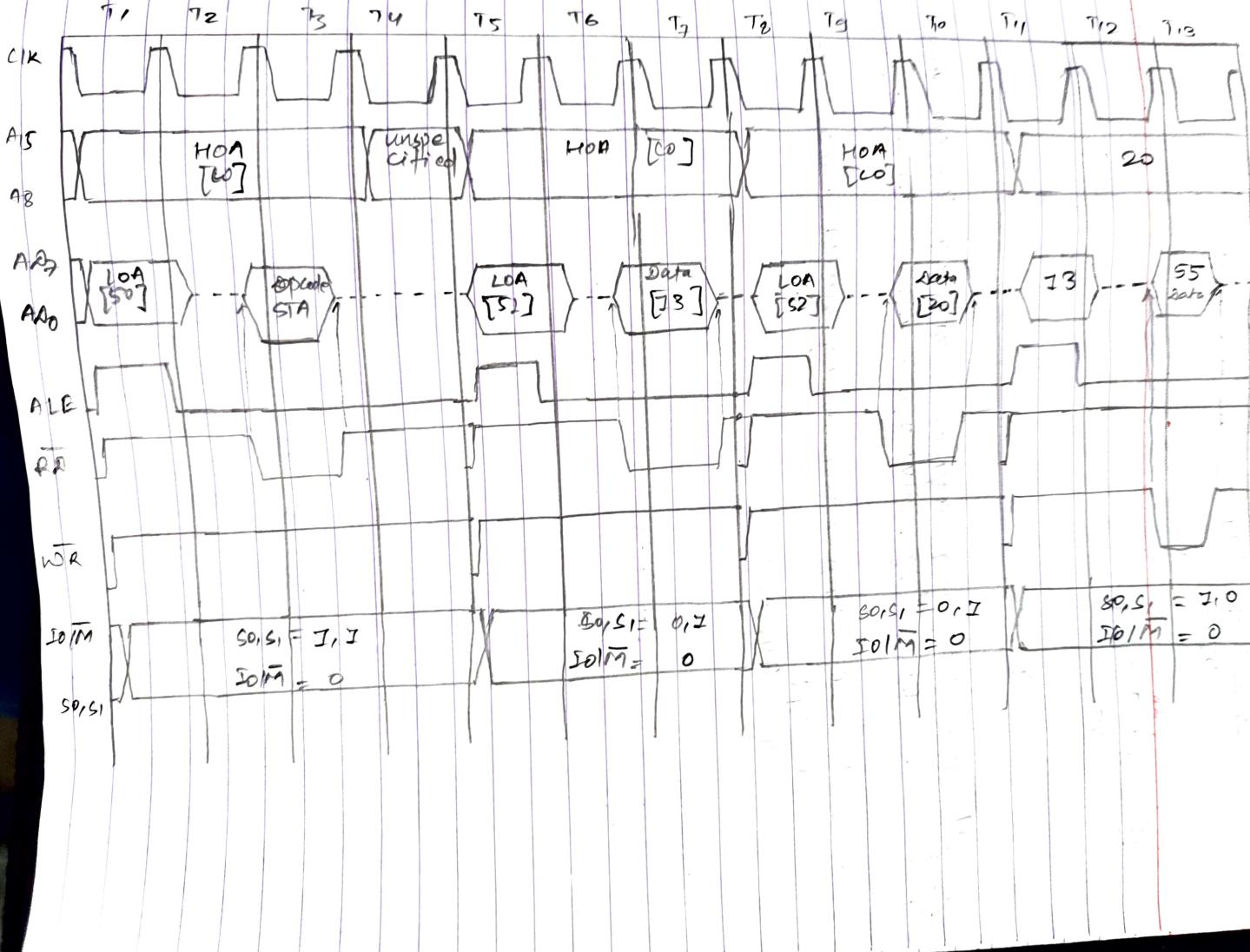
C0S1H: 23 (BT)

C0S2H: 20 (BT)

Also, we need to write the accumulator content to 2033 for which extra 3T state is needed.

So, total number of required T state is 13 : 73.

flag:
• flag is set, it causes string instruction
increment. By clearing SF, it controls
PAGE 5
classmate
or mem -



14 SP 2a

ADD 45H (Add the value 45 with
content of Accumulator,
 $A = A + 45H$)
↳ BT + ↳ Reg(3T)
= > T

(16)

15 SP 2a \rightarrow OUT 34 H

4T

3T

3T (I/O write)

17 fall draw the timing diagram for moving an immediate data to 8086 (e.g: MOV A, 45H)

801n

Here in 8086, microprocessor moving an immediate data is done by:

MOV AH, 45H