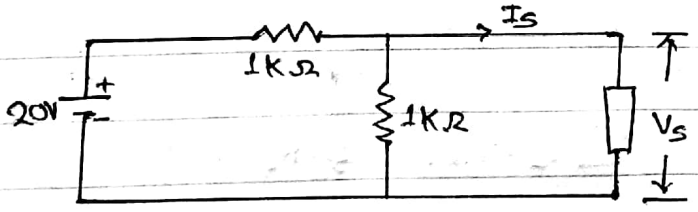
Tutorial-1

1. Define semiconductor & its types. Find the relationship between σ_i, n_i, μ_e, μ_h & q.
2. Discuss the formation of PN junction of S/C along with VI characteristics in both forward & reverse biased condition.
3. How temp effect the VI characteristics of PN junction diode. If reverse saturation current of diode is 5nA at 35°C, find reverse saturation current at 235°C.
4. "Transition capacitance is inversely proportional to the square root of the applied reverse voltage." Justify the statement.
5. What is Junction capacitance. Establish a relation for diffusion capacitance. Differentiate both transition & diffusion capacitance.
6. What do you mean by reverse recovery time of PN diode? Explain.
7. What is schottky diode. How it is different from PN diode.
8. Explain VI characteristics of tunnel diode with help of necessary diagram. Also mention its applications.
9. What are linear devices? Differentiate both linear & non-linear devices.
10. Explain non-linear devices along with its properties. Verify with appropriate example, non-linear device doesn't follow the principle of superposition.
11. Find I_s & V_s for the circuit shown below:

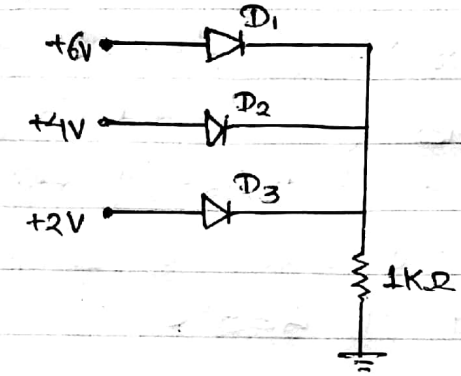


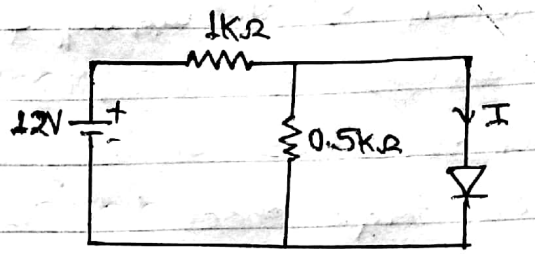
Also find its piecewise linear model

12. "Diode is a non-linear device" Justify the statement.
13. Find piecewise linear model of silicon diode with $I_s = 10^{-11}$ A & $\eta = 1.6$ in the vicinity of operating point $I_D = 1$ mA.

14. For the circuits given, find out the current flowing through resistor. (Assume piecewise linear model of diode.

a)





15. For the circuit shown below. Find

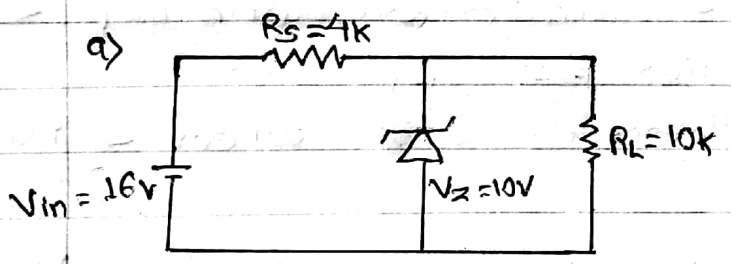
i) O/p voltage

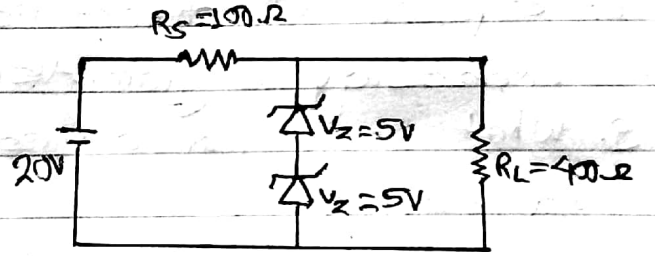
ii) current through zener diode

iii) Voltage across R_S

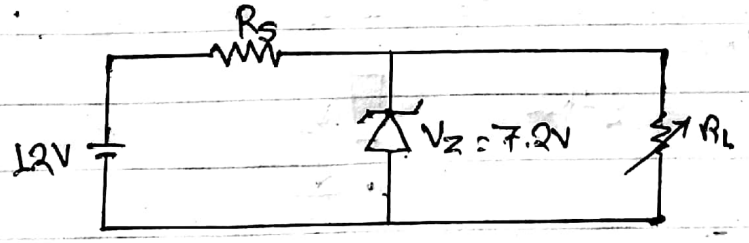
iv) Powd dissipated across Zener diode.

a)





16. For the circuit shown below, load current varies from 12 to 100mA. Find value of series resistance R_S to maintain 7.2V across the load. Minimum Zener current is 10mA.

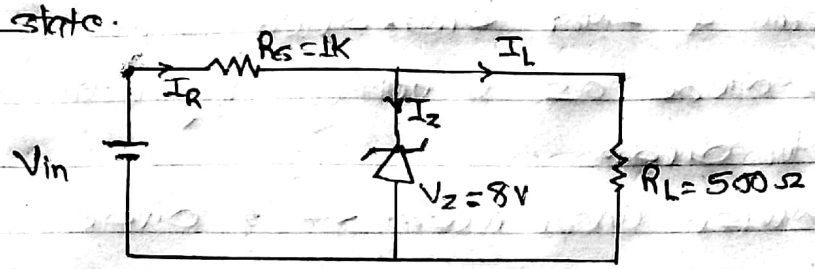


17. For the network shown below, determine:

i) the value of V_{in} that ensure Zener diode is in the ON state. ($V_{in(min)}$).

ii) I_L, I_R, I_Z if $V_{in} = 20V$

(ii) The minimum value of R_L to ensure that the zener diode is in the ON state.

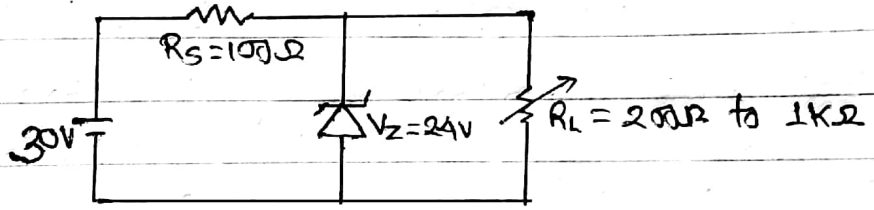


18. A zener regulator has 24V zener voltage with variable load resistance. Calculate: i) maxm & minm load current.

ii) maxm & minm power dissipation across diode

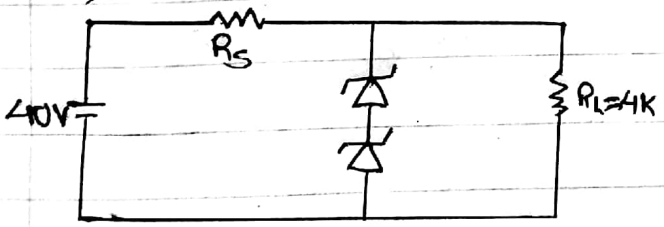
iii) voltage drop across series resistance.

iv) minm value of load resistance to ensure that zener diode is in 'ON' state.

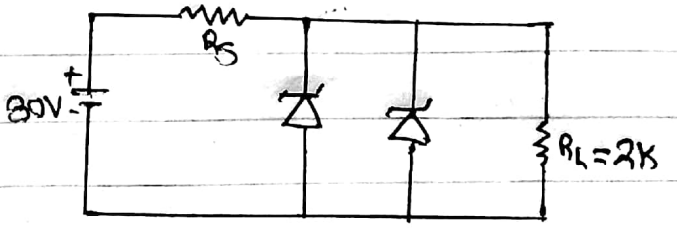


19. The Zener diode ratings connected in the circuit shown below is 10V, 1mA. Find values of series resistance R_S so that o/p across the load is regulated.

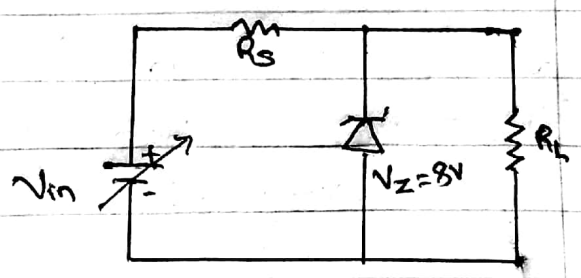
a)



b)



20. Design a zener diode voltage regulator which maintain constant 8V across load for supply voltage of range 10V - 50V. The maxm zener current is $I_{ZM} = 40mA$.



21. Write short Notes on:

a) Static & dynamic resistance

b) Avalanche & zener breakdown

c) Zener diode as a voltage regulator

d) Varactor diode

e) Piecewise linear model of a diode

Tutorial-2

Theory:

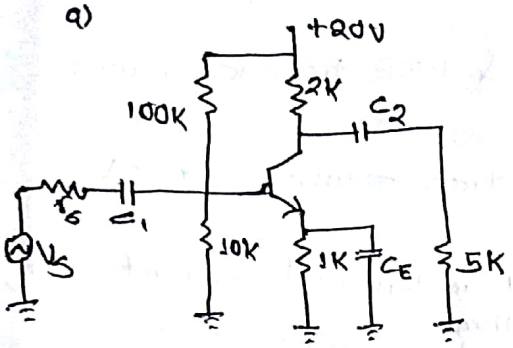
1. Explain current flow mechanism in NPN & PNP transistor with necessary circuit diagram.
2. Draw and explain I/p & O/p characteristics curves for CE, CB and CC transistor configurations.
3. Compare CB, CC & CE configuration of BJT in terms of current gain, I/O impedance, voltage gain & its application.
4. What are modes of operation of transistor. Show that, $I_C = \beta I_B + (\beta+1) I_{CBO}$, where the symbols have their usual meanings.
5. With neat sketch & its significance, explain BJT switching time. What is early effect & punch through.
6. Describe Ebers Moll model of transistor. Transistor can be used as a switch and as an amplifier, Explain.
7. What is stability factor. Derive stability factor for self-biased NPN transistor.
8. Write short Notes on:
   a) Avalanche/Breakdown effect on transistor.
   b) Relationship betn α, β & γ.
   c) AC & DC load line and Q-point
   d) Thermal instability & thermal runway.

Numericals:

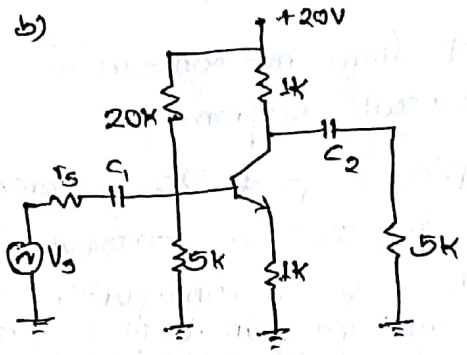
1. Design a CE self-bias circuit for $I_C = 20mA$, $V_{CC} = 20V$, $\beta = 100$.
2. Find Emitter, Base & collector current as well as V_{CE} for given CB transistor amplifier. Also draw DC load line and locate Q-point. Assume $\alpha = 0.9$

3. For the circuit shown below draw DC load line & find operating point. Also locate operating point on DC load line & find the stability factor of circuit. Assume silicon transistor with $\beta = 100$

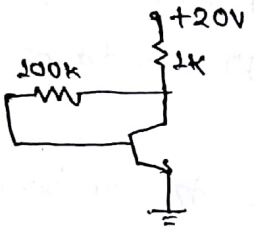
a)



b)



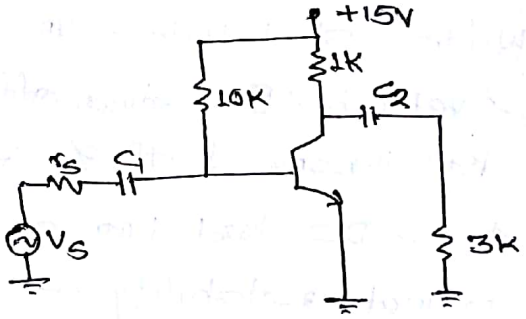
c)



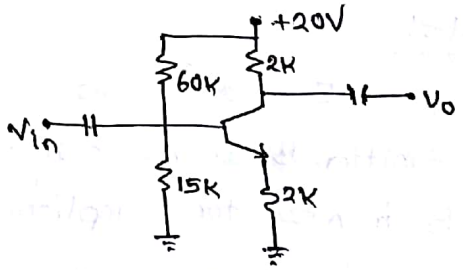
4. Design a base bias circuit having operating point (5V, 1mA). Assume Si transistor with $V_{BE} = 0.6V$ & $\beta = 100$, $V_{cc} = 15V$.

5. Design a voltage divider biasing circuit with $V_{CEQ} = 5.5V$ and $I_{CQ} = 1.5mA$. ($\beta = 100$).

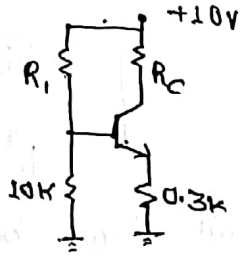
6. For the given circuit, find collector, base, emitter current and voltage across collector emitter junction. Also calculate stability factor. ($\beta = 100$).



7. Find I_B, I_C, V_{CE} & S for following voltage divider biasing circuit. Assume $\beta = 100$.



8. If $I_C = 1mA$, $V_{CE} = 2.5V$, $h_{fe} = 100$ and $I_{CQ} = 0$, find out the values of R_1 & R_C for given circuit.



9. Design voltage divider bias circuit that will satisfy the conditions: $I_C = 2mA$, $V_{CE} = 10V$, $S = 4$. Assume $\beta = 100$ & $V_{cc} = 20V$.

10. Design self bias circuit for Si transistor with $\beta = 100$ & $V_{cc} = 10V$, $V_{CE} = 5V$, $I_C = 1mA$, $R_C = 3.3K$ & $S = 10$.

Tutorial 3

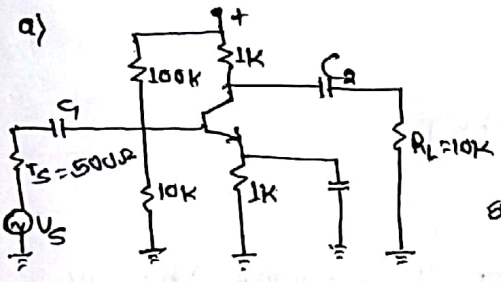
Theory:

1. Explain re model of common base, common collector and common emitter (bypassed and unbypassed) configuration in details.
2. Write short notes:
   a) h-parameter model of BJT

Numerical:

1. For the given transistor amplifier, find its re-model. Also find overall voltage gain & current gain. Also find value of V_L if $V_S = 100mV$. Take $\beta = 100$.

a)



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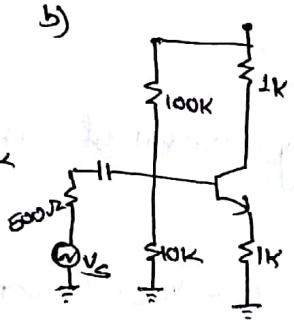

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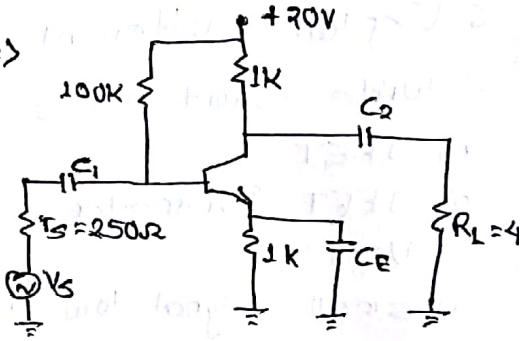
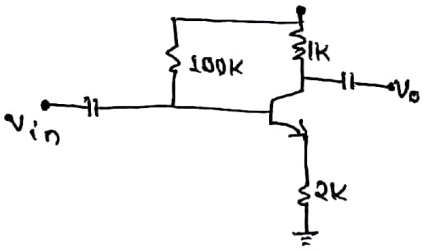


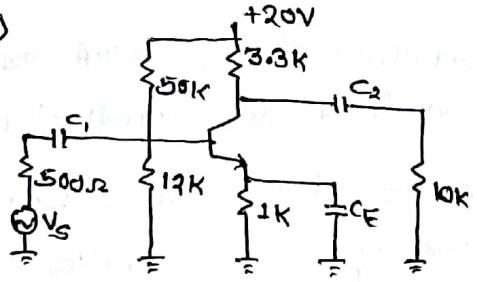
2)



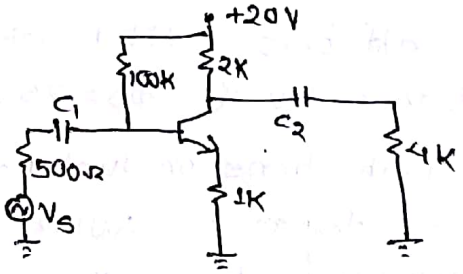
Find R_{in}, $R_{in1stage}$, $R_{of1stage}$ and A_V for given circuit. Take $\beta = 100$.

3) For the given transistor amplifier circuit, the h-parameters are $h_{ie} = 1.6K$, $h_{fe} = 80$, $h_{re} = 20 \times 10^{-4}$ and $h_{oe} = 20\mu A/V$. Find V_L/V_S.

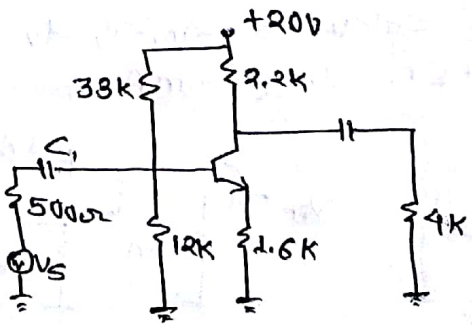
a)



b)



4) For given CE transistor amplifier, write its h-parameter model and find Z_{in}, Z_{out}, V_L/V_S.
Given, $h_{fe} = 90$, $h_{ie} = 1.8K\Omega$, $h_{oe} = 40\mu A/V$ (h_{re} is negligible.



Tutorial 4

Theory

1. Compare BJT & FET. "FET is unipolar device". Justify.
2. Explain working principle of NJFET. Also draw drain and transfer characteristics curves.
3. Draw small signal equivalent ckt of JFET.
4. Prove that conductance of JFET is given by,

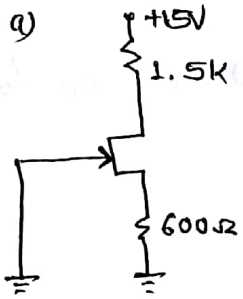
$$g_m = \frac{2}{V_p}\sqrt{I_{DS} \cdot I_{DSS}}$$

5. What is pinch off voltage. Find general expression of saturation current in JFET.
6. Explain different JFET biasing methods.
7. Write short Notes on
   a) JFET
   b) JFET Parameter
   c) UJT
   d) Small signal low frequency model of JFET.

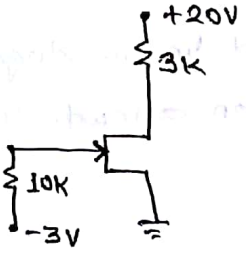
Numerical

1. For the circuit given, find I_D & V_{DS}. Given $I_{DSS} = 10mA$, $V_p = -4V$

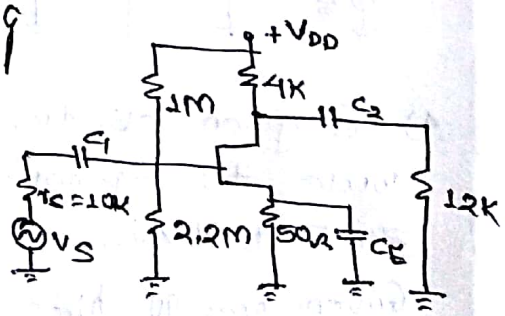
a)



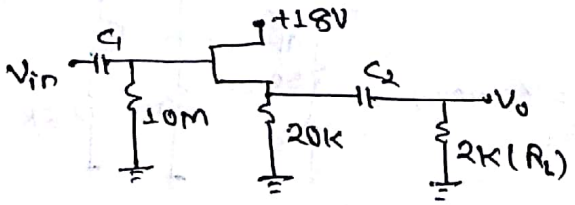
b)



2. Design a voltage divider NJFET ckt operating at 15mA drain current & 10V drain-to-source voltage. $I_{DSS} = 25mA$, $V_p = -4V$
3. Design a self-bias NJFET ckt operating at $I_D = 15mA$, $V_{DS} = 10V$, $I_{DSS} = 25mA$, $V_p = -4V$ & $V_{DD} = 25V$. Also find transconductance.
4. For a JFET with transconductance 4000μs at its bias point. Its drain resistance is 100kΩ. Assuming small signal model, find overall voltage gain.



5. Calculate Z_{in}, Z_o, A_v for common drain JFET. $I_{DSS} = 10mA$, $V_p = -5V$, $r_d = 100K$



Tutorial 5

1. Explain EMOSFET, DMOSFET with necessary diagrams (construction and operation)
2. Differentiate both depletion and enhancement type MOSFET.
3.

Tutorial 6

Theory

1. Draw bridge & center-tap full wave rectifier circuit and explain its operation, along with its parameter.
2. What is half wave rectifier. Find average value, rms, efficiency and ripple factor.
3. What is ripple factor. "Full wave rectifier is more efficient than half wave rectifier". Justify it.

Numerical

1.