Chapter 7

Metal Oxide Semiconductor FET

The Metal oxide s/c FET (MOSFET) is one of the most widely used electronic devices, particularly in digital circuits, bcoz of its relatively small & size & its easy fabrication technique where thousand of devices can be fabricated in a single chip.

MOSFET is constructed with the Gate terminal insulated from the channel, so also called Insulated Gate FET i.e. IGFET. Since most of such devices are made using the oxide of silicon for semiconductor and insulator & metal or heavily doped polysilicon for Gate electrode, it is called Metal Oxide FET.

MOSFET is unipolar & voltage controlled device because their channel conductivity is controlled by Gate-to-Source voltage & current flows due to majority carriers.

There are 2 types of MOSFET.

1) Enhancement type MOSFET (EMOSFET)
2) Depletion type MOSFET (DMOSFET)

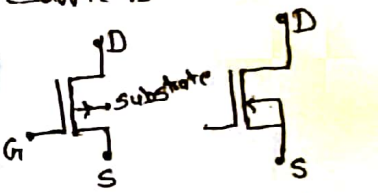


Fig: P-channel & N-channel DMOSFET

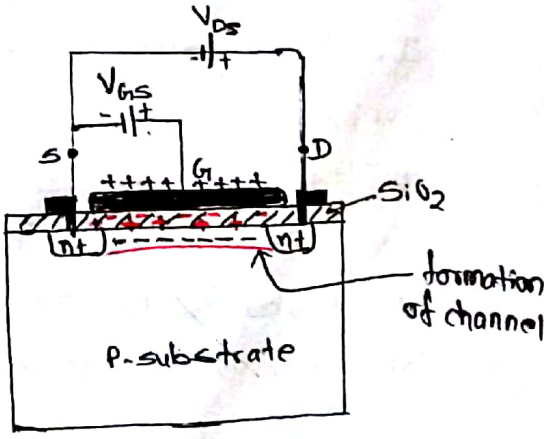
Enhancement MOSFET (EMOSFET)

Structure & construction of N-channel EMOSFET

A N-channel EMOSFET is fabricated on P-type substrate. Two highly doped n+ region i.e. source & drain are created in the substrate. A thin layer of SiO_2 (Silicon dioxide) is grown on the surface of substrate, covering the area between Drain & source.

Metal contacts are made in the source region, drain region & on the top of the oxide layer & also on the substrate.

In EMOSFET, initially, there is no channel betn Drain & source channels are electrically induced when the V_{GS} is applied.



(Metal → Aluminium)

Operation of EMOSFET:

I. When $V_{GS}=0$ & V_{DS} increasing

When $V_{GS}=0$ & V_{DS} is increasing, there will be no drain current since there is no conducting path/channel betn drain & source.

⇒ With +ve voltage at the Gate, the channel forms betn drain & source. The minimum Gate-to-source voltage at which significant current flows is called threshold voltage (V_{TR}).

II. When $V_{GS} > V_{TR}$

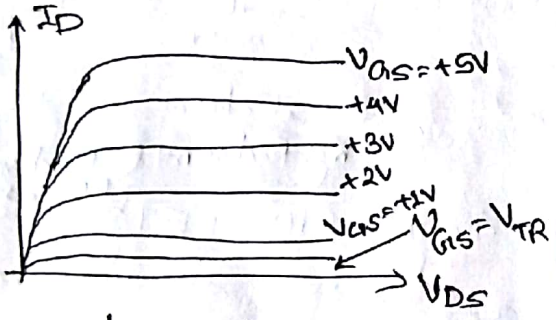
→ drain current increases rapidly & is given by

$$I_D = K(V_{GS} - V_{TR})^2$$

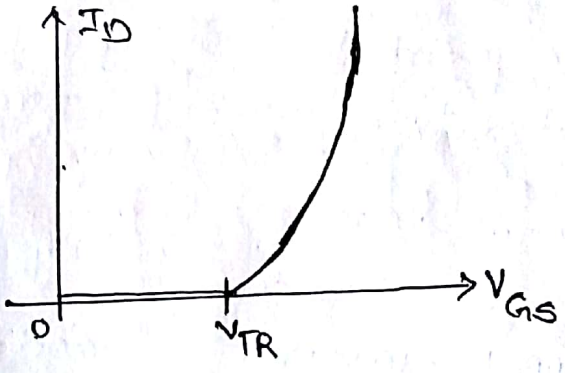
where, K = constant

V_{TR} = threshold voltage,

The transfer characteristics of EMOSFET is,



Drain characteristics



Depletion MOSFET (DMOSFET)

In DMOSFET, there exists a lightly doped n-channel betn heavily doped Drain & source. Thus drain current I_D flows even at $V_{GS}=0$ if V_{DS} is applied.

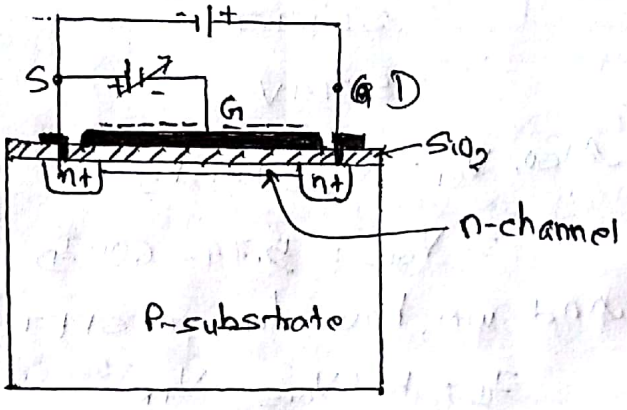
I. V_{GS} = -ve & V_{DS} is applied.

When -ve V_{GS} is applied & V_{DS} too, the channel width reduces due to electrostatic induction, i.e. -ve charge on Gate repels e^- from channel to the P-substrate. Thus drain current reduces. This mode of operation is called depletion mode.

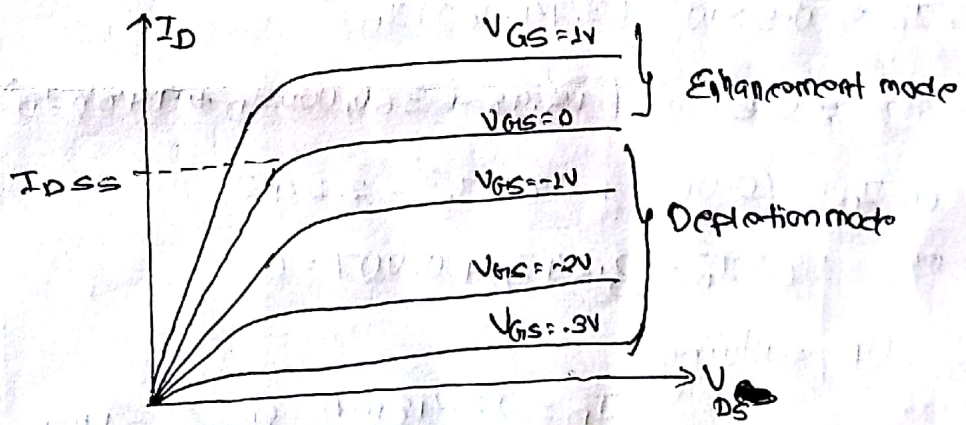
II. V_{GS} = +ve & V_{DC} is also applied

When +ve V_{GS} & V_{DS} is applied, the charge on the Gate (metal) attracts e⁻s from the channel & P-substrate as well & thus the channel width increases and thus increase in drain current. This mode of operation is called enhancement mode.

Thus DMOSFET operates in depletion mode as well as enhancement mode.



The drain characteristics for both the depletion & enhancement mode of DMOSFET is,



EMOSFET Biasing circuit:

For $V_{GS} \geq V_{TR}$

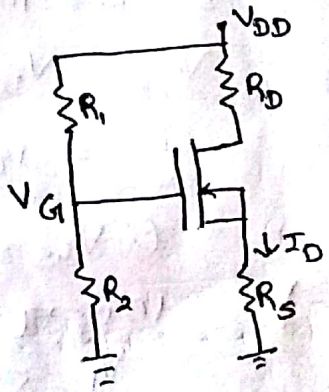
$$I_D = K(V_{GS} - V_{TR})^2$$

Also, from given voltage divider ckt,

$$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD}$$

and, $V_G = V_{GS} + I_D R_S$

$$\Rightarrow V_{GS} = V_G - I_D R_S$$



For given NMOSFET, find values of V_{GS}, I_D & V_{DS} (Self bias EMOSFET) assuming $K = 0.5 \times 10^{-3}$ & $V_{TR} = 2V$. $R_1 = 4.7K$ $R_2 = 2.2K$, $R_D = 2.2K$, $R_S = 600\Omega$ & $V_{DD} = 18V$.

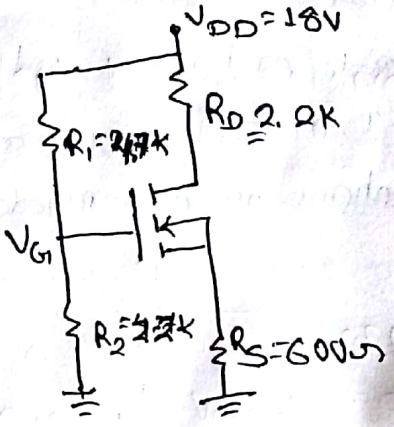
Soln.

Here,

$$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD}$$

$$= \frac{2.2}{2.2 + 4.7} \times 18$$

$$= 5.74V$$



Also, $V_G = V_{GS} + I_D R_S$

$\Rightarrow V_{GS} = 5.74 - 600 I_D$

And we have, for MOSFET,

$$I_D = K.(V_{GS} - V_{TR})^2$$

$$\text{or } I_D = 0.5 \times 10^{-3} (5.74 - 600 I_D - 2V)^2$$

$$\text{or, } I_D = 0.5 \times 10^{-3} (3.74 - 600 I_D)^2$$

$$= 0.5 \times 10^{-3} (13.98 + 360{,}000 I_D^2 - 4488 I_D)$$

$$\text{or, } I_D = (0.007 + 180 I_D^2 - 2.24 I_D)$$

$$\text{or, } 180 I_D^2 - 3.24 I_D + 0.007 = 0$$

On solving, $I_D = 15.48mA$ or $2.51mA$

Case I: When, $I_D = 2.51mA$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

$$= 18 - 2.51 (2.2 + 0.5) = 11.22V$$

& $V_{GS} = 5.74 - 600 \times 2.5 \times 10^{-3} = 4.23V$

For MOSFET to operate in pinchoff region,

$$V_{DS} > (V_{GS} - V_T)$$

$$\text{or, } 11.22 > (4.23 - 2)$$

$$\text{or, } 11.22 > 2.23, \text{ is valid.}$$

$\therefore I_D = 2.51mA$ is valid.

Case II: When $I_D = 15.48mA$

$V_{DS} = 18 - 15.48(2.2+0.5) = -23.79V$

Here V_{DS} can't be -ve.

Also, $V_{GS} = 5.74 - 600 \times (15.48 \times 10^{-3}) = -3.54V$

As both V_{GS} & V_{DS} are invalid,

i.e. $V_D > (V_{GS} - V_T)$

or, $-23.79 > (-3.54-2)$

$-23.74 > -5.54$, is invalid.

Thus, $I_D = 15.48mA$ is invalid.

Thus, $V_{GS} = 4.23V$

$I_D = 2.51mA$

& $V_{DS} = 11.22V$

Depletion Enhancement MOSFET / Depletion MOSFET (DEMOSFET / DMOSFET)

The DMOSFET can be used in both depletion and enhancement mode.

Construction (N-channel DMOSFET):

⇒ It consists of highly doped p-type substrate (or body) into which two blocks of heavily doped N-type material are diffused forming source and drain as shown in figure.

⇒ N-channel is formed by diffusion between source & drain.

⇒ A thin layer of SiO_2 dielectric is grown over the entire surface and holes are cut through the SiO_2 layer to make contact with source & drain.

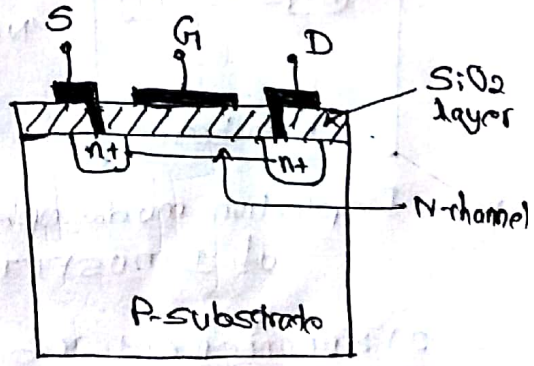


Fig: N-channel DMOSFET

⇒ Metal is deposited through the holes to provide drain & source terminals & a metal plate is deposited on the surface, both, drain and source, which is Gate.

A P-channel DMOSFET is constructed like an N-channel DMOSFET starting with an N-substrate (body), and diffusing P-type Drain & Source blocks and connecting them internally by P-type channel.

Operation of DMOSFET:

The DMOSFET operates in both depletion & enhancement mode as described below:

1) Depletion Mode:

Here Gate is -ve w.r.to Source i.e. V_{GS} = -ve.
When positive drain to source (i.e. $V_{DS} > 0$) is applied drain current starts to flow even if $V_{GS} = 0$. Since V_{GS} is -ve, (i.e. gate is -ve), it repels e^- from N-type channel. This create a depletion region in the channel as shown in figure & the channel becomes narrower and drain current decreases.
On further increase in -ve V_{GS}, makes the channel more narrower & I_D decreases. If -ve V_{GS} is increased sufficiently, channel will be and drain current will be zero.

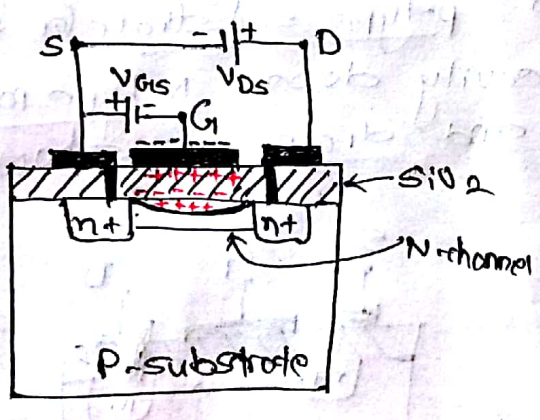


Fig: Depletion mode operation of DMOSFET

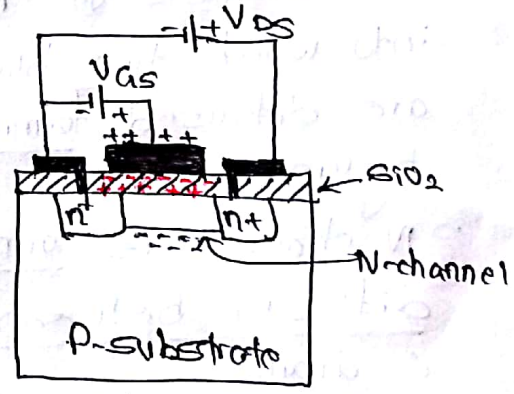


Fig: Enhancement mode operation of DMOSFET

2) Enhancement Mode:

Here Gate is +ve w.r.to Source i.e. V_{GS} = +ve.
When $V_{DS} > 0$, I_D flows even when $V_{GS} = 0$. Since V_{GS} is +ve, i.e. Gate is +ve it attracts -ve charge carriers from P-substrate to N-channel, which reduces channel resistance, i.e. increase in channel width, and

thus increase in drain current I_D. As +ve V_{GS} increases, I_D also increases.

Characteristics of DMOSFET:

1) Drain characteristics:

⇒ plot both I_D Vs V_{DS} for constant V_{GS}.

⇒ for $V_{GS}=0$, I_D current flows because of presence of physical channel.

⇒ when V_{GS} is -ve ($V_{GS}<0$), it operates in depletion and so I_D decreases.

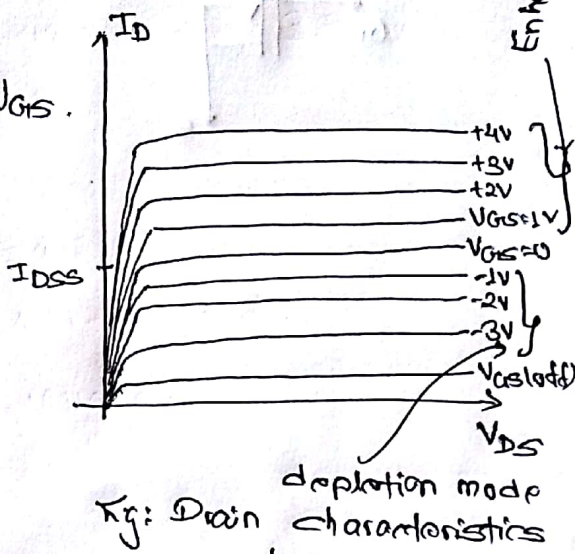


Fig: Drain characteristics

⇒ When V_{GS} = +ve, DMOSFET operates in enhancement mode & thus I_D increases.

⇒ When $V_{GS} \leq V_{GS(off)}$, the channel is pinched-off, so I_D becomes nearly zero.

2) Transfer characteristics:

⇒ plot both I_D & V_{GS} for constant

Here, when $V_{GS}=0$, $I_D = I_{DSS}$

When $V_{GS}<0$, I_D decreases because DMOSFET operates in depletion mode.

When $V_{GS}>0$, I_D increases, as DMOSFET operate in enhancement mode.

When $V_{GS} \leq V_{GS,off}$, pinch off occurs & $I_D \simeq 0$.

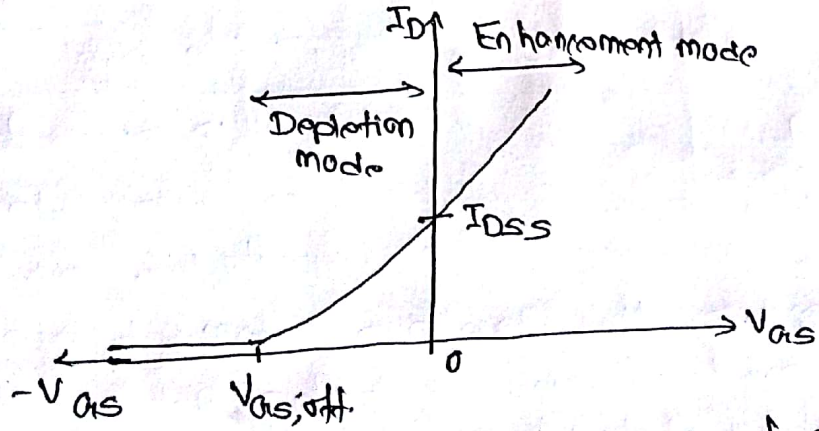
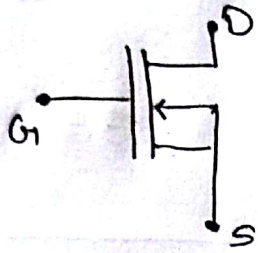


Fig: Transfer characteristics of DMOSFET.

DMOSFET is of 2 types

i) N-channel DMOSFET



ii) P-channel DMOSFET