Computer Organization

HDL simulator:

```
PC =      2244
Data Memory =       1,       2,       0,       0,       0,       0,       0,       0
Data Memory =       0,       0,       0,       0,       0,       0,       0,       0
Data Memory =       0,       0,       0,       0,       0,       0,       0,       0
Data Memory =       0,       0,       0,       0,       0,       0,       0,       0
Registers
R0 =        0, R1 =        1, R2 =        2, R3 =        3, R4 =        4, R5 =        5, R6 =        1, R7 =        2
R8 =        4, R9 =        2, R10 =       0, R11 =       0, R12 =       0, R13 =       0, R14 =       0, R15 =       0
R16 =       0, R17 =       0, R18 =       0, R19 =       0, R20 =       0, R21 =       0, R22 =       0, R23 =       0
R24 =       0, R25 =       0, R26 =       0, R27 =       0, R28 =       0, R29 =       0, R30 =     128, R31 =       0
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```

Basic Instruction

```
PC =      1776
Data Memory =       4,       5,       6,       7,       8,       9,      10,       2
Data Memory =       1,       3,       0,       0,       0,       0,       0,       0
Data Memory =       0,       0,       0,       0,      68,       2,       1,      68
Data Memory =       2,       1,      68,       4,       3,      16,       0,       0
Registers
R0 =        0, R1 =        0, R2 =        5, R3 =        0, R4 =        0, R5 =        0, R6 =        0, R7 =        0
R8 =        0, R9 =        1, R10 =       0, R11 =       0, R12 =       0, R13 =       0, R14 =       0, R15 =       0
R16 =       0, R17 =       0, R18 =       0, R19 =       0, R20 =       0, R21 =       0, R22 =       0, R23 =       0
R24 =       0, R25 =       0, R26 =       0, R27 =       0, R28 =       0, R29 =       0, R30 =     128, R31 =      16
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Advanced set 1

```
PC =       192
Data Memory =      10,       9,       8,       7,       6,       5,       4,       3
Data Memory =       2,       1,       0,       0,       0,       0,       0,       0
Data Memory =       0,       0,       0,       0,       0,       0,       0,       0
Data Memory =       0,       0,       0,       0,       0,       0,       0,       0
Registers
R0 =        0, R1 =        0, R2 =        0, R3 =        0, R4 =        0, R5 =        0, R6 =        0, R7 =        0
R8 =       -4, R9 =        0, R10 =       9, R11 =      10, R12 =      40, R13 =       4, R14 =       8, R15 =       0
R16 =       0, R17 =       0, R18 =       0, R19 =       0, R20 =       0, R21 =       0, R22 =       0, R23 =       0
R24 =       0, R25 =       0, R26 =       0, R27 =       0, R28 =       0, R29 =       0, R30 =     128, R31 =       0
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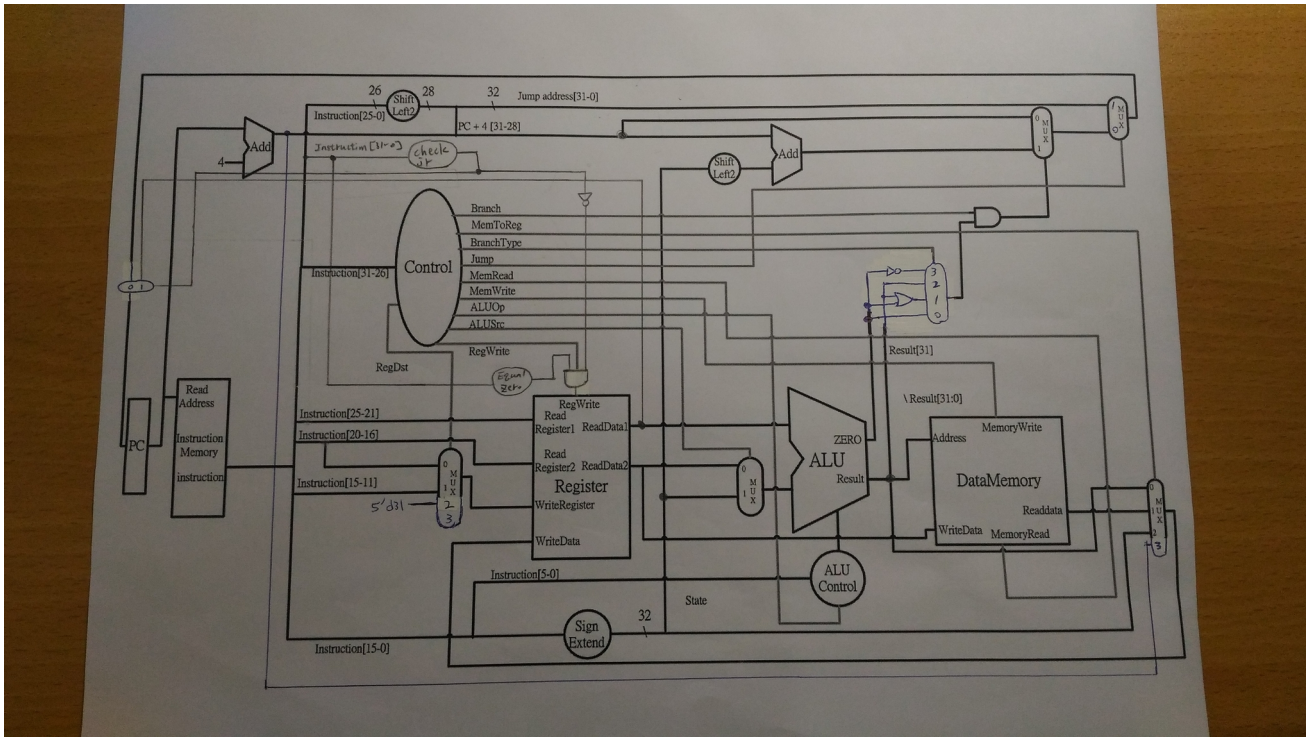
```

Advanced set 2

Architecture diagram:



Detailed description of the implementation:

一開始比較費力的就是加了一些 module 和 Decoder 接出來的 wire，做出來之後 Basic instruction 就填上去應該在的地方就好了。

Advance 1 的重點有兩個：
一個是 jal 要儲存地址，因此需要把 add 4 完後的 PC 接到最後的 MUX，讓 MemToReg 控制 MUX 來選擇寫入的資料，還要在 Register 的 WriteRegister 前面加一個 4 to 1 的 MUX，讓 port 2 接 31 這個數字，代表 stack point，port 3 就先放著不用。
另一個是 jr 因為是 R type，但要做的事跟平常的 R type 實在差非常多，因此我再接了一個 check jr 的 module 來控制跳轉與存儲之類的動作。

最麻煩的就是 Advance 2 了：
接好 ble,bnez,bltz 並不難，只要想好 brach type 那邊的 MUX 要怎麼做就好，比較麻煩的是要自己寫 machine code，讓我好好的複習了各個指令的格式，還花好久時間 de 一個因為 verilog 時序關係而出現的 bug。

Problems encountered and solutions:

Basic instruction 沒有太大的困難，Advance 1 稍微想了一下也很快就做出來了

花最久時間的是 Advance 2
寫 machine code 查了網路資源和跟同學討論才確定好正確版本，很麻煩的一個點就是發生錯誤都要再檢查到底是 machine code 錯還是 verilog code 錯。
另外就是一個時序問題的 bug，反覆確認 machine code 都沒錯時才認命的去把一些可能會錯的 wire print 出來，才找到問題，花了非常多時間。

Lesson learnt (if any):

一、各個指令的格式
二、實際一行一行 trace 指令執行後，register 與 memory 的資料變化
三、verilog 時序的問題