



Capacitor Bank Design Considerations, Fault and Protection

Introduction

Shunt Capacitors, also known as Capacitor Banks, are installed in Power Systems for **reactive power compensation**, which results in **substation loading** and **line loss reduction** and **voltage support** after transformer internal impedance. This report discusses selection, switching considerations, related faults and protection of a capacitor bank.

Selection of Capacitor Bank

Rated power (kVAr) is the first element to consider in sizing a capacitor bank. It is suggested to have at least 10 cells in series to avoid overvoltage and damages when one cell is failed (shorted), and at least 2 strings in parallel to avoid total loss. 132kV capacitor banks are in H-Configuration, ungrounded and 11kV are in double wye, ungrounded. The following are major considerations.

1. To Fuse or NOT to Fuse?

When capacitor fails, dielectric layers in the capacitor, possibly polymer films or kraft papers, may melt or char and foils are weld together, i.e. **shorted**. The latter cells experience higher voltage ($NE/(N-1)$ per cell). The maximum voltage allowed is **110%** of rated. If the string is long enough, i.e. more than 10 cells in series, the other cells do not fail in cascade, hence fuse can be eliminated. The preferred rated current is **135%** of load.

Some cells are **internally fused**, if numbers of series and parallel are large and failing one cell should not lead to force outage; and **externally fused**, for easy identification on failed string. Individual fuse for each capacitor element is provided as required in our Protection Philosophy.

2. To Ground or NOT to Ground?

- a. Grounded Bank:
 - i. Provides a **low impedance path** to ground for lightning surge current and allow surge arrester installation
 - ii. Reduces **transient recovery voltage** (TRV) for switching equipment (approximately twice normal peak voltage)
 - iii. Provides a low impedance path to ground for **triplen harmonics**.
- b. Ungrounded Banks:
 - i. Does not provide a path for **capacitor discharge** current during system fault
 - ii. Does not cause mal-operation of other ground fault protection
 - iii. Does not cause interference to control and communication systems with harmonics
 - iv. Does not allow capacitor discharge to damage any **surge arrester**

3. Delta or Wye Capacitor Bank?

Some indicates that **delta capacitor** requires only 1/3 capacitor cells as required in wye capacitor, from delta-to-wye transformation. Yet, it is not true as it increases voltage stress in each cell, and it is not the first concern in sizing a capacitor. However, delta capacitor is favored for LV as voltage is not a main concern, while **reduced space** is preferred and 2/3

rated reactive power is still be generating (as compared to 1/12) in delta when one branch is in fault. In HV, wye bank is more preferred as it is difficult and spacey to connect the capacitor bank in delta with enough **electrical clearance**. Moreover, harmonic current circulates in delta, creates heating and possibly damages dielectric layers.

4. Single Wye or Double Wye?

Double wye is more preferred as differential (unbalance) protection, as discussed in future section, can be provided against the effect of **harmonics, unbalance system voltage, difference in string impedance** and **inrush current** to the protection of single wye capacitor bank. Yet, double wye capacitor bank takes more space. H-configuration is more preferred than double wye as the protection is **phase discriminative**, i.e. easier to identify the fault point.

5. Network Planning Consideration

A Capacitor Bank is sized to compensate the reactive power (inductive) from load to Power Factor (PF) near to 1.0. Any single failure would not lead to generator side PF and voltage at any point outside the limit.

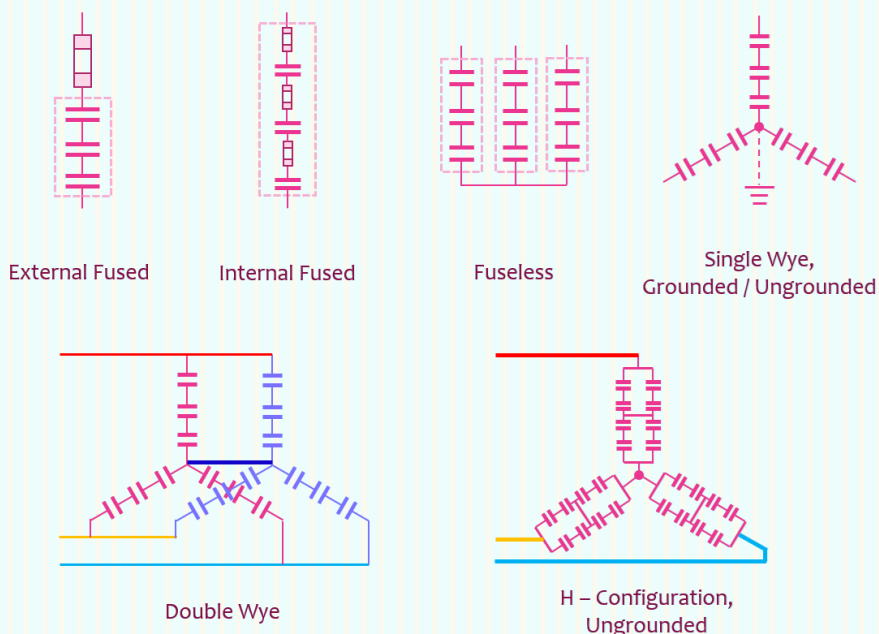


Figure 1:
Type of Capacitor Bank

Capacitor Switching

Three-pole switching applied to capacitor can lead to a large current and voltage surge. **Single Pole Switching**, particularly zero-current opening (ZCS) to avoid inductance current chopping and zero-voltage closing (ZVS) to avoid current surge under step voltage for capacitors, have been embraced over years. Step voltage on switching also depends on **pre-strike and re-strike of CB**, **back-to-back capacitor switching** (with larger and steeper surge), **series resonance** and **load effect**. ZVS (Siemen 3AD) is employed in 11kV VCB while **Point-on-Wave (POW)** Controllers, also known as Synchronizing Switching Controllers (SSC), are employed in 132kV GCB Capacitor Switching.

To perform ZVS in closing, as shown in Figure 2, a VT receiving line voltage across L1 and L2 sense the voltage difference and close L1 and L2 CBs simultaneously. After 90°, L3 is closed. This method is cost effective enough as **dielectric stress** leading to the contact wear and weld is acceptable in 11kV. However, in 132kV, POW Controller is implemented to cater for **synchronizing delay**, **pre-arcing time**, **mechanical vibration damping**, and external factors such as **left charge in capacitor**, **back-to-back energization** and **transformer inrush**. As **rate of recovery of dielectric strength (RRRD)** is normally distributed and pre-arcing requires voltage across CB larger than RRRD, the controller has to sense and predict statistically to determine the closing time, as shown in Figure 3.

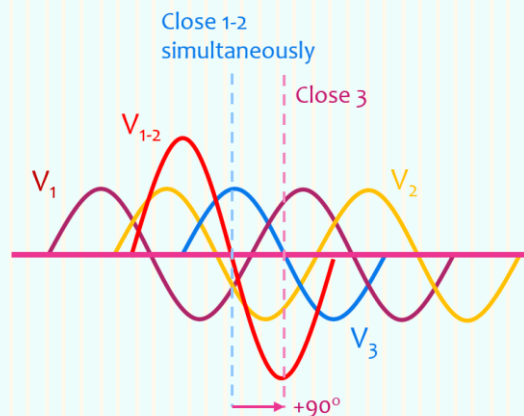


Figure 2:
11kV ZVS Switching
(as depicted in Siemen 3AD IOM)

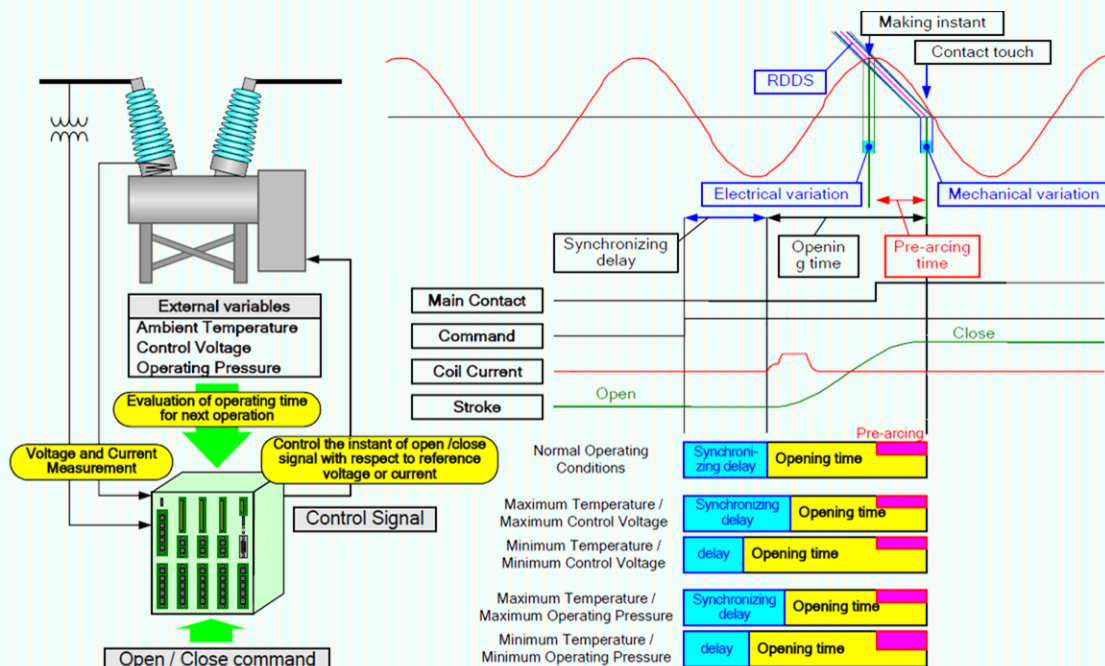
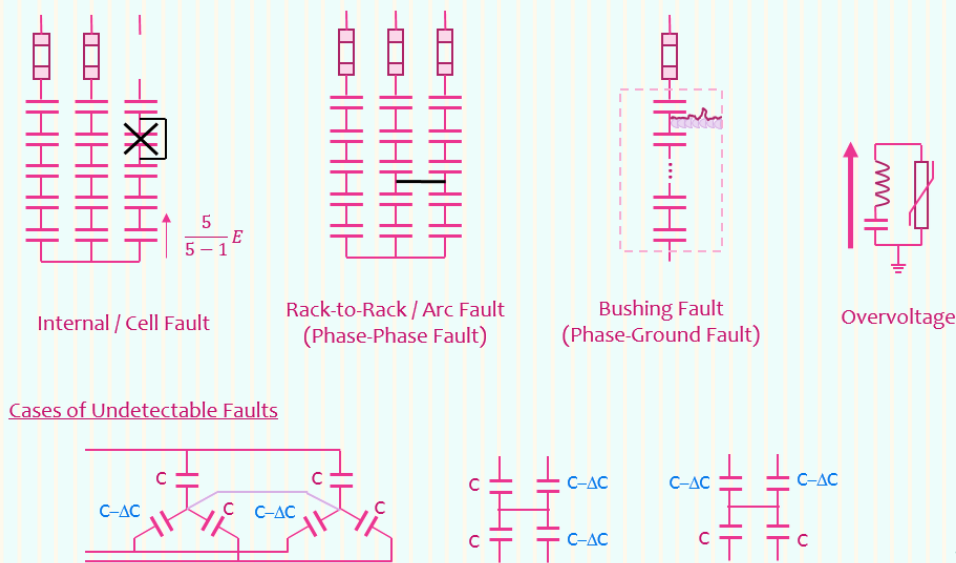


Figure 3:
POW Controllers Methodology

Figure 4:
Types of Faults

Capacitor Bank Fault and Protection

The major reported capacitor bank problems leading to failure are:

1. **Inadequate Voltage Rating** (as it is connected in series with a current limiting inductor L with voltage across capacitor C as $|V_c| = \frac{V_{in}}{1-\omega^2 LC}$, which is potentially larger than input voltage)
2. **Fuse Blowing** (It is caused by short circuit in a capacitor unit, i.e. an **internal fault**, overcurrent due to overvoltage, harmonics or high contact resistance of the fuse unit.)
3. **Thermal Failure** (Capacitor operated at extremely hot condition can fail due to excessive temperature. It may need **forced ventilation**.)
4. **Ferroresonance** (The bank interacts with the source, current limiting inductance and transformer inductance and produces Ferroresonance, which is potentially an **undamped oscillation** in current or voltage. It can lead to capacitor or transformer failure.)
5. **Harmonics** (As capacitor has a low reactance at high frequency, harmonics in nonlinear loads may be absorbed by capacitor bank and causes overheat.)
6. **Dielectric Failure (Capacitance deterioration** is an ageing problem. If one cell is failed and shorted, the latter cell needs to take a higher voltage with deteriorated dielectric, and it can lead to cascade failure.)
7. **Rack Faults and Insulation Failure** (Compact design of capacitor bank can lead to **flashover**. Rack-to-Rack fault is a phase-to-phase fault, while bushing fault is a phase-to-ground fault)
8. **Failure due to External Stress** (Excessive ambient temperature, humidity, temperature cycling, vibrations, shocks and lack of ventilation can also lead to failure)
9. **Human Error** (If protection coordination of fuse selection is not performed correctly, capacitor unit may fail first. For energization of the bank, circuit switcher with closing resistor and current limiting reactor are employed. If CB is opened after fault and is used to energize the capacitor bank without the closing resistor in circuit switcher, the capacitor bank may fail with excessive energization transient.)
10. **Surge Arrester Connection** (During overvoltage, the surge arrester conducts and forces large current to the capacitor if it clamps the reactor only. Note: It requires capacitor grounding if employing a surge arrester)

Common Designs for **Capacitor Bank Protections** are, as illustrated in Figure 5:

- Measure the **neutral voltage** (U_N) of an ungrounded single wye by VT or CVT
- Measure the **tapped capacitor voltage** w.r.t. ground ($3U_o$) and sum up with an **open delta VT**
- Measure the **differential voltage** (ΔU) between bank neutral and busbar
- Measure the **earth current** ($3I_o$) of a grounded single wye with a CT
- Measure the **unbalanced current** with a CT or current differential with two CTs / **unbalance voltage** with a VT between double wye

The above method has compromised the following requirements:

- Stable under **transient** (e.g. inrush, including back-to-back energization with left charge) and **continuous** (e.g. 1 cell failed) **overvoltage**
- Stable under **external unbalance** (i.e. System unbalance voltage does not trigger any protection operation. Capacitor single pole energization can be a concern)
- Stable under **harmonics** (i.e. Triplen harmonics does not trigger any protection operation)
- **Phase Discriminative** (It can be a choice for faster fault location and a concern for single pole reclose)

- **Sensitivity** (The measured voltage portion has a higher sensitivity to faulty cells than the part not measured.)

Protection for Capacitor Bank in 132kV and 11kV are:

- **11kV:** Unbalance Protection + OCEF (inc. Fuse for each element and System OV)
- **132kV:** Unbalance Protection + HSOC as main, OCEF + Balance Protection as backup (inc. Fuse for each element and System OV)

Unbalance Protection in 11kV is in between the two wyes in double wye bank, and that of 132kV is in the H-branch, i.e. phase discriminative. However, as illustrated in Figure 4, there is possibility for NOT tripping, when one cell is blown with differential current not enough to trigger unbalance protection, burns a cell in another side and reaches equilibrium stage again. Hence, a **balance relay**, which triggers after the unbalance alarm is ON (0.08A, 5s) and OFF (0.1s delay), is installed as backup. However, this scheme may not work under some **rack-to-rack fault**.

Conclusion

This report discusses the main concerns and rationales in employing a double wye and H-configuration capacitor bank in 11kV and 132kV respectively, the switching method and protection scheme for them.

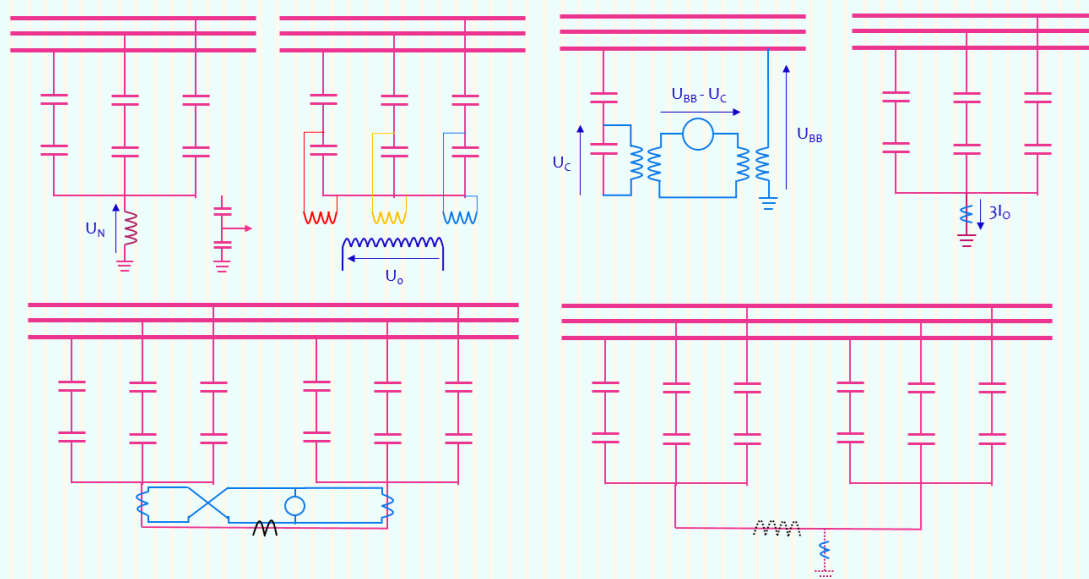


Figure 5:
Capacitor Bank Protection Schemes