Detector and Comparator Circuits in Protection Relaying

In light of technological advancements, protection relaying has transitioned from electromechanical relays—employing coils and induction disks—to static relays that utilize transistor-based circuits to perform the functions of detectors and comparators. Although the practical use of static relays has diminished, digital relays continue to emulate their functions, ensuring stable and rapid operation for protection applications.

Zero Crossing Detector Circuit

Zero Crossing Detector Circuit, as illustrated in Figure 1, basically involves the sine to square wave conversion by a level detector circuit followed by a pulse circuit, which consists of one-shot monostable circuit or a differentiator. The zero-crossing detection is associated with the production of a pulse at a zero-crossing.

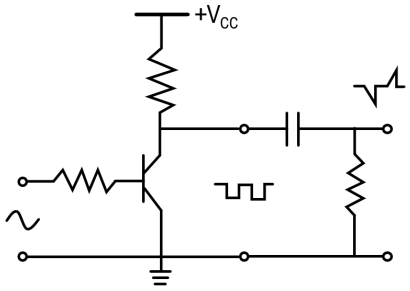


Figure 1: Zero Crossing Detector Circuit

Output Devices

The output contacts of a relay serve multiple functions, including tripping, inter-tripping, alarm signalling, and remote indication. Among static components, the thyristor stands out as an excellent method for tripping circuit breakers using a low-power signal of short duration. It operates with a gate signal lasting microseconds (pickup time: 10–20 ms; dropout time: 100 ms), and once triggered, it remains in conduction until broken by the auxiliary contact of the circuit breaker.

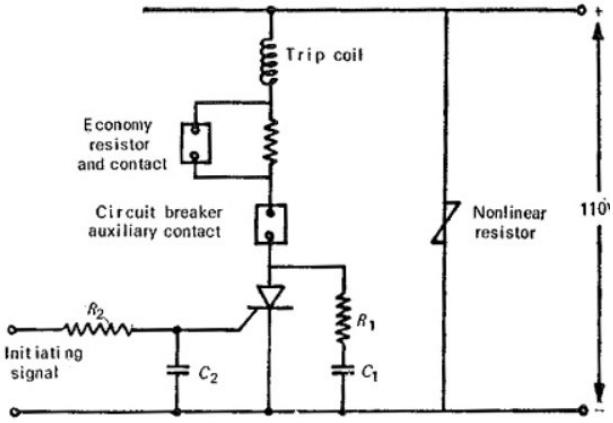


Figure 2: Thyristor Bridge Tripping Circuit

A typical thyristor tripping circuit is shown in Figure 2. R1 and C1 are included to prevent excessive surges appearing across the thyristor. The small resistance R1 limits the capacitor-discharge current on operation. The filter circuit connected to the gate electrode has the capacitor C2 connected immediately adjacent to the thyristor, to minimize pickup voltages on the gate electrode.

Reed relays, though not static in nature, are very much suitable to semiconductor circuits. If properly designed they can also perform fast tripping of circuit breaker, provided the power factor and ratings of trip circuit are specified. The reed relays being very light in weight are susceptible to maloperation due to shock and vibrations.

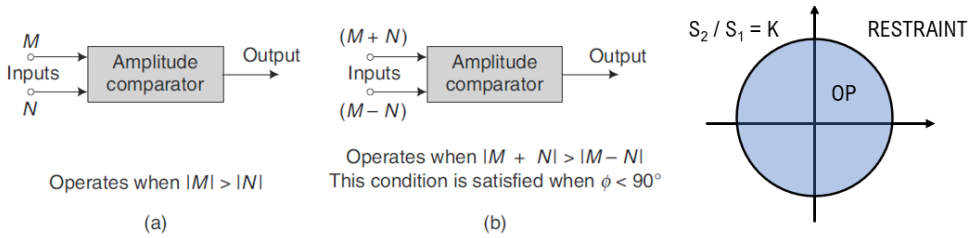


Figure 3: Amplitude Comparison

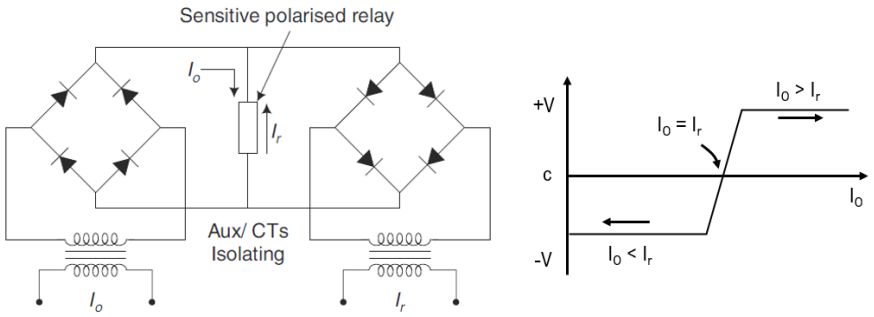


Figure 4: Circulating Current Type Rectifier Bridge Comparator
(a) Basic Circuit (b) Output Voltage
RL – Polarized Relay Operated in Direction Shown.

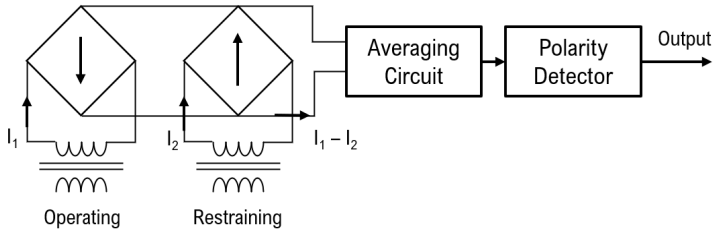


Figure 5: Rectifier Bridge Comparator with Static Output Device

Static Amplitude Comparator

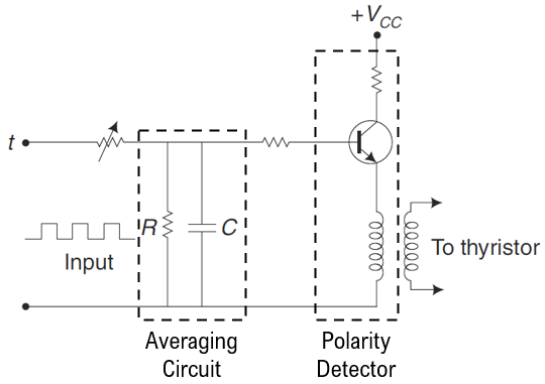
If the two input signals are S1 and S2 the amplitude comparator gives positive output only if S2/S1 ≤ K (Figure 3), S1 is the operating quantity and S2 is the restraining quantity. Ideally, the comparison of the two input signals is independent of their level and their phase relationship. The function is represented by a circle in the complex plane, with its centre at the origin: this defines the boundary of the marginal operation. Static Amplitude Comparator may be of the following types:

- Integrating comparators,
- Instantaneous comparators, and
- Sampling comparators.

Integrating Comparators

It is possible to arrange rectifier bridge networks as amplitude comparators. Rectifier bridge comparator can either be of circulating current type or opposed voltage type.

Basic circuit for the circulating current type of Static Amplitude Comparator is shown in Figure 4. The polarized relay operates when S1>S2, where S1=$K_1 i_1$ and S2=$K_2 i_2$. This arrangement provides a sensitive relay whose voltage may be ideally represented by Figure 4(b). The relay voltage will never exceed twice the forward voltage drop of the rectifiers, and typically will be of the order of 1 volt.



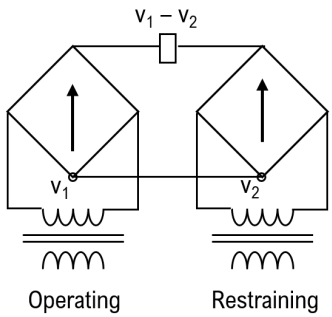


Figure 6: Integrator Circuit

Figure 7: Opposed Voltage Type Rectifier Bridge Comparator

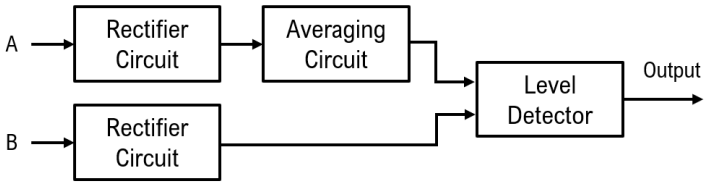


Figure 8: Block Diagram of Averaging Type Instantaneous Amplitude Comparator

Instead of the polarized relay, a static integrator can be used consisting of an averaging circuit and the polarity detector circuit as shown in Figure 5. The two currents i_1 and i_2 are rectified and their rectified difference ($i_1 – i_2$) is averaged. The output is obtained only if the averaged value is positive.

An integrator circuit is shown in Figure 6. The tripping occurs when the capacitor voltage reaches the setting value of the level detector and triggers a thyristor.

The opposed voltage type comparator shown in Figure 7 works with voltage input signals derived from PTs. The operation in this case depends on the average of the difference of the rectified voltages (v_1-v_2). In this case the limiting action is the wrong way, as the rectifiers have higher resistance at lower voltages. The rectifiers are not protected at higher currents.

Instantaneous Comparators

Instantaneous or direct amplitude comparators can be of two types: **averaging type** and **phase splitting type**.

In the averaging type instantaneous amplitude comparator, the restraining signal is rectified and smoothed completely in order to provide a level of restraint. This is then compared with the peak value of the operating signal, which may or may not be rectified, but is not smoothed. The tripping signal is provided if the operating signal exceeds the level of restraint. The block schematic diagram is shown in Figure 8. The wave shapes are shown in Figure 9.

Since the above method involves smoothening, the operation is slow. A faster method is phase splitting before rectification as shown in Figure 10.

Here the input is split into six components 60° apart, so that, it is smoothed within 5%. The averaging circuit can be eliminated. The operating time here is determined by the time constant of the slowest arm of the phase-splitting circuit and by the speed of the output device.

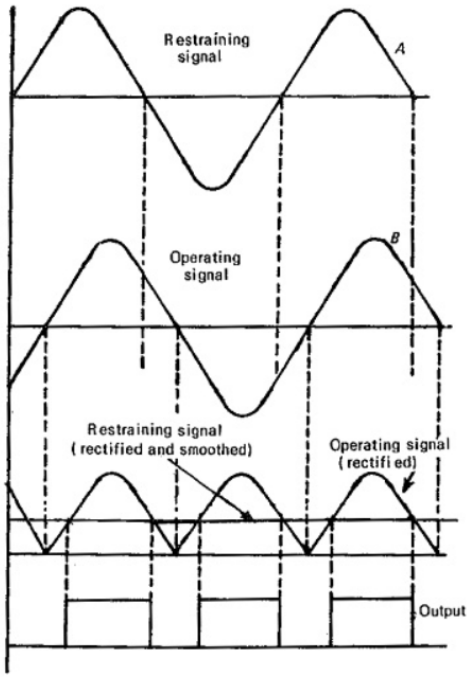


Figure 9: Waveform of Instantaneous Amplitude Comparator

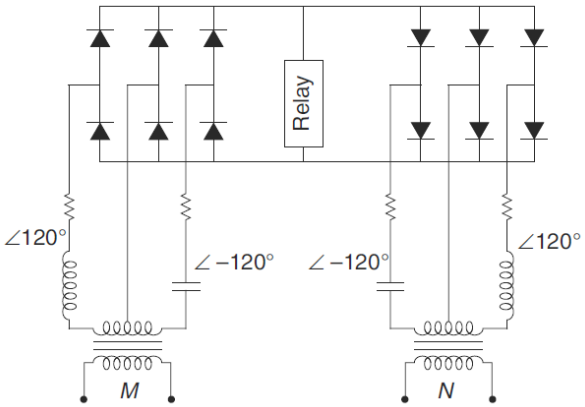


Figure 10: Phase Splitting of Input to Amplitude Comparator

Sampling Comparators

Sometimes it is convenient to get the required characteristics by comparing the magnitude of one input signal at a certain point on its wave against the rectified and smoothed value of the second signal. Reactance characteristic is one such case where the instantaneous value of the voltage at current zero is compared against the rectified and smoothed value of current. If I lags V by an angle Φ, then the value of voltage at current zero is $V_m \sin\phi$.

The reactance relay operates for X < K, i.e.

$$Z \sin\phi < K \;\rightarrow\; \frac{V}{I}\sin\phi < K$$

$$\frac{V_m}{\sqrt{2}}\sin\phi < KI_{avg} \times 1.11 \;\rightarrow\; V_m \sin\phi < K' I_{avg}$$

The block schematic diagram is shown in Figure 11.

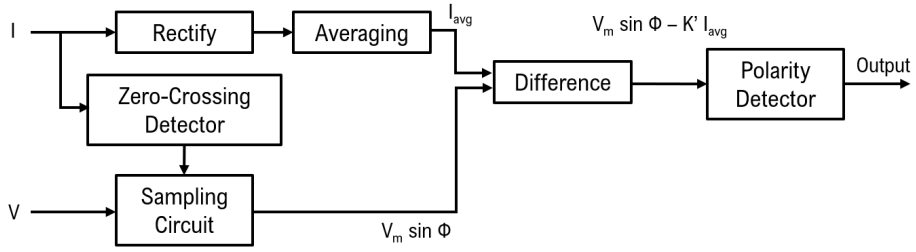


Figure 11: Block Diagram for Reactance Relay Comparing Instantaneous Value of Voltage at Current Zero with Average Current

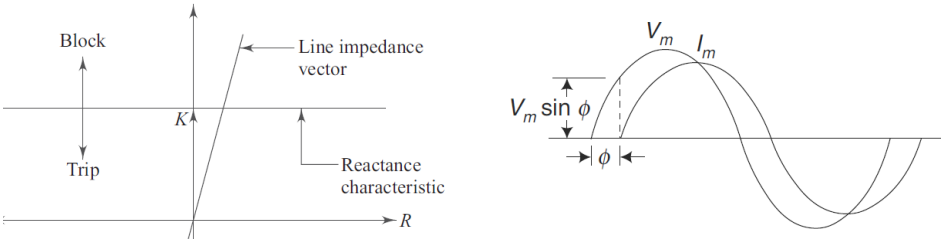


Figure 12: Voltage and Current Waveform of Reactance Relay

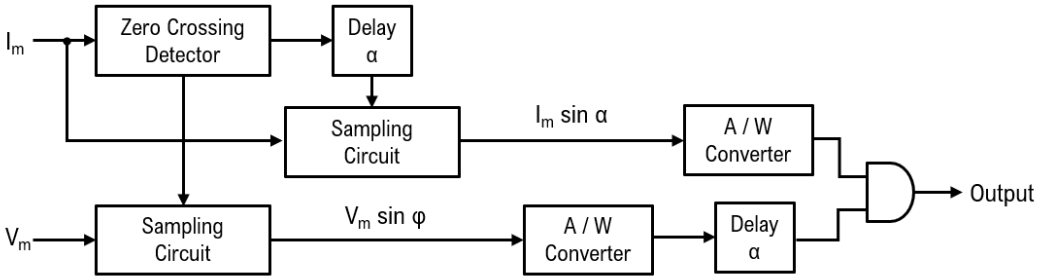


Figure 13: Block Diagram of Sampling Technique

It is also possible to compare the instantaneous magnitude of one signal at a certain moment with the instantaneous magnitude of the second signal at that very moment or at certain other moment. It simply means that one or both signals can be sampled.

For the same reactance relay of the previous case, for operation, we have

$$X < K \rightarrow Z \sin\phi < K \rightarrow \frac{V}{I} \sin\phi < K$$

$$\frac{V_m}{\sqrt{2}} \sin\phi < K \frac{I_m}{\sqrt{2}} \frac{\sin\alpha}{\sin\alpha} \rightarrow V_m \sin\phi < K' I_m \sin\alpha$$

Figure 12 shows the voltage and current waveforms.

Comparison of two instantaneous magnitudes here is made by converting the magnitudes into proportional pulse widths and then comparing with an AND gate. If the two samples are taken at different instants, the pulse width representing the one taken first in time sequence is delayed by the time difference between the two sampling instants, before feeding into the AND gate. The scheme is represented in block diagram in Figure 13 and Figure 14 shows the wave forms.

By using sampling techniques, dispense with the phase shifting and mixing circuits can be dispensed. Yet, the dispense requires a greater degree of sophistication in the relay circuitry but it achieves a saving in both space and cost. The measuring circuits are isolated from the transformer secondaries, except during the 50μs sampling period in each half cycle, and the possibility of maloperation due to spikes on the input wave forms.

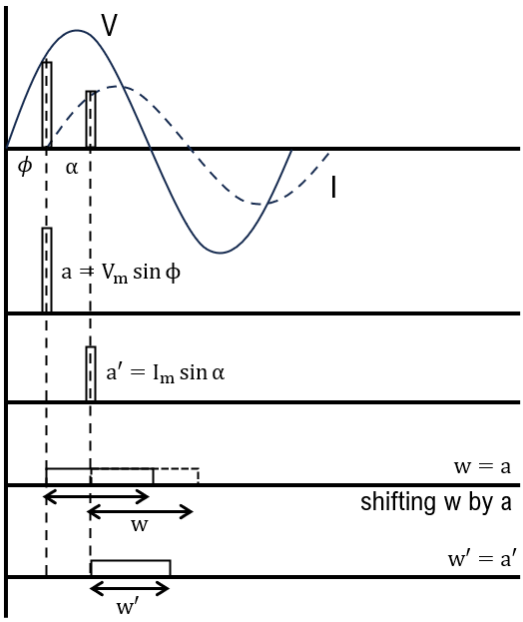


Figure 14: Waveform Illustrating Sampling Technique Principles

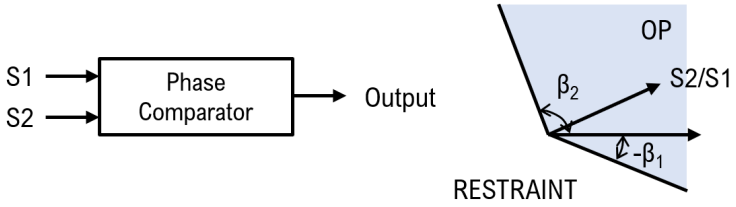


Figure 15: Phase Comparator Output when angle θ between S1 and S2 is within β1 and β2

Phase Comparator Circuit

Phase Comparator Circuit technique is the most widely used for all practical directional, distance, differential and carrier relays. If the two input signals are S1 and S2, the output occurs when the inputs have a phase relationship lying within specified limits.

Both inputs must exist for an output to occur; ideally, operation is independent of their magnitudes, and is dependent only on their phase relationship.

Figure 15 illustrates the Phase Comparator Circuit in its simple form. The function as defined by the boundary of marginal operation is represented by two straight lines from the origin of the complex plane.

The condition of operation can be put mathematically as $-\beta_1 \leq \theta \leq +\beta_2$ where θ is the angle by which S2 leads S1. If $\beta_1 = \beta_2 = 90°$, the comparator is known as cosine comparator and if $\beta_1 = 0$ and $\beta_2 = 180°$ it is a sine comparator.

Static Phase Comparator Circuits may be of the following types:

- Vector Product Comparator
- Coincidence type phase comparator.

Amongst the vector product comparators are the Hall effect phase comparator and the magneto-resistivity phase comparator.

Coincidence Type Phase Comparator

Phase comparison is simple when dealing with signals of equal strength whose coincidence is readily measurable. Coincidence means the period where two waveforms are in same polarity. The period of coincidence ψ of S1 and S2 depends on the phase difference θ, given that the signals are in same frequency. Figure 16 illustrates the coincidence of signals for different phase relationships in Coincidence Type Phase Comparator.

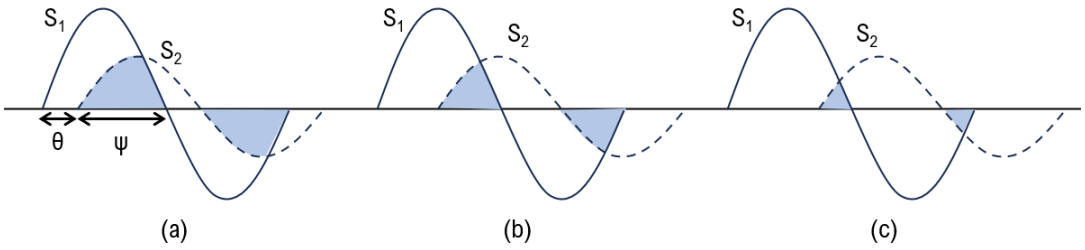


Figure 16: Coincidence of Signals:
(a) S2 lags S1 by less than π/2 (b) S2 lags S1 by π/2
(c) S2 lags S1 by more than π/2

The period of coincidence of two signals with a phase difference of θ is ψ=180-θ. There are different techniques measuring the period of coincidence.

Direct Phase Comparison

The number of basically different methods of obtaining useful characteristics from a direct phase comparator circuit is confined to the following:

(i) **Block instantaneous comparison** in which the duration of polarity coincidence determines the output. The tripping criterion is that the duration of the first coincidence should exceed a specified time, usually one quarter of the power-frequency period.

(ii) **Pulse comparison** in which the polarity of one signal is measured during a short interval in the cycle of the second signal, usually, but not necessarily at the latter's peak.

The block diagram of the pulse relay is shown in Figure 17. Line voltage and current are applied to two measuring circuits, which produce complex output voltages.

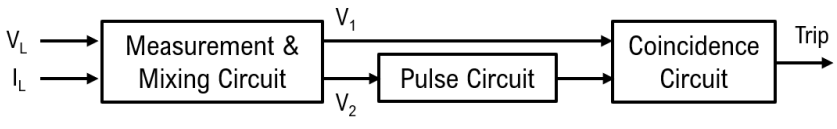
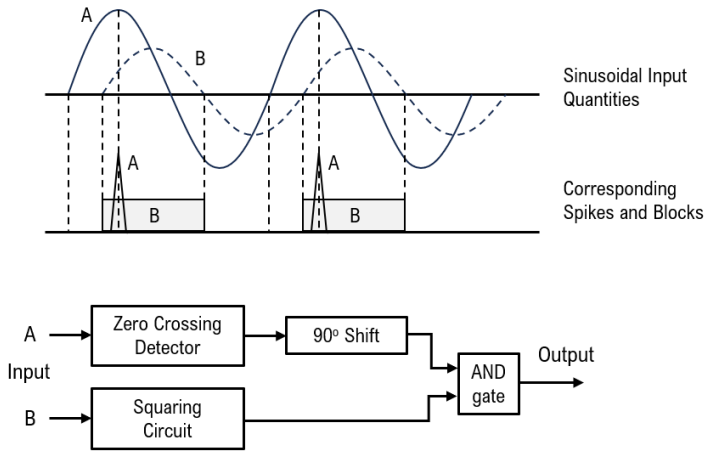


Figure 17: Block Schematics of Pulse Relay

Voltage V_2 is applied to a pulsing circuit which produces a positive pulse once every cycle, when V_2 is at its positive maximum. V_1 and the pulse derived from V_2 are then applied to the terminals of a Coincidence Type Phase Comparator circuit of the type requiring both input terminals to become positive before producing any potential change at its output terminals. The criterion for relay operation is thus defined, since the coincidence circuit only yields an output when the pulse is present, and then only if V_1 is positive at this instant. If θ is the angle between V_1 and V_2, it follows that $-90° \leq \theta \leq +90°$ for V1 to be positive at the instant of V2 maximum.



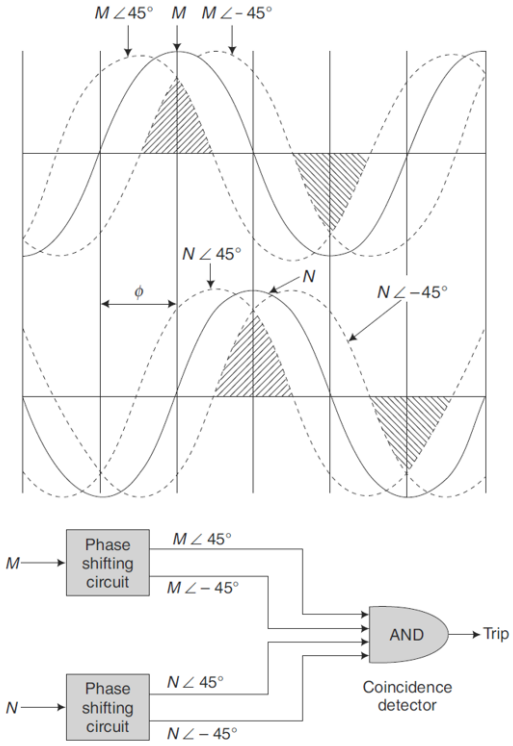


Figure 18: Block Diagram and Waveform of Block Spike Method (Left)
Figure 19: Phase Comparator with Phase Split Input (a) Waveform (b) Block Schematic (Right)

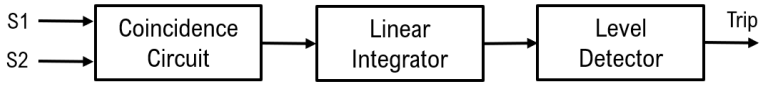


Figure 20: Block Schematics for Integration of Coincidence Blocks

Another method for direct phase comparison is by block spike method. Input B is squared and input A turns into a spike preferably at the instant of its peak value; the spike and block signals are then fed through an AND gate, as illustrated in Figure 18. Coincidence Type Phase Comparator of input signals occurs only for $-90° \leq \theta \leq +90°$.

Phase Splitting Technique

Phase splitting technique requires two phase shifted components (±45°) for each of the input signals and, these four components are fed to an AND gate. An output results if all the four are simultaneously positive at any time in the cycle. Figure 19 shows an activated relay with input phase difference is in range of $-90° \leq \theta \leq +90°$.

With smaller time constants of phase shifting circuits, the method is slightly faster than the previous method. By using two such comparators one for each polarity the time of operation can be reduced to less than half a cycle.

Integrating Phase Comparison

Time overlap of the two sinusoidal inputs is measured for each cycle by integrating the output of an AND gate through which they are fed. The period of coincidence is measured, and only if it exceeds 90° (for a symmetrical comparator) the output is obtained, so that the condition is $-90° \leq \theta \leq +90°$ (Cosine Comparator).

In earlier integrating phase comparators transistor-type AND gate was employed. In recent types, the periods of coincidence are integrated and then fed into a level detector, the critical operating threshold of which occurs when the periods of coincidence and noncoincidence are equal, i.e. $\theta = \pm 90°$. Figure 20 shows the basic arrangement for the integration of coincidence blocks.

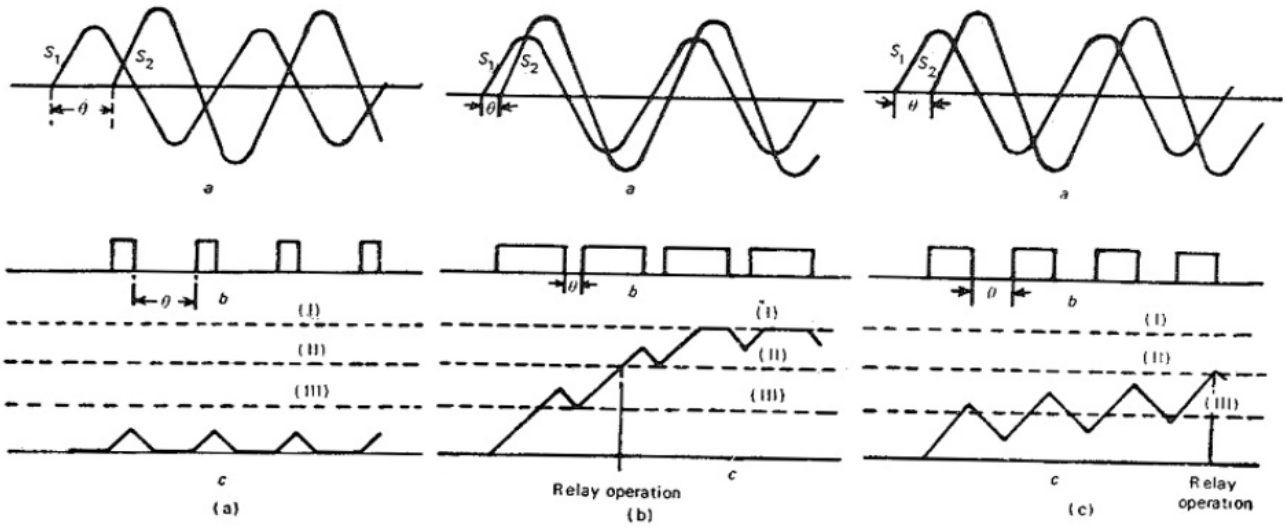


Figure 21: Effect of Varying Period of Coincidence:
(a) θ > π/2 (b) θ < π/2 (c) θ = π/2
(a) Input signals to coincidence circuit, (b) output from coincidence circuit, (c) integrator output
(i) upper limit, (ii) set level, (iii) reset level

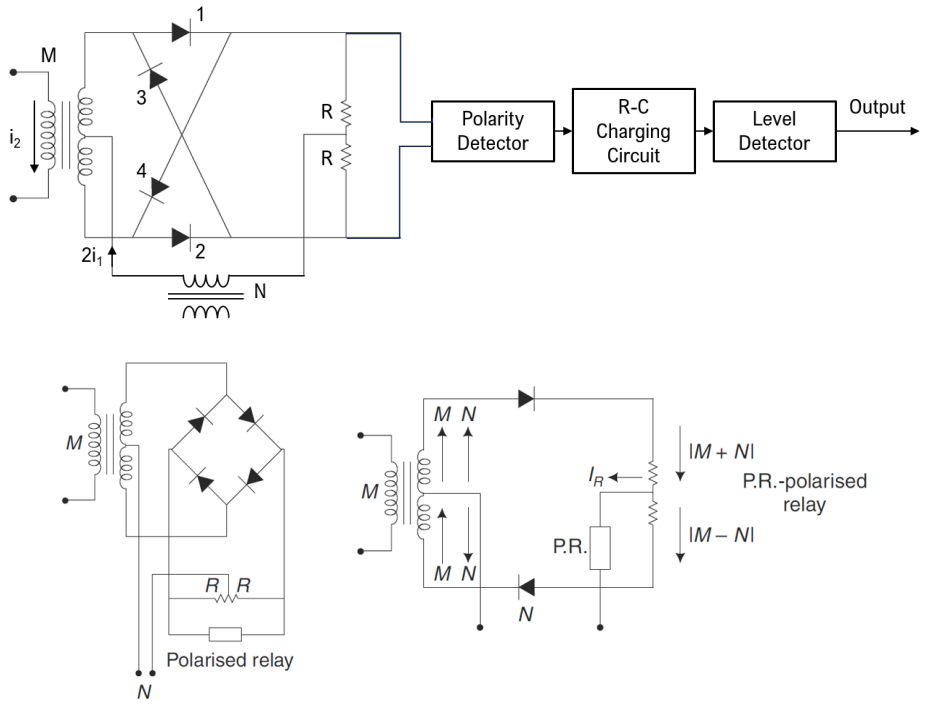
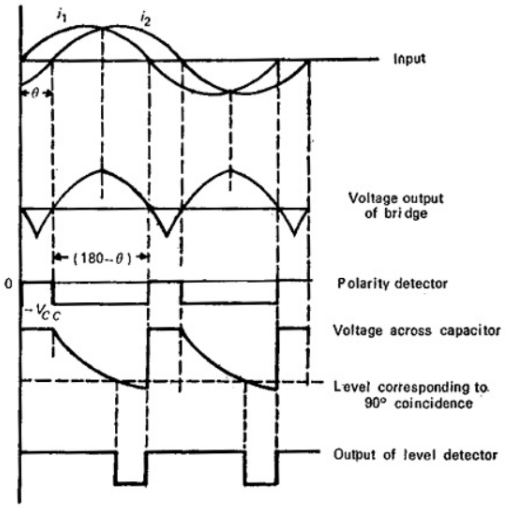


Figure 22: Basic Circuit of An Integrating Phase Comparator using Rectifier Bridge AND gate

The input quantities S1 and S2 are compared in a coincidence circuit producing standard output pulses, which are positive when S1 and S2 are of the same polarity and negative when they are of opposite polarity. The pulses are applied to an integrating circuit whose output increases linearly during the time when the pulse is positive and falls at the same rate when the polarity reverses. The level detector switches when the integrator output exceeds some preset value, and resets when the output falls below some second value. The operation resulting from differing coincidence periods is illustrated in Figure 21. The rise and fall rates in the integrator are at the designer's disposal, so that the critical phase angle may be set to any desired value. Both the level detector set and reset levels are critical in relation to the total excursion limits of integrator linearity and to the slope of the output.



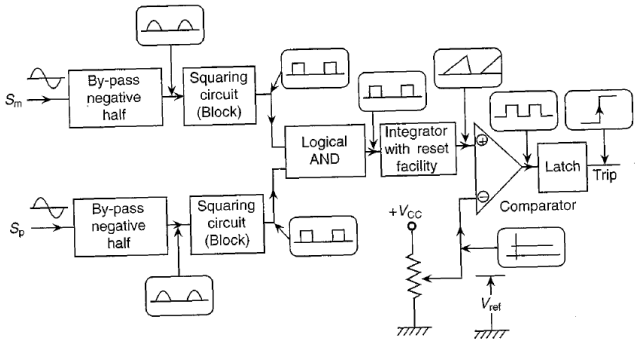


Figure 23: Waveform of Integrating Phase Comparator (Left)
Figure 24: Cosine-Type Phase Comparator based on Coincidence Principles (Right)

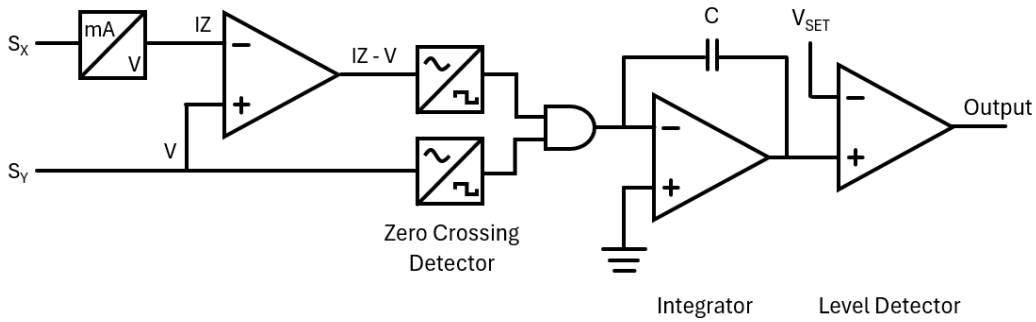


Figure 25: Phase Comparator in Modern Protection Scheme

Another type of integrating phase comparator employs a rectifier bridge AND gate. This approach offers advantages in terms of simplicity and cost-effectiveness. The system utilizes a rectifier bridge following a polarity detection circuit. The basic circuit, depicted in Figure 22, operates with current-form inputs.

The output current of the rectifier bridge supplied to a centre tapped resistance R-R is at any moment equal to the smaller of the two input currents. The path of the current through the bridge is established by the larger of the two currents and depends upon their relative instantaneous polarity.

- If $i_1 > i_2$, the current will flow in rectifiers 1 and 2, if i_1 is positive; and in rectifiers 3 and 4, if i_1 is negative.
- If $i_2 > i_1$, the current flows in rectifiers 1 and 4 if i_2 is positive; and rectifiers 2 and 3, if i_2 is negative.
- If i_1 and i_2 have the same polarity the voltage across R-R (output voltage) is positives whereas this is negative if the two currents have opposite polarities (see Figure 23). In other words, the output voltage is positive during positive and negative coincidence periods; and negative during the period of anti-coincidence (opposite polarities).

The time of operation with single bridge is less than half a cycle.

THE END