# Bare Demo of IEEEtran.cls for Journals

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Abstract—The abstract goes here.

Index Terms—

#### I. Introduction

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mds December 27, 2012

A. Subsection Heading Here

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#### II. CARRY SELECT ADDER

- A. Introduction
- B. Timing Models for n-bit Carry Selct Adder

In this section, we describe the modeling method for the CSA timing, with the aim of forming the relationship between the operating frequency and the corresponding maximum word-length of CSA. This information can be employed to determine the truncation error based on the models presented in Section.xxx.

In an n-stage CSA, let the stage delay be denoted as  $d_0 \dots d_{n-1}$ , where  $d_0$  and  $d_{n-1}$  represent the delay of MSB stage and LSB stage, respectively. In our analysis, we follow the previous assumption that delay is caused due to carry propagation and, in this case, multiplexing. Thus the delay of the  $i^{th}$  stage can be obtained through (1), where  $\mu_{carry}$  denotes the delay of 1-bit carry propagation and  $\mu_{mux}$  detnoes the delay of multiplexer.

$$d_i = n_i \cdot \mu_c + xxx \cdot \mu_{mux} \tag{1}$$

Under the timing-driven design environment, the delay of each stage of CSA is set to be approximately uniform to lead to the fastest operation. In this case we obtain (2).

$$d_0 = d_1 = \dots = d_{n-1} \tag{2}$$

Substituting (1) into (2) yields (), which denotes the word-length of stage i.

$$n_i = n_0 - xxx \cdot \frac{\mu_{mux}}{\mu_c} \tag{3}$$

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Therefore the word-length of CSA is given by (4).

$$n_{CSA} = \sum_{i=0}^{n-1} n_i = cn_0 - \frac{\mu_{mux}}{\mu_{carry}} \cdot \frac{(c+1)(c-2)}{2}$$
 (4)

In the conventional situation, the word-length of both RCA and CSA should be truncated in order to meet timing. Hence we obtain (5), where  $n_{RCA}$  is determined through (xxx).

$$\mu_c \cdot n_{RCA} = \mu_c n_0 + \mu_{mux} \tag{5}$$

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Based on (4) and (5) we form the relationship between the word-length of CSA and RCA under a given timing constraint, as presented in (6).

$$n_{CSA} = c n_{RCA} - \frac{\mu_{mux}}{\mu_c} \cdot \frac{(c+2)(c-1)}{2}$$
 (6)

In addition, combining (3) and (5) to ensure that  $n_{c-1} > 0$ . Therefore the stage number is bounded by (7).

$$c < n_{RCA} \cdot \frac{\mu_c}{\mu_{mux}} + 1 \tag{7}$$

- C. Model Verification
- D. Comparison between CSA and RCA

III. CONCLUSION

The conclusion goes here.

## APPENDIX A

PROOF OF THE FIRST ZONKLAR EQUATION

Appendix one text goes here.

## APPENDIX B

Appendix two text goes here.

## ACKNOWLEDGMENT

The authors would like to thank...

### REFERENCES

[1] H. Kopka and P. W. Daly, A Guide to ETeX, 3rd ed. Harlow, England: Addison-Wesley, 1999.

Michael Shell Biography text here.

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John Doe Biography text here.

Jane Doe Biography text here.