Virtex-6 FPGA

Control Logic

System Clock → Memory Control → Frequency Generator Control

Test Clock Generator

MMCM1 → MMCM2

Test Vectors → Memory

LR
LR
…
LR

Test Clock

Circuit Under Test

SR
SR
…
SR

Validation

Memory Address

Input Vectors

Results

Error-free Data → Error-free Results → Computation of Errors

Off-line Comparison