Efficient FPGA Implementation of Overclocking Friendly Online Arithmetic Operators

***Abstract*—The abstract goes here.**

I. Introduction

II. Background and Relevant Work

A. Online Arithmetic

B. FPGA Architecture

III. Digit-parallel Online Adder on FPGAs

IV. Digit-parallel Online Multiplier on FPGAs

V. Results

VI. Conclusion

The conclusion goes here.

Acknowledgment