Bare Demo of IEEEtran.cls for Journals

Michael Shell, *Member, IEEE,* John Doe, *Fellow, OSA,* and Jane Doe, *Life Fellow, IEEE*

Abstract—The abstract goes here.

Index Terms—

I. INTRODUCTION

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December 27, 2012

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II. CARRY SELECT ADDER

A. Introduction

B. Timing Models for n-bit Carry Selct Adder

In this section, we describe the modeling method for the CSA timing, with the aim of forming the relationship between the operating frequency and the corresponding maximum word-length of CSA. This information can be employed to determine the truncation error based on the models presented in Section.xxx.

In an n-stage CSA, let the stage delay be denoted as $d_0 \ldots d_{n-1}$, where d_0 and d_{n-1} represent the delay of MSB stage and LSB stage, respectively. In our analysis, we follow the previous assumption that delay is caused due to carry propagation and, in this case, multiplexing. Thus the delay of the ith stage can be obtained through (1), where μ_{carry} denotes the delay of 1-bit carry propagation and μ_{mux} detnoes the delay of multiplexer.

$$d_i = n_i \cdot \mu_c + (i+1) \cdot \mu_{mux} \tag{1}$$

Under the timing-driven design environment, the delay of each stage of CSA is set to be approximately uniform to lead to the fastest operation. In this case we obtain (2).

$$d_0 = d_1 = \cdots = d_{n-1} \tag{2}$$

Substituting (1) into (2) yields (3), which denotes the CSA word-length of stage i. Note that the word-length of stage

M. Shell is with the Department of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, 30332 USA e-mail: (see http://www.michaelshell.org/contact.html).

J. Doe and J. Doe are with Anonymous University.

$c - 1$ and $c - 2$ are identical, since the least significant stage is composed of RCA.

$$n_i = \begin{cases} n_0 - i \cdot \frac{\mu_{mux}}{\mu_c}, & \text{if } i \in (2, c-2] \text{ and } c > 2 \\ n_0 - (c-2) \cdot \frac{\mu_{mux}}{\mu_c}, & \text{if } i = c-1 \text{ and } c \geqslant 2 \end{cases} \tag{3}$$

Therefore the word-length of CSA is given by (4).

$$n_{CSA} = \sum_{i=0}^{n-1} n_i = cn_0 - \frac{\mu_{mux}}{\mu_{carry}} \cdot \frac{(c+1)(c-2)}{2} \tag{4}$$

In the conventional situation, the word-length of both RCA and CSA should be truncated in order to meet timing. Hence we obtain (5), where n_{RCA} is determined through (xxx).

$$\mu_c \cdot n_{RCA} = \mu_c n_0 + \mu_{mux} \tag{5}$$

Based on (4) and (5) we form the relationship between the word-length of CSA and RCA under a given timing constraint, as presented in (6).

$$n_{CSA} = c \cdot n_{RCA} - \frac{\mu_{mux}}{\mu_c} \cdot \frac{(c+2)(c-1)}{2} \tag{6}$$

It can be seen that $c = 1$ leads to $n_{CSA} = n_{RCA}$. This is because the least significant stage of CSA is built by RCA. In addition, combining (3) and (5) to ensure that $n_{c-1} > 0$. Therefore the stage number is bounded by (7).

$$c < n_{RCA} \cdot \frac{\mu_c}{\mu_{mux}} + 1 \tag{7}$$

C. Model Verification

As seen in (6), the value of μ_{mux}/μ_c should be determined before applying the timing model. This is achieved by keeping $i = 0$ in (1) while varying the value of n_0. The corresponding d_0 is recorded through the timing analysis tool. Hence μ_{mux}/μ_c can be obtained by fitting those values, as presented in Figure.xxx. Out experimental results show that $\mu_{mux}/\mu_c \approx 8$.

Using this information, we verify our model with the results obtained through post place and route simulations of Xilinx Virtex-6 FPGA. Figure.xxx demonstrates both the modeled value and the experimental results of the maximum word-length of RCA and 2-stage CSA, respectively, under a given operating frequency. Note that tht maximum input word-length is 16-bit, hence the modeled value is set to 16 if it expires.

It can be seen that our model provide slight conservative outcomes than the experimental data, especially at higher operating frequency. This is because the model coefficients are obtained based on timing analysis, which is designed to ensure correct functionality across a range of operating conditions. In addition, routing delay might be introduced to enlarge the overall delay, while our models consider logic delay only.

D. Area Overhead

Figure.xxx demonstrates the maximum word-length for RCA and CSA with 2 stages and 3 stages respectively under a range of operating frequencies. We only investigate 3 stages since the maximum stages number predicted in (7) is 3. It can be seen that in comparison to RCA, CSA achieves greater word-length when frequency is intially increased. This means smaller truncation error can be obtained by CSA for a given frequency. RCA outperforms than CSA when very high frequency is applied, which in turn leads to small word-length for both structures. In addition, the word-length of 3-stage CSA is always greater than 2-stage CSA across the entire frequency domain, as expected.

However, the accuracy benefits brought by CSA comes with the cost of large area overhead. Figure.xxx depicts the resource usage (in terms of the number of Look-Up Tables (LUTs)) used for all three structures. It can be seen that the 3-stage CSA consumes $2.4\times \sim 3.7\times$ area than RCA, while the number is $1.7\times \sim 3.1\times$¡++¿

the 3-stage CSA costs

The stage number is determined by (7)

III. Conclusion

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Appendix A
Proof of the First Zonklar Equation

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Appendix B

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Acknowledgment

The authors would like to thank...

References

[1] H. Kopka and P. W. Daly, *A Guide to LATEX*, 3rd ed. Harlow, England: Addison-Wesley, 1999.

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