erform an offline comparison of the output of the original circuit at the rated frequency with the output of the over-clocked as well as the truncated designs using the same input vectors.

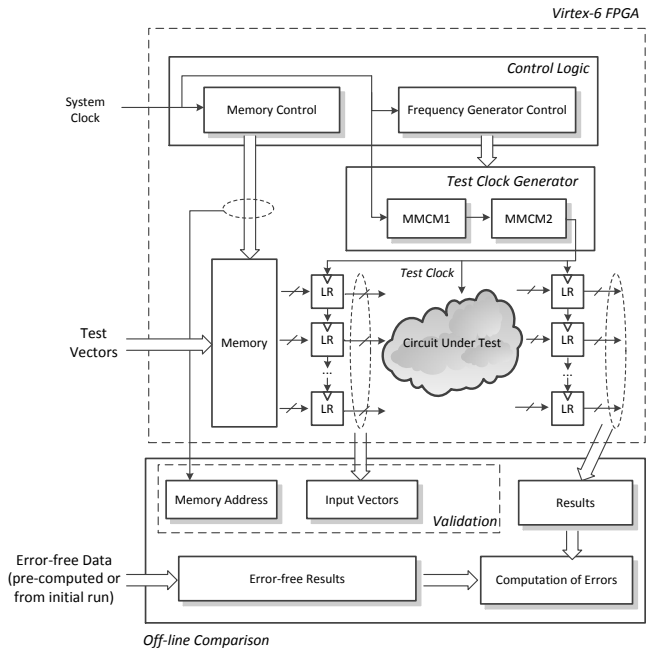

Fig. 1. Test framework, which is composed of a measurement architecture (the dotted box) on an FPGA and an off-line comparator using software.

The test frequency generator is implemented using two cascaded mixed-mode clock managers (MMCMs), created usi