Title

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***Abstract*—The abstract.**

***Index Terms*—**

I. Introduction

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II. Carry Select Adder

A. Introduction

Since the delay of RCA is determined by the length of carry chain, there are several alternative adder architectures proposed to shorten the carry chain. For instance, the carry select adder (CSA) is designed to overlap carry propagation in sections such that the operating speed can be boosted. In a CSA, the carry chain is divided into multiple stages. Each stage contains two RCAs and two multiplexers. For a given input, computations are performed twice simultaneously, with the carry input as zero and one respectively. The results are then selected according to the actual carry input. Although this structure brings timing benefits, it costs extra hardware resources than RCA as the carry chain is duplicated and multiplexers are expensive especially in the FPGA technology. In this section, silicon area is incorporated as the third metric besides accuracy and performance. We explore the trade-offs between these three factors for both adder structures. The objective is to demonstrate the best design choice for a given set of design constraints.

B. Timing Models for n-bit Carry Select Adder

We initially describe the modelling method for the CSA timing, with the aim of forming the relationship between the operating frequency and the corresponding maximum word-length of CSA. This information can be employed to determine the truncation error based on the models presented in Section.xxx.

In a CSA with c stages, let the stage delay be denoted by $d_0 \dots d_{c-1}$, where d_0 and d_{c-1} represent the delay of the most significant stage and the least significant stage, respectively. Unlike other stages, the least significant stage is built by one RCA only, since it is directly driven by the carry input. In our analysis, we follow the previous assumption that delay is due to carry propagation as well as, in this case, multiplexing the carry output. Therefore the delay of the i^{th} stage can be obtained through (1), where μ_c denotes the delay of 1-bit carry propagation and μ_{mux} denotes the delay of multiplexing.

$$d_i = n_i \cdot \mu_c + (i+1) \cdot \mu_{mux} \tag{1}$$

Under the timing-driven design environment, the delay of each stage of CSA is set to be approximately uniform for the fastest operation. In this case we obtain (2).

$$d_0 = d_1 = \cdots = d_{n-1} \tag{2}$$

Substituting (1) into (2) yields (3), which denotes the CSA word-length of stage i. Note that the word-length of stage $c-1$ and $c-2$ are identical, since the least significant stage is composed of RCA.

$$n_i = \begin{cases} n_0 - i \cdot \frac{\mu_{mux}}{\mu_c}, & \text{if } i \in (2, c-2] \text{ and } c > 2 \\ n_0 - (c-2) \cdot \frac{\mu_{mux}}{\mu_c}, & \text{if } i = c-1 \text{ and } c \geqslant 2 \end{cases} \tag{3}$$

The word-length of CSA is then given by (4).

$$n_{CSA} = \sum_{i=0}^{n-1} n_i = cn_0 - \frac{\mu_{mux}}{\mu_{carry}} \cdot \frac{(c+1)(c-2)}{2} \tag{4}$$

In the conventional situation, the word-length of both RCA and CSA should be properly selected in order to meet timing. In this case, (5) can be obtained, where n_{RCA} is determined by current timing information through (xxx).

$$\mu_c \cdot n_{RCA} = \mu_c n_0 + \mu_{mux} \tag{5}$$

Based on (4) and (5), we may obtain the representation of the word-length of CSA in terms of a given timing constraint, as presented in (6).

$$n_{CSA} = c \cdot n_{RCA} - \frac{\mu_{mux}}{\mu_c} \cdot \frac{(c+2)(c-1)}{2} \tag{6}$$

It can be seen that $c = 1$ leads to $n_{CSA} = n_{RCA}$. This is because RCA forms the least significant stage of CSA. In addition, combine (3) and (5) to ensure $n_{c-1} > 0$, we obtain the upper bond of the stage number by (7).

$$c < n_{RCA} \cdot \frac{\mu_c}{\mu_{mux}} + 1 \tag{7}$$

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C. Model Verification

As seen in (6), the value of μ_{mux}/μ_c should be determined before applying the timing model. This ratio can be obtained through timing analysis. Specifically, varying the word-length of a single stage n_i and recording the corresponding delay value d_i through the timing analysis tool. According to (1), the ratio can be obtained by fitting those values using linear polynomials, as presented in Fig. (1). Out experimental results show that $\mu_{mux}/\mu_c \approx 8$.

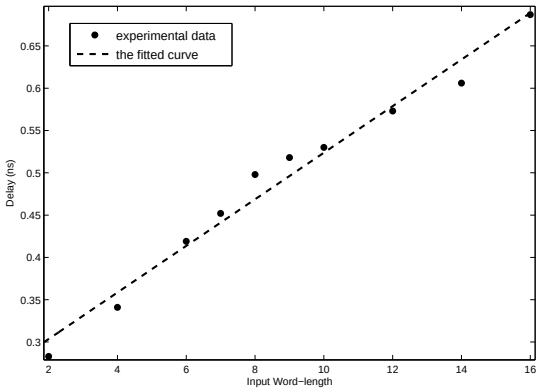

Fig. 1. Fitted curve of (1) for the most significant stage ($i = 0$), based on the given input word-length and the corresponding delay value obtained through the Xilinx Timing Analyzer.

Using this information, we verify our timing model with experimental results, which are obtained from post place and route simulations on Xilinx Virtex-6 FPGAs. Fig. 2 demonstrates both the modelled value and the experimental results of the maximum word-length of RCA and 2-stage CSA, respectively, across a range of operating frequencies. The maximum input word-length in our experiments is 16-bit, hence the modelled value is set to 16 if it expires.

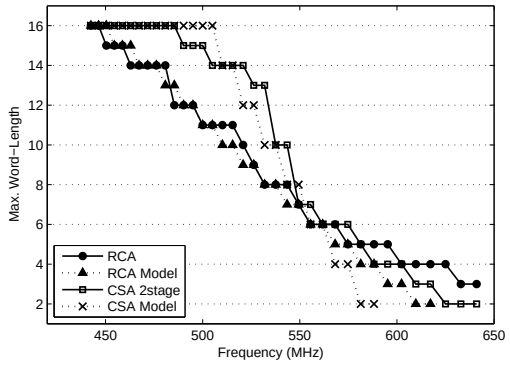

Fig. 2. Comparison of the maximum word-length for a given operating frequency between the modelled value and the experimental results from FPGA simulations.

It can be seen that our timing models match well the experimental results for both RCA and CSA, except that the modelled outcomes are slight conservative, especially at higher operating frequencies. This is because the model coefficients are obtained based on timing analysis, which is designed with safety margins to ensure correct functionality for diverse operating conditions. In addition, routing delay might be introduced during timing analysis such that the overall delay is enlarged, while our models consider logic delay only.

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D. Area Overhead

Fig. 3 demonstrates the maximum word-lengths for RCA and CSA with 2 stages and 3 stages under a range of operating frequencies. We only investigate 3 stages as the maximum stages number predicted in (7) is 3. It can be seen that in comparison to RCA, CSA achieves greater word-length when frequency is initially increased. This corresponds to smaller truncation errors. RCA only outperforms than CSA when very high frequency is applied. In addition, the word-length of 3-stage CSA is always greater than 2-stage CSA across the entire frequency domain, as expected.

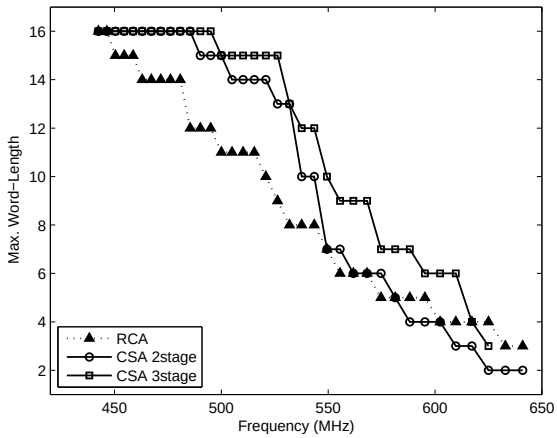

Fig. 3. Maximum word-length for RCA and CSA across a variety of frequencies.

However, the accuracy benefits brought by CSA comes with the cost of large area overhead. Fig. 4 depicts the resource usage (in terms of the number of Look-Up Tables (LUTs) in the FPGA) used for all three structures. It can be seen that for a given frequency, the 3-stage CSA consumes $2.4\times \sim 3.7\times$ area than RCA, while the number of the 2-stage CSA is $1.7\times \sim 3.1\times$. This finding poses a question of whether CSA with higher stage numbers still offer better accuracy than RCA under a limited area budget.

E. Exploring Trade-offs Between Accuracy, Performance and Area

To answer this question, we explore the trade-offs between accuracy, performance as well as area in this section. If the available hardware resources are limited, the full word-length of both CSA and RCA might not be implemented. The precision lose might generates large errors even at low frequencies. This is demonstrated by experiments where an area constraint is applied besides the timing requirement. Both of the constraints are met by reducing the word-length of

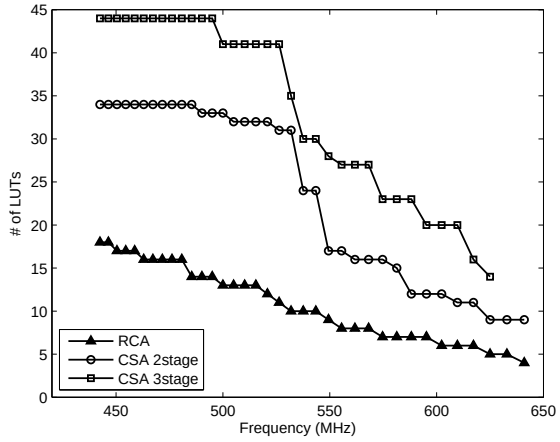

Fig. 4. Area overhead for RCA and CSA.

the input signal. The errors at the outputs are recorded with the reference to the original word-length. In addition, another designing method is adopted where RCA is implemented with the maximum possible word-length under the given area budget, while the timing constraints are met by overclocking. For instance, Fig.xxx to Fig.xxx illustrate error expectations of all the described design scenarios when setting the LUTs number to 45, 35, 25 and 15 respectively. The optimal design metric with the minimum error expectation is labelled for each area constraint.

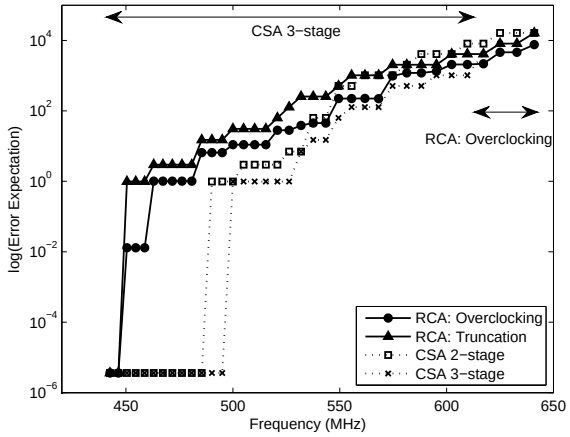

Fig. 5. LUT=45

If the available area is large enough, as shown in Fig.xxx, CSA with higher stage numbers can be implemented with full precision and it is the optimal design choice unless very high frequencies are applied. This is because at lower frequencies, the long carry chain is divided into multiple overlapped sections, and the higher stage number the shorter the carry chain length of each stage. When the frequency increases, however, the multiplexer delay becomes comparable to the carry chain delay, and this will limit the maximum word-length of CSA. It can be seen that the overclocked RCA achieves best accuracy at higher frequencies.

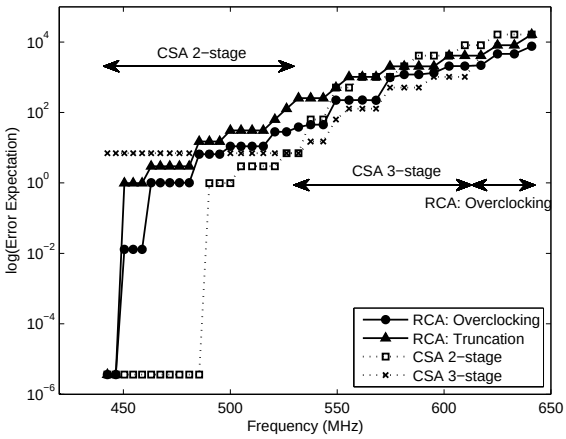

Fig. 6. LUT=35

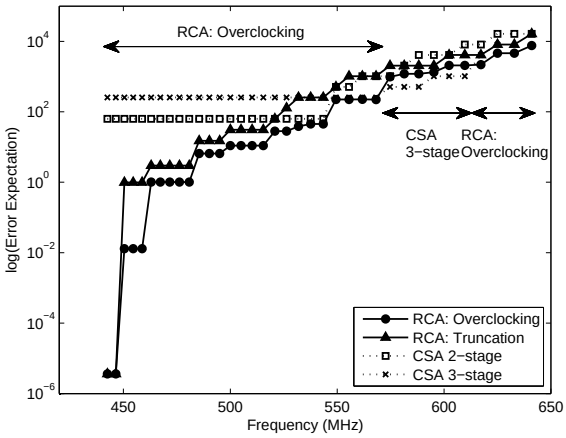

Fig. 7. LUT=25

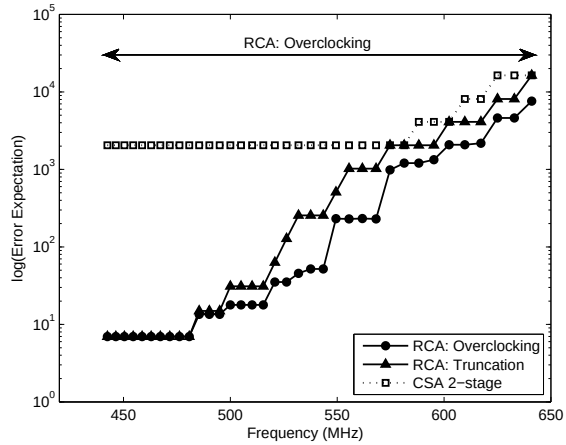

Fig. 8. LUT=15

For a tighter area budget, only part of the complex structures can be implemented, whilst the simple structure still keeps full precision. As can be seen in Fig.xxx and Fig.xxx, area instead of timing becomes the dominate factor when frequency is initially increased. This lead to a large truncation error for both 2-stage and 3-stage CSA. In this situation, overclocking RCA serves as the optimum choice with respect to accuracy.

For an even stringent area constraint, the word-length of RCA is also limited. This results in truncation error initially for all design scenarios, as shown in Fig.xxx. Meanwhile, CSA with high stage numbers could not be implemented at all. In this situation the overclocked RCA achieves best accuracy across the whole frequency domain.

In general, the error expectations at the output of all four design method for a set of timing and area constraints are demonstrated in Fig. 9.

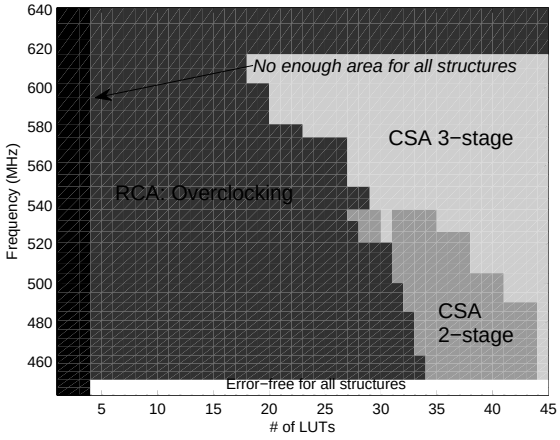

Fig. 9. Trade-offs between accuracy, performance and area for 4 design methodologies.

III. Conclusion

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Acknowledgment

The authors would like to thank...

References

[1] H. Kopka and P. W. Daly, *A Guide to LaTeX*, 3rd ed. Harlow, England: Addison-Wesley, 1999.

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Michael Shell Biography text here.

John Doe Biography text here.

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