As the delay of online adder is small, the occurrence of timing violation requires very fast frequency. Hence we only model the overclocking error in the radix-2 OM. From Figure **??** we observe two types of delay chains. One is caused by generation and propagation of $P_{[j]}$ among different stages. The other is the generation of online inputs $X_{[j]}$ and $Y_{[j]}$ from the appending logic. Since the appending logic is basically wires and simple combinational logic [**?**], the overall latency will eventually be determined by the delay of the $P_{[j]}$ path, especially with increasing operand word-lengths. As such, we initially model the delay of each stage within an OM to be a constant value μ, as shown in Figure **??**(b). We also assume that the generation of online inputs costs no delay.