Progress Report

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1 Design of Digit-parallel On-line Multiplier

2 Probabilistic Model of Overclocking Error in On-line Multiplier

2.1 Worst-case Analysis in On-line Multiplier

While the delay in a digit-parallel on-line multiplier might be derived from many sources such as the computation delay to generate outputs, the overall delay will eventually be determined by the longest propagation delay between stages with increasing operand word-lengths. Let the propagation delay between two adjacent stages in a N-digit olMult be dentoed by μ, hence the delay of the longest chain which propagates from the MSD to the LSD is given by d_w as shown in (1).

$$d_w = (N + \delta - 1) \cdot \mu \tag{1}$$

However, we note that the chain is annihilated at a certain stage if the propagation inputs of this stage change while the propagation outputs keep unchanged. For instance at time t, assume the value of propagation inputs and outputs is $Pin(t)$ and $Pout(t)$ respectively. After delay μ, the input value changes to $Pin(t + \mu)$, while the outputs remains $Pout(t)$. In this case, the overall path delay is reduced by μ because of the annihilation. Moreover, a new chain will be generated if $t = 0$ in the previous example.

2.2 Probability of Overclocking Error in On-line Multiplier

2.3 Magnitude of Overclocking Error in On-line Multiplier

3 Probabilistic Model of Truncation Error in On-line Operators