Designing a Common Interface to SPI EEPROM and SPI Flash Memory Devices

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SPI devices, be they EEPROM or Flash, have many common attributes.

- Control signals: /CS (active low chip select), SI (serial input), SO (serial output), SCK (serial clock), /Hold (active low Hold), Vcc (positive supply voltage), Vss (zero volt reference, aka ground).
- Instructions: Read, Write, Read Status Register, Write Status Register, Write Enable, Write Disable.
- Protocol: Bytes shift in or out most significant bit first. SI data is latched on the rising edge of SCK. SO data is changed on the falling edge of SCK (assuming SPI "mode 0" operation).
- Block Protection Bits: Permit protection of some, all, or none of the data in memory.

Additionally, there are some subtle differences between the two.

- Auto Erase: EEPROM devices automatically erase the previous contents of a memory cell before writing to it. Flash devices must specifically be told to erase their previous data, either on a sector-wide or device-wide (bulk) basis, prior to writing new data.
- Additional Instructions: Flash devices also support Fast Read, Sector Erase, Bulk Erase, Deep Power Down, and Read Electronic Signature instructions.
- Capacity: EEPROM devices have capacities ranging from 2k bits through 256K bits. Flash devices have capacities ranging from 1M bits through 64M bits.
- Speed: EEPROM devices support SCK frequencies up to 5 MHz. Flash devices support SCK frequencies up to 25 MHz (for Fast Read); 20 MHz otherwise.
- Number of Address Bits: EEPROM devices support the use of 8, 9, or 16 address bits, depending on the memory capacity of the device. Flash devices use only a 24-bit addressing scheme.
- Hold Behavior: With EEPROM devices, in order for the Hold feature to work properly, the /Hold line must be brought low while SCK is already low and it must be released (brought high) while SCK is still low. Flash devices allow the /Hold line to be brought low or released at any time, regardless of the state of the SCK line. The Hold feature will then commence the next time SCK goes low or it will terminate the next time SCK goes high.
- Number of Block Protect Bits: EEPROM devices have only two block protect bits. Some Flash devices (depending on capacity) may have as many as three block protect bits. The more block protect bits available, the finer the granularity with which the memory contents can be protected.
- Behavior of Block Protect Bits: In Flash devices, if any of the available block protect bits are set, the Bulk Erase instruction becomes ineffectual, i.e. no data gets erased.